Advancements Toward High Operating Temperature Small Pixel Infrared Focal Plane Arrays: Superlattice Heterostructure Engineering, Passivation, and Open-Circuit Voltage Architecture

Dissertation

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By

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Abstract

Infrared detector technology has proven useful in a wide range of imaging applications including, but not limited to, astronomy, military surveillance, industrial manufacturing processes, medical diagnostics, and automotive applications. Infrared detectors and sensors have developed into sophisticated structures since their inception in the 1950's when infrared detectors and scanning systems were first introduced.[1] Present day imagers consist of staring large format focal plane arrays (FPAs) based on HgCdTe, InSb, and III-V strained layer superlattice (SLS) material systems.[2] Type II superlattice (T2SL) detector structures based on the III-V SLS, are emerging as a versatile material system due to their low Auger recombination, high effective electron mass, and detection tunability across the mid-wave infrared (MWIR, 3-5 μm) and long-wave infrared (LWIR, 8-12 μm) wavelength regions.[3]

However, several physical factors currently limit the T2SL detectors in the context of high-density and high operating temperature (HOT) conditions in the MWIR and LWIR. Currently, the low operating temperature of these detectors is costly as imaging degrades and becomes unstable with higher detector operating temperature. Imager systems are also trending toward larger format FPAs with smaller pixel pitch, therefore scaling to high-density arrays comes with adverse radiometric effects. In this dissertation, scientific research challenges limiting current SLS detector technology from achieving high-density, HOT conditions are identified and investigated to understand the underlying device physics and mitigate poor performance with three main contributions: (1) superlattice

heterostructure engineering, (2) detector surface leakage current suppression with passivation, and (3) demonstration of an open-circuit voltage photodetector (VocP) architecture.

Through superlattice heterostructure engineering, we designed, simulated, fabricated, and tested unipolar barrier nBp detectors with InAs/GaSb, InAs/InGaSb, and InAsSb/GaAsSb SLS material systems. The measured results were compared to simulations retrieved from the NRL Bands™ *k·p* modeling tool to understand the differences between ideal detector behavior and the behavior of the as-grown devices. The nBp detector dark current results of the as-grown sample led to an important conclusion that fully delineating the barrier detector unintentionally inverts p-type absorber designs, confirming previous p-type absorber research, and also confirmed in this work to occur in InAs/GaSb LWIR SLS absorbers. We concluded this study with several paths forward to further optimize these designs for future LWIR detector structures, including the use of passivation.

We investigated the use of passivation on a dual-band LWIR InAs/GaSb pBp barrier detector and a MWIR InAs/InAsSb pn detector to reduce the surface leakage current seen in these detectors. By using Al_2O_3 and ZnO via atomic layer deposition (ALD), we were able to employ these passivation techniques through fabrication and measure the dark current to understand the surface effects on the fully delineated detector pixels. Results between passivated and unpassivated detectors were compared using variable area diode arrays, and show that both the Al_2O_3 ALD film and the ZnO ALD treatment reduced the sidewall surface leakage current on these single pixel detectors by at least two orders of

magnitude, where the passivated samples showed bulk-limited dark current characteristics over a range of diode sizes from 50 μm^2 to 500 μm^2 under reverse-bias voltage at 77 K. Further optimization to improve the bulk-limited performance at other biases and temperatures is needed, but the techniques used for this research have attained bulk-limited performance of small pixel detectors.

Lastly, a more device-centered approach was developed where we re-examined the relative advantages of using the reverse-bias photocurrent of a photodetector versus using the open-circuit voltage under the same conditions. We investigated the detector physics through analytical modeling, fabrication, integration, and test of a VocP detector and explored the potential of using this architecture for small pixels in FPAs under HOT conditions. The comparison of the developed models to the measured data support the premise that the open-circuit voltage operation can be modeled using standard diode physics. Further analysis found favorable operating conditions for the open-circuit voltage detector through noise equivalent temperature difference (NEDT) models using standard radiometric optics for high density FPAs. The resultant radiometric demonstration of the VocP architecture provided good agreement between the developed model and the measured data over three orders of magnitude in irradiance ranging from 10^{15} – 10^{18} photons/s-cm^2. We believe the VocP detector provides a solution to support large format FPAs with small pixel pitch and small capacitor ROICs for HOT MWIR and LWIR operation. Applications that can trade off longer integration times for increased sensitivity and dynamic range will especially benefit from the VocP architecture, ultimately filling a technological void in infrared imaging under HOT MWIR conditions.

Overall, this research has expanded the fundamental boundaries in infrared detector technology through material system designs and processes, and through the critical role of the detector to readout integrated circuit (ROIC) interface for future advancements toward high-density, HOT FPAs.

Dedication

I dedicate this work to my family, especially to my parents Mabel and Michael.

Thank you for all your love, encouragement, and prayers.

"Results!" cried Edison, in surprise, "No results? Why, man, I have gotten a lot of results! I know several thousand things that won't work."

-Thomas Edison

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O-H!

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T. Specht, S. Myers, T. J. Ronningen, A. Kazemi, D. Hollingshead, E. Fuller and S. Krishna, "*Side Wall Passivation of LWIR P-type Superlattice Detectors using Atomic Layer Deposition*," in *2018 IEEE RAPID*, Mirimar Beach, FL, USA, 2018.

Fields of Study

Major Field: Electrical and Computer Engineering

Table of Contents

List of Tables

List of Figures

1 Introduction

Modern infrared detectors are an important sensing technology with broad application in military, industrial, medical, automotive, and scientific fields. The diverse range of applications implementing non-invasive sensor technology require sensor improvement, especially across present day imager technology consisting of staring large format focal plane arrays (FPAs) based on photonic material systems including HgCdTe, InSb, and III-V strained layer superlattices (SLS).[2] Further development in infrared imager sensing capabilities is limited due to their cryogenically low operating temperatures as well as the limited pixel density for large format imaging systems. Advancing toward increased operating temperature and increased scalability for high density imagers are needed. This dissertation focuses on investigating the underlying physics and performance of semiconductor materials, detector fabrication processes, and device operation, as a means of mitigating these limiting factors.

1.1 Background

Infrared sensors are a revolutionary commercial and military technology that has made rapid advances since the 1950's.[1] Infrared detectors have unique sensor sensitivity that spans through a large segment of the electromagnetic spectrum from the short-wave infrared region (SWIR) starting at about 0.9 μm to the long-wave infrared region (LWIR) ending at about 15 μm.[4] The entire infrared region is divided into further groups as defined by the natural atmospheric transmission windows that are distinguished by absorbing molecules such as H_2O, CO_2, or O_3. These groups or windows, called spectral bands, lie

within the absorbing atmospheric regions and are defined as: short-wave infrared (0.9μm – 2.5μm); mid-wave infrared (3μm – 5μm); and long-wave infrared (8μm – 15μm), which also includes very long-wave infrared (15μm – 1mm). Unlike the limited information collected from visible sensing, infrared sensing technologies take advantage of each of these infrared spectral band regions by sensing unique infrared signature properties through thermal or chemical identification created by the objects targeted in their environment.

Currently, the low operating temperature of these detectors is costly as the higher temperature degrades the imaging capability and becomes unreliable. Imager systems are also trending toward larger format FPAs with smaller pixel pitch, therefore scaling to high-density arrays comes with adverse radiometric effects. Current progress in infrared focal plane array (IRFPA) technology is focused on the two particular topics of which my research focuses on: improving higher operating temperature (HOT) conditions and producing larger format imagers where higher pixel densities and smaller pixel pitch is required.

While much of the technology revolves around the long-standing HgCdTe (MCT) bulk material, III-V strained-layer superlattice (SLS) material systems are making a convincing argument for their favorable material properties (i.e. bandgap tunability) and benefits in commercialization (i.e. large uniform growth).[5-7] This work expanded the limits of fundamental concepts in infrared detector technology using investigations into designing SLS material heterostructure systems, different approaches to detector processing, and examining new alternatives to detector operation. These discoveries will improve

performance parameters of III-V SLS affecting high-density, large format LWIR detectors under HOT conditions.

1.2 Fundamentals of Infrared Detectors

Photodetectors based on semiconductor materials historically have demonstrated superior performance over other detector devices (i.e., bolometers) for infrared-specific applications. These solid-state photodetectors are beneficial conclusively through fundamental properties such as bandgap selection, high optical absorption coefficient, high electron mobility, and low thermal generation rate for high speed and high sensitivity with low noise.[1] Solid-state infrared photodetectors are separated into several categories according to the different energy bands in the infrared region, as demonstrated in Figure 1.

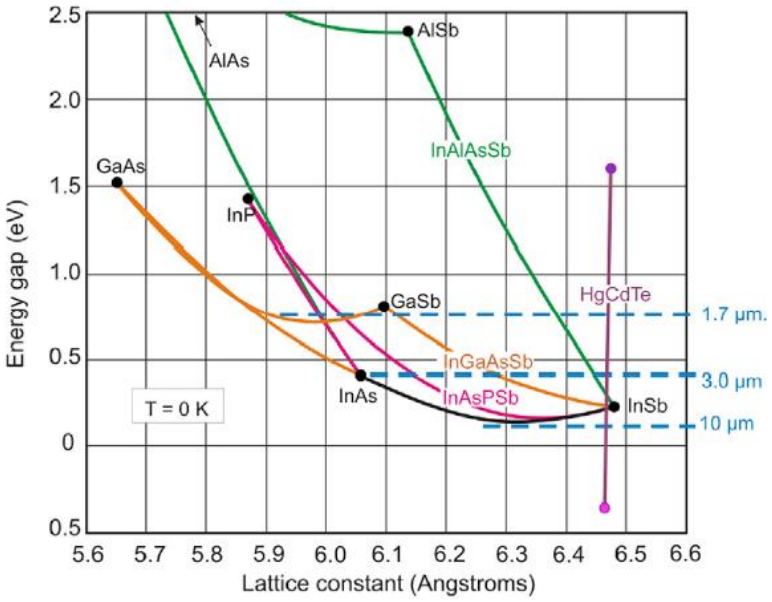

Figure 1. Diagram of bandgap energy and wavelength versus the lattice constants of semiconductor materials systems.[8]

The III-V semiconductor materials of interest are highlighted in orange and black, while the II-VI semiconductor materials are highlighted in purple. Different material

compositions, such as II-VI and III-V compound materials, determine the operable wavelength range based on the bandgap energy of the material.[9] For example, in the LWIR wavelength region of 8 μm – 14 μm, materials that have sufficient bandgap energies to detect photons in this wavelength region are: HgCdTe (MCT), InSb, InAsSb, and InGaSb. For these materials, their bandgap energies fall within the dashed blue lines for long wavelength in Figure 1.[9] With the appropriate growth and fabrication techniques, these materials are made into devices to operate in this region and satisfy the desired operational wavelength needed to collect the useful information from the scene for the specific sensing application.

Several review articles give an extensive summary of infrared focal plane array (IRFPAs) technology over the last few years, demonstrating how quickly the field is changing over time.[1, 10, 11] A recent paper from Rogalski compares type-II superlattice (T2SL) and HgCdTe (MCT) semiconductor photodetectors, as a comprehensive summary of the state-of-the-art technology for each material system to date.[8]

Rogalski summarizes the current status of the field through Table 1 where the typical properties of MCT and SLS detectors operating at a temperature of 77 K are compared:

Parameter	**HgCdTe**	**InAs/GaSb SL**	**InAs/InAsSb SL**
$\boldsymbol{\Delta E_c, \Delta E_v}$		~930 meV; ~510 meV	~142 meV; ~226 meV
Background Doping	$5 \times 10^{13}\ cm^{-3}$	$< 10^{15}\ cm^{-3}$	$> 10^{15}\ cm^{-3}$
Quantum Efficiency	80%	~50-60%	~40%
Thermal GR Carrier Lifetime	10 μs	~0.1 μs	~1 μs
R_0A Product ($\lambda_c = 10\ \mu m$)	1000 Ωcm^2	500 Ωcm^2	~100 Ωcm^2

Table 1. Typical properties of HgCdTe and T2SL photodiodes at 77 K.[8]

Parameter	HgCdTe	InAs/GaSb SL	InAs/InAsSb SL
R_0A Product ($\lambda_c = 5\ \mu m$)	108 Ωcm^2	107 Ωcm^2	~105 Ωcm^2
D* ($\lambda_c = 10\ \mu m$), FOV=0)	$3 \times 10^{12} cmHz^{1/2}W^{-1}$	$1 \times 10^{12} cmHz^{1/2}W^{-1}$	$4 \times 10^{11} cmHz^{1/2}W^{-1}$

This table presents the detector figures of merit (FOM), giving multiple avenues to compare SLS with MCT and demonstrates that the overall performance of MCT detectors is better than SLS detectors with a higher quantum efficiency, longer GR carrier lifetime, and higher detectivity (D*). Despite the appealing advantages SLS material systems offer, their overall performance remains inferior to MCT technology, but claims have been made that there is room for improvement for both III-V and II-VI technologies.

Experimental measurements and analysis show that the SLS detectors have been able to achieve dark currents close to Rule 07 when using a barrier architecture. The Rule 07 empirical formula for dark current density is shown by:

$$J_d = J_0 e^{C(1.24q/k\lambda T)} \text{ (A/cm}^2\text{)} \qquad (1.1),$$

where J_0 is a constant equal to 8367.0000185 A/cm^2, C is an exponential constant equal to -1.16239, q is the charge of an electron, k is the Boltzmann constant, and T is the operating temperature.[12, 13] Typically, the dark-current density quoted through Rule 07 is diffusion limited at the operating temperature at which the device is being measured or simulated. A comparison of state-of-the-art SLS with Rule 07 was presented by Klipstein *et al.*, along with experimental results from a LWIR FPA with a quantum efficiency of about 50% as seen in Figure 2.[14]

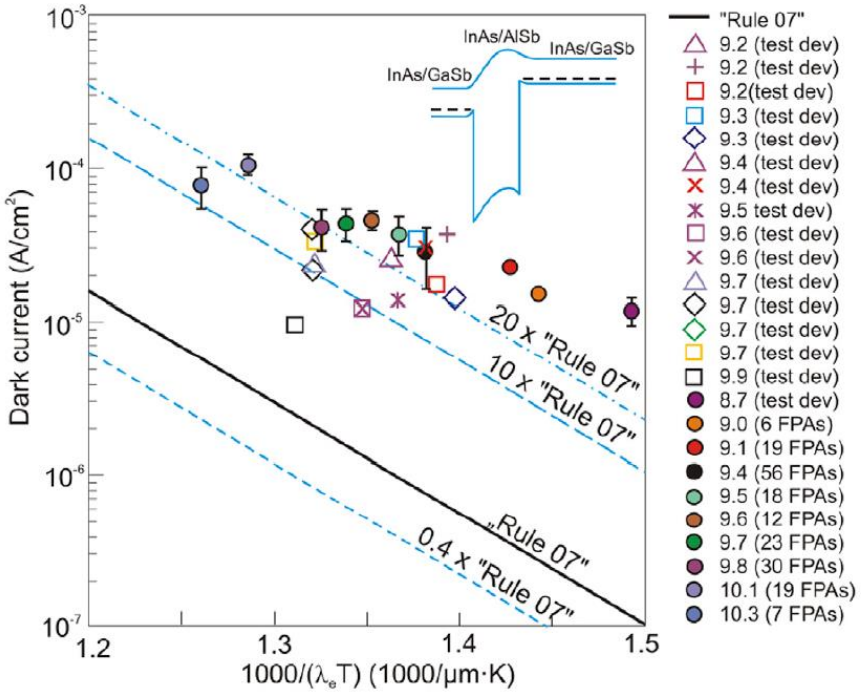

Figure 2. Dark current density of pBp T2SL detectors in comparison with Rule 07 where the range of wavelengths is 9 μm - 10.3 μm.[14]

Klipstein *et al.* have given compelling evidence through LWIR research that high operability of these detectors and FPAs is moving forward and will continue to move forward as better understanding of the physics occurring in these materials is realized.[15] One aspect that Klipstein *et al.* have not appeared to present in recent work is the effect of indium in the GaSb superlattice layer.

1.3 Modern Infrared Imaging

Several semiconductor infrared technologies have become more prominent front runners in both the military and commercial industries and have been qualitatively summarized for their advantages and challenges in the MWIR and LWIR regions in Table 2. The four material systems considered as highly marketable options for large format,

HOT infrared imaging are: HgCdTe, InSb, InAs/GaSb SL, and InAs/InAsSb SL (known as Ga-free SLS).

Detector Type	HgCdTe	InSb	InAs/GaSb SL	InAs/InAsSb SL
Wavelength Range (μm)	1 – 20	5	1 – 20	3 – 14
MWIR Quantum Efficiency	High	High	High	Medium
MWIR Operating Temperature	High	Low	High	High
LWIR Quantum Efficiency	High	N/A	High	Low
LWIR Operating Temperature	High	N/A	High	Medium
Multicolor Operation	Yes	No	Yes	Yes
"-ability" Arguments	Low	High	Medium	Medium
Material Yield	Low	Medium	High	Low

Table 2. Summary of qualitative metrics comparing the state-of-the-art infrared imagers for the MWIR and LWIR.

Detectors made from each of these materials systems have their strengths and weaknesses, but overall research has launched these particular material systems to more established detectors based on their particular roles in the application space and their research, development, and manufacturing cost. Characteristics such as "-ability" arguments[8] such as: availability, manufacturability, sensitivity, uniformity, scalability, operability, affordability, etc. were considered as a collective metric to convey the possibility of further commercial development for these detectors.

In particular, InSb detectors are a leading industry technology for the MWIR because of the material's inherent 5 μm cutoff wavelength. The III-V bulk semiconductor material can also be managed and manufactured easily by typical III-V semiconductor foundries. However, the drawback to InSb is its best asset, because it is not tunable in bandgap energy like the other semiconductor materials in the table. For InSb, the III-V bulk material quality is also a challenge because of impurities leading inherent trap states

in the bulk material, therefore it is typically only used in MWIR applications for smaller format FPAs and imagers.

MCT has been the industry leading technology for high-resolution, large format FPA imagers and systems in the LWIR region, and has held off other technologies for approximately fifty years.[16] However, MCT has three known limitations regarding growth of low bandgap material for the LWIR region: (1) material growth composition variations that affect bandgaps for LWIR applications, (2) high dark currents due to high band-to-band tunneling, and (3) low operating temperature for LWIR applications as a result.[16]

A modern investigation into alternative materials has yielded the importance of SLS material systems, and their list of advantages. These advantages surpass MCT technology, and are starting to be adopted as a standard IR material for both government and commercial entities.[17] Specifically, SLS materials are uniform and their growth is controlled easily using available growth technologies. MCT requires exquisite growth temperature control and stoichiometric control of the Hg content to achieve uniformity of wavelength. Such a level of control is not achievable with present growth technology. Because of growth uniformity, SLS materials have high FPA operability and yield once the fabrication process is complete. SLS materials use available commercial substrates such as GaSb for growth and can utilize established III-V foundries to expand research technology into the commercial space. In contrast, MCT requires a vertically integrated FPA process in each facility due to lack of diverse applications for MCT detectors and highly specialized foundry equipment build for the sole purpose of developing MCT technology. SLS FPAs have large scalability because commercial foundries for these

materials that are already built for purposes other than infrared detectors can be leveraged over MCT operation circumstances, therefore creating an opportunity to lower the fabrication costs by eliminating complexity and custom components. Likewise, as these material components break into the competitive commercial market, SLS materials are becoming more affordable. Furthermore, SLS materials are less biologically and environmentally harmful than MCT, therefore these broad parallel benefits warrant research in SLS materials.

These advantages have induced industry to make strategic moves to implement SLS into their technology, rather than rely on MCT FPAs alone. Several industrial and military applications have explored use of SLS materials in detectors as a significant cost-saving mechanism. Lockheed Martin recently announced that Raytheon will provide the next-generation F-35 sensor system based on T2SLs.[18] L3Harris Technologies also recently discussed company plans to adopt the SLS material system as their primary photonic sensing capability for high operability, high-density IRFPAs. The Air Force Research Laboratory (AFRL) also has presented to the infrared community cost surveys that explore the cost drivers of more economical FPAs.[19] These surveys demonstrate the advantage of material processes and growth yields of SLS FPAs when compared to MCT. This observed trend has given rise to motivating further SLS research.

1.3.1 Hot Operating Temperature Focal Plane Arrays

Currently, the low operating temperature of SLS detectors is costly because operating SLS detectors at higher temperatures degrades the imaging capability and becomes unreliable due to the material properties producing unfavorable operating

conditions at the individual detector pixel level. As the temperature moves up, the FPA performance goes down and the spectral imaging capability is negatively affected. An example of this is shown in Figure 3.

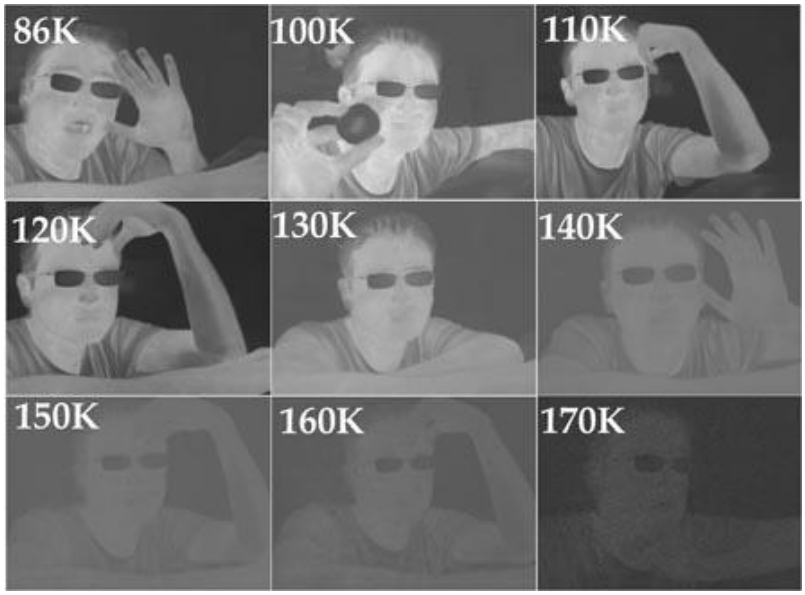

Figure 3. Images produced using a MWIR type-II superlattice FPA at different temperatures to pictorially demonstrate image degradation as detector operating temperature moves up.[20]

Finding ways to mitigate that degradation with better materials and detector designs is a focus of MWIR and LWIR research. The goal is to improve performance under HOT conditions, treated in this work as above 200 K, such that the array can be cooled via thermoelectric cooling. Integrated cryogenic coolers that operate below 200 K are a significant fraction of the cost, size, and complexity of MWIR imagers, accounting for an estimated 50% to 75% of the cost of imager production, as displayed in Figure 4.[19]

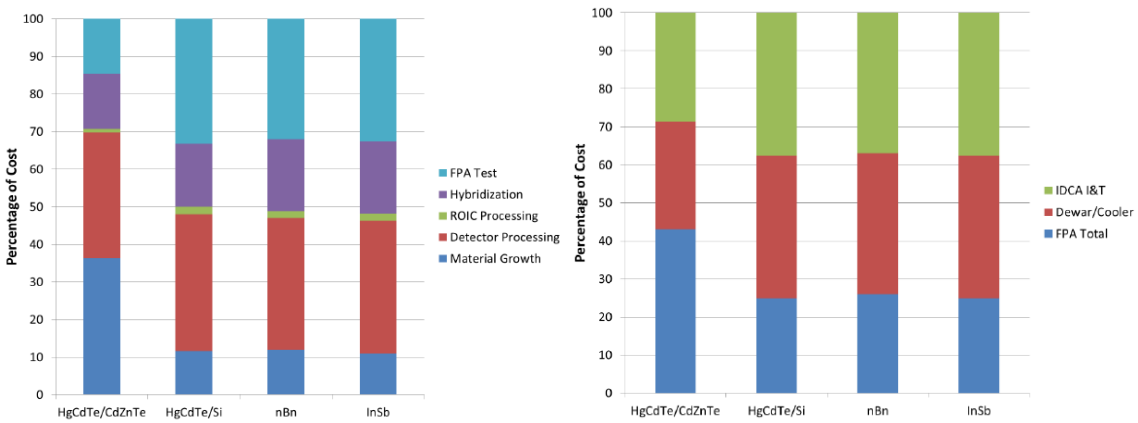

Figure 4. (Left) Cost analysis of IRFPA fabrication and characterization based off of different semiconductor materials (Right) Cost analysis of physical sensor system with FPA and cooler included [19]

If the cooler is designed to be smaller, the cost of the overall IR imager development will be driven down. Arguably, the cost of the integration and testing of these imagers would also be reduced because the integration process is indirectly affected by the coolers through the high-touch packaging of these modern imagers. Figure 4 also shows that the cost of the cooler (both by cooling capacity and monetary capacity) is the same in both the MCT and SLS technologies, therefore not allowing for a convincing case to use MCT technology over SLS when considering the size, weight, and power (SWAP), a common argument to continue the push for HOT detectors. Recently, prototype imagers have been demonstrated with increasing operating temperature such as SL imagers operating at ~160 K.[21, 22] The rapid increase in dark current as a function of temperature is unfortunately the limiting factor for the operating temperature of these detectors, therefore HOT MWIR imagers continue to seek solutions to mitigate high dark current.

Research in superlattice topics to date has one particularly iconic direction: the introduction of the barrier in superlattice detectors. Maimon and Wicks describe a unipolar

barrier design (nBn) that blocks majority carriers while allowing minority carriers to flow through the material by an n-doped (n) top contact, a unipolar electron barrier (B), and a lightly n-doped (n) infrared (IR) absorber region, as seen in the Figure 5(b) band diagram.[23]

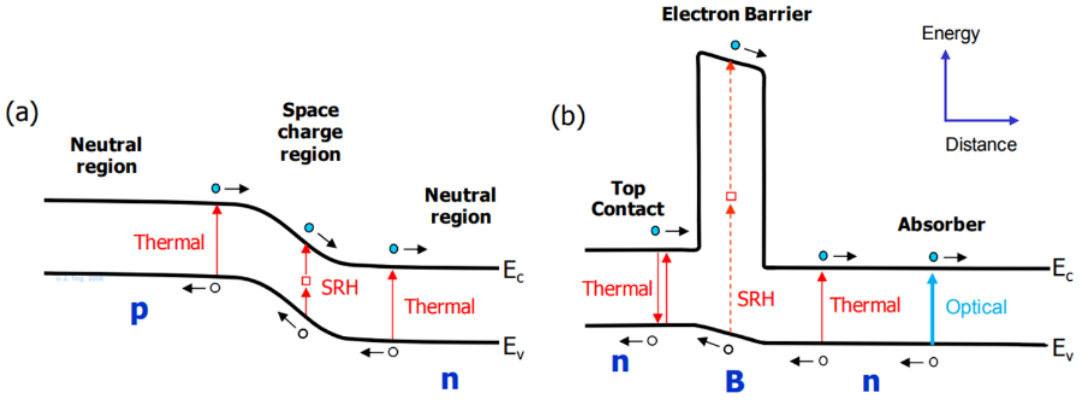

Figure 5. Energy-band diagram of (a) p-n junction and (b) a nBn barrier detector.[15, 23]

Compared to the traditional p-n junction photodiode, whose energy-band diagram is seen in Figure 5(a), the nBn barrier detector is designed to be highly effective in dark current suppression without inhibiting the photocurrent coming from photo-generated minority carriers. [23-25] This is accomplished by replacing the junction with a larger bandgap barrier material.[23-25] This serves to reduce the generation-recombination (G-R) dark current due to Shockley-Read-Hall (SRH) processes, which keeps the detector in diffusion-limited performance at higher temperatures.[23] Figure 6 displays an example of this concept by comparing the p-n photodiode and the nBn detector as an Arrhenius plot of the dark current where the $e^{-E_g/2kT}$ term trends up exponentially as temperature increases. The "X" indicated in the detector structure abbreviation (XBn) refers to the nomenclature describing that the n-doped (n) top contact can also be a p-doped (p) top contact depending on the

selected heterostructure design. Thus, the barrier detector structure using either dopant type will have the same improved performance over the standard pn detector structure and concludes the use of a barrier in the detector stack pushes the operating point to a higher temperature or higher sensitivity at the same temperature of the p-n diode. [15, 23]

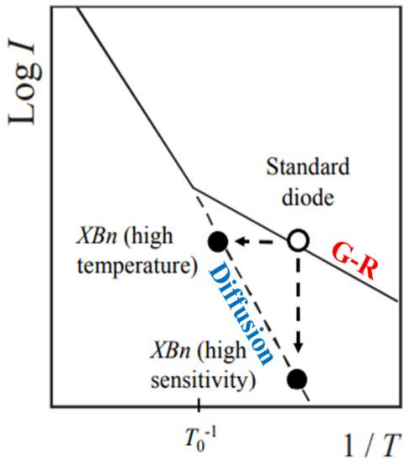

Figure 6. Arrhenius plot of the dark current of a standard p-n junction diode (solid line) compared to the XBn device (dashed line) pushing the operating point to a higher temperature or higher sensitivity. [15, 23]

To achieve higher operating temperatures using SLS material, a barrier must be included in the detector stack. Because these detectors have achieved HOT conditions near 150 K, their inclusion in the device structure stack when HOT condition requirements need to be met has become standard practice.[26]

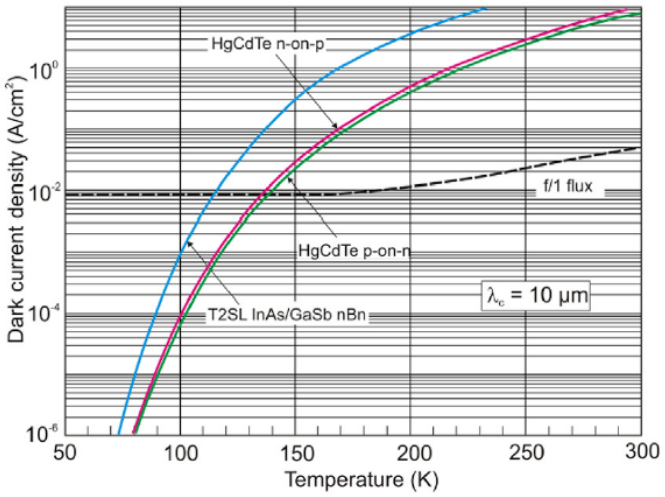

Figure 7. Dark-current density versus temperature for several detectors including a nBn detector in comparison with MCT for a 10 μm system with a background dark current calculated for f/1 optics.[8]

Increasing the operating temperature beyond the diffusion limit requires examining the available thickness of barrier detector designs. Since the diffusion length is long, the probability to collect carriers decreases if the thickness does not meet the diffusion length. Changing the detector design to one based on a multistage detection mechanism may increase absorption efficiency. An interband cascade photodetector (ICP) is such a detector design that maintains the current flowing through the device, while suppressing noise and increasing D* when the absorber thickness is reduced.[27] Therefore, it is useful to consider ICP designs as a candidate for HOT detector solutions.

1.3.2 High Density and Large Format Infrared Imagers

In the past decade, antimonide based infrared photonic detectors have demonstrated dramatic improvement in performance including quantum efficiency, dark current and noise equivalent differential temperature (NEDT). In particular, Type II superlattices (T2SL) based on the InAs/GaSb system combine the advantages of a manufacturable III-

V horizontally integrated foundry platform with the flexibility of detection in the entire MWIR and LWIR regions. Along with these advances, T2SL infrared focal plane array pixel sizes are shrinking, resulting in an increase in the individual pixel surface area to volume ratio that consequently increases the contribution of surface current to the overall leakage current of the device. For example, Figure 8 shows the shrinking trends of MCT detectors in FPA development over the last 20 years.

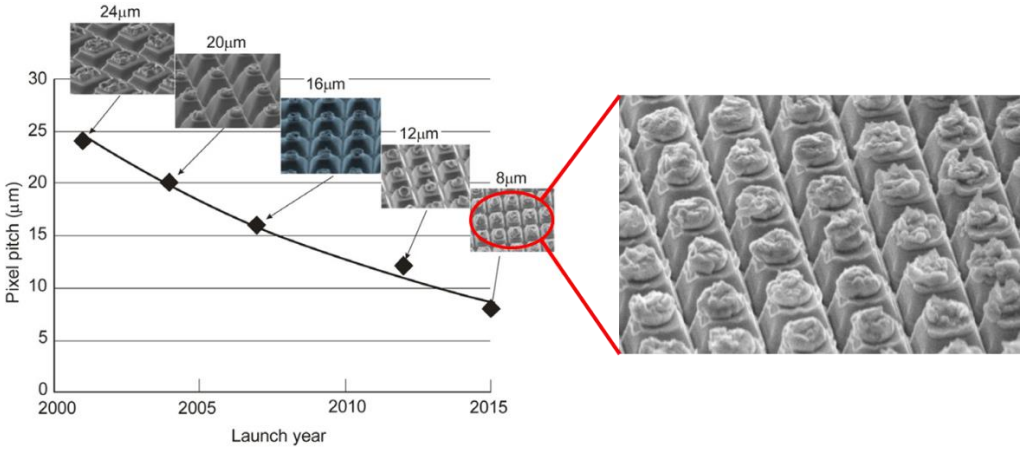

Figure 8. MWIR pixel pitch development of MCT detector arrays in chronological order, with a feature of a focused SEM image of an detector array with 8 μm pixel pitch.[28]

Research efforts within the infrared community are enabling reduced pixel pitch for high-resolution imaging arrays without increasing the size of the FPA by increasing the individual detector pixel density in the FPA.[29] The increase in format size for IR imagers drives the diffraction limited vs. detector limited argument, especially as you move out to longer wavelengths where the diffraction limit starts to become proportional to wavelength.[30] As the push to reduce the detector size to increase the format of the FPA, the field-of-view and resolution are affected to the point where they become ineffective as fundamental system optics limits are reached.

This has led to the commercial testing and introduction of MWIR FPA products with decreased pitch including an InSb planar detector at 10 μm,[31] a III-V Sb-based superlattice (SL) detector at 5 μm,[32] and a HgCdTe detector at 5 μm and 7.5 μm.[33] Imager systems are also trending toward larger format FPAs with smaller pixel pitch, therefore scaling to high-density arrays comes with adverse radiometric effects.

1.4 Organization and Contribution of This Work

The research presented in this dissertation explores fundamental concepts in the physics and the science of infrared detector technology. This work has focused on the overall improvement of the performance of MWIR and LWIR detectors for HOT conditions at small pixel pitch. Scientific research challenges limiting current SLS detector technology from achieving high-density, HOT conditions are identified and investigated to understand the underlying device physics and mitigate poor performance with three main contributions:

- **Superlattice Heterostructure Engineering**: We designed, fabricated, and tested unipolar barrier nBp detectors with InAs/GaSb, InAs/InGaSb, and InAsSb/GaAsSb SLS detectors. The design, modeling, and optimization of LWIR SLS absorber materials improved performance, measured by increasing the absorption coefficient of the absorber layer, which allows for informed development of more efficient functional infrared detectors and imagers.
- **Suppression of Surface Leakage Current with Passivation:** We investigated the use of Al_2O_3 and ZnO via atomic layer deposition (ALD) to reduce the surface leakage current in LWIR detectors. Developing two passivation techniques on fully

delineated detector pixels to quantify the effects of surface dark currents on LWIR detector designs and improve performance metrics for HOT conditions using these fabrication processes.

- **Demonstration of an Open-circuit Voltage Photodetector (VocP) Architecture:** We re-examined the relative advantages of using the reverse-bias photocurrent of a photodiode versus using the open-circuit voltage under the same conditions. We investigated the detector physics through analytical modeling, fabrication, integration and test of a VocP detector and explored the potential of using this for small pixels in FPAs under HOT conditions and expand the understanding of the pixel architectural interface between the III-V detector material and the silicon ROIC.

The results of exploring these three research objectives, as applied to III-V antimonide-based detectors in the MWIR and LWIR, expanded the fundamental boundaries in infrared detector technology through material system designs and processes, and through the critical role of the detector to readout integrated circuit (ROIC) interface for the next generation of large format high-density, HOT IRFPAs.

The dissertation is divided into seven chapters. Chapter 1 consists of introductory statements and presentation of research goals. Chapter 2 contains detailed information regarding the infrared materials, specifically focusing on SLS materials, and methods involving growing, fabricating, and testing infrared detectors. Chapter 3 includes detailed modeling and design of superlattice heterostructures for the LWIR region, along with experimental supporting evidence of LWIR absorber designs based on simulations of SLS

absorbers. Chapter 4 discusses fabrication challenges for detectors with LWIR p-type absorbers and the techniques used to passivate and treat the detector surfaces to improve the detector operability. Chapter 5 introduces an analysis of the semiconductor physics surrounding the open circuit voltage operation of a photodetector and compares the NEDT of detectors operating under reverse-bias condition and open-circuit condition. Chapter 6 uses the conclusions made in Chapter 5 to propose a novel photodetector architecture design to use for IRFPAs as HOT conditions for large format imagers become limiting factors for detector performance. Finally, Chapter 7 will wrap up the dissertation with concluding remarks and visions of future work based on the findings in this research.

2 Materials, Methods, and Metrics

Performance parameters that establish the quality of HOT and high pixel density infrared detectors and FPAs are presented in this chapter to offer some background on the fundamentals of infrared detectors. This chapter contains information needed to understand advanced concepts throughout the rest of the dissertation regarding infrared SLS materials and research methodology involved in material growth, detector fabrication processes, and testing of infrared detectors to quantify performance.

Typical logical steps to demonstrate new research initiatives in infrared technology flows like other engineering processes and starts with the design of the imaging system and can focus on many subsystems within that design space. To illustrate the overall research methodology landscape in infrared detectors, Figure 9 presents a process flow diagram of the engineering practices needed to design, build, and test an infrared detector.

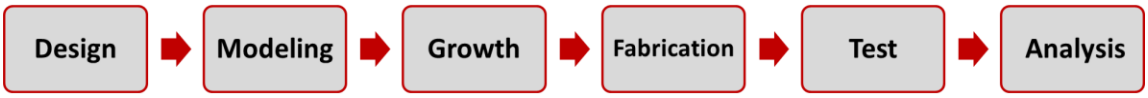

Figure 9. Process flow diagram laying out the research methodology of the engineering steps needed for infrared detector research.

The design-to-demonstration research process is intended to connect each separate engineering task through a process flow to parse the overall fundamental questions proposed by infrared detector researchers into manageable experiments. In a new infrared detector development effort, the researcher will move through the engineering tasks in the process flow diagram and concentrate their efforts on one or two particular steps to

determine how the outcome impacts the overall detector improvement. The findings are used as a feedback into the process flow.

The process flow starts with the design and simulation of the infrared detector material, being that it meets the desired wavelength range needed for the sensing application. Once the detector material and detector structure have been identified, the material is grown to those specifications. This is completed in iteration with the material measurement step since the material must be optimized to have the correct parameters (i.e. doping, barrier, compressive strain, etc.) before moving forward to fabrication. After the growth, the material is fabricated into detectors for full device test and measurement. Once measurements are complete, analysis of the detector performance can assist in iterating the process flow using feedback from the results.

The particular steps this dissertation research focused on the design and simulation of these detector materials and structures, the detector fabrication process, and the detector test and measurement for feedback and analysis of the detector improvement. The following sections will discuss these processes and tasks in detail to give some appreciation for what is considered when researching and developing infrared detectors.

2.1 Basics of Superlattices

Photon detectors are significant contributors to the detector industry, and a variety of photon detector structures are available to choose from to specifically address the needs of each application. One such structure called a “superlattice” (SL) was introduced by Esaki and Tsu in 1970,[34] with follow-up research on strained-layer superlattices (SLS) proposed by Mailhiot and Smith in 1987.[35] Many groups have followed suit and have

extensively studied superlattices through modeling[36], growth[37], fabrication[38], and characterization[27]. SL materials are complex material structures using the periodicity of two different III-V semiconductor compounds through alternating monolithic layering to achieve smaller band gap materials. The resultant material satisfies a large span of wavelength ranges with bulk-like, favorable characteristics that individual bulk semiconductors cannot attain on their own. SL structures are an example of band-engineered materials that have shown favorable characteristics for improved device performance such as suppressed Auger recombination compared to traditional materials like MCT.[35]

Distinctively, SL material structures are based on the heterostructure layering of two different III-V semiconductor compositions. The alternating layers form quantum wells where the electron and hole wave-functions in the layers overlap and forms conduction (electron) and valance (heavy and light hole) minibands respectively as seen in Figure 10. Since the layers are strained around the GaSb substrate lattice constant (6.1 Å), the splitting of heavy and light hole minibands occurs in the layers to promote the smaller energy bandgap to form. Therefore, the energy bandgap of the SLS materials are determined by the layer thickness rather than the molar fraction applied in compound semiconductors. Doping the layers to form structures such as pin diodes or more advanced detector structures is achievable. Despite the layered material structure, they still use the fundamental theory of direct interaction of light onto the lattice of the material to produce an electrical signal. An example of the superlattice structure is featured in Figure 10 showing the different alternating layers of InAs and GaSb material grown using molecular

beam epitaxy (MBE) where thin layers of semiconductor form a single crystal with bulk-like behavior due to the minibands created by the wave function.[39]

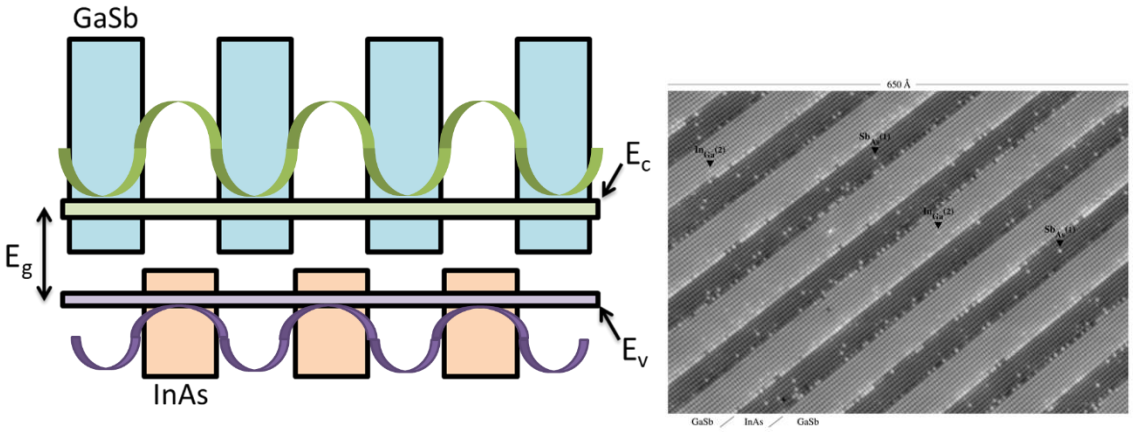

Figure 10. Energy band diagram of a SLS with a conduction miniband (E_C) and a valence miniband (E_V) shown to form the new energy bandgap (E_g) of the material. Also shown, Atomic-resolution cross-sectional STM image of an InAs/GaSb SLS grown by MBE.[39]

Based off this information, a matrix of combinations is used to create these periodic superlattice structures at varying periods, thicknesses, and doping concentrations. These parameters are varied to achieve the desired operability of the detector, which results in favorable material characteristics such as: large effective electron mass, reduced tunneling effects, reduced Auger recombination, and reduced dark current.[5, 40] The design and simulation of these band-engineered materials and other infrared materials is completed using computational tools to provide quick feedback to the researcher. Modeling suites such as NextNano, Silvaco, Crosslight, etc. have developed platforms to assist researchers understand the semiconductor physics and optimize the devices for anticipated results before the growth.

2.2 Design of Superlattice Materials

The imaging applications taking advantage of IR detector technology have a wide range of engineering requirements demanded from these systems. Each individual application prioritizes specific system requirements leading to tradeoffs between detector solution; thus, the project or application must designate specific requirements to achieve the best possible performance from the materials that serve as IR detectors. With these project requirements in mind, design considerations aim to incorporate SLS materials into the IR detector technology. By using the SLS material heterostructure characteristics from their thin periodic layers, we can design for specific fundamental semiconductor parameters such as favorable bandgaps. Then the material parameters are applied to the material design, optical performance, energy-band engineering, and architecture of the detector.

2.2.1 Superlattice Heterostructures

Research trends within the III-V community have determined several key parameters to optimize the SLS material performance for IR detectors from a systems engineering perspective.[41-43] Important bandgap-engineered material metrics are: absorption coefficient, effective mass, oscillator strength, valence band offsets from InSb, doping concentration, and minority carrier lifetime; which ultimately affect the cutoff wavelength, dark current, external quantum efficiency (EQE), and detectivity of the detector. As mentioned in section 2.1, these parameters come from the behavior associated with the superlattice structure, where the periodic repetition of dissimilar III-V semiconductor materials with different lattice constants and energy-band offsets appear as

heterojunctions within the new crystal structure. Examples of heterostructure band alignments can be found in Figure 11. In particular, the heterojunction band alignment formed between the InAs and GaSb is referred to as a type-II broken bandgap where the electron and hole wavefunctions are localized in InAs and GaSb, respectively.[44] This is referred to commonly as a type-II superlattice (T2SL) material system based on the InAs/GaSb design, and will be the focus of the simulations presented within this scope of work.

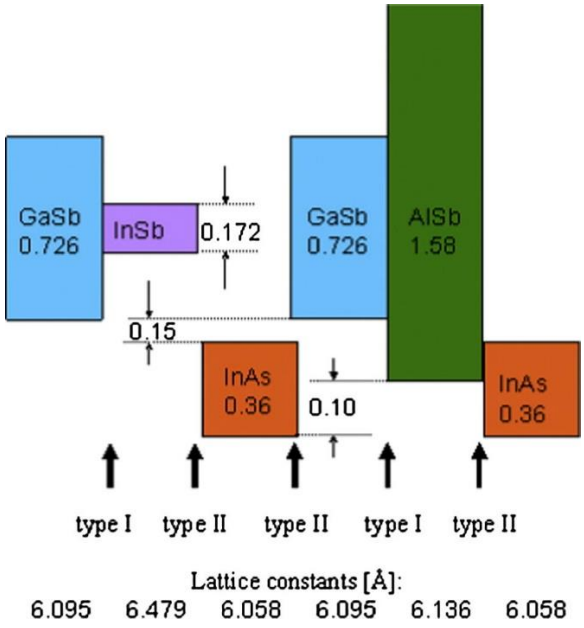

Figure 11. Bandgaps of III-V compound semiconductors used for SLS materials based on the 6.1 Å family.[45]

The electron wavefunction propagation is very sensitive to the resultant quantum wells and barriers in the direction of the multilayer growth and affects the narrow energy subbands called minibands.[46] Changing the thickness of the constituent layers changes the separation between the lowest confined conduction subband and the highest valence

subband that forms a new smaller energy bandgap.[34] This physical behavior is quantified by solving the wavefunctions from the Schrodinger's equation and Lowdin's perturbation theory, along with the changes in the optical and electronic properties of the new material, including the key material metrics mentioned above. Optimizing these metrics and allowing for tradeoffs to reconcile, the IR detector material then can then be used to build an absorber layer for the detector.

Figures of merit (FOM) to establish the material quality and detector quality are use these material parameters to quantify the overall detector performance. The infrared research community typically uses several numerical parameters as fundamental FOM to determine the quality of infrared detectors both through material properties and device properties. Parameters such as absorption coefficient, dark current, R_0A product, quantum efficiency, detectivity, and lifetime are a few examples of these parameters that are used to quantify and compare material and device candidates for infrared detection.

One particular FOM is the specific detectivity, in which the D* equation contains the ratio between the absorption coefficient and the thermal generation rate *(α/G)*. The absorption coefficient describes the penetration depth at which light of a particular wavelength can pass through before it is absorbed. The absorption coefficient is calculated from the SLS material parameters in the detector absorber layer. Maximizing the absorption coefficient leads to optimizing the absorber efficiency in a given detector made for a specific cutoff wavelength. The absorption coefficient is related directly to the cutoff wavelength, and establishes a starting point of design for specific application requirements:

$$\alpha = \frac{4\pi k}{\lambda} \ (\text{cm}^{-1}) \qquad (2.1)$$

where α is the absorption coefficient, k is the extinction coefficient, and λ is the cutoff wavelength.

SLS materials of different compositions and layer thicknesses have varying absorption coefficients, and determining those coefficients requires extensive calculation because the optical absorption relates to the overlap of electron and hole wavefunctions in the superlattice layers. These wavefunctions are calculated in several ways using developed semiconductor physics-based theories including tight-binding, density functional theory, pseudopotential method, and multi-band k·p perturbation theory. Modeling resources mentioned above (i.e. NextNano, Silvaco, Crosslight, NRL MultiBands™ etc.) have been created that assist in these calculations and provide quicker iterative design opportunities for SLS materials through bandgap engineering research.

It should be noted that the thermal generation rate is further translated into the minority carrier lifetime as it is an inverse to the net G-R carrier lifetime under the assumption of equilibrium.[47] The minority carrier lifetime is also a crucial parameter for determination of dark current and affects the maximum operating temperature of the photodetector. As previously discussed, barrier heterostructure detectors improve device performance with the goal of diffusion limited performance where the diffusion dark current is represented by:

$$J_{diff} = q\frac{n_i^2 W}{N_0 \tau} \text{ (Amperes/cm}^2\text{)} \qquad (2.2)$$

where J_{diff} is diffusion limited dark current, τ is the minority carrier lifetime, q is the electron charge, n_i is the intrinsic carrier density, N_0 is the majority-carrier density and W is the absorber thickness.[3] The minority carrier lifetime is observed to be inversely

proportional to the dark current. Consequently, a long minority carrier lifetime is important to minimize the dark current and an indication of good material quality for high performing infrared detectors.

Recent research thrusts in detector development have focused on bandgap engineering for the LWIR region, which cater to small bandgap semiconductors. There are three types of SLS that are feasible for LWIR due to their composition and ability to achieve LWIR energy bandgaps with reasonable layer thicknesses: InAs/GaSb, InAs/InGaSb, and InAs/InAsSb. These SLS materials are part of the 6.1 Å family where each compound semiconductor lattice constant lies around 6.1 Å, including a commercially available substrate (GaSb) for viable MBE growth.[48] Previous research efforts offer an outlook on selected designs that have undergone material and device characterization. InAs/InAsSb has the lowest absorption coefficient of the three SLS types due to the spatial separation of the carriers, but it has the highest carrier lifetime because of the narrower dispersion of the minibands, enhancing transport properties.[49, 50] InAs/GaSb has a higher absorption coefficient with an added enhancement of Auger suppression due to the spatial distribution of electron-hole carriers.[51-53] Because of their favorability, this research effort focuses on two different types of SLS materials that use the InAs/GaSb design.

2.2.2 Detector Heterostructures

Bandgap engineering has led to well-defined absorber designs in which the favorable properties contribute to effective detector structures that meet the requirements of specific applications. A similar engineering process is leveraged in building the overall detector stack for optimal detector performance under HOT conditions. Detectors using

band-diagram engineering, such as the nBn barrier detector introduced in Chapter 1, allows for further control of majority and minority carrier behavior within the detector structure that comes from SLS absorber material. The ground-breaking concepts surrounding the nBn detector have changed engineering requirements to modern systems and have made this heterostructure a common-place detector structure when using SLS absorber designs.

The biggest design considerations when incorporating a barrier into the detector stack are: whether the material has a sufficiently wide bandgap to block carriers, how well the barrier material lattice constant matches the GaSb substrate and as-grown absorber layer, and how well the barrier energy bands line up with the energy bands of the absorber layer. Typically, III-V compound materials containing aluminum (Al-V) are suitable for matching the first two criteria because the bandgaps of Al-V compounds are naturally much higher than the SLS absorber bandgaps and the lattice constant of some Al-containing compound semiconductors are within that 6.1 Å lattice constant based on GaSb. The Al-containing barrier layer energy band offset to the absorber layer constrains the material selection significantly because the materials used for barriers may have too large of an offset compared to the absorber layer energy bands. The barrier alignment also depends on absorber doping type and must align with the minority carrier band to allow minority carrier flow while blocking majority carrier flow (i.e., valance band alignment for n-type absorber and conduction band alignment for p-type absorber). Consequently, the barrier will also block the minority carriers from reaching the other side of the detector if the barrier energy band offset is not aligned with the correct absorber layer energy band in the

detector stack. Ultimately no current will flow through the detector. An example of this is shown in Figure 12 with a nBn detector.

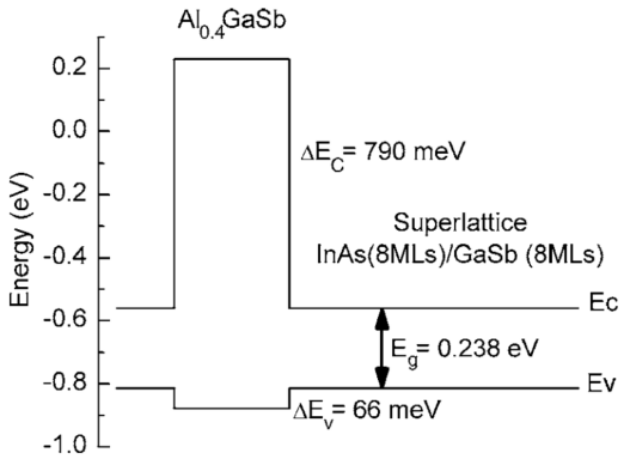

Figure 12. Band diagram of a nBn structure stack with calculated offsets between the barrier layer and the absorber layer.[41]

The structure architecture is optimized to a specific absorber and barrier combination. SLS heterostructures also can be used to design custom barriers, specifically an Al-containing SLS such as InAs/AlSb, which is used to support detector barriers for LWIR p-type as a result of the favorable heterostructure band alignment and bandgap to typical p-type absorbers. Thus, the barrier can also be tuned with SLS band engineering just like the absorber layer. Doping the barrier layer also can affect the alignment of the barrier to the absorber layer, further minimizing the difference in energy band offset at the absorber-barrier interface.

2.2.3 NRL MultiBands™ Modeling

It was mentioned above that bandgap-engineering research has produced different modeling resources to assist in design calculations for SLS materials and subsequent

detectors. NRL MultiBands™ is one such computational software suite developed by the Naval Research Lab. It is specifically built to model SLS materials and detector structures.[54, 55] Starting with the basic understanding of layer thickness and composition, the solver is used to calculate the absorption coefficient as well as other parameters of SLS materials using a combination of empirical inputs and the eight-band *k·p* method.[55, 56] The Luttinger–Kohn model *k·p* perturbation theory is a generalized version of the commonly known single-band Kronig-Penney (*k·p*) method, and essentially relates energy levels (*E*) in a momentum space (*k*), to the effective mass using perturbation theory.

Simulations resulting from NRL MultiBands™ using *k·p* modeling calculations result in what is commonly known as the *E-k* diagram. The *E-k* diagram shows the semiconductor band structure in vicinity of the bandgap (E_g) found within the first Brillouin zone in momentum (*k*) space. Figure 13, provides examples of *E-k* diagrams for both direct and indirect semiconductors, showing the conduction band (CB), the valence band (VB), and the semiconductor bandgap (E_g).

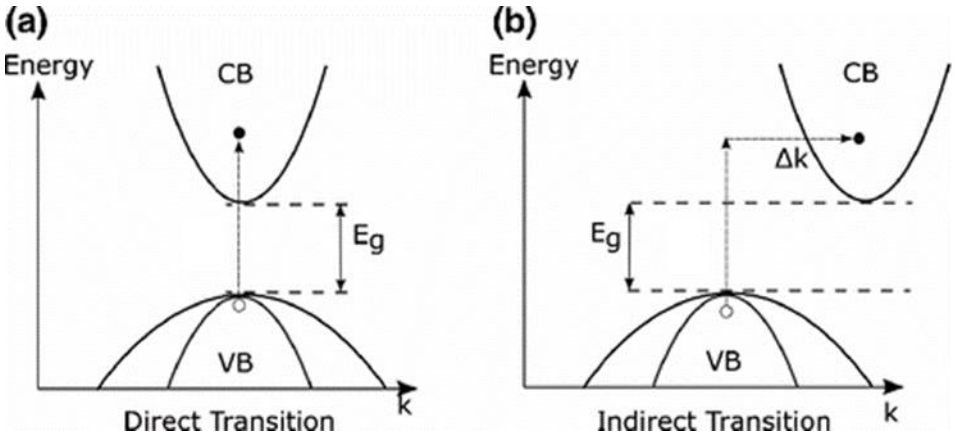

Figure 13. Energy vs. momentum diagram of a semiconductor with a (a) direct bandgap and (b) indirect band gap.

The SLS bandgap is determined from this transition. Other material parameters also are calculated using several methods such as charge transport, Poisson equation for electrostatics, and recombination mechanisms. The results contain material metrics such as: electron effective mass, hole effective mass, lattice constant, the valence band offset relative to InSb, photoluminescence (PL), absorption coefficient, lattice mismatch from the GaSb substrate, light hole and heavy hole energy bands, cutoff wavelength, and overall period thickness, to name a few.

Other performance metrics are calculated for different simulated detector structure compositions and designs, such as: absorbance, dark current, and quantum efficiency using the drift-diffusion model built for device modeling. The data and wavefunction solutions for the SLS design can be used for other calculations outside of the suite as well.

The assumptions-dictated system-level requirements are used as inputs to the solver. This includes operating temperature of the desired system, which transposes as the operating temperature of the SLS material. Also included is the cutoff wavelength and correlating SLS layer thickness to achieve that bandgap. A good rule of thumb for selecting layer thickness is to keep the layers thin and the ratio of the two compound semiconductors as small as possible for good carrier localization and propagation across the resulting absorber layer. The growth temperature also is considered to help determine the residual strain and the overall lattice constant achieved after the SLS growth. Several design examples are discussed further in the following sections.

2.3 Growth of Superlattices

The semiconductor material manufacturing method that provides custom-designed semiconductor crystal material based on the SLS structure is typically completed using Molecular Beam Epitaxy (MBE). Generally, MBE is the deposition of a single crystalline layer(s) on a crystalline substrate, creating an “epi” overlayer that builds to a desired thickness. This happens at an atomic level where a small layer of atoms is deposited onto the surface of the lattice-matched substrate in measurable incremental concentrations via a molecular beam from an elemental source in an ultra-high vacuum chamber. These incremental layers are called periods or monolayers (ML) because the layer of atoms is measured in Angstroms, which will be important in Chapter 3 when discussing the SLS layer thicknesses in the absorber designs.

This growth process uses highly specialized equipment to achieve the conditions needed for high-precision, high-accuracy monolayer crystal growth and requires careful calibration of several parameters for each growth including substrate temperature, III-V ratio, elemental material flux flow, source temperature, chamber vacuum levels, source shutter timing, etc. For SLS growth, the parameters are incredibly various, but with carful calibration and monitoring, SLS layer thicknesses as low as 2 ML have been demonstrated. For InAs/GaSb SLS heterostructure growths, the epi-layer of SLS material requires four different sources (indium, arsenic, gallium, and antimony), thus the amount of shutter movements to grow the SLS layers requires four different shuttering schemes with correlated timing. Then, when doping elements are included, the growth becomes more complex. While this is attainable with ease using the MBE equipment available for research

purposes, industry motivates the reduction of mechanical movements, thus reaches for simplified growths as they are advantageous when it comes to growing SLS materials.

2.4 Material Characterization

Once the growth process has completed through collaboration with other research group members, the epi material grown by MBE on the GaSb substrate is ready for the next step in the task flow and moves to material characterization of the new SLS material. X-Ray Diffraction (XRD), photoluminescence (PL), and Nomarski are standard measurements of the bare crystalline material where each individual measurement validates if the material characteristics are favorable to the goal of creating the desired SLS epi layer for absorber material.

The XRD measurement confirms the strain and the layer thickness of the SLS absorber material grown by the MBE. Reduced strain reduces defects and increases the carrier lifetime within the material. The PL measurement finds the SLS material's resultant bandgap, which also confirms the cutoff wavelength, through time-resolved photoluminescence (TRPL) or time-resolved microwave reflectance (TMR). The SLS material is also scanned for glaring defects on the surface using Nomarski imaging through a filtered microscope. Stacking faults and other growth defects can be seen during this visual check to confirm the growth conditions were fully optimized.

The iterative feedback provided by these measurements is necessary to calibrate the growths for SLS absorber materials and the subsequent heterostructure detector designs. The growths completed for this research were done in collaboration with other research group members who specialize in SLS growth. This research uses the PL to confirm the

correct operating wavelength range for grown material systems as well as XRD measurements to validate strain balancing. These measurements were completed by the growers during calibration runs for the SLS growth on the MBE.

Additional absorption measurements on the new SLS absorber material were completed using the transmission spectra extracted from Fourier-transform infrared (FTIR) spectroscopy. As previously demonstrated, measuring the absorption can help determine material quality.[8, 36, 57, 58] Higher quality, defect free absorber materials readily absorb more photons, which excite a higher amount electrons into the conduction band, and increases the detector QE.[59]

The absorption is determined by measuring the transmission of the bare crystal material using a FTIR spectrometer containing a glo-bar IR source, a KBr beam splitter, a deuterated triglycine sulfate (DTGS) thermal detector, and a sample holder carrying the SLS material. A beam of IR light is sent through a beam splitter, where two split beams are reflected and recombined to construct an interference pattern. This interference pattern (interferogram) is sent through the semiconductor material sample with the transmitted light of the interferogram hitting a reference detector. This action captures a raw beam spectrum in the detector over the defined range. A Fourier transform is performed to obtain the full spectrum as a function of wavenumber.[60] Figure 14 illustrates the IR beam path and sample placement in a diagram to show how the sample information is captured.

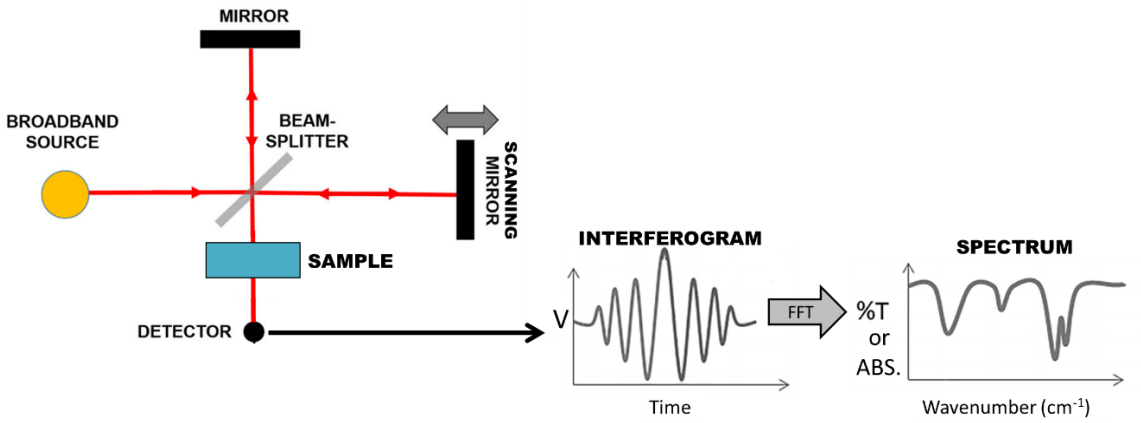

Figure 14. Block diagram of FTIR spectroscopy measurement setup used to measure transmission and absorption of semiconductor material.

The raw spectrum can be described in either transmission, single beam, or absorbance depending on the settings within the FTIR software. It is possible to measure the sample absorption at room temperature, but lowering the temperature of the semiconductor material reduces thermal movement of carriers and increases the signal output, creating a strong spectrum.[61] Then, the transmission data is used to calculate the absorption coefficient, a specific metric that will later be used in Chapter 3 to understand and compare different designs of the SLS materials to function at HOT conditions.

2.5 Device Fabrication

The resultant SLS detector wafer containing the designed SLS absorber material and designed detector structure stack is then fabricated into individual pixel detectors using standard lithography techniques. Attempts to improve the detector performance through these steps is warranted mostly through etching and passivation. An overall process diagram is shown in Figure 15, indicating how the bare material from the growth is formed into a measurable infrared detector.

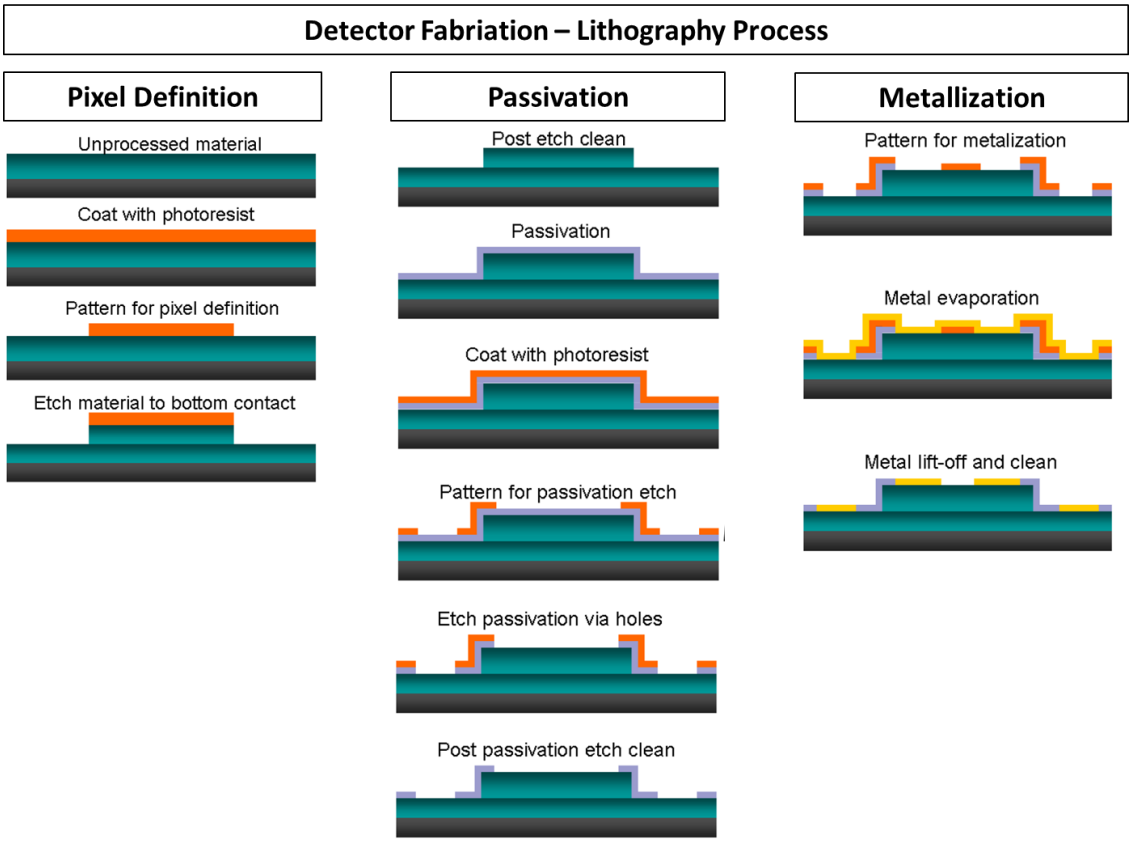

Figure 15. An overall view of the detector fabrication process for single element detector pixels.[62]

Fabricating a detector happens in three major segments: pixel definition, passivation, and metallization. Pixel definition takes the bare crystal material and defines the pixel mesas using photolithography patterns for mesa etching. Variable-sized mesa structures are created in this step to form variable area diode arrays (VADA), shown in Figure 16. These arrays define the detector area for experimentation and analysis.

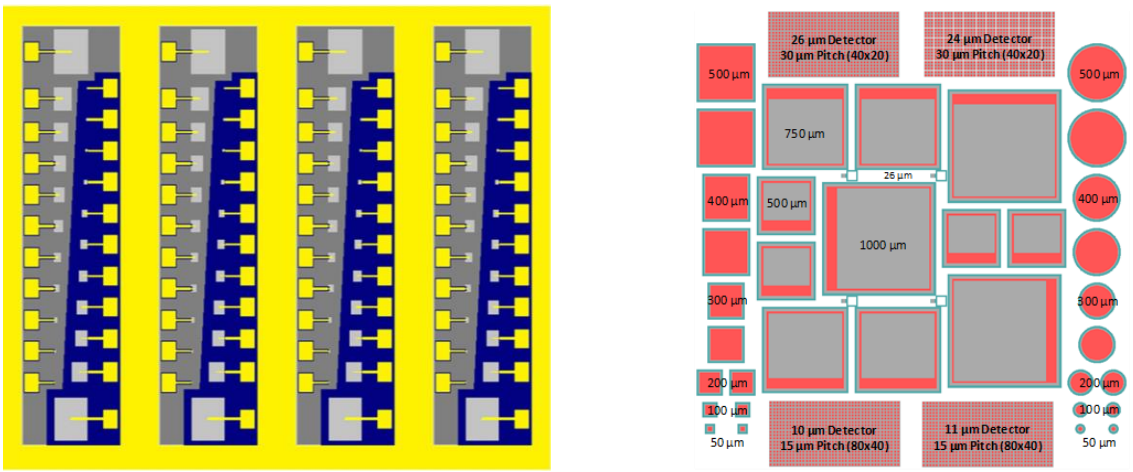

Figure 16. Examples of mask designs containing variable area diode array (VADA) detectors.

Wet and dry etching techniques were employed to define the mesa structures throughout this research. For the wet etch, a citric acid solution ($C_6H_8O_7$: H_3PO_4 : H_2O_2 : H_2O) at a ratio of (2:1:1:8) was mixed to etch the SLS epi material. In the dry etch case, a stepped dry etch process to etch the SLS material was done with a PlasmaTherm SLR 770 ICP Chlorine Etcher with a flow rate of BCl_3 at 15 sccm and Argon at 5 sccm during the inductively coupled plasma (ICP) reactive ion etch (RIE). The RIE power was set to 100 W and the ICP power was set to 300 W.

The passivation segment concentrates on treating the fully delineated pixel surfaces to mitigate the negative effects on detector performance due to the surface. This research focuses on this segment in detail as it is one of the main challenges concerning small pixel pitch. The VADA arrays from Figure 16 assist in studies considering surface dark currents on fully delineated pixels. For example, the newly etched side wall surface is directly exposed to air if not passivated.[63] According to previous research on III-V materials such as GaSb, “GaSb has a highly reactive surface and on exposure to air it will form a native

oxide layer".[63] This natural reactivity has led research efforts to concentrate on how to minimize the formation and impact of these oxide layers on the device performance. Studying the surface effects will be revisited in Chapter 4.

Finally, the detector goes through the metallization segment where the contact metal layer is patterned on with standard photolithography and deposited using standard techniques. The ohmic top and bottom contacts were deposited by e-beam evaporation using Ti/Pt/Au (500/500/2500Å). This combination has proven to make good ohmic contacts on T2SL materials and has been adopted as a standard metal stack for SLS detectors.[64] Once the metal has been deposited, the detectors are ready for testing.

2.6 Detector Characterization

The final step in the process of researching IR detector performance is the detector testing and measurement of the detector, also interchangeably described as detector characterization. Determining the performance characteristics of the detector consists of testing the detector using measurement tools to acquire figures of merit (FOM) parameters, as they generally define the quality of the detector structure performance. Characterization is an important part of the infrared detector industry because it allows the community to quantify and compare sensor performance to theoretical specifications of other device designs whose performance has been reported.[8]

The FOM below have been measured throughout this work to quantify and compare the results of the heterostructure barrier detectors, the detectors used in the passivation study, and the VocP architecture detector. These FOM measurements have also aided in determining future paths forward for this research based on the analyzed results.

2.6.1 Current-Voltage Analysis

The basic current-voltage (IV) characteristics of a photodetector demonstrates initial performance and overall quality of the fabricated detector structures. Several current mechanisms are analyzed by measuring the IV of a detector structure. Dark current is described as the current measured across the detector when no incident light or radiation is exciting the detector material and ideally reflects the Shockley equation behavior as proven by Shockley regarding p-n junction theory in 1949.[65] The lack of incident light on the detector minimizes the optical performance of the detector material, exposing the influences on the overall signal due to different mechanism such as the random generation and recombination occurring in the depletion region of the detector.[66] This can also be influenced by the radiation caused by the surrounding environment's temperature, as well as material defects in the detector.[66] The expression for diode current is described in (2.3):

$$I_{diode}(V_b) = I_{sat}\left(exp\left(\frac{qV_b}{n_{diode}k_BT}\right) - 1\right) - I_{ph} + \frac{V_b}{r_{sh}} \qquad (2.3)$$

where I_{diode} is the total diode current, I_{sat} is the reverse saturation current, q is the charge of an electron, n_{diode} is the diode ideality factor, I_{ph} is the photocurrent, $\frac{V_b}{r_{sh}}$ is the representation of the parasitic leakage current across the p-n junction, and k_BT/q is the thermal voltage at temperature T.

The depiction of the Shockley equation is expanded out in (2.3) to consider other factors, such as non-ideal losses and illumination conditions. Under these illumination conditions, the shape of the IV curve is found to be similar with an offset in the direction of reverse bias and reverse current, as shown by the dashed red lines seen in Figure 17 in the detector IV curve. The ideal diode equation from Shockley is in blue. And the total

diode current is displayed in black, where the IV curve characteristics show different current curve shapes measured under reverse bias voltage and forward bias conditions. The analysis of the total current measured under dark conditions provides detector parameters, such as: diffusion, generation-recombination, trap-assisted tunneling, band-to-band tunneling, and ohmic series and shunt resistances. These parameters are useful in determining material and device metrics for overall performance comparisons.

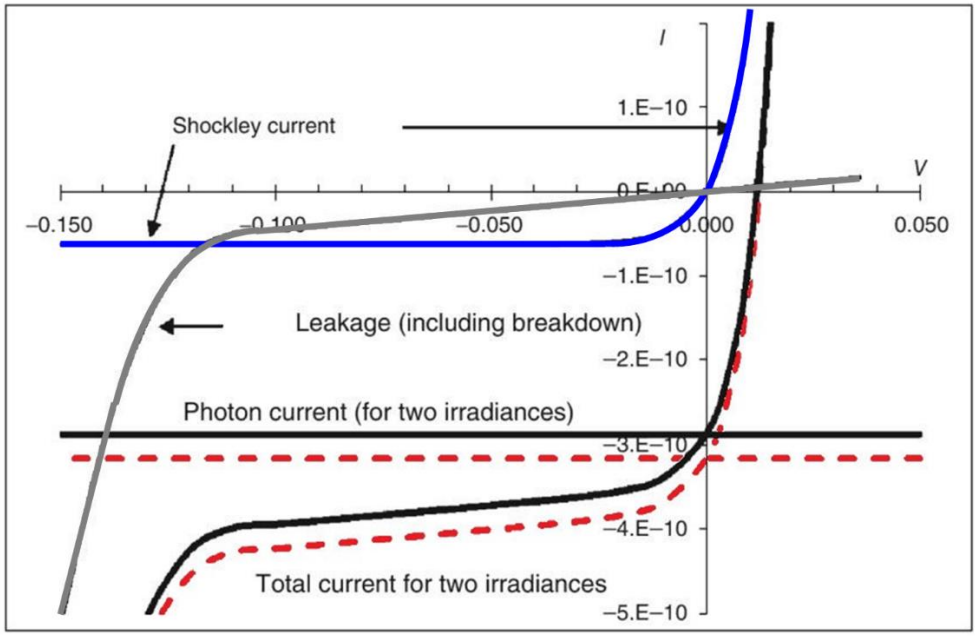

Figure 17. Diode current-voltage (IV) curve representing dark conditions and light conditions using the Shockley equation, photocurrent, leakage current, and breakdown current.[67]

The method for attaining the IV is to measure the current versus bias voltage, which is collected using a dark current measurement test setup as seen in Figure 18. The test setup uses a closed-cycle cryostat cooled with a LHe compressor, a temperature controller to control the detector temperature, and either a parameter analyzer or source-measure unit (SMU) to source the bias voltage to the two leads of the detector. The current across the

detector is measured simultaneously as the voltage bias changes. This is done by grounding the bottom contact of the detector and applying the voltage bias across the detector with the top contact.

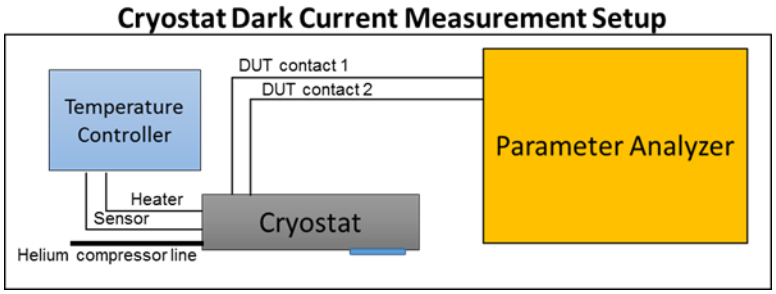

Figure 18. Dark current measurement test setup using a closed-cycle cryostat to measure IV at temperatures as low as 11 K with the semiconductor parameter analyzer.

The IV measurement for the detector current characteristics is a good indicator of material behavior that could eventually lead to exposing material defects or other phenomenon related to the characteristics of the material such as leakage current due to the device structure.[38]

An analysis to determine the effects of the surface leakage current along the detector structure is described to give context to later analysis complete in Chapter 4. The VADA masks are used to fabricate detectors of different sizes to give an idea for what to expect as the pixel moves down in pitch size. For the surface current to bulk current analysis, the measured dark current is converted to dark current density to simplify the comparison across the different-sized diodes. We can separate the currents from the measured dark current into the bulk current and the surface current through:

$$J_d(V_b) = \frac{I_{dark}(V_b)}{A} = J_{surface} + J_{bulk} = \frac{1}{r_{surface}}\frac{P}{A} + J_{bulk} \qquad (2.4),$$

where the dark current density is J_d, the voltage bias is V_b, and the perimeter-to-area ratio is $\left(\frac{P}{A}\right)$. The slope of the resultant calculation is broken down to the surface resistance of the detector through $\left(\frac{1}{r_{surface}}\right)$ and is used to analyze the surface effects on the detector as the dark current density is plotted for various perimeter-to-area ratios. Ideally, a horizontal line in this analysis would signify that the surface resistance is constant across all area pixels at the designated applied voltage bias. An illustration of this analysis is shown in Figure 19.

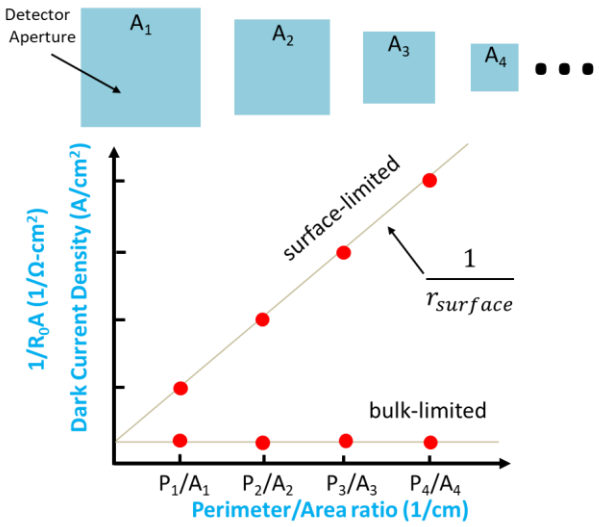

Figure 19. Analysis of the R0A product at different perimeter-to-area ratios. The slope indicates the quantitative resistance of the surface. If there are no adverse surface effects, there will be no slope, and the diode is bulk-limited.

Another method to determine the improvement of a detector structure using passivation is the R_0A product. The R_0A product is based on the derivative calculation of dark current density in Eq. (4.2), to achieve an expression using the dynamic resistance (R_0) and the diode area (A) as defined in Eq. (4.3).

$$\frac{1}{R_0A} = \frac{1}{R_0A_{bulk}} + \frac{1}{r_{surface}}\left(\frac{P}{A}\right) \qquad (2.5)$$

This equation also contains the same slope in the perimeter-to-area data, $\left(\frac{1}{r_{surface}}\right)$. Therefore, the indication of a parasitic resistance due to the conductive carriers shunting the detector sidewall constrains the detector to be surface-limited. When there is no slope to this line across the different perimeter-to-area ratios, the detector is designated as bulk-limited.

2.6.2 Spectral Response

The spectral response of a detector is a spectrum of the material's molecular absorption and transmission over a wavelength range.[68] This spectral curve information is used for responsivity measurements by using the curve to normalize the responsivity of the detector material. It is also known as relative spectral response RR(λ) or normalized spectral response.

To complete this measurement, the sample detector is cooled and is connected to a trans-impedance Amplifier (TIA) to amplify the signal. The detector is then biased using the TIA and fed into the FTIR spectrometer via an external interface box to take the spectral response at various bias voltages and temperatures if desired. The sample is subjected to infrared radiation directed by a mirror from the FTIR spectrometer, and the resulting response curve is reported in % transmission by the FTIR.

The cryostat spectral response setup is identified in Figure 20. The cryostat was the only test setup used for this measurement because it was not possible to measure this parameter with the probe station due to the top-view optical window port on the probe station. The detector samples were cooled to 77K for this measurement and were operated at a 0V voltage bias.

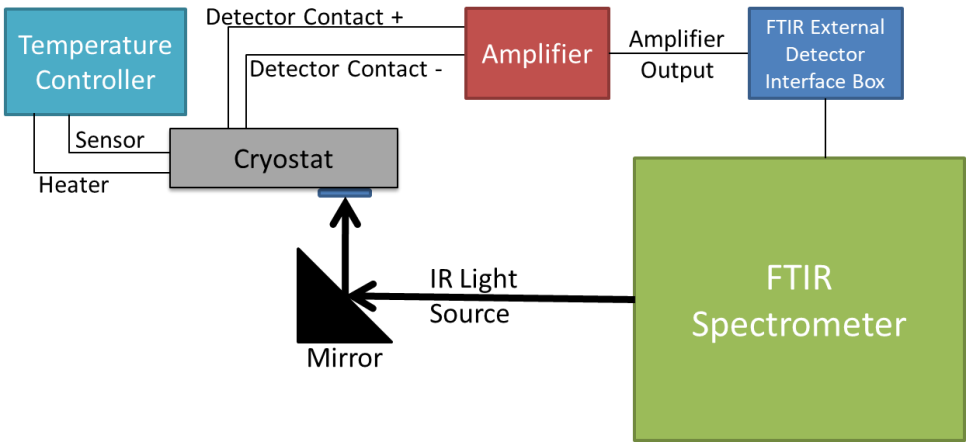

Figure 20. Spectral Response Measurement Setup

The spectral response is also used for determining the spectral quantum efficiency by using the relative spectral response in the same way across the spectral range by normalizing it to a quantified QE measurement.

2.6.3 Quantum Efficiency

Quantum efficiency (QE) is the number of photons incident on the detector's active area to the number of independent electrons generated. The QE is extracted from photocurrent (I_{ph}) measurements done using the measurement setup in Figure 21.

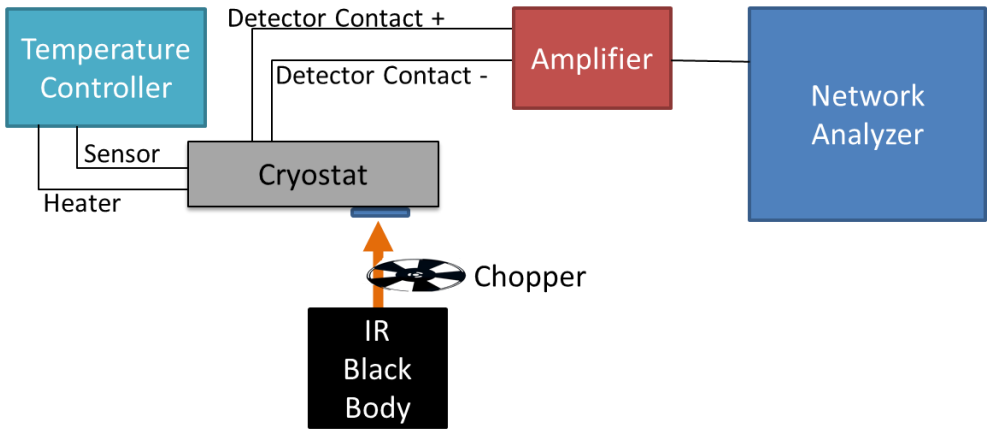

Figure 21. QE measurement setup

The QE measurement consists of cooling the detector and operating the detector at various voltage biases and temperatures while measuring photocurrent using a network analyzer. The measurements presented in this work used the QE measurement setup to determine the quantum efficiency, where the detector was cooled to 80 K, the blackbody source temperature was set to 800 K, a narrow-band spectral filter was used (MWIR = 3.4 μm notch filter), and the chopping frequency was set to 400 Hz. The network analyzer then measured the signal and the noise centered around the 400 Hz chopping frequency with a 200 mHz bandwidth. The relationship between the photocurrent and the quantum efficiency is described by using the equation (2.1):

$$I_{ph} = q\eta E_q A_{diode} \quad (2.6),$$

where η is the quantum efficiency of the photodiode, E_q is the photon irradiance (photons/sec-cm^2), and A_{diode} is the area of the diode. This parameter gives a percentage describing the efficiency of the conversion process of received photons to free electron hole pairs, and is reported as a percentage in literature. [69]

2.6.4 Noise

The total photodetector noise associated with the total current signal of the detector is broken down into two dominating noise components: Johnson noise and Shot noise.[44, 69] The diode noise is described using both the Johnson noise and Shot noise as the main sources of noise.

$$i^2_{(diode)noise} = i^2_{(Johnson)noise} + i^2_{(Shot)noise} \quad (2.7)$$

The Johnson noise is generated fundamentally in all resistive elements due to the thermal motion of the charge carriers in the p-n junction.[44] The Johnson noise is found by the expression:

$$i^2_{(Johnson)noise} = \left({}^{4n_{diode}k_bT}/_{r_d}\right)\Delta f \qquad (2.8)$$

where Δf is the frequency bandwidth, r_d is the dynamic resistance, and T is the diode operating temperature, as defined and measured in the diode signal analysis above. The overall impact of the Shot noise originates from the random arrival of carriers at the p-n junction, thus describing the unavoidable current fluctuations in the diode:[67]

$$i^2_{(Shot)noise} = 2q\left(|I_{dark} + 2I_{sat}| + I_{ph}\right)\Delta f \qquad (2.9),$$

where I_d is the total diode current, I_{sat} is the reverse saturation current, and I_{ph} is the photo-generated current. These equations are used with the instrument noise baseline to determine the noise of the detector.

The measurement setup to determine the detector noise uses the same setup configuration as the quantum efficiency measurement pictured in Figure 21. The noise spectrum is measured while the detector is illuminated at the same E_q as the signal measurement by the same blackbody temperature, operating temperature and bias voltage settings, and chopping frequency.

2.6.5 Detectivity

One key FOM that is used to quantify a detector's performance is known as the specific detectivity or normalized detectivity, which respectively compares different

detector performances under the same conditions by normalizing the individual detector detectivity using the signal to noise ratio (SNR) out of a detector when 1 watt of radiant power is incident on 1 cm^2 detector area at a noise equivalent bandwidth of 1 Hz.[26] This is shown by Equation 1:

$$D^* = \frac{(A_{det}\Delta f)^{1/2}}{\Phi_e}(SNR) = \frac{\lambda}{hc}\left(\frac{\alpha}{G}\right)^{1/2} \text{(Jones)} \qquad (2.10)$$

where D^* is the normalized detectivity, λ is the wavelength, h is Planck's constant, c is the speed of light, α is the absorption coefficient, and G is the thermal generation rate.[8] While D* is an important FOM to quantify through experimental measurements, the ratio between the absorption coefficient and the thermal generation rate (α/G) is a more critical parameter. These two material parameters directly affect the overall photodetector performance. Therefore in order to maximize a photodetectors' D*, the (α/G) for the photodetector material needs to also be maximized to realize the highest performing infrared photodetector.[8, 11]

D* is the baseline FOM that can be used to compare any detector with another detector. However, when discussing comparisons between FPA performances, noise equivalent differential temperature (NEDT) is used as the primary FOM instead.

2.6.6 NEDT

Noise Equivalent Differential Temperature (NEDT) of a detector represents the temperature change due to the incident radiation upon the detector where the output signal is equal to the root mean squared noise level.[70] Nomenclature of NEDT versus Noise Equivalent Temperature Difference (NETD) or Noise Equivalent Differential Temperature (NEΔT) are the same and are interchangeable terms within literature. A complete equation

to represent the NEDT is described from an equation developed by Kinch[30] and also reported by Rogalski[8]:

$$NEDT = \frac{(J_{dark}/J_{\phi})+1}{\sqrt{N_W C}} \tag{2.11}$$

where J_{dark} is the detector dark current, J_{ϕ} is the total background flux current density including the consideration for the optics, $\sqrt{N_W}$ is the readout integration capacity, C is the scene contrast through the optics given by equations (2.12) and (2.13).

$$\sqrt{N_w} = \frac{(J_{dark}+J_{\phi})\tau_{int}}{q} \tag{2.12}$$

$$C = \left(\frac{1}{\phi_B}\right)\frac{d\phi_B}{dT} \tag{2.13}$$

The parameters used in these equations are the integration time (τ_{int}), the background flux (ϕ_B), the electron charge (q), and the detector operating temperature (T).

NEDT is typically used for infrared focal plane arrays; this measurement is not typically used as a Figure of Merit for single pixel detectors because there is too much variance between each pixel to be able to compare this parameter accurately. The measurement setup for NEDT is similar to the QE measurement, but with some optical complexity because of the optics associated with the FPA size, radiometry, and blackbody source size. This dissertation does not complete measurements of NEDT, but the calculations here are relevant to the work done in Chapter 5.

3 Modeling and Design of Superlattice Heterostructures

Continuing the discussion of state-of-the-art infrared focal plane array (IRFPA) technology, we have affirmed these detectors are trending toward higher operating temperature (HOT) conditions and large format, small pixel pitch FPAs. While the state-of-the-art revolves around HgCdTe (MCT) bulk material, III-V strained layer superlattice (SLS) material systems have favorable properties that make SLS FPAs an appealing alternative material system for the next generation of IRFPAs.

SLS material systems are advantageous because of their ability to produce a wide range of bandgaps through the alternating layers of semiconductor compounds. With the ability to tailor the period of the superlattice as described in Chapter 2, the changes in the band structure enhances the fundamental aspects of the semiconductor bulk-like behavior including the bandgap, effective mass, and mobility. With the increased complexity of band structure compared to bulk, SLS materials are themselves heterostructures on a rudimentary scale. This chapter builds on these ideas and presents detailed investigations of various SLS heterostructures through design, modeling, and experimental results with the goal of understanding the impact on the external quantum efficiency (EQE) and overall performance of IR detectors.

Semiconductor parameters such as compound composition, absorption coefficient, energy band alignments, energy band offsets, lattice mismatch, material doping, and growth conditions will be discussed to show how they play an important role in determining the best SL material for the desired application specifications, such as cutoff wavelength and substrate selection. While, in theory, SLS material systems can cover the

entire IR spectrum, recent research has focused specifically on the longer wavelength regions because their extremely small bandgaps make it difficult to achieve the desired specifications.. There are several challenges and advantages to using antimonide-based SLS materials for LWIR detectors. These challenges and advantages are demonstrated here using two different types of SLS materials, [LWIR SLS absorber material] and [Type B], which are based on the InAs/GaSb design. The LWIR SLS absorber material was then examined more closely for diffusion-limited performance. Simultaneously, a barrier detector was designed for it to combat detrimental dark currents to promote HOT performance, but such design proved to have challenges related to scaling down the pixel size.

3.1 Ga-bearing T2SL (Binary-Binary)

As a starting point, the established InAs/GaSb T2SL material system[46] was used to study the physics of SLS materials for the LWIR in terms of design, modeling, fabrication, and measurement. Research goals aiming to improve the EQE for LWIR detectors based on III-V SLS material systems across the targeted 8 – 10 μm wavelength range provide the initial design inputs for the desired system. Based on these requirements, with the goal of designing a SLS material to absorb across this specific wavelength range, the cutoff wavelength dictates the trade space between layer thickness, indium fraction, and growth temperature for the design of the absorber layer. The absorption coefficient and PL is quantified through the NRL MultiBands™ suite and compared to iteratively optimize these conditions.

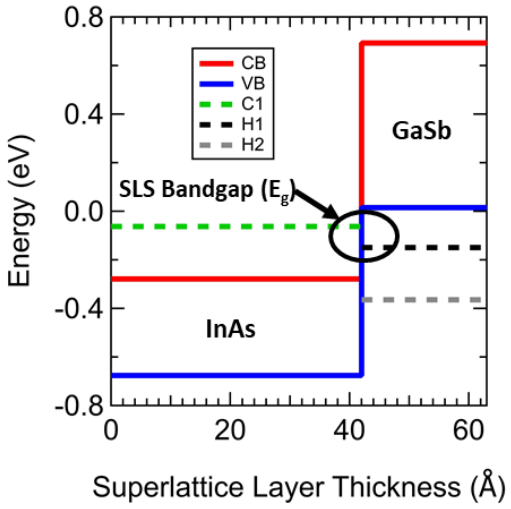

Figure 22. InAs/GaSb (14ML/7ML) SLS material.

The trade space considered for this study also consisted of absorber doping. Doping the absorber increases the carrier concentration, which is advantageous, but comes with challenges due to the vertical mobility of holes in n-type SLS materials and unfavorable surface conduction in p-type SLS materials. For this study, doping the p-type absorber was chosen to enhance the minority electron carriers, knowing the challenge of surface conduction effects for the LWIR SLS materials.

Simulations in NRL MultiBands™ show a focused set of material metrics that address the relationship between the simulated absorber design and the targeted system-level requirements in Table 3. The inputs used for each layer thickness were 14 monolayers (ML) for InAs and 7 monolayers (ML) for GaSb. A growth temperature of 698 K (425 °C) was used to calculate the lattice mismatch between the absorber and GaSb substrate. Typically, the mismatch is represented in parts per million (ppm), but this can be quantified as the percentage of strain that should not exceed 1000 ppm or 1% of the lattice constant.

The temperature was then lowered to 80 K accommodate for the detector operating temperature.

InAs/(In)GaSb Layer Thickness	Indium fraction	Bandgap (eV)	λc (μm)	InSb CBO (meV)	InSb VBO (meV)	Abs coeff. (8μm/10μm)	Mismatch (ppm)
14ML / 7ML	0.0	0.1382	8.97	-40.189	-178.41	840 / 0	-157.4

Table 3. Simulated results for the Binary-Binary InAs/GaSb (14ML/7ML) SLS absorber design.

From these inputs, the calculated bandgap, cutoff wavelength, energy band offsets from InSb, and absorption coefficient are reported. These parameters were chosen to be analyzed based off of their potential to find a SLS absorber design combinations that fit the lattice-matched GaSb substrate, achieved a good and balanced ratio between the layer thicknesses of the heterostructure materials, maintained absorption across the specified wavelength range, and energy band offsets to determine the appropriate barrier detector design for the absorber.

Clearly the Binary-Binary InAs/GaSb SLS design summarized here does not cover the entire required targeted wavelength range out to 10 μm. To extend the cutoff wavelength without compromising the layer thickness ratio, indium is introduced into the GaSb layer. As Smith and Maliholt reported, the LWIR needs a strain compensation to balance the InAs and GaSb layers, and indium is used to accommodate this strain through added composition to attain smaller energy band gaps and longer wavelength ranges.[35] The difference between InAs/GaSb and InAs/InGaSb is the indium fraction within the GaSb layer, giving it a built-in strain balancing that further enhances the absorption coefficient to longer wavelengths by also reducing the layer thickness needed between the layers for optimal quality growth conditions. The layer thickness and material composition were

varied to maximize the absorption across the entire target wavelength range and cutoff wavelengths then are used to extract the absorption coefficient and the photoluminescence of the material. Material metrics are presented in Table 4 with the corresponding absorption coefficients and PL spectra in Figure 23.

	InAs/(In)GaSb Layer Thickness	Indium fraction	Bandgap (eV)	λc (μm)	InSb CBO (meV)	InSb VBO (meV)	Abs coeff. (8μm/10μm)	Mismatch (ppm)
1	14ML / 7ML	0.1	0.138	10.85	-56.55	-170.77	1200 / 700	-1526.31
2	12ML / 10ML	0.1	0.117	10.59	12.95	-104.12	1300 / 600	-93.57
3	13ML / 9ML	0.11	0.097	12.81	-20.47	-117.25	1400 / 1200	-375.47
4	14ML / 7ML	0.2	0.087	14.28	-62.22	-149.03	1400 / 1200	589.25

Table 4. Simulated results for the InAs/GaSb SLS absorber layer designs

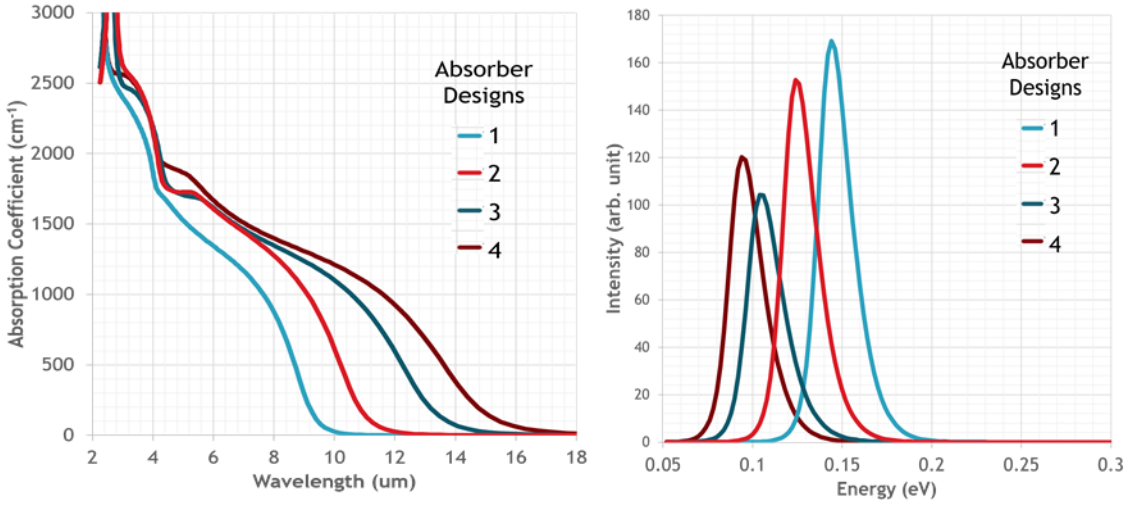

Figure 23. Simulation results for the designed absorber layers of the SLS material systems designs in Table 4. (Left) Comparison of InAs/GaSb SLS absorption coefficients across the LWIR wavelength range. (Right) Comparison of InAs/GaSb SLS PL spectra.

The resultant absorber layer then dictates the barrier layer design based on the simulated bandgap, minority carrier concentration, and energy band offset to match to the barrier material. In particular, the valence band offset from InSb. In particular, the valence

band offset from InSb is important to pay attention to because it can be used to calculate the barrier alignment and the absorber alignment. These barrier-design material metrics are presented in Table 5.

	Barrier Composition and Layer Thickness	Bandgap (eV)	λc (μm)	InSb CBO (meV)	InSb VBO (meV)	Mismatch (ppm)
1	InAs / AlSb SLS 16ML / 5ML	0.4744	2.61	-50.96	-525.36	-2428.41
2	InAs / AlSb SLS 13ML/10ML	0.4943	2.51	37.65	-456.65	49.54
3	InAs / AlSb SLS 15ML / 7ML	0.4243	2.92	-20.19	-444.49	435.29
4	InAs / AlSb SLS 13ML / 7ML	0.5145	2.41	26.53	-487.97	-1000.85

Table 5. Barrier designs corresponding to the absorber designs for the InAs/GaSb SLS absorber study. The combination of the two are used in pBp detector structure simulations.

These detector structure designs were implemented in combination to form a detector structure, and experiments were designed to study the four simulated SLS absorbers and their corresponding detector structure designs. Figure 24 shows an example of the design results of a pBp detector structure, given by NRL MultiBands™ simulations based on the absorber design InAs / ($In_{0.11}$)GaSb (13ML/9ML) and corresponding barrier design InAs and AlSb (15ML/7ML).

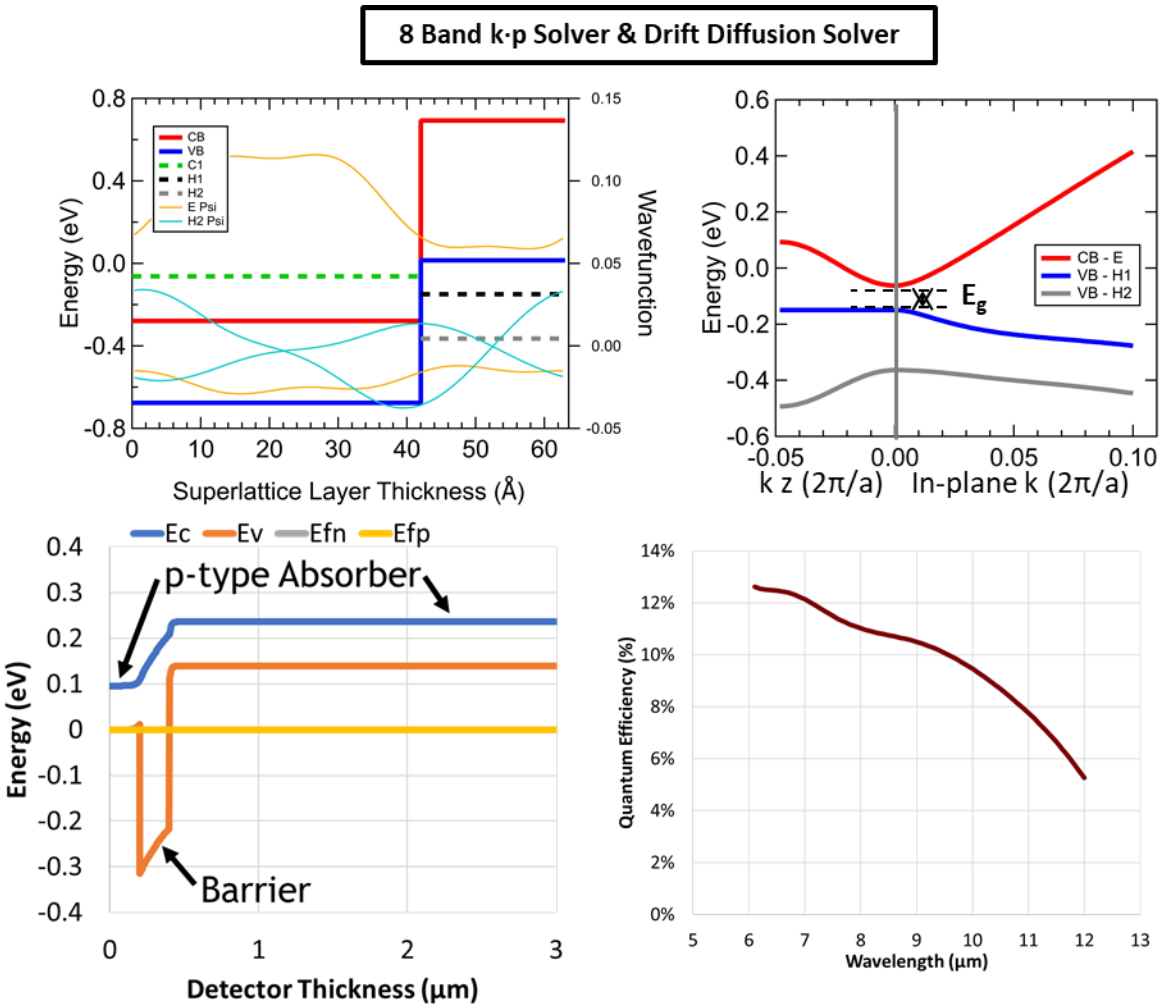

Figure 24. Example of the NRL MultiBands™simulation results for a pBp SLS LWIR detector structure design containing an InAs / $In_{0.11}GaSb$ (13ML/9ML) absorber layer with a barrier layer containing alternating layers of InAs and AlSb (15ML/7ML) for optimal band alignment.

The detector structures were grown, fabricated, and characterized using methods in Chapter 2 to determine their performance. Comparing those results with the simulated detector design have been completed with a PIN detector structure and an nBp detector structure based on this analysis.

3.1.1 PIN

Growths were completed by MBE through collaboration with other research group members to calibrate the growth chamber in preparation for the absorber study discussed above. First, PIN detector structures were grown to study the physics behind the LWIR material absorbers using the simulated Binary InAs/GaSb (14ML/7ML) superlattice system. To keep the absorber system simple and provide quick feedback for the grower, the layer thickness and indium composition were kept at InAs/GaSb (14ML/7ML) with a 0% indium fraction. This system was used as a baseline comparison for the more complex material systems and structures described in the simulation. An example of the structure stack is pictured in Figure 25.

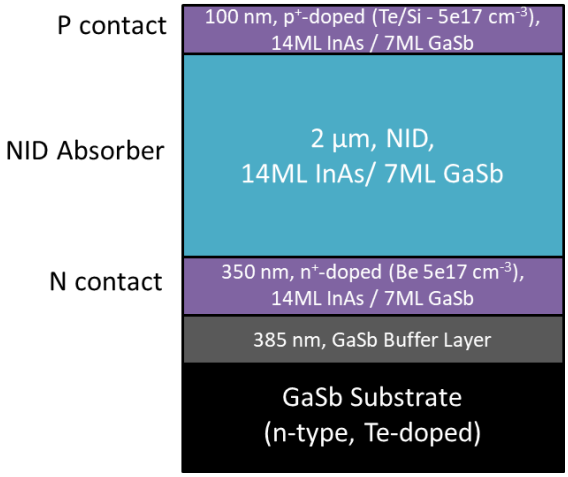

Figure 25. LWIR InAs/GaSb (14ML/7ML) SLS PIN detector structure stack.

The X-Ray Diffraction (XRD) analysis was completed on the PIN structure wafer sample showing lattice mismatch between the GaSb substrate and the epi material grown on top. PL spectral measurements also were taken at 11 K and 77 K to confirm the

InAs/GaSb (14ML/7ML) epi material bandgap. The XRD analysis and the temperature-dependent PL measurements are shown in Figure 26(a), and Figure 26(b), respectively.

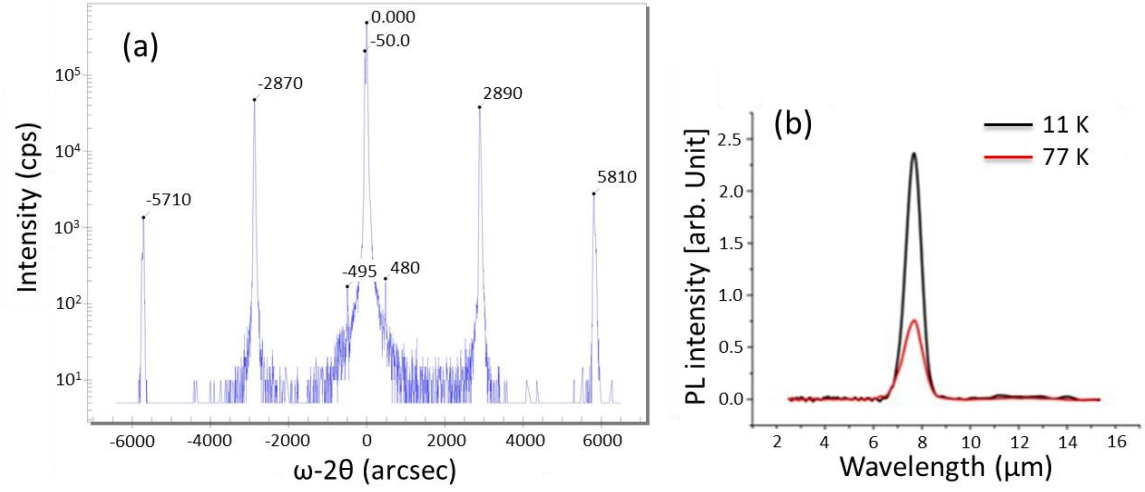

Figure 26. (a) XRD measurement of InAs/GaSb (14ML/7ML) SLS material. (b) PL measurement of the same crystalline material at 11 K and 77 K with a peak intensity corresponding to an 8.1 μm cutoff wavelength.

The XRD results given in Figure 26(a) are congruent with the material structure details of the PIN detector given in Figure 25 to show the periodicity of the superlattice layers. The peaks seen in the plot give the diffraction pattern of the crystalline material where strain and layer thickness are calculated. The XRD indicates the growth completed was strained compressively by about 50 arc sec. This means that the material grown had low mismatch between the InAs and GaSb layers, giving way to an optimal lattice constant and comparably matches the native GaSb substrate. The surface of the semiconductor looked effectively defect free under Nomarski. The XRD, PL, and Nomarski were done in collaboration with other research group members. The measurements of the bare crystalline material help understand the material characteristics favorable to the goal of creating a baseline metric for this study.

The PL intensity, seen in Figure 26(b), is taken during material characterization as well. This measurement provides the bandgap of the material through time-resolved microwave reflectance (TMR) at an operating temperature of 77 K. The plotted data was compared to the simulated data given by the NRL MultiBands™ software, shown in Figure 27(b), resulting in a slight offset in the InAs/GaSb (14ML/7ML) SLS material bandgap prediction by less than 1 um from the predicted 8.99 μm cutoff wavelength to the measured 8.1 μm cutoff wavelength. While this is a shorter cutoff wavelength than expected, the bandgap of the material is within the targeted wavelength range and will be used as valuable feedback to the grower in future growth iterations.

The material was measured optically with Fourier-transform infrared spectroscopy (FTIR) to obtain the transmission properties of the bare crystal, as discussed in Chapter 2. From this measurement, the IR absorption spectrum for the semiconductor material over the IR spectral range is determined, and the absorption coefficient was calculated using the collected data. Figure 27(a) displays both the simulated and measured absorption coefficient spectrums of the InAs/GaSb (14ML/7ML) T2SL PIN detector, which was grown on a single-side polish GaSb substrate wafer. The roughness of the wafer consequently led to a weak absorption response because the high reflections due to surface roughness typically disperses the light needed to collect the transmission spectra. This behavior is indicated through the oscillatory wave pattern within the measured results around the MWIR region and is pointed out in Figure 27(a). Other peaks in the absorption coefficient, specifically in the SWIR wavelength region are band transitions of the SLS heavy-hole and light-hole mini bands to the conduction band.[58]

The measured data was taken at room temperature (295 K), resulting in the overall shape of the simulated data as expected, where higher absorption is observed at the shorter wavelengths and the absorption coefficient is measured to be about 5000 cm^{-1}. The absorption coefficient is measured to be about 1100 cm^{-1} at 6.5 μm (as expected), with an eventual cutoff close to the bandgap and corresponding cutoff wavelength of 8.1 μm. Cooling the material to 77 K would enhance the signal to give a closer comparison to the simulated absorption coefficient curve.

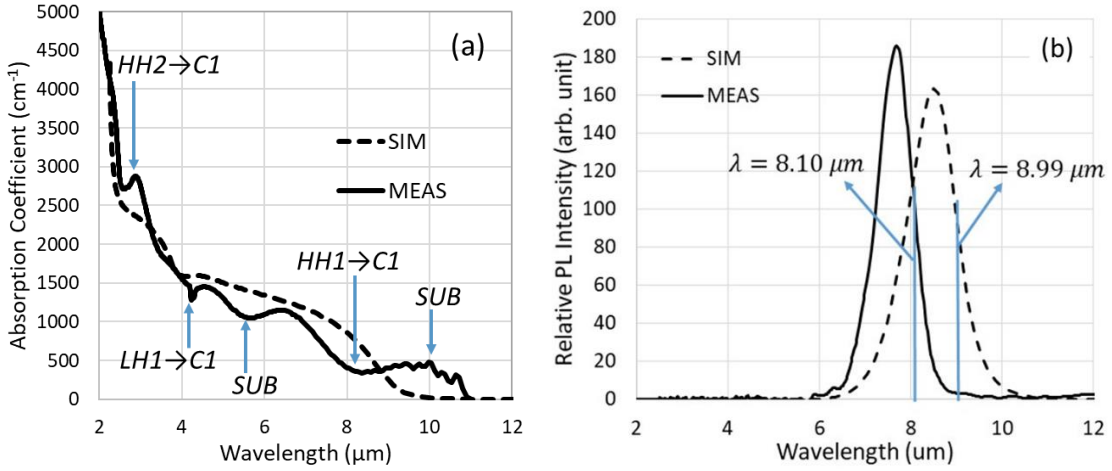

Figure 27. (a) Simulated and measured absorption coefficient for the InAs/GaSb SLS PIN detector. SUB is used to signify substrate roughness artifacts due to the single-sided polish substrate. (b) Simulated and measured photoluminescence (PL) measurement for the PIN detector.

The detector fabrication process of the bare crystalline material into diode structures for electrical and optical testing was completed. This process included photolithography, wet etching, and contact deposition to form various-sized diodes ranging from 50 μm to 1000 μm detector areas using a simple mask set. These detectors were cooled and tested for their dark current and spectral quantum efficiency performance using the cryostat and test setup described previously in Chapter 2 under detector characterization.

Figure 28 shows the preliminary dark current results at 80K for two of the detectors tested. These results show good diode rectification in reverse bias at low temperatures, but the dark current density is still high on the order of 10 mA/cm^2. Spectral measurements described in Chapter 2 were completed at an operating temperature of 80 K to determine the PIN detector photocurrent at a bias voltage of -0.1 V. The spectral quantum efficiency (QE) was calculated, with those results in Figure 28, affirming the 8 μm cutoff wavelength and overall detector response across the 2 μm – 10 μm wavelength range.

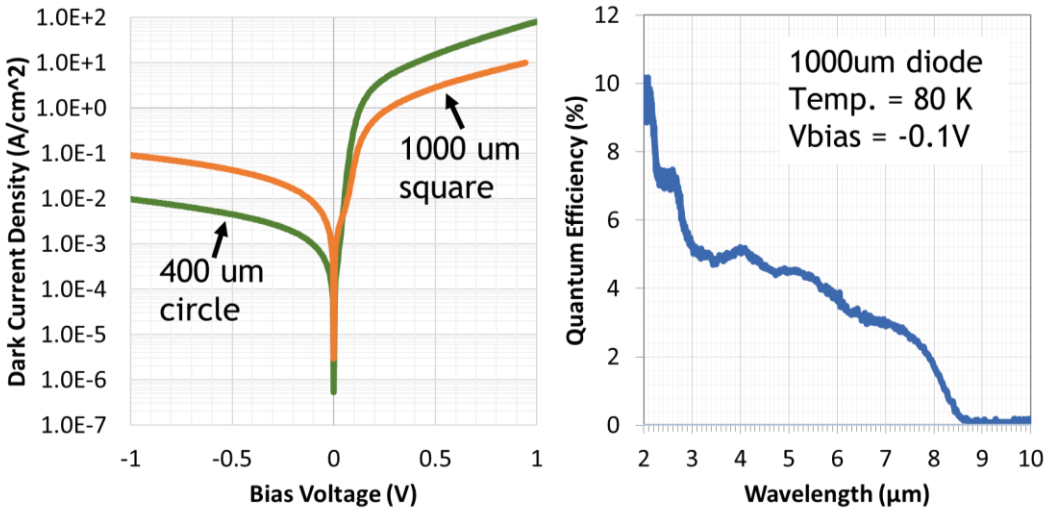

Figure 28. Dark current and resultant spectral QE of the InAs/GaSb SLS PIN detector.

As predicted, however, LWIR material has poor dark current characteristics at room temperature and responded as ohmic or shunted due to the higher temperature. This should be improved with the planned complex structures with the barrier designs to give higher operating temperature and quantum efficiency.

3.1.2 nBp

The design of experiments to study the four simulated LWIR SLS detector structure designs were examined using the same simulation techniques through NRL MultiBands™ to address the need for more focused research on the absorber itself. A diffusion length study of the baseline InAs / GaSb (14ML/7ML) absorber was proposed. By understanding the diffusion length, the absorber layer thickness can be changed to achieve the best performance from the proposed barrier detector structures. The nBp detector structure was chosen to complete this study because the n-type contact would allow for a good top contact while also allowing the p-type absorber to be unaffected by the rest of the detector stack. The growth of the nBp detector stack in Figure 29 was completed by MBE using the simulated and measured Binary InAs / GaSb (14ML/7ML) superlattice system studied in the previous PIN detector structure section.

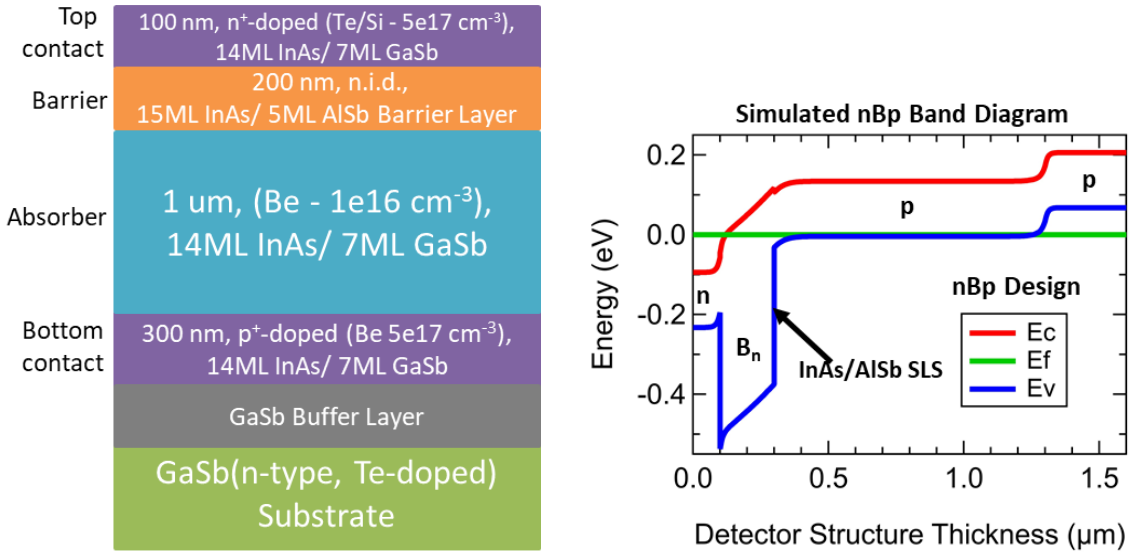

Figure 29. LWIR InAs / GaSb (14ML/7ML) SLS nBp detector structure stack and simulated band diagram.

XRD results given in Figure 26(a) are used as feedback for the grower to optimize the conditions for the growth of the nBp detector. The same also can be said for the PL given in Figure 26(b). These measurements are not typically done on detector structure stacks due to the variability between the absorber layers and the barrier layer in the stack; therefore, any results coming from these measurements would not have any consistency.

The detector structures were fabricated from the bare crystalline material for electrical and optical testing. The processing follows the PIN detector processing and includes photolithography, wet etching, and contact deposition to form various-sized diodes ranging from 50 μm to 1000 μm detector areas using a simple mask set. These detectors were cooled and tested using a cryostat and testing setup described in Chapter 2 discussing detector characterization.

As discussed above, the barrier detector structure should improve the operating temperature and QE of the LWIR material. Unfortunately, the dark current results remained high for the nBp detectors to the point where the IV characteristics measured ohmic behavior even at cryogenic temperatures (80 K). Despite completing the fabrication on the bare crystal twice, the shorted behavior observed when measuring the detector IV curves persisted. The subsequent modeling describes why these detectors might be shorting.

3.1.3 Analysis of Inversion

The following analysis deliberates the possible explanation for the ohmic behavior observed during the nBp measurements. According to the NRL MultiBands™ simulations presented for the nBp detector structure, the detector should have given better rectifying results and reduced dark currents compared to the pin dark current results in Figure 28(a).

However, if the growth conditions are off and absorber doping concentration is higher than anticipated, an inversion of the absorber layer will occur. Another possibility may be that the fabrication process is affecting the material because the detector was not passivated during detector processing. In either case, the simulated data showing a p-type absorber is incorrect. A new set of simulations were run to understand what would happen to the detector under the condition that the absorber layer is n-type and can be found in Figure 30 as it effects the heterostructure detector band alignments and in Figure 31 regarding the dark current density over the full bias range.

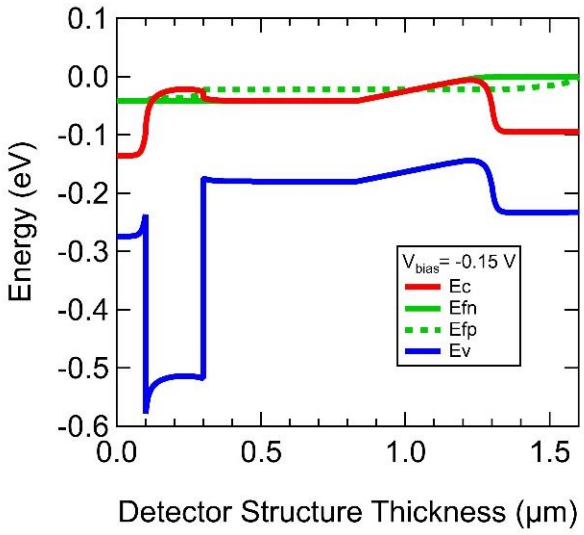

Figure 30. Simulated band diagram of the nBp detector structure at a reverse bias voltage of -0.15 V with n-type surface conduction, leading to an inversion of the absorber layer from p-type to n-type.

Upon further investigation, we discovered that the inversion can be simulated with NRL MultiBands™ to confirm the hypothesis that the ohmic behavior seen during IV measurement comes from the inversion of the p-type absorber design to an n-type due to the accumulation of charged carriers on the surface of the detector sidewall because the

detector was not passivated during fabrication. Results of the simulated band diagram in Figure 30 indicate how the resultant detector blocks the minority carrier electrons from flowing through the detector design as intended. The measured dark current was compared to the simulated dark current results, showing good agreement between the surface-limited absorber theory, essentially showing the inverted type absorber to have ohmic properties over the desired rectifying properties of the ideal simulation of the nBp design.

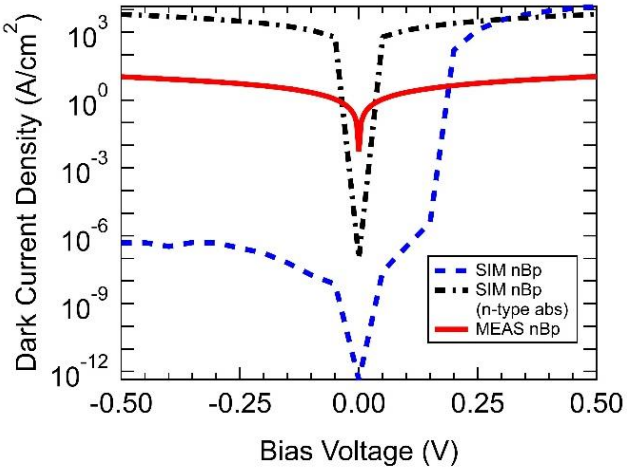

Figure 31. The simulated dark current as a result of the absorber layer n-type inversion during the nBp structure demonstration.

The inversion of the absorber layer from p-type to n-type seen by the nBp detector conveys the importance of doping and surface effects on these small bandgap materials and detectors. This leads to an important conclusion that fully delineating the barrier detector unintentionally inverts p-type absorber designs, confirming previous p-type absorber research, and was confirmed in this work to also occur in p-type InAs/GaSb LWIR SLS absorbers. Fortunately, some recovery efforts have been explored for these types of situations, particularly for p-type absorbers, regarding the mitigation of the surface current effects on the detector operation. The detector surfaces will be discussed in Chapter 4.

3.2 Ga-bearing T2SL (Ternary-Ternary)

Initial efforts to explore the SLS material systems for the LWIR first showed that only certain layer thicknesses and ternary compositions could be used to optimize the absorption coefficient, energy band offset, and lattice mismatch in order to achieve high spectral EQE performance. To influence future barrier detector designs and alleviate growth challenges of LWIR SLS materials, a ternary-ternary InAsSb/GaAsSb SLS heterostructure design was proposed with a high Sb fraction within the detector. By fixing the Group-V parameters for the As and Sb compositions, the growth conditions aim to theoretically promote easier shutter sequencing.

Simulations were conducted and summarized in an absorber study that was focused on using the NRL MultiBands™ *k·p* modeling tool to explore absorbers that have the InAsSb-GaAsSb ternary-ternary superlattice compositions with a high antimony (Sb) fraction ranging from 35% to 57% as summarized in Table 6. In the former T2SLbinary-binary study, the Sb fraction was kept low to minimize the lattice mismatch between the superlattice absorber layer and the GaSb substrate, but the design requirements needed to be changed when MBE growth conditions were not allowing for small fractions of Sb (on the order of 10% to 12%) to be controlled easily.

These SLS material systems intended to act as the absorber region within a LWIR detector. The resulting matrix also shows key properties known to indicate high EQE performance between 8 – 10 μm wavelengths, such as cutoff wavelength (calculated through the bandgap) and lattice mismatch.

InAsSb / GaAsSb Layer Thickness	Indium fraction	Bandgap (eV)	λc (μm)	InSb CBO (meV)	InSb VBO (meV)	Mismatch (ppm)
27ML / 7ML	0.3	0.2617 (D) 0.1314 (I)	4.7 9.4	-129.1 -129.1	-390.81 -260.49	169.7
20ML / 7ML	0.35	0.2698 (D) 0.1559 (I)	4.6 8.0	-75.89 -75.93	-345.68 -231.83	120.38
20ML / 15ML	0.50	0.2129 (D) 0.1320 (I)	5.8 9.4	72.35 72.352	-140.58 -59.62	-110.85
16ML / 16ML	0.57	0.2558 (D) 0.2013 (I)	4.8 6.2	165.06 165.06	-90.76 -0.03621	324.4

Table 6. Simulated results for the InAsSb/GaAsSb SLS absorber layer designs. Each design has two different sets of data showing the results using the direct bandgap, designated as (D) and indirect bandgap (I).

These distinct layer thicknesses and material compositions pose an interesting situation where the GaAsSb tie line seems to give an indirect bandgap when the Sb fraction is around 50%. The small range in the GaAsSb ternary compositions where the tie line shows a possible indirect bandgap in the band energy versus lattice constant diagram was used to determine the bounds of the study. The InAsSb composition was left the same throughout the study to compare the SLS absorber designs by layer thickness and variation of the GaAsSb composition layer. Both the Sb fraction and the layer thicknesses were varied to maintain low lattice mismatch in parts per million (ppm) while also monitoring the resultant bandgap between the energy bands in momentum space (k-space). The valence band maximum and the conduction band minimum were used to calculate bandgap, regardless of their location in the semiconductor k-space.

The SLS heterostructure provided favorable preliminary results, which indicated a possible direct-to-indirect bandgap transition that has not been previously explored, especially for the InAsSb/GaAsSb SLS with an Sb fraction of 50%. Preliminary results of the proposed designs also show a type-I band alignment that can be viewed in Figure 32.

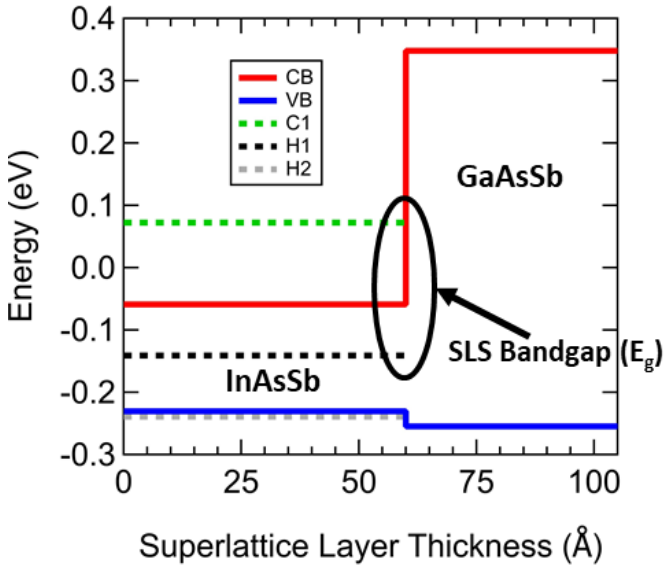

Figure 32. Band alignment of InAsSb and GaAsSb (20ML/15ML) at 50% Sb fraction. NRL MultiBands™ simulations show that all the new ternary-ternary designs have a Type I band alignment, which allows for the possible rise in hole mobility.

A literature survey was completed to understand any reporting on the SLS superlattice (InAsSb/GaAsSb). While MWIR SLS detectors using ternary SLS materials has been demonstrated,[58] few results indicate these ternary-ternary SLS compositions have not been studied for LWIR applications. Therefore, the two superlattice layers of InAsSb and GaAsSb were used to produce the feasibility of a LWIR absorber.

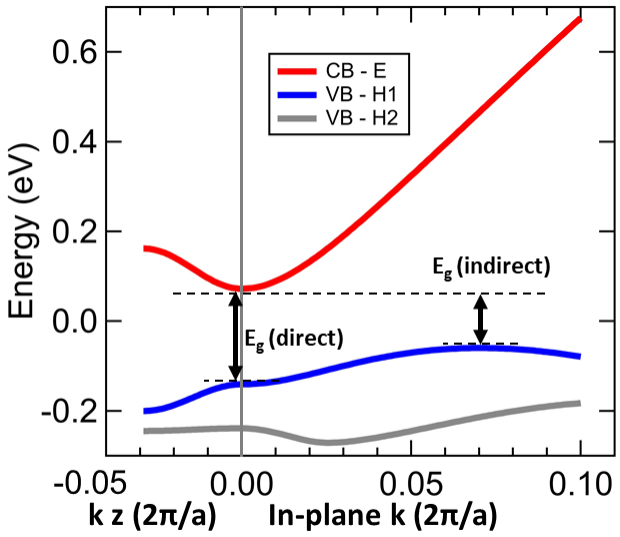

Figure 33. Simulation results for the Ternary-Ternary SLS material containing alternating layers of InAsSb and GaAsSb (20ML/15ML) at 50% Sb where the Energy versus momentum (k) space diagram shows the direct transition and the indirect transition.

Results show two band transitions that may indicate the superlattice has an indirect bandgap, but the tool only reveals the direct transition at k = 0 during the calculation. The absorption coefficient cannot be calculated due to the nature of the *k·p* calculations being using in the NRL MultiBands™ suite. One of the reasons this could be the case is because of the Type 1 band alignment of the two superlattice layers. The Type 1 band alignment can be misleading when it comes to cutoff wavelength and resultant bandgap; however, it can be favorable when the minority-carrier hole mobility is larger. An example of these band alignments can be found in Figure 32.

A preliminary detector design was also proposed and simulated to prove the InAsSb/GaAsSb heterostructure can be used in a viable barrier detector. The nBn detector was designed using the InAsSb/GaAsSb (20ML/15ML) heterostructure absorber layer design with a 50% Sb fraction. The barrier of the detector was designed with a proven

barrier layer, a $(AlAs_{0.08}Sb_{0.92})_{0.05}(GaSb)_{0.95}$ quaternary, whose composition is lattice matched to GaSb.

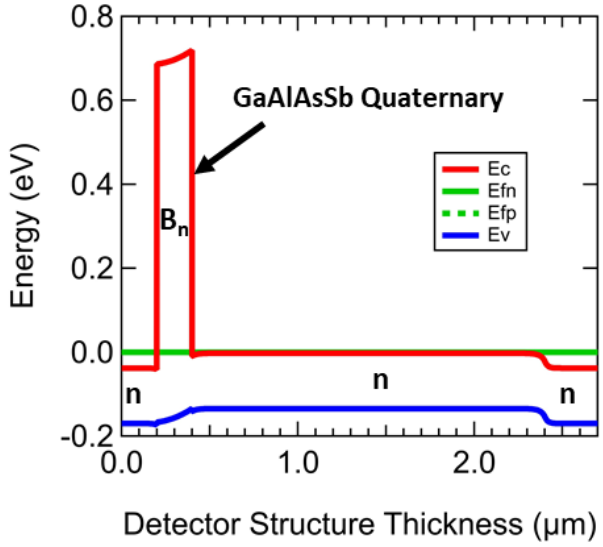

Figure 34. Band structure using the proposed InAsSb/GaAsSb (20ML/15ML) with 50% Sb fraction heterostructure absorber layer design with a nBn barrier detector using a $(AlAs_{0.08}Sb_{0.92})_{0.05}(GaSb)_{0.95}$ quaternary barrier layer whose composition is lattice matched to GaSb.

These preliminary results show that this design needs to be reviewed further, but the nBn detector structure to understand the band offset and possible barrier detector designs for moving forward with this research in the future. Validation with another simulation tool needs to be done to determine if the *k·p* calculation was reached in error, but there is strong evidence that if the material can produce a weak PL peak at the longer wavelengths, there is evidence that there is an indirect transition occurring in the superlattice absorber. These designs will require more research to understand the advantages involved in the ternary-ternary design, but growing, fabricating, and testing the proposed barrier detector design will help realize an alternate solution to the growth

challenges faced when developing LWIR detectors and would be incredibly useful establish the viability of the ternary-ternary design to the community.

3.3 Summary

In summary, the designs presented in this chapter demonstrate how heterostructure detectors based on SLS materials are viable options for detector performance across the LWIR spectrum. Through SLS heterostructure engineering, several unipolar barrier nBp detectors using the binary-binary InAs/GaSb and InAs/(In)GaSb, and the ternary-ternary InAsSb/GaAsSb SLS material systems were designed and simulated using NRL MultiBands™.

A baseline study was conducted using the well-studied 14ML/7ML InAs/GaSb T2SL heterostructure, to which a pin detector and a unipolar barrier nBp detector were grown, fabricated, and tested. The measured results were compared to simulations retrieved from the NRL MultiBands™ *k·p* modeling tool to understand the differences between the simulated ideal detector behavior and the behavior of the as-grown devices. Results from the baseline pin structure show good agreement with the simulations, but the dark current density was too high and the EQE was too low to be considered for future FPA development.

By optimizing the detector design to include a barrier in the detector stack, the nBp detector was simulated to reduce the overall dark current observed during the pin detector study. The nBp detector design was grown, fabricated, and measured, but dark current results of the as-grown sample were ohmic due to the surface effects created by the fully delineated pixel, which ultimately inverted the intended detector design. This lead to an

important conclusion that fully delineating the barrier detector unintentionally inverts p-type absorber designs, confirming previous p-type absorber research, and was confirmed in this work to also occur in p-type InAs/GaSb LWIR SLS absorbers.. It was also discovered that the inversion can be simulated with NRL MultiBands™ to show how the resultant detector blocks the minority carrier electrons from flowing through the detector design as intended.

To influence future barrier detector designs and alleviate growth challenges of LWIR SLS materials, a ternary-ternary InAsSb/GaAsSb SLS heterostructure design was proposed with a high Sb fraction within the detector. By fixing the Group-V parameters for the As and Sb compositions, the growth conditions aim to promote easier shutter sequencing. Simulations using NRL MultiBands™ across a range of As and Sb fractions of 35% to 57% for the InAsSb/GaAsSb SLS heterostructure provided favorable preliminary results, which indicated a possible direct-to-indirect bandgap transition that has not been explored, especially for the InAsSb/GaAsSb SLS with an Sb fraction of 50%. These designs will require more research to understand the advantages involved in the ternary-ternary design, but growing, fabricating, and testing the proposed barrier detector design will help realize an alternate solution to the growth challenges faced when developing LWIR detectors and would be incredibly useful establish the viability of the ternary-ternary design to the community.

We conclude these studies with several paths forward to further optimize these designs for future LWIR detector structures, including the use of passivation. The inversion from a p-type absorber to a n-type absorber seen by the nBp study conveys the importance

of surface effects on these small bandgap materials and detectors. For the LWIR, this inversion can occur more prominently as detector pixel pitch shrinks; therefore, surface currents impacting the detector performance also should be considered because attempts to mitigate these effects using only detector design is not enough. Investigation of these surface effects is presented in Chapter 4 to show the negative consequences on IR detector performance is mitigated. Future work based on these conclusions will also be discussed in Chapter 7.

4 Surface Passivation for Photodetectors

In Chapter 3, improvement to the spectral QE and overall performance of LWIR FPAs through materials research was discussed at length. Specifically, the challenges and advantages of using antimonide-based SLS materials for IR detectors was addressed, however, surface dark currents still evade resolution. T2SL structures have demonstrated dramatic improvements in performance, including their quantum efficiency, dark current, and noise equivalent differential temperature (NEDT).[10] In the models from Chapter 3, the LWIR SLS absorbers were able to demonstrate good improvement of these performance measures through the use of extremely small bandgaps. However, there are physical limitations to these devices when higher operating temperatures or small pixels for high-density FPAs are required.

As T2SL IRFPA pixel dimensions shrink, there is an increase in the individual detector surface-area-to-volume ratio, as well as increase in the contribution of surface current to the overall detector leakage current.[2] The increased surface current contribution from the larger surface-area-to-volume ratio dominates the dark current of these smaller pixels (<100 μm^2), making it difficult to reach HOT conditions due to large dark currents. The surface current is symptomatic of a number of mechanisms occurring including conductive native oxide accumulation on the sides of the pixel mesas, Fermi level pinning, and interfacial trap states, all of which are physical limitations that negatively affect overall device operation.[71-73]

This chapter will address these physical limitations through several means. First, the individual detector pixel fabrication and the detector surface chemistry will be

discussed to show what research has been done to understand the surfaces of SLS materials by studying their native oxides. Then, the fabrication processes will be discussed, and solutions presented that use passivation techniques to improve the performance of these detectors. Furthermore, the process of measuring passivated detector performance is explored to give needed detail into the device interface performance, which ultimately contributes to the overall performance of the detector.

4.1 Detector Structure Surfaces and Interfaces

As previously discussed in Chapter 3, SLS IR detectors are composed of a complex system of alternating layers of semiconductor material to make structures like pin diodes and barrier heterostructures. By including a barrier in the detector stack of the heterostructure, we can achieve higher operating temperatures using SLS material as it suppresses detrimental dark current mechanisms in the material itself. An example of a heterostructure stack is displayed in Figure 35(a), showing the different layers of material grown using MBE on a GaSb substrate.

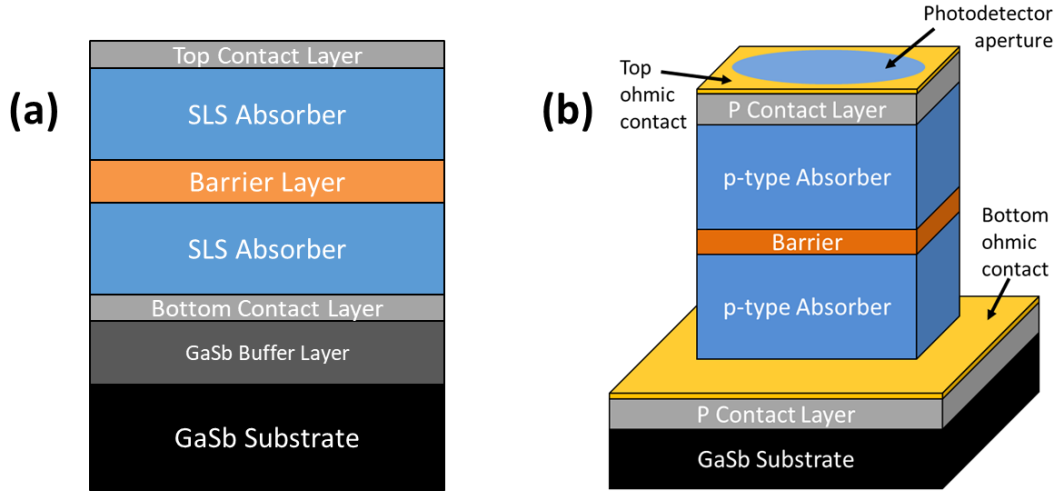

Figure 35. (a) Schematic barrier detector heterostructure stack as grown on a GaSb substrate by MBE. (b) Schematic of a fully delineated detector pixel after fabrication processes are performed on the detector stack.

With the superlattice structure grown to the desired specification, the resultant wafer then is processed into individual pixel detectors using standard lithography techniques as described in Chapter 2. A summary of the detector structure fabrication process also is outlined in the process diagram in Figure 36 for a process steps to fabricate a variable area diode array (VADA) of single pixel detectors.[9, 74]

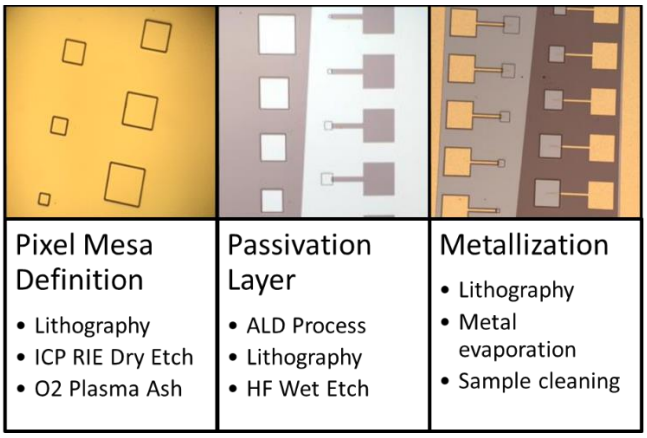

Figure 36. Summary of general fabrication process steps to fabricate a variable area diode array (VADA) of single pixel detectors to understand the passivation performance.

In the pixel mesa-definition process, etching exposes the layers of the superlattice material. This exposure forms features called mesas, which eventually become the individual detector pixels. These mesa features take the general form of a cube, as seen in Figure 35(b), which include sidewall interfaces and a top interface. During fabrication, the mesa delineation from either dry or wet etching creates a discontinuity of the periodic crystal structure. This results in the formation of unsatisfied chemical bonds on the etched surfaces, explained schematically in Figure 37.

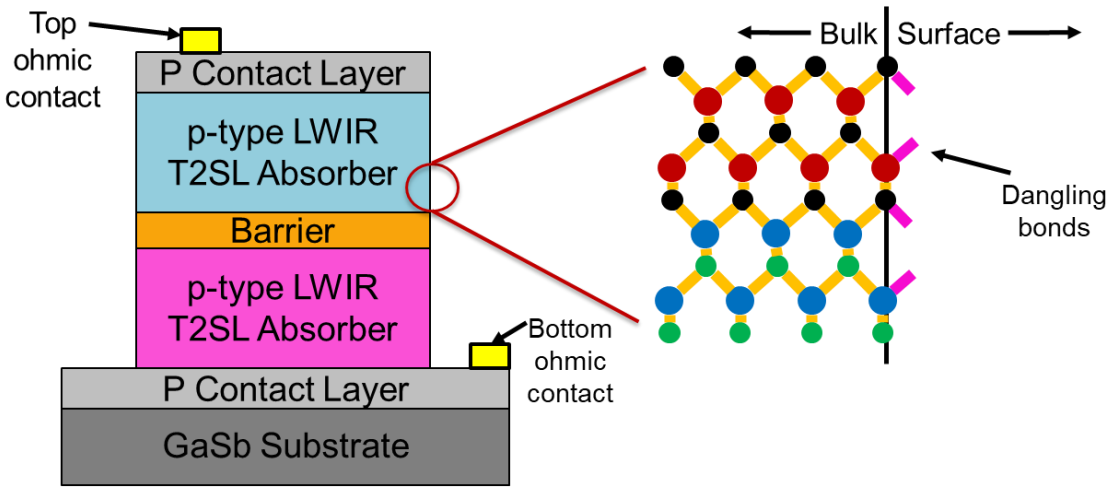

Figure 37. Unsatisfied chemical bonds (dangling bonds) are created due to the process of etching and mesa delineation, which disrupts the periodic crystal structure of the semiconductor material.

The cleanly etched surfaces are highly reactive. When the dangling bonds on these surfaces are exposed to small amounts oxygen and hydrogen, they are satisfied via oxidation by these atmospheric elements. Unfortunately, the oxygen reacting with the unsatisfied dangling bonds causes conductive accumulation of excess carriers on the sides of the mesas, forming a degenerate, n-type surface layer. In this layer, the oxidized material forms a native oxide layer, and has been reported in literature on III-V materials such as GaSb.[63] When these conductive native oxide layers form on the surfaces of the mesas, the resulting native oxides and resulting accumulation of excess carriers create conduction pathways that unintentionally shunt the intended bulk conduction of the detector.[75]

Figure 38 shows the energy band diagram at the sidewall of the detector, which gives an understanding of the band bending occurring between the bulk and the surface of the detector material when the carrier accumulation at the surface occurs. Here, we can also show, through the bulk-to-surface energy level alignment in the band diagram, where

Fermi level pinning occurs that essentially creates a two-dimensional electron gas (2-DEG) region on the pixel sidewall surface.

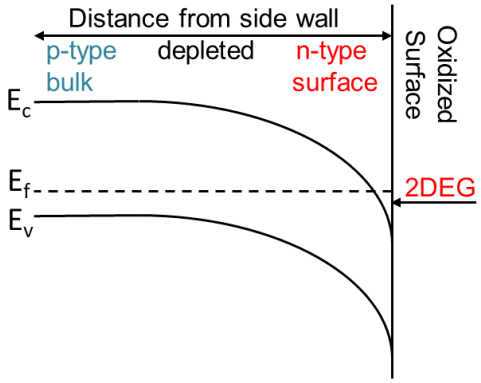

Figure 38. Band diagram showing band alignment at the surface of the sidewall where the accumulation layer builds into the 2-DEG observed at surface.[75]

These large densities of defect states are an unavoidable property of the surface of practical detectors. Electrically, this behavior can be considered the equivalent circuit of the surface current and bulk current pathways due to a shunt resistance in Figure 39(a). The unintended carrier accumulation on the surface can be represented as a resistor (r_{shunt}) running in parallel with the bulk diode structure as shown in Figure 39(b).

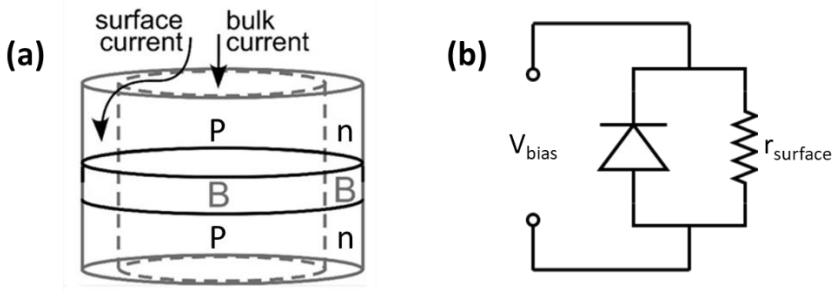

Figure 39. (a) Schematic of a fully delineated detector pixel showing surface current and bulk current pathways due to shunt resistance. (b) Equivalent circuit diagram showing the two pathways of conduction in a delineated detector pixel.

Additionally, these oxides diminish the overall detector performance because the carrier conduction path, as a result of unsatisfied dangling bonds along the exposed

surfaces, runs parallel to the bulk current, therefore the surface leakage current additively contributes to the overall dark current of the detector, leading to the possibility of shorted non-operative detectors in an FPA. This natural reactivity has led research efforts to concentrate on how to minimize the formation and impact of these oxide layers on the device performance during the fabrication process.[9, 38, 76] The idea is to create an intentional passivation layer over the detector surface to improve the performance of the pixel, rather than diminish it, as seen in Figure 40.

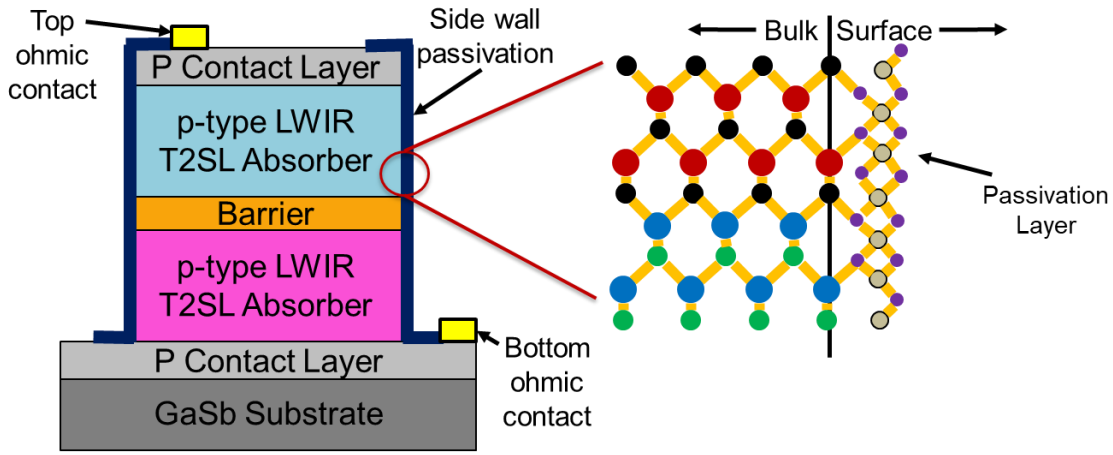

Figure 40. By creating a passivation layer on the pixel sidewall, the dangling bonds are satisfied, reducing conductive surface carriers, and unpins the Fermi level energy band.

Passivation of the mesa sidewall on these infrared detector pixels inherently recuperates the depreciated performance of the detectors by satisfying the dangling bonds and reducing the surface energy associated with the conductive surface charge carriers accumulated along the detector sidewall.[73, 76] The effects from the unintentional shunt from the surface conduction (r_{shunt}) is reduced as depicted schematically in Figure 41(b), and the bulk-to-surface energy-level alignment in the band diagram changes through the

unpinning of the Fermi level. The 2-DEG region no longer exists along the pixel sidewall as presented in Figure 41(a).

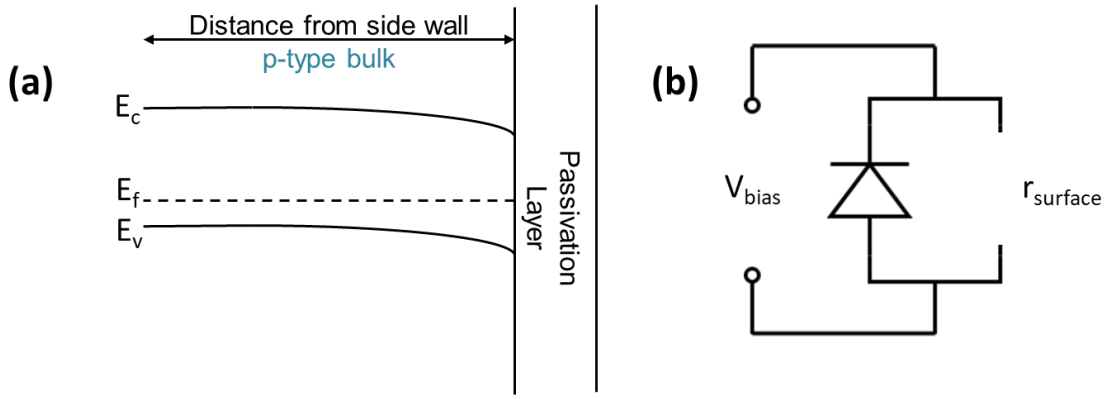

Figure 41. (a) Band diagram showing band alignment at the surface of the sidewall where the passivation layer relieves the 2-DEG observed at the surface. (b) Equivalent circuit diagram showing the reduced r_{shunt} in a delineated detector pixel.

Effective surface passivation is critical to ensuring that the surface leakage does not become the dominant noise source in the detector. If surface effects dominate the noise, the detector element will not operate at higher operating temperatures because the overall dark current will be higher. The detector will not be able to operate at smaller diode areas for the desired benefits when it comes to moving to large format, high pixel density FPAs.

Native Oxides

Native oxides are abundant in superlattice materials due to the semiconductor chemistry involved in the material structure composition in the superlattice and how reactive each of the chemical compositions are upon exposure to air. [71, 77].[77] For example, the high oxidation rate of GaSb yields an interfacial oxide layer composed of native oxides, such as Ga_2O_3 and As_2O_3, shown by the reaction:

$$2GaSb + 3O_2 \rightarrow Ga_2O_3 + Sb_2O_3.$$[78]

These bonds naturally form on the GaSb because their enthalpy reaction is very high which creates a thin layer of new oxide compound on the semiconductor surface. This is also the case for other elements that make up the T2SL material systems, like InAs. This high reaction enthalpy is inversely proportional to the Gibbs free energy of the chemical compound: the lower the Gibbs free energy, the more reactive the compound is because of the minimum amount of energy required to start a reaction. The formula of this relationship is shown in Eq. (4.1) as:

$$\Delta G = \Delta H - T\Delta S \tag{4.1}$$

where (ΔG) is the Gibbs free energy that is associated with a chemical reaction used to do work. The total energy of a system in (4.1) is the sum of the change in enthalpy of formation (ΔH) with the product of the change in entropy (ΔS) and the temperature of the system (T) in Kelvin. A comparison of specific native oxides and their thermodynamic properties are found in Table 7.

Energies of Formation Thermodynamic Data		
Oxide	***ΔH° (kJ/mol)***	***ΔG° (kJ/mol)***
In_2O_3	-925.7	-830.7
As_2O_3	-657.4	-576.1
Ga_2O_3	-1089.0	-998.3
Sb_2O_3	-898.5	-
Al_2O_3	-1675.7	-1582.3
ZnO	-350.5	-320.5

Table 7. Comparison of thermodynamic properties of SLS oxides, along with aluminum (Al2O3) and zinc (ZnO) oxides for reference.[79-81]

The larger thermodynamic enthalpy of formation is indicative of how reactive the compound is due to the amount of energy available to start a reaction. Once the native oxide enthalpy of formation and Gibbs free energies are compared to the enthalpy of

formation and Gibbs free energies of the passivation material, as shown in Table 7, there is an obvious correlation with reactivity and the change in enthalpy of formation that can be leveraged. Salihoglu *et al*. observed that the Gibbs free energy of Al_2O_3 is lower than all oxides and all surface native oxides investigated in the study when demonstrating improvement in surface leakage current in InAs/GaSb T2SL MWIR detectors using different dielectric passivation materials.[76, 82] Therefore, not only should good passivation materials satisfy the dangling bonds and clean the surface of native oxides, but they should also protect the surface against the environment. Thus, choosing a passivation material with a lower Gibbs free energy than the material's native oxides will be more energetically preferred than other potential reactions available.

4.2 Atomic Layer Deposition Passivation

To prevent the native oxide accumulation and reduce the surface current contribution to the dark current, the pixel typically is encapsulated with a wide bandgap dielectric material to create an intentional passivation layer. Since the detectors are small, the passivation layer needs to be thin, conformal, and non-conductive. This can be done in several ways during detector fabrication either as treatments or as a coating including, but not limited to:

- Coating the surface of the detector with polymer materials
- Treating the surface with a hydrogen-based processes like (H_2S)
- Chemical Vapor Deposition (CVD)
- Atomic Layer Deposition (ALD)
- Annealing the sample at high temperatures

- Re-growth of other semiconductor layers through MBE on the detectors

Several groups have reported their success in passivating III-V SLS semiconductor materials as a solution to mitigate the leakage current from the side walls of the detector that is affecting the overall device dark current. Kim *et al*. exhibits how, a polymer (SU-8) passivation of a single pixel superlattice detector lowers the dark current density compared to the unpassivated superlattice detector, which inadvertently contributes to the improvement of the overall focal plane array (FPA) dark current performance.[38] Salihoglu *et al.* presents how the different passivation materials using ALD onto the superlattice detector lowered the dark current of the device by three orders of magnitude from the unpassivated detector dark current measurement.[76] The materials and surface treatments explored are numerous, but all have one underlying theme of lowering the dark current to improve small pixel, detector performance.

Now that there is an understanding that passivation layer should be a good dielectric material to avoid introducing additional conductive channels at the surfaces[83] and that several fabrication techniques can be employed to install passivation layers onto the detectors, we will explore one particular passivation technique using ALD.

ALD is an intentional passivation fabrication technique. ALD coats the mesas monolayer by monolayer to promote a good insulating layer with a high-dielectric material to control the electrical behavior of the side walls in a structure similar to the structure in Figure 35.[77] George *et al.* states that no other thin-film technique can approach the conformality achieved by ALD on high aspect structures because of the self-limiting, efficient growth. An illustrative figure of how the ALD process is performed is shown in

Figure 42. This process typically is completed in a reactor deposition system that uses metal organic precursors and de-ionized water (H_2O) in pulsed, cyclic steps to form the thin-film layer of the material.

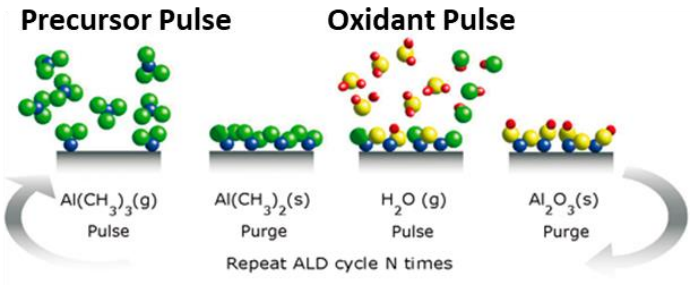

Figure 42. Schematic representation of ALD process flow using self-limiting surface chemistry in a binary reaction sequence between the TMA precursor pulse and the H2O oxidant.[84]

As shown in Figure 42, the sample initially is heated to a high temperature in the reactor to encourage the chemical reactions that will take place on the surface of the detector mesas. The metal organic precursor is pulsed into the chamber and given a specific settling time to rest onto the sample. The oxidant then is pulsed into the chamber and reacts with the precursor. The oxidant also is given a settling time to allow for a complete reaction to take place. This completes one cycle of the ALD and leaves a single monolayer about 0.1 nm thick of the desired resultant deposited material. Alternating the exposure of the precursor and oxidant cyclic process can be repeated until the material reaches the desired thickness.

The process can be varied in several ways, including the type of precursor used, the settling time, the sample temperature, etc., to achieve the best conformal and uniformly deposited thin film of material for passivation. Therefore, we can take advantage of the

ALD process and deposit a conformal passivation material onto complex mesa structures created for infrared detectors.[77]

4.3 Passivation Study Using Aluminum Oxide

Effective passivation of T2SL devices recently was demonstrated using ALD to deposit Al_2O_3 onto a p-type LWIR SLS detector. In this study, we investigated the use of ALD to treat the device sidewalls of a LWIR pBp InAs/GaSb T2SL detector using Al_2O_3. The detector structure was grown commercially by MBE to form a dual-band LWIR pBp detector design with cutoff wavelengths of 9.5 µm and 11.5 µm as seen in Figure 43(a).

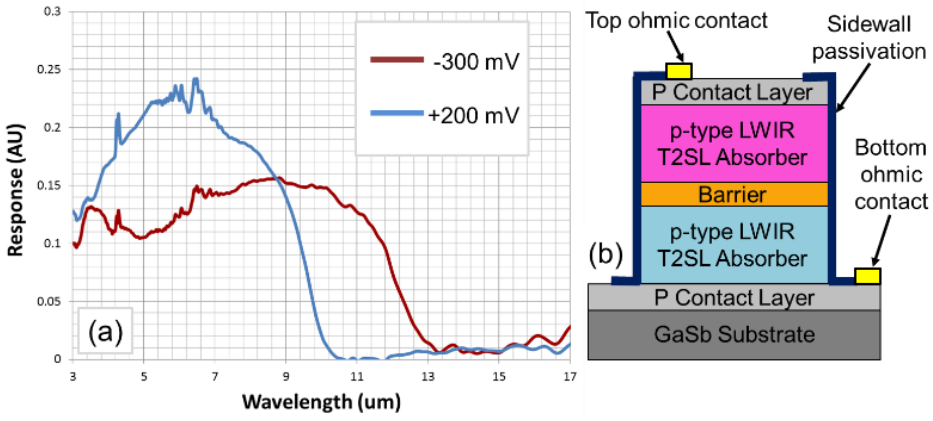

Figure 43. (a) Spectral response of dual-band LWIR T2SL pBp detector at specified voltage biases for the targeted wavelengths. (b) Overall single pixel photodetector structure including sidewall passivation.[73]

Single pixel photodetectors with square detector areas ranging from 15 µm × 15 µm to 500 µm × 500 µm were fabricated using a VADA that consists of both passivated and unpassivated single element pixels in the same sample area by removing the passivation from half of the pixels during additional processing steps. A diagram of the detector structure is shown in Figure 43(b).

With these detectors, the study assessed the impact of the wafer substrate temperature during ALD, testing temperatures between 100 °C and 300 °C in increments of 50 °C. The Al_2O_3 thin film was deposited onto the single pixel detector structures through ALD with a wafer substrate temperature of 150 °C using a PicoSun SUNALE R-150B ALD reactor deposition system. Trimethylaluminum (TMA) was used as the metal organic precursor for Al_2O_3 formation while the oxygen source was de-ionized H_2O. To initiate the self-limiting ALD process, 50 pulses of TMA were deposited onto the sample as a pre-treat step. Once completed, 300 cycles of the process flow depicted in Figure 42 finished the ALD growth. At ~0.1 nm per cycle, the 300-cycle ALD process created a 30 nm layer of Al_2O_3 on the entire sample. The new Al_2O_3 layer was wet etched with a HF and H_2O mixture at a 100:1 ratio to define the passivated and unpassivated photodiodes in the sample. Finally, an ohmic contact was made by depositing Ti/Pt/Au on the sample to serve as the bottom and top contacts of the detectors.

The surface coverage of the pixel sidewall was captured using SEM imaging to confirm the uniformity of the Al_2O_3 thin film. Figure 44 shows a single pixel photodiode mesa with the Al_2O_3 layer on the mesa sidewalls; the bottom contact surface surrounding the passivated pixel is visible as the brighter region in the image. The top of the mesa is the darker region etched after the ALD growth to maintain optical transparency of the pixel. The mask region is smaller than the detector pixel, so there is an extended ~3 μm region on top of the mesa with Al_2O_3. Overall, the uniformity in color and good surface coverage verified the good material quality of the Al_2O_3 ALD passivation layer on the sidewall interface.

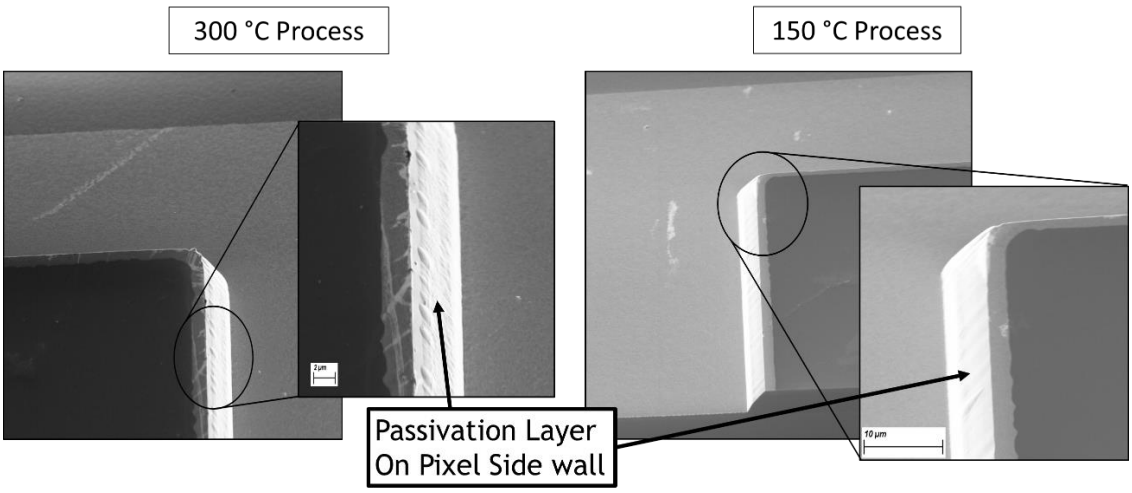

Figure 44. SEM image of a single pixel photodetector, illustrating the Al_2O_3 layer applied by ALD to the mesa sidewalls and substrate surface. The top of the detector was masked to maintain infrared transparency of the optical window.

4.3.1 Dark Current Analysis of Aluminum Oxide Passivated Detectors

The detector dark currents were determined through IV measurements using 11 distinct area sizes of passivated and unpassivated single pixels at 77 K. The electrical performance of passivated and unpassivated detectors was compared to assess the impact of the Al_2O_3 passivation on the dark current. The measured dark current was converted to dark current density to simplify the comparison. Using the electrical schematic in Figure 39(b), we can separate the currents from the measured dark current into the bulk current and the surface similar to the IV analysis in Chapter 2 and repeated here:

$$J_d(V_b) = \frac{I_{dark}(V_b)}{A} = J_{surface} + J_{bulk} = \frac{1}{r_{surface}}\frac{P}{A} + J_{bulk} \quad (4.2),$$

where the dark current density is J_d, the voltage bias is V_b, and the perimeter-to-area ratio is $\left(\frac{P}{A}\right)$. The slope of the resultant calculation is broken down to the surface resistance of the detector through $\left(\frac{1}{r_{surface}}\right)$ and is used to analyze the surface effects on the detector as the

dark current density is plotted for various perimeter-to-area ratios. Ideally, a horizontal line in this analysis would signify that the surface resistance is constant, and too large to shunt the detector, across all area pixels at the designated applied voltage bias.

Therefore, the indication of a parasitic resistance due to the conductive carriers shunting the detector sidewall constrains the detector to be surface-limited. When there is no slope to this line across the different perimeter-to-area ratios, the detector is designated as bulk-limited.

Figure 45 shows the dark current density as a function of the pixel perimeter to area ratio at applied voltage biases of -300 mV and +200 mV for the targeted wavelengths of the detector. These plots of dark current density versus the ratio of pixel perimeter (P) to surface area (A), emphasize the impact of surface charge effects on dark current by observing the increasing trend between the passivated pixels and the unpassivated pixels as the perimeter over area ratio increases.

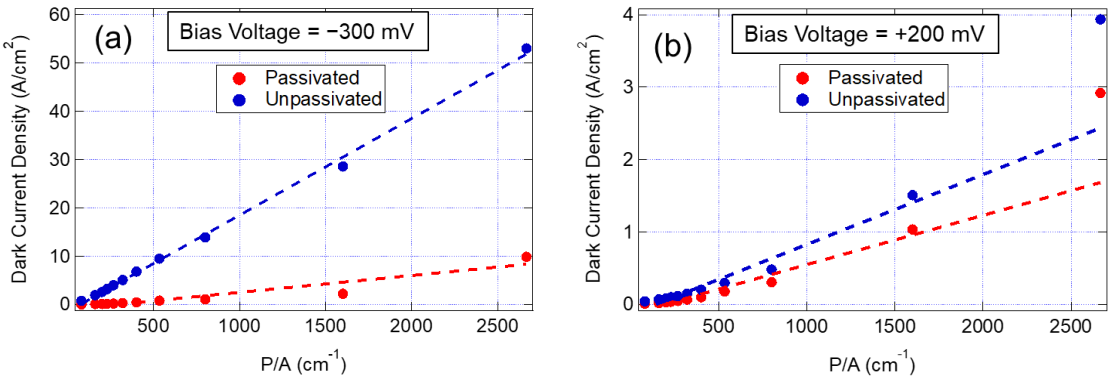

Figure 45. Reduction in dark current density measured for passivated pixels compared to unpassivated pixels. (a) Dark current density as a function of perimeter over area at bias voltage equal to -300mV. (b) Dark current density as a function of perimeter over area at bias voltage equal to +200 mV.[73]

The difference in the slopes of the passivated versus unpassivated pixels indicates a reduced surface charge contribution to the dark current density after passivation. It is important to note that the reported dark current densities in these figures, particularly in Figure 45(a), where the dark current densities are fairly high due to the 300 K viewport on the probe station, can be accounted for during analysis as a constant underlying background current.

The fact that the slopes are non-zero for both the unpassivated and passivated pixels confirms that surface effects are significant contributors. The slope of the line is reduced, though in Figure 45, for the ALD passivated pixels, confirming that ALD performed under these conditions is effective at suppressing these surface contributions. The improved surface characteristics due to passivation impacts the smallest detectors (largest P/A) the most because the surface area to volume ratio is the largest. The ALD passivation results demonstrate that ALD deposition of Al_2O_3 does suppress dark current further than native oxidation by an order of magnitude.

Detector Area (μm^2)	**P/A (cm^{-1})**	**Dark Current Density at -300 mV (A/cm^2)**		**Dark Current Density at +200 mV (A/cm^2)**	
		Unpassivated	Passivated	Unpassivated	Passivated
15	2666.7	53.0755	9.9137	3.9397	2.9212
25	1600	28.6176	2.2736	1.5087	1.0338
50	800	13.9440	1.1187	0.4824	0.3037
75	533.3	9.5217	0.8562	0.2956	0.1754
100	400	6.8754	0.4936	0.2026	0.0969
125	320	5.1189	0.3349	0.1470	0.0656
150	266.7	4.0297	0.2466	0.1158	0.0459
175	228.6	3.2462	0.1954	0.0984	0.0347
200	200	2.6430	0.1649	0.0801	0.0271
250	160	1.9846	0.1356	0.0680	0.0181
500	80	0.8312	0.0813	0.0412	0.0079

Table 8. Dark current density for each perimeter over area at reverse bias voltage equal to -300mV and forward bias of +200 mV for Al_2O_3 ALD passivation results.

The results from this study show that Al_2O_3 ALD passivation reduces pixel dark current by an order of magnitude over unpassivated pixels. Therefore, this work supports the use of Al_2O_3 for passivating the pixel sidewall of a p-type LWIR T2SL photodetector. However, it is not yet understood how strongly other ALD parameters influence the quality of the passivation layer. For instance, neither the pulse timing nor the pretreat (50-cycle TMA) were varied from previous laboratory procedures and may not be optimum for this detector material. Therefore, the order of magnitude improvement observed may not be the upper limit on the improvement that is possible. A subsequent design of experiment that incorporated additional ALD process steps, such as pulse timing and precursor pretreat cycles, would be needed to find this optimum improvement. Once optimized, a direct comparison with other passivation approaches, such as silicon oxide or silicon nitride, to quantify their relative benefits would be valuable.

4.4 Passivation Study Using Zinc Oxide

A separate effort was completed to study other ways to treat the sidewalls of detectors using the ALD passivation technique to reduce the diode dark current. Here, the detectors fabricated have a PN diode architecture after being etched from a more advanced architecture from a different project. The absorber layer has been characterized to respond to the LWIR region as well, becoming a good candidate for the study due to its small bandgap and susceptibility to Fermi-level pinning induced by native oxide accumulation on the detector sidewall.

During the fabrication process, single pixel detectors were etched using a VADA mask and the diode sidewall was treated with 50 cycles of a Zn precursor deposited by

ALD. The sample was then annealed through a rapid thermal annealing (RTA) system to force the Zn bond to form with the superlattice elements and break the native oxide bonds from the superlattice sidewall. This was accomplished to help satisfy the dangling bonds. Based on this annealing process, we assume that the Zn energetically moves the native oxides out of the way and "diffuses" into the sidewall.

Since the entire sample was annealed, the sample needed to be re-etched to open a metal pad layer for metal deposition. This processing became complicated but was necessary to keep the correct doping profiles for the diode to operate properly. A sample with VADA diodes that were not treated also was fabricated to compare with the treated sample.

4.4.1 Dark Current Analysis of ZnO Treated Detectors

The dark-current study focusing on Zn treatment on the sidewalls of the detector are shown in Figure 46. Measurements of the VADA sample confirm that the dark current taken at 77 K for the treated diodes are lower than the untreated diodes.

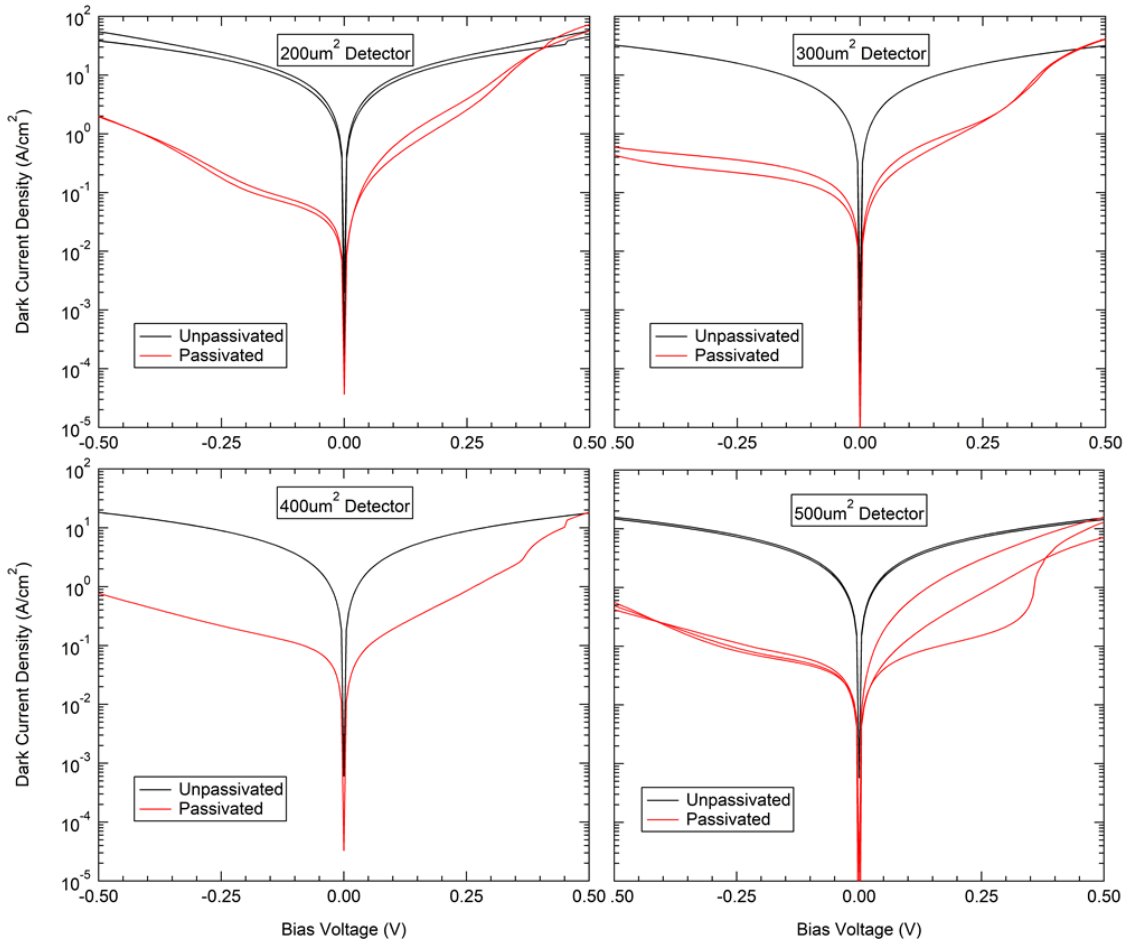

Figure 46. The detector dark current of several detector areas comparing the treated diodes with the Zn precursor (Passivated-Red) and not-treated diodes (Unpassivated-Black). The diodes were measured at an operating temperature of 77 K.

In Figure 46, the symmetric characteristic seen in the black curves show an ohmic or resistor-like behavior that is an indication of the negative effects of accumulated carriers on the sidewall of the detector, which is not favorable to detector performance. The treatment using the ZnO precursor from the ALD with the RTA heat cycle recovered some rectification of the diodes. The red curves displaying the asymmetric behavior, signifies how the recovered rectification is more favorable to diode operating, ultimately improving the overall detector performance.

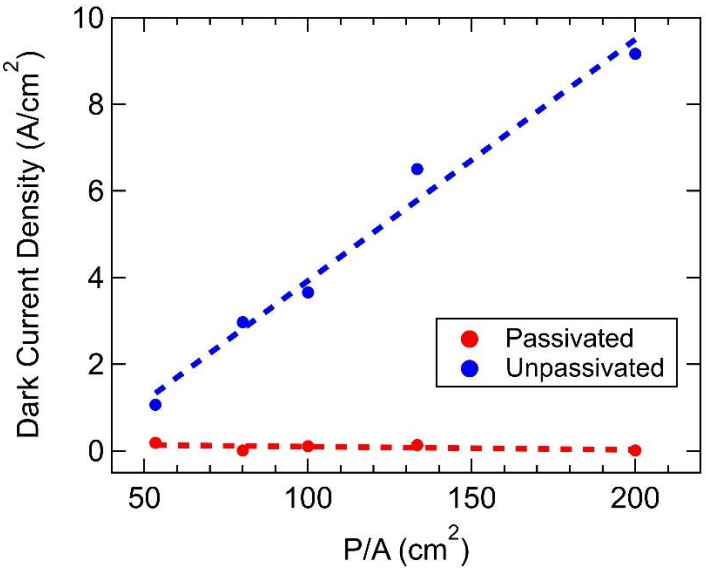

Figure 47. Reduction in dark current density measured for passivated pixels compared to unpassivated pixels. Dark current density as a function of perimeter over area at bias voltage equal to -10mV.

Observations made when comparing the passivated and unpassivated detectors in the Al_2O_3 ALD study can be used in the same way for the ZnO study. By using the perimeter over area ratio, we can isolate the surface component from the bulk component of the dark current density to reveal the effective surface resistance across variable area diodes. The difference in the slopes of the passivated versus unpassivated pixels indicates a reduced surface charge contribution to the dark current density after the ZnO ALD passivation treatment.

The slope fit lines of the unpassivated and passivated pixels confirms that surface effects are significant contributors for the ZnO study, which is similar to the Al_2O_3 results. The slope of the red fit line fitting the dark current density of the measured passivated pixels is significantly reduced compared to the unpassivated pixels. This confirms that the ZnO ALD treatment performed on these detectors is effective at suppressing the sidewall

surface contributions of the dark current to the point where the detectors return to bulk-like conduction paths. Further experimentation needs to be conducted at smaller pixel sizes, but the study indicates future work to optimize the processing is needed to fully realize the impact this treatment process has on SLS detectors.

Detector Area (μm^2)	P/A (cm^{-1})	Dark Current Density at -10 mV (A/cm^2)	
		Unpassivated	Passivated
200	200	9.1666	0.0124
300	133.3	6.5092	0.1325
400	100	3.6584	0.1113
500	80	2.9732	0.0110
750	53.33	1.0653	0.1845

Table 9. Dark current density for each perimeter over area at reverse bias voltage equal to -10mV ZnO-treated passivation results.

As seen in Table 9, the improved surface characteristics due to passivation impacts the smallest detectors (largest P/A) the most because the surface area to volume ratio is the largest. The ALD passivation results demonstrate that ALD deposition of ZnO precursor in combination with RTA heating suppresses the surface component of the detector dark current by an order of magnitude.

4.5 Summary

We investigated the use of passivation on a dual-band LWIR InAs/GaSb pBp barrier detector and a MWIR InAs/InAsSb pn detector to reduce the surface leakage current in the detectors. We were able to employ passivation techniques using Al_2O_3 and ZnO via atomic layer deposition (ALD) through fabrication processes and measure the dark current to understand the surface effects on the fully delineated detector pixels. Results between passivated and unpassivated detectors were compared using variable area diode arrays, and show that both the Al_2O_3 ALD film and the ZnO ALD treatment reduced the sidewall

surface leakage current on these single pixel detectors by at least two orders of magnitude at the smaller pixels, where the passivated samples showed bulk-limited dark current characteristics over a range of diode sizes from 50 μm^2 to 500 μm^2 under reverse-bias voltage at 77 K. Further optimization to improve the bulk-limited performance at other biases and temperatures is needed, but the techniques used for this research have attained bulk-like performance of small pixel detectors and present how passivating small pixels can be completed using ALD, specifically with Al_2O_3 and ZnO.

While it would be fair to conclude the ZnO-treated detectors performed better because of their lower dark current densities after passivation, each study was conducted on a different detector stack, therefore the two ALD processes would have to be administered on the same detector structure to be properly compared. This can be done most effectively by choosing a barrier detector with a p-type absorber because the shunt resistance due to surface effects is more prominent in p-type materials. Completing a comparison study would be beneficial to understand the commercial benefits of ALD passivation and provide a standard way of treating the sidewalls of p-type SLS detectors. This work solidifies that ALD can be used as a proven passivation technique to improve p-type SLS FPA performance, but future study is needed for confirmation. Future work is discussed in Chapter 7.

5 Physics of Diodes Operating Under Open Circuit Conditions

The successful studies using different passivation techniques on small pixel detectors in Chapter 4 proved detector performance is improved with passivation, and supports the drive for large format FPAs at smaller pixel pitch; however, the push for higher operating temperature also needs to be considered.[30] Chapter 5 will continue with the theme of investigating detector physics to mitigate the limiting factors of large format, HOT imagers by reconsidering the individual detector operation.

Significant research efforts have been focused on the development of innovative semiconductor detector material and heterostructures with complementary advancements in readout integrated circuit (ROIC) technology.[2] This has led to the commercial testing and introduction of MWIR FPA technology with decreased pixel pitch. The MWIR research has also focused on improving high operating temperature (HOT) performance to reduce detector cooling needs as a cost benefit.[19] Prototype imagers have been demonstrated with increasing operating temperature such as SL imagers operating at ~160 K.[21, 22] The rapid increase in dark current as a function of temperature was the limiting factor for the operating temperature of these detectors, therefore HOT MWIR imagers continue to seek solutions to mitigate high dark current despite solutions using passivation.

The objective of this chapter is to investigate the detector physics for HOT MWIR detectors through analytical modeling and experimental measurements to re-examine one of the fundamental underlying assumptions of MWIR detector architectures: the relative advantages of using the reverse-bias photocurrent in a diode (I_{diode}) as the signal versus

using the diode open-circuit voltage (V_{OC}). There are reports in the literature of using V_{OC}, which uses a laterally connected series of diodes and vertical interband cascaded detectors in a photovoltaic mode, for HOT MWIR applications.[85-88] While these reports offer examples of using voltage as the main driver for signal measurement, the need to scale the technology to FPA imagers is ignored. Ultimately using the open-circuit voltage to drive a pixel in an FPA would be an end-goal, and the study presented here addresses this possibility. Our analytical modeling of the signal and noise of a photodiode operating in open-circuit conditions predicts that there are potential advantages compared to reverse-biased photodiodes in performance metrics such as Noise-Equivalent Differential Temperature (NEDT) for HOT MWIR imagers with reduced pixel pitch.

5.1 Signal

5.1.1 Diode Concepts Using Current

To investigate the relative advantages of using the photodetector V_{OC} for MWIR detector operation, we need to revisit the photodetector operation at the fundamental level. Consider the non-ideal p-n junction diode, where the Shockley equation[65] can be used to describe the current-voltage (IV) characteristics of the diode operating at an applied bias (V_b):

$$I_{diode}(V_b) = I_{sat}\left(exp\left(\frac{qV_b}{n_{diode}k_BT}\right) - 1\right) \quad (5.1),$$

where I_{diode} is the total diode current, I_{sat} is the reverse saturation current, q is the charge of an electron, n_{diode} is the diode ideality factor, and k_BT/q is the thermal voltage at temperature T.

This can be expanded out to consider other factors, such as non-ideal losses and illumination conditions as expressed in (5.3). Under these illumination conditions, the shape of the IV curve is found to be similar with an offset in the direction of reverse bias and reverse current, as described in Chapter 2 as the photo-generated current (I_{ph}) in the detector IV analysis. A reminder of this concept is displayed in Figure 48.

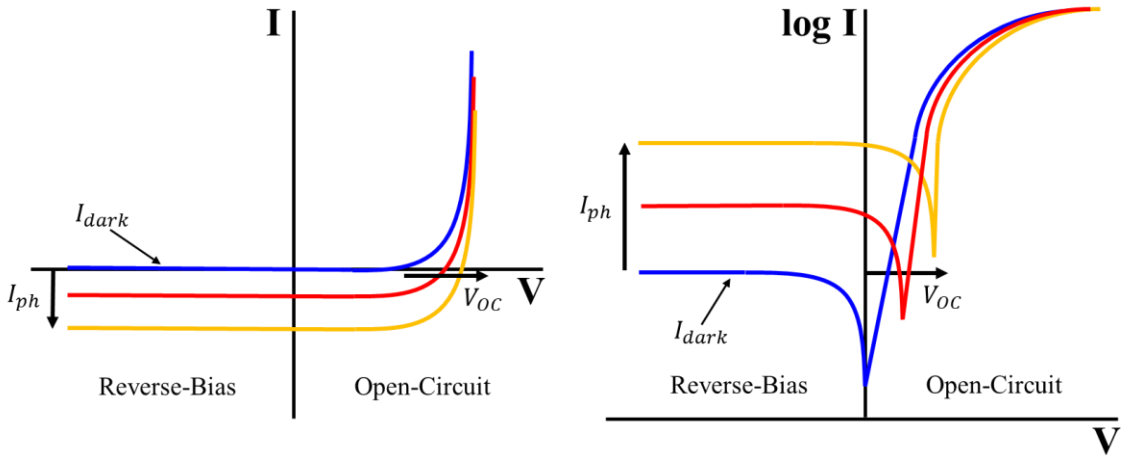

Figure 48. IV characteristics the diode under dark conditions and under illumination conditions. The logarithmic IV curves are also shown.

To establish the beginning of the analytical model to find the expression for V_{OC}, first, we examine the total current as a combination of the dark current of an ideal diode, (I_{dark}), the photo-generated current (I_{ph}) of the diode, and the parasitic current leakage across the p-n junction (I_{shunt}):

$$I_{diode}(V_b) = I_{dark} - I_{ph} + I_{shunt} \quad (5.2).$$

Substituting into this equation the determination of (I_{shunt}) using the shunt resistance (r_{sh}), and V_b, we achieve:

$$I_{diode}(V_b) = I_{sat}\left(exp\left(\frac{qV_b}{n_{diode}k_BT}\right) - 1\right) - I_{ph} + \frac{V_b}{r_{sh}} \quad (5.3).$$

Here, the total current is described as a combination of the dark current of an ideal diode (I_{dark}), the diode's photo-generated current (I_{ph}), and the parasitic current leakage across the p-n junction (I_{shunt}) determined by the shunt resistance (r_{sh}), and V_b. This establishes the beginning of the analytical model to find the expression for V_{OC}.

In order to assess the diode signal concepts, Figure 49 presents an illustration of the IV measurements of a MWIR single pixel photodetector design based on a InAs/InAsSb superlattice heterostructure grown by molecular beam epitaxy (MBE). The IV measurements were taken at multiple irradiance levels while the photodetector temperature was held at 80 K. The test setup used is similar to the test setup described in the detector characterization in Chapter 2.

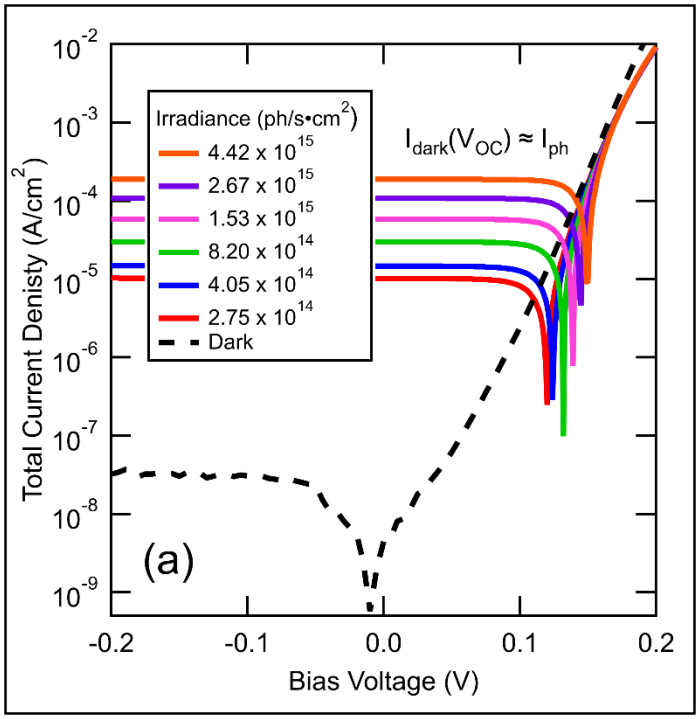

Figure 49. Total current density measured as the MWIR photodiode is illuminated with increasing irradiance.[89]

5.1.2 Diode Concepts Using Voltage

Under open-circuit conditions, the photo-generated current becomes equal to the dark current flowing in the opposite direction, such that $I_{diode} = 0$.[44] By solving Eq. (5.3) for this open-circuit condition and substituting $V_b = V_{OC}$, an expression for the open-circuit voltage (V_{OC}) can be derived via:

$$I_{diode}(V_{OC}) = I_{sat}\left(exp\left(\frac{qV_{OC}}{n_{diode}k_BT}\right) - 1\right) - I_{ph} + \frac{V_{OC}}{r_{sh}} = 0 \qquad (5.4).$$

For this analysis, we assume that the shunt current remains negligible and ignore it for simplicity; this assumption is generally valid unless V_{OC} is near zero.

$$0 = I_{sat}\left(exp\left(\frac{qV_{OC}}{n_{diode}k_BT}\right) - 1\right) - I_{ph}$$

$$I_{ph} = I_{sat}\left(exp\left(\frac{qV_{OC}}{n_{diode}k_BT}\right) - 1\right)$$

$$\frac{qV_{OC}}{n_{diode}k_BT} = \ln\left(\frac{I_{ph}}{I_{sat}} + 1\right)$$

$$V_{OC} = n_{diode}\frac{k_bT}{q}\ln\left(\frac{I_{ph}}{I_{sat}} + 1\right)$$

In addition, I_{ph} can be determined from $I_{ph} = q\eta E_q A_{diode}$, where η is the quantum efficiency of the photodiode, E_q is the photon irradiance (photons/sec-cm^2), and A_{diode} is the area of the diode. Substituting this into the equation for V_{OC}:

$$V_{OC} = n_{diode}\frac{k_BT}{q}\ln\left(\frac{q\eta E_q A_{diode}}{I_{sat}} + 1\right) \qquad (5.5).$$

Observing the relationship in Eq. (5.5), we can draw several conclusions about the open-circuit voltage. We can determine that V_{OC} depends simply upon the ratio between the photo-generated current and the reverse-saturation current. In order to obtain a large open-circuit voltage, the ratio between the photo-generated current and the reverse-

saturation current must be large. Examining the V_{OC} behavior versus irradiance shows that the V_{OC} has a weak logarithmic dependence on the irradiance. Therefore, the irradiance is not tracked linearly with the V_{OC}, but is well defined and can be predicted through analytical fitting using the natural log of the ratio of the photo-generated current and reverse-saturation current.

The open-circuit voltage was measured under the same radiometric conditions as the IV measurements using a Keithley 2182A nanovoltmeter. For each irradiance, an open-circuit voltage was recorded and is shown in Figure 50. This measurement is valuable because we can extract the V_{OC} using reasonable techniques outside of the IV measurement. We are also able to fit analytically the weak logarithmic relationship of the photo-generated current and reverse-saturation current determined in Eq. (5.5), as shown in Figure 50.

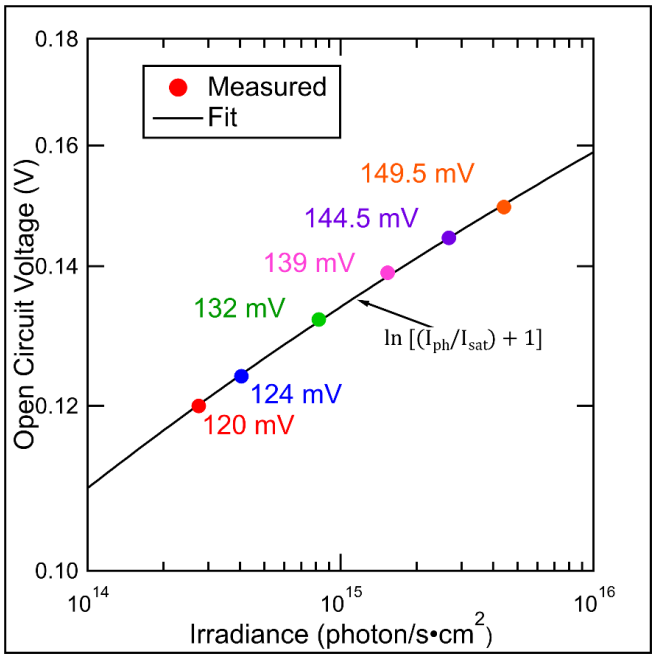

Figure 50. Measured V_{OC} as the MWIR photodiode is illuminated with increasing irradiance. The analytical logarithmic fit expected from the derived V_{OC} equation is shown to align with the measured V_{OC} of the detector.[89]

5.1.3 Dynamic Resistance

The p-n junction diode IV analysis can be examined further using the concept of dynamic resistance. The dynamic resistance of the diode (r_d) is derived from the Shockley equation by defining the resistive nature of the diode through the derivative of the diode current with respect to bias voltage. Therefore, the r_d being independent of irradiance across the range of V_{OC} can be proven and is shown below.

The r_d typically is represented when discussing the small signal analysis of the diode to determine how the diode characteristics fluctuate when experiencing instantaneous or infinitesimal changes in current and voltage. The r_d is calculated as the reciprocal of the tangential slope of the IV curve; Figure 51 conveys this derivative conceptually. The dynamic resistance also is called the AC resistance when conducting the small signal analysis on the diode.[90]

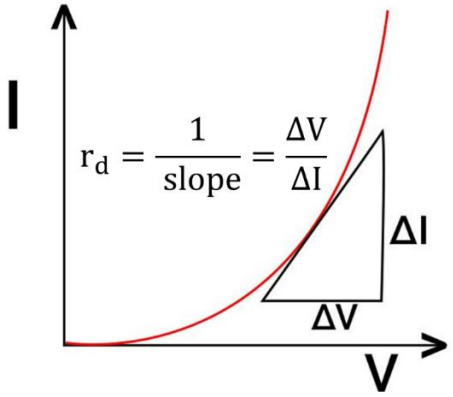

Figure 51. The reciprocal of the tangential slope between the change in voltage versus the change in current represents the dynamic resistance of a p-n junction.

It is conventional to use the IV analysis as described in Chapter 2 to evaluate photodetectors, and with the signal analysis considered from the previous section, the r_d

also can be evaluated to understand the diode characteristics under open-circuit conditions by taking the derivative of the Shockley equation from (5.1) with respect to V_b as described below. First, the derivative is provided:

$$r_d(V_b) = \left(\frac{dI_{diode}}{dV_b}\right)^{-1} \tag{5.6}$$

Then, substituting terms discussed above regarding the total diode current (I_{diode}) and the bias voltage (V_b) in to the derivation, the argument is completed for the dynamic resistance calculation under open-circuit conditions:

$$\frac{dI_{diode}}{dV_b} = \frac{qI_{sat}}{n_{diode}k_BT}\ exp\left(\frac{qV_b}{n_{diode}k_BT}\right) \tag{5.7}$$

Under open-circuit conditions, the derivative of the Shockley equation can be translated to include the V_{OC}, thus, the previous derivation of the V_{OC} from (5.5) can be used as a substitute for the voltage bias in (5.6).

$$\left(\frac{dI_{diode}}{dV_b}\right)_{V_b=V_{OC}} = \frac{qI_{sat}}{n_{diode}k_BT}\ exp\left(\frac{q}{n_{diode}k_BT}\left(\frac{n_{diode}k_BT}{q}\ln\left(\frac{I_{ph}}{I_{sat}}+1\right)\right)\right)$$

$$\left(\frac{dI_{diode}}{dV_b}\right)_{V_b=V_{OC}} = \frac{qI_{sat}}{n_{diode}k_BT}\left(\frac{I_{ph}}{I_{sat}}+1\right)$$

$$\left(\frac{dI_{diode}}{dV_b}\right)_{V_b=V_{OC}} = \frac{q}{n_{diode}k_BT}\left(I_{ph}+I_{sat}\right) \tag{5.8}$$

Therefore, the dynamic resistance under open-circuit conditions can be calculated using (5.7) and (5.8), and r_d simplifies to r_{OC} in (5.9).

$$r_{OC} \equiv r_d(V_{OC}) = \left(\frac{dI_{diode}}{dV_b}\right)^{-1}_{V_b=V_{OC}} \tag{5.9}$$

$$r_{OC} = \frac{k_BT}{q}\ \frac{n_{diode}}{(I_{ph}+I_{sat})} \tag{5.10}$$

Using the measured IV data, the dynamic resistance was calculated across the full bias range, as shown in Figure 52. This result confirms that the dynamic resistance is independent of irradiance, as expected, across the range of V_{OC}.

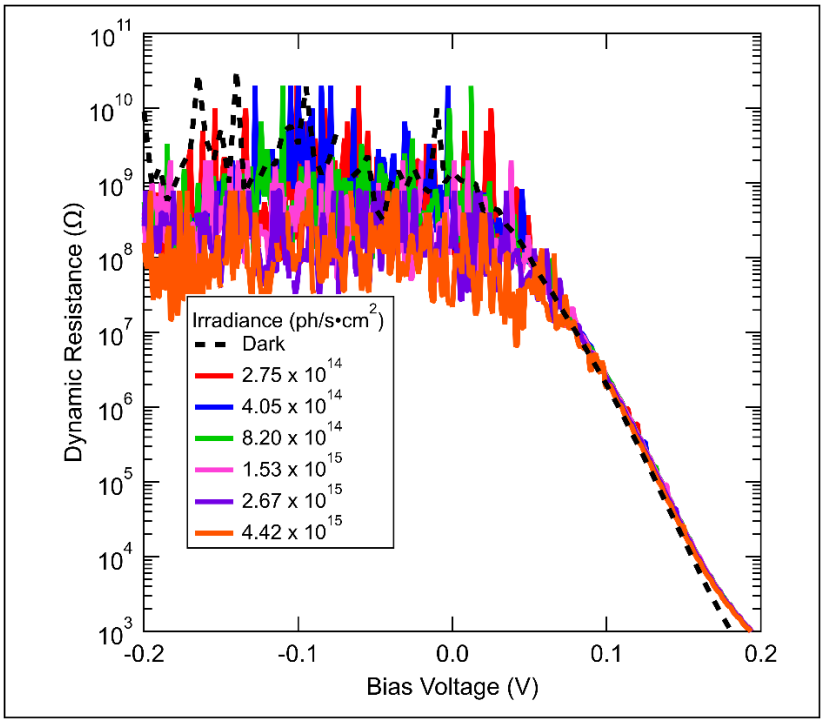

Figure 52. Calculated dynamic resistance from the IV measurements. The dynamic resistance does not change with irradiance, as expected.[89]

The results of the extracted dynamic resistance show that the dynamic resistance is independent of radiant flux, ultimately conveying that the diode impedance does not change with irradiance across the reverse-bias range. The dynamic resistance also can be described functionally in the forward-bias region of the diode operation, and is also independent of irradiance, as a first order analysis.

5.1.4 Effects on Diode Performance

As reviewed in Chapter 1, the operating temperature of the diode plays a pivotal role in fundamental limiting factors surrounding current FPA research. It is pointed out that the pixel area is also of great importance, specifically for high pixel pitch densities in IR imaging technologies. To take these concepts back to a fundamental level, the temperature effects and area effects on MWIR diodes are evaluated.

A proof-of-concept experiment to demonstrate the temperature effects on the performance of a diode under open-circuit conditions is presented. Specific measurements were conducted to validate the independence of the photodetector's open-circuit voltage versus detector area as well as operating temperature through preliminary radiometric measurements such as dark current and photocurrent.[87]

The photodetector component of the VocP pixel demonstration used a MWIR detector design based on a bulk InAsSb barrier detector structure grown by molecular beam epitaxy (MBE) with a cutoff wavelength of about 4 μm. Single pixel photodetectors with square device areas ranging from 15 μm × 15 μm to 500 μm × 500 μm were fabricated using a variable area diode array (VADA). In determining overall material quality using radiometric characterization at various temperatures, this material was determined to have favorable infrared detection characteristics. Some of these results can be seen in Figure 53 as dark current and photocurrent over a range of biases, temperatures, and detector sizes.

The MWIR single pixel detectors were packaged using a leadless chip carrier (LCC) and mounted in a closed-cycle cryostat for electrical and optical characterization at a number of operating temperatures. IV curves in dark and illuminated conditions of the

single pixel detectors were measured at 80 K, 120 K, 160 K, and 200 K, as shown in Figure 53. The photocurrent of each single pixel detector was measured under flood illumination conditions using a halogen lamp as a blackbody source with a peak wavelength of 1900 K. The V_{OC} was extracted from these measurements. Signal and noise measurements were also taken using a radiometric setup consisting of the halogen lamp, a germanium filter at a long pass of about 2 μm, a current pre-amplifier, and a network analyzer.

A summary of dark current versus photocurrent over voltage bias of the single pixel detectors can be seen in Figure 53 with detector pixel areas ranging including 50 μm^2, 150 μm^2, and 250 μm^2.

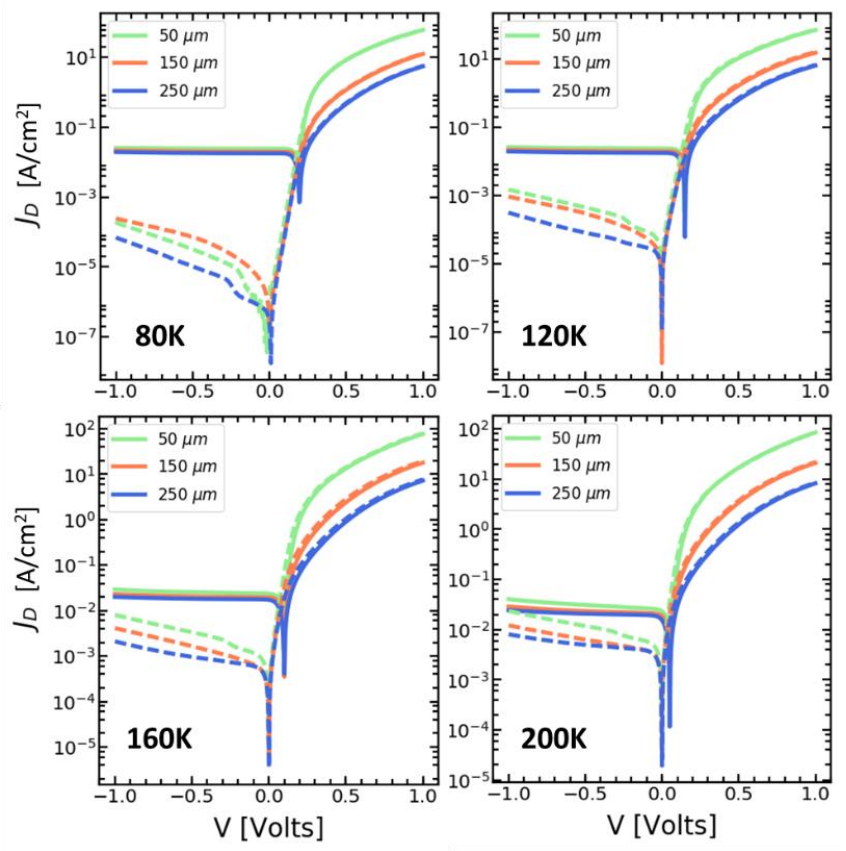

Figure 53. Dark-current density versus voltage bias of various single pixel detectors under dark-current conditions (dashed lines) and photocurrent conditions (solid lines) at 80 K, 120 K, 160 K, and 200 K.[87]

The overall behavior of the photodetector material as the operating temperature increases shows how the open-circuit voltage shifts downward while the dark current moves up as expected.

The independence of voltage versus detector size is shown in Figure 54. The V_{OC} shows reduced dependency on the diode area, and is within the range of 200 mV at 80 K. As the sample operating temperature is raised, V_{OC} is reduced to the 50 mV range at 200 K and moves to about 10 mV at 240 K. When comparing Figure 53 to Figure 54, the IV curves under dark and illuminated conditions also give way to distinguish that as the operating temperature increases, the increase in dark current due to thermal effects reduces the V_{OC} as well as the photocurrent.

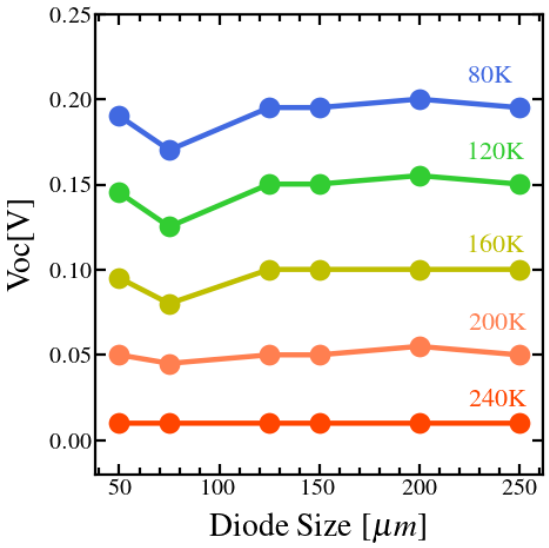

Figure 54. Open circuit, V_{OC}, measurements for various pixel areas of single pixel detectors at an operating temperature of 80 K, 120 K, 160 K, 200 K, and 240 K. As temperature increases, the observed V_{OC} decreases, but stays at a constant level over a wide range of pixel sizes for that temperature.[87]

The InAsSb photovoltaic material used for this demonstration is not an optimized structure to take advantage of the V_{OC} across the diode at room temperature, however, when

cooled to about 200 K, the V_{OC} is sufficient enough to induce an open circuit voltage of about 50 mV. While the variation of the voltage across each diode also was not consistent entirely, as seen in Figure 54 at the approximate detector size of 50 μm^2, carefully choosing an optimal infrared heterostructure design could contribute to the success of the diode concepts presented in this chapter by implementing these diodes in different circuit architectures.

5.2 Noise

To analyze the photodiode noise, the total current defined in (5.3) can be broken down analytically into two noise components, Johnson noise and Shot noise.[44, 91] Typically, the Johnson noise and Shot noise are considered as current noise when discussing the noise processes of a diode as Buckingham *et al.* state when discussing inherent noise in p-n junction diodes.[91] However, we also are considering the open-circuit conditions of these equations through the total current noise and voltage noise to understand their differences and similarities.

5.2.1 Diode Noise Using Current

To begin, a first order estimate of the diode noise is described using both the Johnson noise and Shot noise as the main sources of noise found in the p-n junction:

$$i^2_{(diode)noise} = i^2_{(Johnson)noise} + i^2_{(Shot)noise} \tag{5.11}$$

Other noise sources, such as generation-recombination noise, are excluded because those noise mechanisms minimally contribute and are estimated to be negligible for a diode under open-circuit conditions.[44]

The Johnson noise is generated fundamentally in all resistive elements due to the thermal motion of the charge carriers in the p-n junction.[44] The Johnson noise can be found by:

$$i^2_{(Johnson)noise} = \left({}^{4n_{diode}k_bT}/_{r_{sh}}\right)\Delta f \qquad (5.12)$$

where Δf is the frequency bandwidth, r_{sh} is the shunt resistance, and T is the diode operating temperature, as defined and measured in the diode signal analysis above. The shunt resistance and diode operating temperature are the only parameters affecting the Johnson noise in p-n junction over a given frequency bandwidth.

The overall impact of the Shot noise originates from the random arrival of carriers at the p-n junction, thus describing the unavoidable current fluctuations in the diode:[67]

$$i^2_{(Shot)noise} = 2q\left(|I_{dark} + 2I_{sat}| + I_{ph}\right)\Delta f \qquad (5.13),$$

where I_d is the total diode current, I_{sat} is the reverse saturation current, and I_{ph} is the photo-generated current, as defined and measured in the signal analysis section.

Combining and substituting equations (5.10 – 5.12), the definition for the total current noise is expressed as:

$$i^2_{(diode)noise} = 4\left(\frac{n_{diode}k_bT}{r_{sh}}\right) + 2q\left(|I_{dark} + 2I_{sat}| + I_{ph}\right)\Delta f \qquad (5.14).$$

Since V_{OC} operation is being considered, the noise model is simplified. When analyzing the noise due to carriers across the depletion layer, Buckingham *et al.* state that the p-n junction under an open-circuit condition has current flowing in each direction for a net current flow of zero for i_d.[91] In addition, the values of the forward current and the reverse current are both much greater than the reverse-saturation current because the overall diffusion current is minimized under forward bias.[91] We can then assume that for open-

circuit operation, the balance between the generation due to the photo-generated current and recombination due to dark current exactly matches: $I_{ph} = |I_{dark}|$. Therefore, we can substitute this into the Shot noise equation to achieve the following derivation.

$$i^2_{(Shot)noise} = 2q\left(\left|I_{ph} + 2I_{sat}\right| + I_{ph}\right)\Delta f$$

$$i^2_{(Shot)noise} = 2q\left(2I_{ph} + 2I_{sat}\right)\Delta f$$

$$i^2_{(Shot)noise} = 4q\left(I_{ph} + I_{sat}\right)\Delta f \quad (5.15)$$

Using information from the discussion on dynamic resistance, and that r_d provides a good estimate of the r_{sh},[67] the photo-generated current, and the reverse-saturation current are reduced to Eq. (5.9), specifically under open-circuit conditions. This relationship can be substituted in for $\left(I_{sat} + I_{ph}\right)$ in the Shot noise Eq. (5.14) to achieve:

$$i^2_{(Shot)noise} = 4q\left(\frac{n_{diode}k_BT}{r_{oc}}\right)\Delta f \quad (5.16).$$

If we also assume that the diode is ideal, then $n_{diode} = 1$, and the Shot noise would be equated to (5.16) as the ideal case. This brings the current noise associated with the Shot noise term to be equivalent to the Johnson noise of the diode in:

$$i^2_{(Shot)noise} = \left({}^{4k_bT}/_{r_{oc}}\right)\Delta f \quad (5.17)$$

$$i^2_{(Shot)noise} = \left(\left({}^{4k_bT}/_{r_{oc}}\right) + \left({}^{4k_bT}/_{r_{oc}}\right)\right)\Delta f \quad (5.18)$$

$$i^2_{(ideal,Open\ Circuit)noise} = 2\left({}^{4k_bT}/_{r_{oc}}\right)\Delta f \quad (5.19)$$

This is only true when the applied bias is at the open-circuit condition $V_b = V_{OC}$. Therefore, the Shot noise under open-circuit conditions is defined by (5.18) with the above

assumptions considered. This noise formula is convenient because only r_{OC} is needed to predict the noise characteristics of a photodiode.

5.2.2 Diode Noise Using Voltage

The goal of analyzing diode noise using voltage is to describe the noise under open-circuit voltage conditions by relating the voltage noise to the V_{OC} and using the previously developed concepts of diode noise using current. The voltage noise of the diode can be determined from the net current noise by further analyzing the net resistance components of each noise contribution. Consider the net noise current of two noise currents in parallel. The corresponding resistive contributions are also in parallel. To obtain the net Johnson voltage noise of the system, the current noise is multiplied by the parallel resistance of the two resistive components:

$$v^2_{(diode)noise} = i^2_{(diode)noise}(R_{sh}||r_{OC})\Delta f \qquad (5.20),$$

where R_{sh} is the diode shunt resistance and r_{OC} is the dynamic resistance under open-circuit conditions. When we substitute Eq. (5.18) giving the diode current noise into Eq. (5.19) for the voltage noise, we get:

$$v^2_{(diode)noise} = \left(2\left({}^{4k_bT}/_{r_{oc}}\right)\right)(R_{sh}||r_{OC})\Delta f \qquad (5.21).$$

While we account for the realistic model of the system by adding these resistive contributions to the overall noise, we need to minimize them to separate their contribution from the diode Johnson noise. To do this, we assume the parallel resistance ($R_{||}$) to be very high, so that it simplifies to r_{OC} as the limiting resistance:

$$R_{||} = (R_{sh}||r_{OC}) = r_{OC} \qquad (5.22).$$

$R_{||}$ is very high when it meets or exceeds 1 MΩ, otherwise this assumption breaks down and the resistive components cannot be separated from each other or from the diode noise. Substituting Eq. (5.21) for $R_{||}$ into Eq. (5.20) for voltage diode noise, we get:

$$v^2_{(diode)noise} = \left(2\left({}^{4k_bT}/_{r_{oc}}\right)\right)(r_{OC})\Delta f$$

$$v^2_{(diode,Open\ Circuit)noise} = 2\left({}^{4k_bT}/_{r_{oc}}\right)\Delta f \tag{5.23}$$

Thus, we arrive at a conclusion for total voltage noise, summarized in Eq. (5.22) that is parallel to conclusion for the total current noise. This conclusion gives a balanced, simplified version of the total voltage noise that can be used to estimate the noise seen on the V_{OC} of the diode under open-circuit conditions.

To test these voltage noise models, an experiment to measure the diode noise under open-circuit conditions was completed on the same MWIR single pixel photodetector used in the signal analysis. The noise spectrum was measured by connecting the diode directly to a spectrum analyzer while it was illuminated at the same E_q as the signal measurement. To compare the measurement and the models, the experimental results are shown in Figure 55 along with the predicted voltage noise based on Eqs. (5.20) and (5.32).

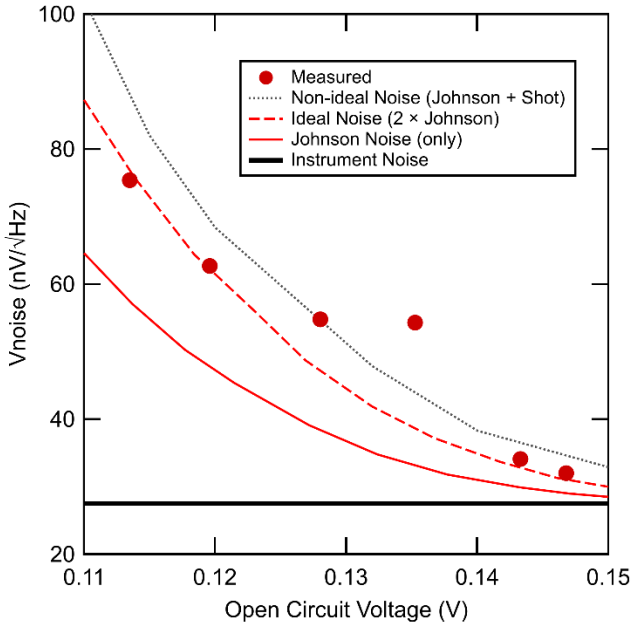

Figure 55. Comparison of directly measured noise and the developed noise model predictions calculated using Johnson noise and Shot noise as it pertains to ideal and non-ideal diode models.[89]

The noise model predictions were calculated using the voltage form of (5.20), which accounts for a non-ideal diode; and (5.33), which assumes an ideal diode. The theoretical noise model developed in (5.20) includes both the diode Johnson noise and Shot noise, and the theoretical Johnson noise model depicted in (5.27) is the ideal case. Experimental values measured for r_d, I_{dark}, I_{sat}, and I_{ph} were used in these calculations. Effective parasitic losses from the instrument noise due to the test setup were accounted for and will be discussed in the next section in detail, and is shown as the baseline noise level in Figure 55.

The comparison of these relationships to the measured data demonstrate that the V_{OC} operation reasonably can be modeled using basic p-n junction physics in terms of the

Shockley equation, Johnson noise, and Shot noise rather than just Johnson noise alone, as some traditional concepts use to estimate diode noise.

5.2.3 Considering Resistance for Noise Measurements

Instrument noise and parasitic losses in the test setup affect the results when measuring such low noise levels. They have been taken into account during the noise discussion above; however, they require a more detailed discussion. The instrument noise and parasitic losses are determined by examining the impact of the test setup on the measurement. First, the total voltage noise can be expanded to include the instrument voltage noise:

$$v^2_{noise(measured)} = \left(v^2_{noise} + v^2_{noise(Instrument)}\right)\Delta f \qquad (5.24),$$

where v^2_{noise} represents the different noise models developed throughout the noise discussion including the ideal (Johnson) case and the non-ideal (Johnson and Shot) case. In addition, the resistance associated with each noise component becomes an effective resistance due to the parallel nature of the measurement scheme and test setup. The instrument input resistance (r_{input}), which sits at room temperature ($T_{input} = 300$ K), is taken into account and can be defined in (5.37). This forms a parallel to the diode dynamic resistance (r_d), at its temperature ($T_{input} = 80$ K), where the formula in (5.38) is used to make a distinction between the temperature differences in the setup.

Further, a procedure to deal with these cases was developed and is described in the following breakdown analysis. The v^2_{noise} is expanded into the noise spectral density (NSD) of the total noise in (5.35), including the diode noise and the instrument noise.

$$NSD = \sqrt{v_{noise(Johnson)}^2 + v_{noise(Shot)}^2 + v_{noise(Instrument)}^2} \quad (5.25)$$

Where $v_{noise(Johnson)}^2$, $v_{noise(Shot)}^2$, and $v_{noise(Instrument)}^2$, can be broken down into different components with the appropriate effective resistances calculated.

$$v_{noise(Johnson)}^2 = \frac{V_{noise(diode)}^2 \times V_{noise(input)}^2}{V_{noise(diode)}^2 + V_{noise(input)}^2}$$

$$v_{noise(input)}^2 = 4k_B(T_{input})(r_{input}) \text{ and } v_{noise(diode)}^2 = 4k_B(T_{diode})(r_d)$$

$$v_{noise(Shot)}^2 = 2qi_{ph}r_{eff}^2 \text{ , where } r_{eff}^2 = \frac{r_d \times r_{input}}{r_d + r_{input}}$$

The input parameters used in this effective resistance calculation are based on both measured and calculated data. The dynamic resistance previously was described as the calculated r_d from the IV measurements; the instrument noise is measured, where here $v_{instrument}$ = 2.75 nV; and the r_{input} is the instrument impedance, which is assumed to be 1 MΩ for the spectrum analyzer that is measuring the diode noise directly as it is illuminated.

In summary, the diode noise was analyzed in great detail by considering many factors affecting the calculations and measurement. The non-ideal case is more difficult to measure because test-system errors compound. However, under V_{OC} operation, the effective resistance can be used to determine the diode noise when using the basic p-n junction physics in terms of the Shockley equation, Johnson noise, and Shot noise. In the subsequent NEDT analysis, the NSD model for the total voltage noise is used.

5.3 NEDT Analysis

After analyzing the signal and noise, the models that have been defined can be used to predict the FPA performance of photodiodes using V_{OC} operation and to compare that to conventional reverse-bias operation. We can use the commonly measured NEDT to compare the conventional reverse-bias operation and V_{OC} operation of the diode:

$$NEDT = \frac{T_{high} - T_{bkg}}{SNR} = \frac{(T_{high} - T_{bkg}) noise_{bkg}}{signal_{high} - signal_{bkg}} \quad (5.26),$$

where the SNR is the signal-to-noise ratio given by the scene background noise ($noise_{bkg}$) and ($signal_{high} - signal_{bkg}$) as the scene signal difference, and ($T_{high} - T_{bkg}$) is the scene temperature difference.[92, 93]

Unlike other figures of merit, the NEDT is a metric that uses only the scene temperature difference to allow a direct comparison in terms of the unitless SNR, which can use either voltage or current.[93] For a given diode and integration time, Eqs. (5.3) and (5.18) are used with Eq. (5.25) to determine NEDT for reverse-bias operation, and Eqs. (5.4) and (5.22) are used with Eqs. (5.23) and (5.25) for V_{OC} operation. Figure 56 compares the computed NEDT between reverse-bias operation and V_{OC} operation for a diode with the same quantum efficiency (70%), dark current (10×Rule07),[13] F/2 optics, cutoff wavelength (5 μm), and pixel pitch (15 μm).

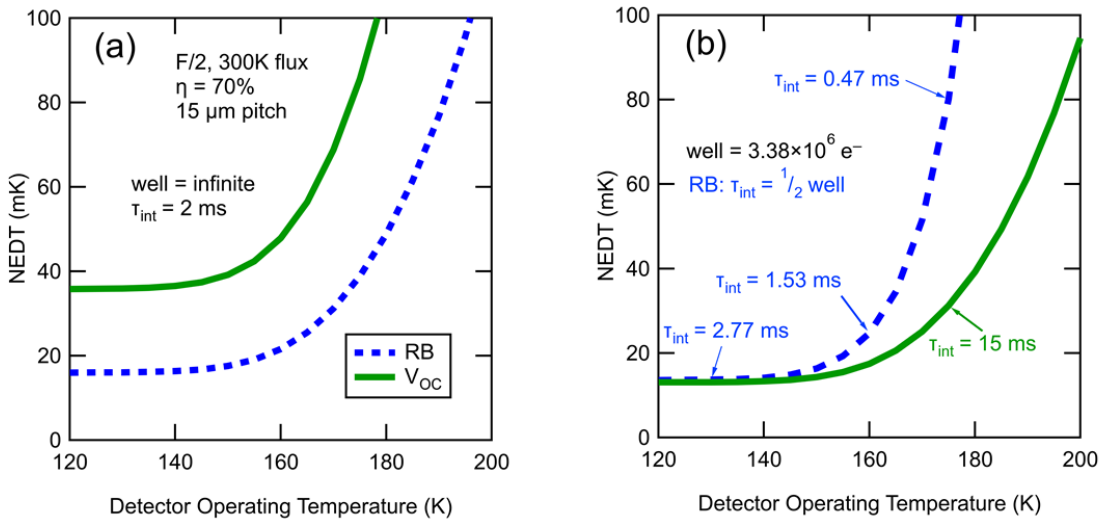

Figure 56. (a) Calculated NEDT versus operating temperature for an FPA under reverse-bias operation (RB) and open-circuit operation (VOC) with the same integration time used. (b) Calculated NEDT versus operating temperature with a shorter integration time for RB and a longer integration time for VOC operation to mimic a realistic well capacitor size.[89]

In Figure 56(a), the modeled NEDT was compared in the two operation modes assuming an infinite charge well capacity with a fixed integration time (τ_{int} = 2 ms). However, most ROICs have a fixed pixel capacitance that limits the charge capacity and, hence, the integration time. This is particularly relevant to real-world performance at elevated temperatures where detector dark current is high. In Figure 56(b), we have assumed a finite well density of 30,000 electrons/μm^2 based on specifications from a commercial ROIC by FLIR[94] (corresponding to a capacity of 3.38×10^6 electrons for this pixel pitch) and varied the integration time for reverse-bias operation to restrict the total charge (dark and photo) to the half-well condition. We compare this with the NEDT of the V_{OC} operation using an integration time of 15 ms, assuming this is always under half-well capacity. Under conventional analysis of NEDT versus integration time, the same equations and assumptions are used, however this analysis focuses on the open-circuit

voltage operation and compares the NEDT using only voltage as a new metric in understanding the motivation for using the open-circuit voltage as the main driver for IR sensing.

Figure 56(a) shows that V_{OC} operation offers no advantage over reverse-bias operation if the charge capacity is not a limiting factor. However, the integration time is the performance equalizer in cases in which the NEDT is limited by the finite charge capacity of the ROIC. This occurs at higher operating temperatures when the dark current is high. At these temperatures, the reverse-bias forces a shorter integration time, and NEDT degrades rapidly, as seen in Figure 56(b) because the charge equivalent to the higher dark current is saturating the integration capacitor before attaining any signal information. V_{OC} operation is not bound by the same integration charge limitation as reverse-bias operation. This enables V_{OC} operation to use a longer integration time, reducing its noise, and achieving a lower NEDT at all operating temperatures. This predicts an advantage for V_{OC} operation when accounting for realistic FPA integration capacitors, rather than integrating photocurrent on an ideally large capacitor. For FPA applications that can operate with longer integration times and prioritize high-temperature operation, V_{OC} operation is a promising alternative to reverse-bias operation.

5.4 Summary

A more device-centered approach was developed where we re-examined the relative advantages of using the reverse-bias photocurrent of a photodetector versus using the open-circuit voltage under the same conditions. We investigated the detector physics through analytical modeling, fabrication, integration, and test of an InAs/InAsSb MWIR

superlattice heterostructure detector and explored the potential of using this architecture for high operating temperature (HOT) small pixels in FPAs.

The comparison of the developed models to the measured data support the premise that the open-circuit voltage operation can be modeled using standard diode physics. The diode noise was also analyzed in great detail by considering many factors affecting the calculations and measurement. Under V_{OC} operation, the effective resistance can be used to determine the diode noise when using the basic p-n junction physics in terms of the Shockley equation, Johnson noise, and Shot noise. The simple analytical models built can be used in the future analysis of infrared detectors and their noise characteristics across bias and temperature under open-circuit conditions.

Further analysis found favorable operating conditions for the open-circuit voltage detector through noise equivalent temperature difference (NEDT) models using standard radiometric optics for high density FPAs. Under conventional analysis of NEDT, the same equations and assumptions are used when considering reverse-bias conditions and integration time. When the NEDT analysis focuses on the open-circuit voltage operation, the NEDT comparison over integration time sheds new light on a common concept and a new way of understanding the motivation for using the open-circuit voltage as the main driver for IR sensing. The integration time becomes the performance equalizer in cases in which the NEDT is limited by the finite charge capacity of the ROIC, especially when high dark currents due to HOT operating conditions saturate the integration capacitor before building any signal charge information. This predicts an advantage for V_{OC} operation when

accounting for small FPA integration capacitor sizes and will be explored using a proposed architecture in the following chapter.

6 Open-Circuit Voltage Photodetector Architecture

This chapter will use concepts from Chapter 5 and analytical modeling and experimental measurements to evaluate the potential for using an open-circuit voltage photodetector (VocP) architecture for HOT MWIR detectors. As discussed in Chapter 5, V_{OC} is logarithmically dependent on photon irradiance (E_q). One way to mitigate this effect is by coupling the diode V_{OC} to the gate of a complementary metal-oxide semiconductor (CMOS) transistor operating in sub-threshold mode. In this mode, the drain current has an exponential dependence on the gate-source voltage (V_{GS}). This VocP architecture decouples the photodiode dark current from the pixel charging capacitor in the circuit and adjusts the logarithmic relationship with the irradiance. Alleviating these two limitations leads to the possibility of using longer integration times for imaging applications where the charge-capacitor size is limited due to smaller pixel pitch, creating an opportunity to improve the NEDT without compromising ROIC design.

In this chapter, we will cover the overall concept and operating principle of the VocP architecture, develop the analytical model, and discuss the experimental radiometric results supporting the developed model. Then, specific impact factors, such as multiple diode strings and the VocP dynamic range, will be discussed to present more advantages of using the VocP for HOT, small pixel pitch IR imaging capabilities.

6.1 VocP Concept

In the interest of advancing IRFPA performance, the architectural interface between the III-V detector material and the silicon readout integrated circuit (ROIC) technology was studied to provide a proposed pixel architecture as part of a highly collaborative effort

across several research groups.[87, 89, 95] As depicted in Figure 57(a), an overall circuit diagram shows a FPA unit pixel, selected to reflect a conventional ROIC, with a four-transistor (4T) topology used in CMOS Image Sensor (CIS) technology. To compare, Figure 57(b) illustrates the conventional or traditional diode configuration that is used with this pixel topology. The conventional method of detection uses a direct-injection current into the ROIC pixel to determine the illumination seen by the diode.

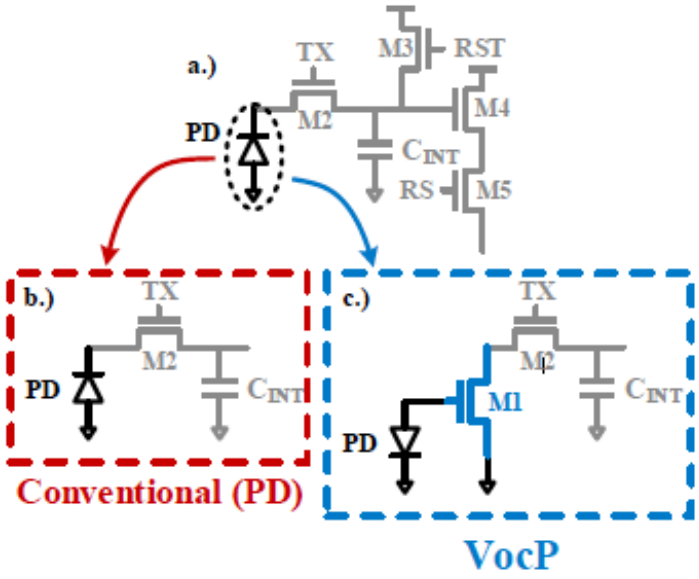

Figure 57. (a) A ROIC pixel unit cell that can be configured with either (b) a conventional diode configuration that directly injects current or (c) a VocP configuration with current modulated through an NMOS transistor.[95]

Leveraging a diode operating under open-circuit conditions with the advantages outlined in Chapter 5, a circuit architecture that achieves a linear response to irradiance, E_q was developed. The VocP, illustrated in Figure 57(c), is a new approach to photon detection that uses a conventional IR photodiode to generate an open-circuit voltage (V_{OC}) under IR illumination, and controls the drain current of a transistor through the gate. The current

flowing through the transistor operating in the sub-threshold region is determined by V_{OC}, is proportional to E_q, and is the current monitored rather than the photo-generated current of the photodiode. This provides the basis for the concept, and specific derivations will be presented in the operating principle section to provide a more detailed proof and analytical model.

The VocP architecture is predicted to provide three main advantages for infrared detection over the conventional reverse-bias current implementation. First, the sensitivity of conventional reverse-bias operating diode is dependent on pixel size, whereas for the VocP architecture, this is not the case. This was proven in Chapter 5 when considering pixel area dependence on the diode V_{OC}. Second, the VocP circuit topology is designed to be compatible with a CIS architecture, currently used in visible cameras, to reduce the cost associated with a custom IRFPA ROIC. This choice also was dictated by the desire to break away from traditional custom ROIC design to promote a path forward for small pixel integration. Finally, the dynamic range is increased due to the V_{OC} and the resulting linear increase of the transistor current with incident photon irradiance versus the conventional photodiode. The dynamic range will be discussed in a later section.

6.1.1 Operating Principle

In the VocP architecture, two distinct components come together to form the individual unit: a photodiode and a transistor. The photodiode was extensively discussed in Chapter 5, and those results are considered in the VocP diode analysis. Some additional background is needed for perspective for the transistor operation in this configuration. The transistor used in the VocP circuit architecture operates in the sub-threshold region of the

IV characteristic curve, where the gate-source voltage (V_{GS}) is less than the threshold voltage (V_{th}) of the transistor, as seen in Figure 58. A gross approximation that the drain current is zero in this region is typical. However, a closer look at the carrier drift between the drain and the source when $V_{GS} < V_{th}$ brings a non-zero result to the transistor drain current below threshold. This produces a leakage current that is dependent on the semiconductor properties of the transistor. In sub-threshold, the transistor functions exponentially with V_{GS}, as seen in Figure 58(b). This exponential function will be leveraged as the diode and the transistor are connected together.

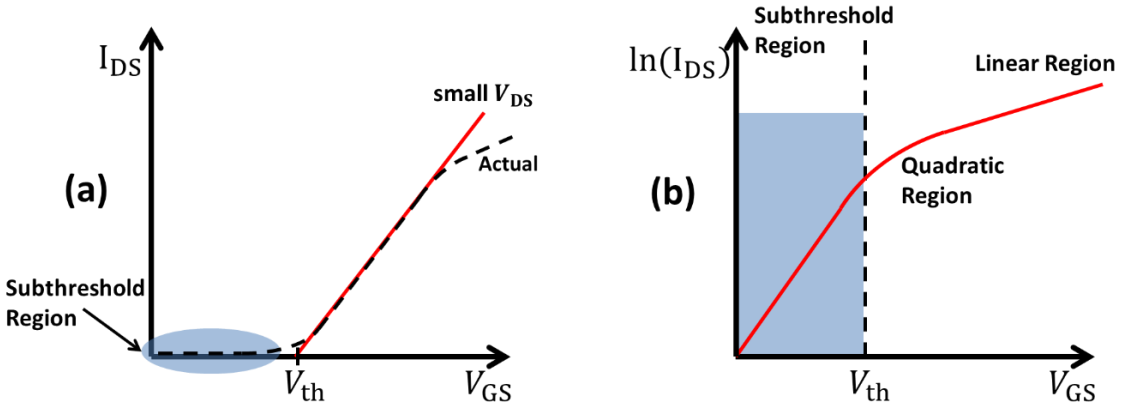

Figure 58. (a) The IV characteristics of an NMOS transistor for fixed VGS voltages, where the linear region operates like a resistor and the saturation region operates like a current source. (b) The IV characteristics of an NMOS transistor in the sub-threshold region in a log-linear plot.

For the demonstration of the VocP architecture, the diode anode is connected directly to a gate of an n-type metal-oxide semiconductor (NMOS) transistor operating in sub-threshold (see Figure 57(c)). The cathode is connected to the ground or common line of the ROIC. Due to the high impedance of the NMOS gate terminal, the VocP diode effectively is loaded by an open circuit. Therefore, no current flows through the diode, and

a V_{OC} is established that depends on E_q. The remainder of the selected ROIC pixel unit cell can remain the same. Here, the 4T pixel topology (Figure 57(a)) is being treated as the remainder of the ROIC to complete the explanation of the VocP signal chain, but will not be considered in the analytical model of the VocP architecture.

The expected current signal out of the VocP ($I_{Signal,VocP}$) is derived from combining the open-circuit voltage equation (5.9) repeated here:

$$V_{OC} = n_{diode}\frac{k_B T}{q}\ln\left(\frac{q\eta E_q A_{diode}}{I_{sat}} + 1\right) \tag{5.9}$$

with the NMOS sub-threshold drain-to-source current ($I_{DS,s-t}$) equation given by:

$$I_{DS,s-t} = I_{D0}\left(\frac{W}{L}\right) exp\left(\frac{V_{GS}}{n_{FET}}\frac{q}{k_B T}\right) \tag{6.1},$$

and the transistor leakage current (I_{D0}) given by: [96-98]

$$I_{D0} = \mu_n C_{ox}(n_{FET} - 1)\left(\frac{k_B T}{q}\right)^2 exp\left(\frac{-V_{th}}{n_{FET}}\frac{q}{k_B T}\right)\left[1 - exp\left(\frac{-V_{DS}}{n_{FET}}\frac{q}{k_B T}\right)\right] \tag{6.2},$$

where the NMOS variables are its ideality factor (n_{FET}), transistor gate aspect ratio $\left({}^{W}/_{L}\right)$ where W is the width and L is the length, and the gate-source voltage (V_{GS}). The transistor leakage current I_{D0} is process dependent because the electron mobility (μ_n) and the oxide capacitance density (C_{ox}) are dictated by the silicon semiconductor material and the drain-source voltage (V_{DS}).

The combination of these equations, and resultant VocP analytical model equation, are explained in detail here. First, Eq. (6.2) is substituted into Eq. (6.1) to expand the transistor sub-threshold current:

$$I_{DS,s-t} = \mu_n C_{ox}(n_{FET} - 1)\left(\frac{k_B T}{q}\right)^2 exp\left(\frac{-V_{th}}{n_{FET}}\frac{q}{k_B T}\right)\left[1 - exp\left(\frac{-V_{DS}}{n_{FET}}\frac{q}{k_B T}\right)\right]\left(\frac{W}{L}\right) exp\left(\frac{V_{GS}}{n_{FET}}\frac{q}{k_B T}\right).$$

For the sake of simplifying the equation, the equation is rearranged and the constants grouped into the sub-threshold diode saturation current term, $I_{S,s-t}$ that considers $\left({}^{W}/_{L}\right)$ with I_{D0}:

$$I_{DS,s-t} = I_{S,s-t} exp\left(\frac{V_{GS}-V_{th}}{n_{FET}}\frac{q}{k_B T}\right)\left[1 - exp\left(\frac{-V_{DS}}{n_{FET}}\frac{q}{k_B T}\right)\right].$$

Then, because V_{DS} is a constant large voltage and V_{DS} is much larger than V_{GS}, ($V_{GS} \ll V_{DS}$), it is assumed that the small signal approximation when $1 - exp(\mathrm{x}) = 1$ can be used, and the term containing V_{DS} to equal 1 is allowed, giving a further simplified version of $I_{DS,s-t}$:

$$I_{DS,s-t}(V_{GS}) = I_{S,s-t} exp\left(\frac{V_{GS}-V_{th}}{n_{FET}}\frac{q}{k_B T}\right).$$

The NMOS transistor and diode are selected to ensure that V_{OC} remains below the nMOS threshold voltage (V_{Th}). For the total VocP signal current ($I_{Signal,VocP}$), the open-circuit voltage equation (5.9) is substituted for V_{OC} as the V_{GS} voltage into $I_{DS,s-t}$:

$$I_{DS,s-t}(V_{OC}) = I_{S,s-t} exp\left(\frac{V_{OC} - V_{th}}{n_{FET}}\frac{q}{k_B T}\right)$$

$$I_{DS,s-t}(V_{OC}) = I_{S,s-t} exp\left[\frac{-n_{diode} V_{th}}{n_{FET}} \ln\left(\frac{q\eta E_q A_{diode}}{I_{sat}} + 1\right)\right].$$

Using the basic rules of exponents and logarithms, we essentially can cancel out the exponential and logarithmic problems with the two individual equations and come to a linear relationship between the diode characteristics and the transistor characteristics as they are joined together. The $I_{DS,s-t}$ rearranges to be:

$$I_{DS,s-t}(V_{OC}) = I_{S,s-t} exp\left(\frac{-V_{th}}{n_{FET}}\frac{q}{k_B T}\right)\left(\frac{q\eta E_q A_{diode}}{I_{sat}} + 1\right)^{\beta},$$

$$\beta = \frac{n_{diode}}{n_{FET}} \qquad (6.3).$$

Finally, we use a new term I_{Leak} to define the leakage term in the equation that is created by the threshold voltage component,

$$I_{Leak} = I_{S,s-t} exp\left(\frac{-V_{th}}{n_{FET}} \frac{q}{k_B T}\right)$$

with a substitution it into $I_{DS,s-t}$:

$$I_{DS,s-t}(E_q) = I_{Leak}\left(\frac{q\eta E_q A_{diode}}{I_{sat}} + 1\right)^{\beta} \quad (6.4).$$

The final result in Eq. (6.4) allows us to relate the drain-source current of the NMOS ($I_{DS,s-t}$) directly to the V_{OC} and, therefore, E_q.

In order to find the expected current signal out of the VocP ($I_{Signal,VocP}$), the scene contrast is needed to develop the difference between the current signal when the diode is illuminated with the IR irradiance versus the background irradiance of the scene. This is essentially the VocP version of what is traditionally called the photo-generated current. In the case of VocP, this comes from the difference between two transistor drain currents at two different irradiances ($E_q - E_{q,bkg}$), which now can be defined as $I_{Signal,VocP}$:

$$I_{Signal,VocP} = I_{DS,s-t}(E_q) - I_{DS,s-t}(E_{q,bkg})$$

$$I_{Signal,VocP} = I_{Leak}\left[\left(\frac{q\eta E_q A_{diode}}{I_{sat}} + 1\right)^{\beta} - \left(\frac{q\eta E_{q,bkg} A_{diode}}{I_{sat}} + 1\right)^{\beta}\right] \quad (6.5)$$

At low E_q, $I_{Signal,VocP}$ is linear, and at high E_q, it has a polynomial dependence on β. By taking these steps through the functions of each component of the VocP architecture, and incorporating them together, we have developed a full analytical model of the diode and transistor combination. A radiometric experiment was conducted to validate the concepts

proposed to understand how measured data would fit to the developed model and will be discussed in the next section.

6.1.2 Radiometric Demonstration

Once the analytical model for the VocP architecture as defined by Eq. (6.5), a proof-of-concept demonstration is presented to understand the measured performance of the VocP. An electro-optical characterization test setup, similar to what has been described for radiometric measurements in Chapter 2, was combined with the custom ROIC developed for the transistor component of the VocP to connect to MWIR photodiodes. The transistor was integrated into the custom ROIC chip developed for the VocP concept and tested using a coordinating analog-to-digital converter (ADC) development board with pixel timing. Figure 59 presents a schematic diagram for the test. The measurement was taken with the ROIC by operating the diode in both the reverse-bias and VocP configurations, giving a direct comparison of the VocP pixel to a traditional photodiode under reverse-bias current conditions.

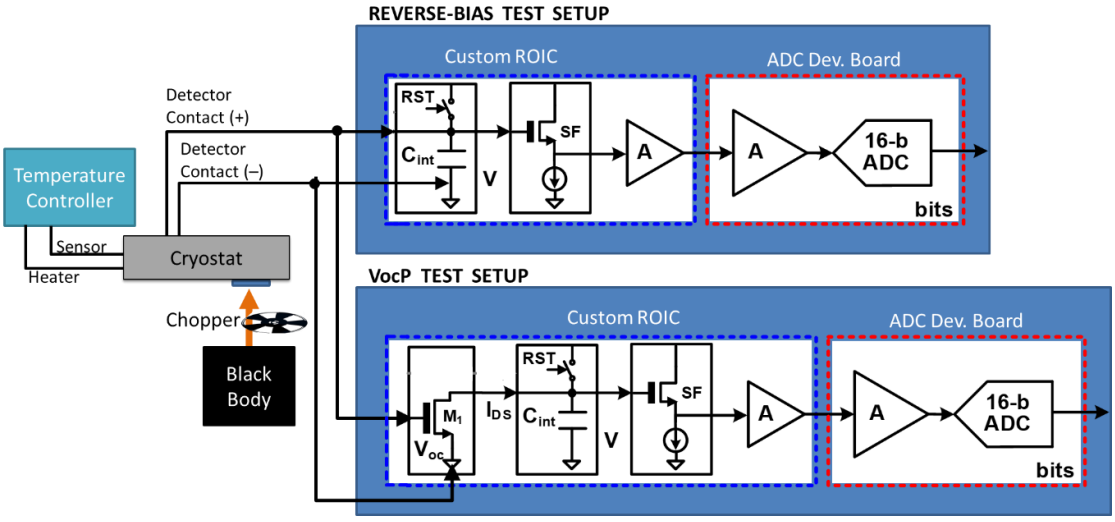

Figure 59. Radiometric test and measurement setup to determine the VocP model performance and compare the reverse-bias diode model performance.

The VocP detector configuration was tested and the signal vs. irradiance was verified to fit these estimations analytically, which is displayed in Figure 60. The irradiance is controlled by adjusting the temperature of a calibrated blackbody in increments of 10 C to vary the irradiance incident upon the MWIR detector under test. The measured data were fit to the model defined by (6.2). For both tested diodes, a commercial series of InAsSb diodes (Hamamatsu P13243-011MA) designed for room-temperature photovoltaic operation and an interband cascade diode were used,[27] and the quality of the fit and the fit coefficients support this model for the VocP signal. These experimental results confirm that the VocP configuration leads to the expected signal, $I_{Signal,VocP}$ across a large irradiance range of 10^{15} – 10^{18} photons/s-cm^2.

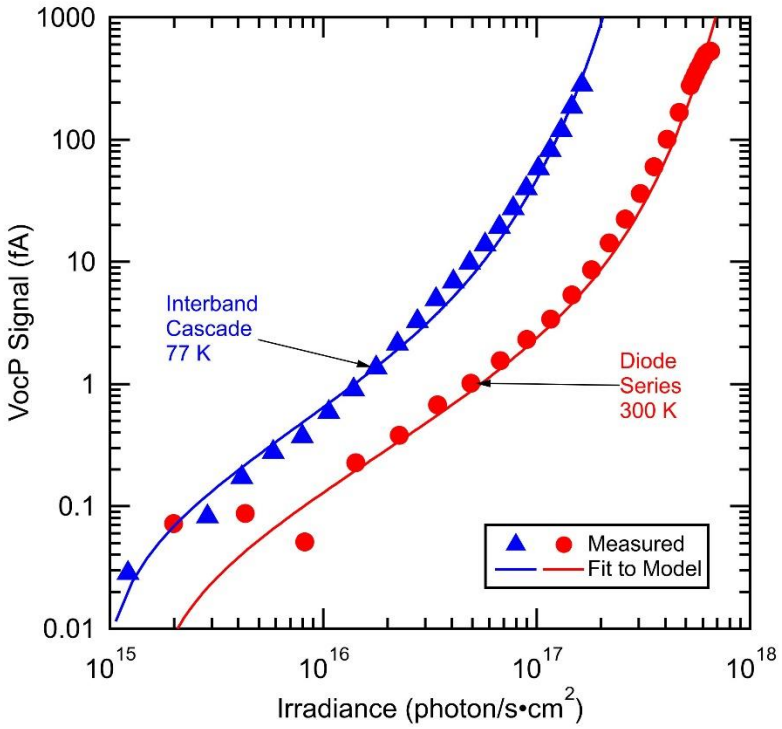

Figure 60. Comparison of measured VocP signal current (also the output NMOS drain current) as a function of the input irradiance for two different diodes at 300 K and 77 K, with a best fit to the model defined by (6.5).[89]

The fits to the developed model were analyzed and reflected reasonable coefficients for several parameters that were considered in the analytical equation in (6.5). For instance, the NMOS ideality factor, n_{FET}, was found to be between 1.25 and 1.32, which was within the conventional transistor ideality factor range of 1 – 1.5. The leakage current, I_{Leak}, was fit to be between 1.5 – 2.7 pA, which is realistically low as expected. The difference in exponential term β in (6.3) leads to a difference in the two diodes tested. In the case of the commercial series of InAsSb diodes, this ratio is dominated by the number of diodes in series and leads to a large β. In the interband cascade, the β is theorized to be dominated by the number of cascade junctions, but the n_{diode} term was difficult to match to the theory, and did not match up with the number of cascade junctions as predicted. However, the difference between the detector irradiance and the background irradiance were quite similar between the two test diodes and was found to be about 8×10^{-20} – 12×10^{-20} s-cm^2/photon.

The investigation of the diode physics and the potential for using a novel open-circuit voltage photodetector architecture instead of the conventional reverse-biased current for its advantages related to small pixels and potential for higher operating temperatures has been discussed. Good agreement has been obtained for the signal and noise between experimental results and an analytical model. The photodiode and transistor combination restricts the dark current by orders of magnitude over the intrinsic dark current of the diode and provides a roughly linear dependence on irradiance with reasonable fit coefficients to support the model parameters. As infrared imagers continue reducing the pixel pitch, and consequently the ROIC integration capacitor size, the dynamic range becomes important for MWIR and LWIR high-density FPAs under HOT conditions. The

proposed VocP architecture could have potential benefits in the design of imaging circuits with high speed, high dynamic range, and low noise in the IR region as well as in the visible region.[95] Further considerations on diode series performance and dynamic range are presented below.

6.2 Considering Multiple Diodes

When considering the analytical model developed for the VocP architecture in (6.5), the exponential term β in (6.3) was analyzed to identify the impact a series of diodes would have on the VocP. Previous measurements have shown that devices connected in series operating in open-circuit mode can provide enhanced signal by increasing the number of diodes connected. This is based on Eq. (6.3), where the diode ideality factor can increase in favor of the diode operation, and essentially magnify the V_{OC} with the same E_q Also, establishing that at a DC level, diodes build voltage when connected in series, similar to Figure 61, favors the addition of V_{OC} with its advantages to enhance the V_{OC} signal for the VocP architecture.

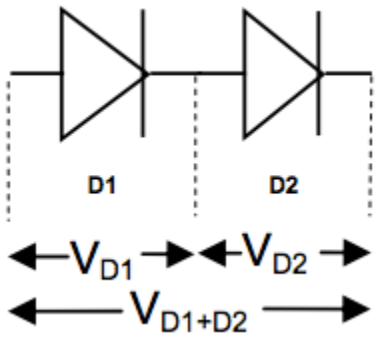

Figure 61. Diodes in series with one another can add up to larger voltage levels that one diode could not accomplish on its own.

Equipped with the knowledge that series-connected detectors build voltage, preliminary attempts to fabricate several individual pixel detectors in series were completed as a backside illuminated set of diodes for radiometric demonstration of the VocP concept with diodes in series. Initial fabrication results can be found in the SEM images in Figure 62 and Figure 63.

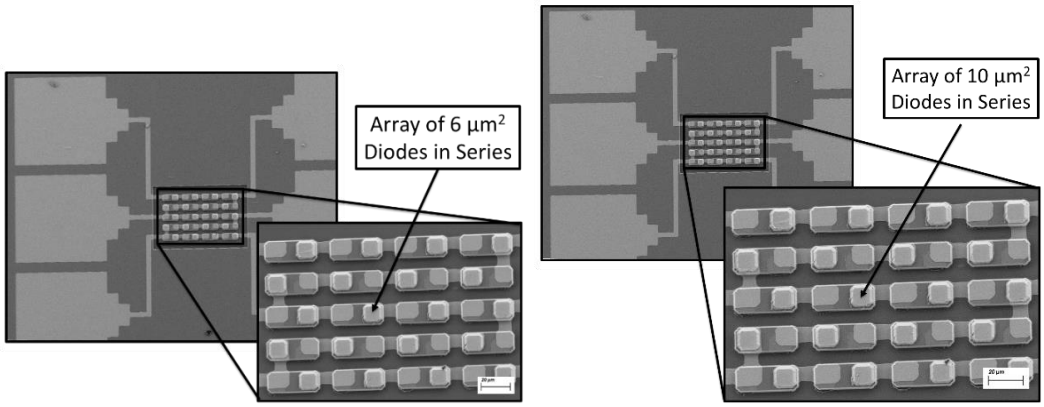

Figure 62. SEM images of fabricated diodes in series with an individual active area of 6 µm2 each and 10 µm2 each to use in proof-of-concept backside illumination design for radiometric test and measurement.

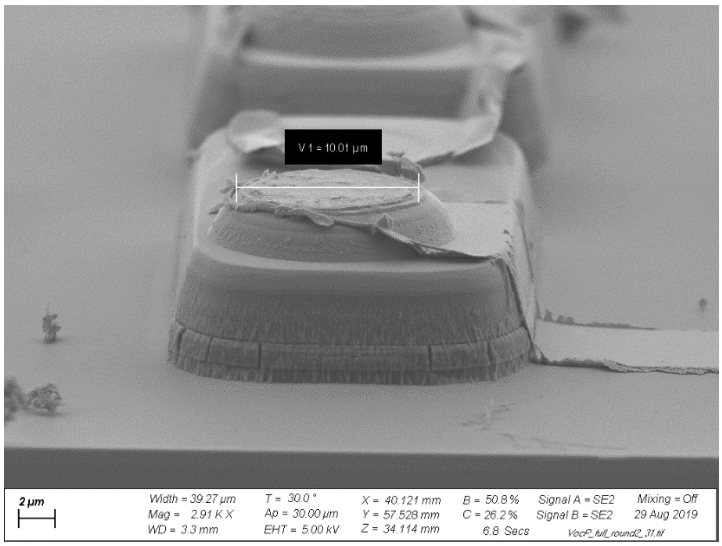

Figure 63. SEM image of single fabricated diode in series with other fabricated diodes with an active area of 10 µm^2. The diodes were connected in series with Au metal contacts as shown along the sidewall of the diode.

Fabricating the series connected diodes provided experience for fabricating smaller diode pixels. The variation of signal and noise as the series can be broken into smaller groups and can be compared to the individual pixel V_{OC} measurements as seen in Figure 54. Measuring the linearity of the detector is also needed as well as the associated fixed pattern noise generated in the open circuit mode. The SEM images show the series of 10 μm^2 diodes connected together in Figure 62 and Figure 63. However, further fabrication optimization is required.

Overall, optimizing the scaling of the photodiode and transistor to the smaller dimensions required by IRFPAs will demonstrate how much the noise and dark current levels will reduce as overall pixel size is reduced.

6.3 Dynamic Range

The radiometric demonstration of the VocP architecture showed the predicted performance across multiple orders of magnitude in irradiance ranging from 10^{15} – 10^{18} photons/s-cm^2. The VocP has a large span due to its dynamic range that comes from the V_{OC} as it increases logarithmically with incident irradiance, and the photocurrent through the transistor as it increases exponentially with V_{OC}. In combination, this equates to a linear increase in the signal of the VocP architecture at current levels that are several orders of magnitude lower than conventional direct-injection photodetector currents. Moreover, gain provided by the transconductance of the NMOS transistor enables faster operation of the VocP detectors for that same reason.

As discussed in the NEDT section in Chapter 5, infrared imagers continue to reduce the pixel pitch, making the ROIC integration capacitor size follow suit, which limits the

charge capacity due to the smaller real estate dictated by the pixel size. In addition, raising the operating temperature inherently raises the dark current and forces the FPA to operate at a shorter integration time because the dark current saturates the capacitor and the small pixel real estate will not allow for a large capacitor. This ultimately reduces the dynamic range of conventional FPAs operating at HOT conditions. In contrast, the VocP architecture takes advantage of the significantly reduced current levels and leverages those currents to obtain large dynamic range even when the ROIC integration capacitor size is small.

The extent to which VocP pixel sensitivity can be improved is dependent on the ability of the photodetector to generate sufficiently high V_{OC} at high temperatures and small detector area. The indirectly generated photocurrent equivalent, I_{DS}, in the VocP pixel provides potentially lower current noise and leakage at the integration node than the noise current directly contributed by the photocurrent in a typical infrared photodetector. This improved NEP enables room temperature operation of the VocP and provides comparable or superior performance for pixels below 50 μm in size.

However, any incumbent imaging technologies will continue to be used despite the development due to the variation in open-circuit voltages between individual detectors on an FPA. While the dark current of the individual detector is decoupled from the ROIC integration capacitor in the VocP architecture, the traditional direct-injection configuration provides a more stable, uniform signal condition for the overall FPA operation through detector biasing.

One caveat to the VocP architecture is in the theory of operation for the transistor. The NMOS transistor is designed to operate in the sub-threshold region, which means the transistor needs to be designed specifically to expand that region as much as possible before turning over into the linear region. The open-circuit voltage also needs to stay within that design constraint or else the resultant drain-source current will yield unpredicted behavior, and the presented model will break down. While we could probably model for the behavior in the linear region, the uniformity effects from pixel to pixel will be a larger issue because the impact of the non-uniform voltages and current on the overall FPA system will limit the system performance. In terms of technological impact, the VocP architecture will support applications that can trade off longer integration times for increased sensitivity and dynamic range, but research on these effects is needed and proposed future studies are described in Chapter 7.

6.4 Summary

The modeling and experimental measurements to evaluate the potential for using an open-circuit voltage photodetector (VocP) architecture for HOT, small pixel detectors was introduced. In the VocP architecture, two distinct components come together to form the individual unit: a photodiode and a transistor, where photodiode is connected to the gate of a NMOS transistor operating in the sub-threshold region to provide an open-circuit voltage signal based on an irradiance level to the gate-source voltage (V_{GS}) of the transistor.

The resultant radiometric demonstration of the VocP architecture provided good agreement between the developed analytical model and the measured data over multiple orders of magnitude in irradiance. The photodiode and transistor combination restricts the

dark current by orders of magnitude over the intrinsic dark current of the conventional diode, and provides a roughly linear dependence on irradiance with reasonable fit coefficients to support the model parameters.

As infrared imager designs continue to reduce the pixel pitch, the ROIC integration capacitor size, the transistor, and the dynamic range become important for VocP operation. ROIC integration capacitor size follows the pixel pitch and constraint the charge capacity, but using the VocP architecture allows for longer integration times because the high dark currents don't saturate the integration capacitor as it is decoupled from the photodiode through the transistor. In terms of technological impact, the niche that the VocP detector provides a solution to support large format FPAs with small pixel pitch and small capacitor ROICs for HOT MWIR and LWIR operation. Applications that can trade off longer integration times for increased sensitivity and dynamic range, such as photon-starved scenes, will especially benefit from this architecture.

Focusing on the fundamental characteristics of the photodiode, the variances on the open-circuit voltage reveal how the generation-recombination can affect the detector. Material defects can create traps and surface effects can produce parallel shunt resistances, consequently both scenarios would degrade the open-circuit voltage component for the detector that is integrated into the VocP architecture. These issues can be improved or mitigated with high-quality, uniform epi growth and with passivation. Advanced modeling of both the detector and the ROIC will help bridge these design constraints and find optimized configurations for both components of the VocP architecture for future imaging technologies.

7 Conclusions and Future Work

This dissertation research has focused on the overall improvement of the performance of MWIR and LWIR detectors for HOT conditions at small pixel pitch for future IR sensor technologies. This chapter completes the dissertation with concluding remarks and visions for future work based on the research findings contributing toward HOT, high-density FPA imagers. Several research challenges associated with the development of small SLS detector pixels operating at high temperatures were noted, including investigating the underlying device physics in heterostructure engineering, passivation, and the interface between detector materials and ROICs. Three main contributions were highlighted for their results and potential impact on the scientific knowledge base, specifically connecting to superlattice heterostructure engineering, detector surface leakage current suppression with passivation, and demonstration of an open-circuit voltage photodetector (VocP) architecture.

7.1 Conclusions

This work contributes to the research community knowledge by identifying some of the scientific challenges limiting current detector technology related to high-density, HOT FPAs and investigating the underlying device physics to mitigate poor performance through three main contributions as summarized below:

- **Superlattice Heterostructure Engineering**: Designed, fabricated, and tested unipolar barrier nBp detectors with InAs/GaSb, InAs/InGaSb, and InAsSb/GaAsSb SLS detectors.

- **Suppression of Surface Leakage Current with Passivation:** Investigated the use of Al_2O_3 and ZnO via atomic layer deposition (ALD) to reduce the surface leakage current in LWIR detectors.
- **Demonstration of an Open-circuit Voltage Photodetector (VocP) Architecture:** Re-examined the relative advantages of using the reverse-bias photocurrent of a photodiode versus using the open-circuit voltage under the same conditions. Investigated the detector physics through analytical modeling, fabrication, integration, and test of a VocP detector and explored the potential of using this for high operating temperature (HOT) small pixels in FPAs.

7.1.1 Superlattice Heterostructure Engineering

Through SLS heterostructure engineering, several unipolar barrier nBp detectors using the binary-binary InAs/GaSb and InAs/(In)GaSb, and the ternary-ternary InAsSb/GaAsSb SLS material systems were designed and simulated using NRL MultiBands™. A baseline study was conducted using the well-studied 14ML/7ML InAs/GaSb T2SL heterostructure, to which a pin detector and a unipolar barrier nBp detector were grown, fabricated, and tested. The measured results were compared to the NRL MultiBands™ simulations to understand the differences between ideal detector behavior and the behavior of the as-grown devices. Results from the baseline pin structure show good agreement with the simulations, but the dark current density was too high and the EQE was too low to be considered for future FPA development. By optimizing the detector design to include a barrier in the detector stack, the nBp detector was simulated to reduce the overall dark current observed during the pin detector study. The nBp detector

design was grown, fabricated, and measured, but dark current results of the as-grown sample were ohmic due to the surface effects created by the fully delineated pixel, which ultimately inverted the intended detector design. This led to an important conclusion that fully delineating the barrier detector unintentionally inverts p-type absorber designs, confirming previous p-type absorber research, and was confirmed in this work to also occur in InAs/GaSb LWIR SLS absorbers. It was also discovered that the inversion can be simulated with NRL MultiBands™ to show how the resultant detector blocks the minority carrier electrons from flowing through the detector design as intended.

To influence future barrier detector designs and alleviate growth challenges of LWIR SLS materials, a ternary-ternary InAsSb/GaAsSb SLS heterostructure design was proposed with a high Sb fraction within the detector. By fixing the Group-V parameters for the As and Sb compositions, the growth conditions aim to promote easier shutter sequencing. Simulations using NRL MultiBands™ across a range of Sb fractions for the InAsSb/GaAsSb SLS heterostructure provided favorable preliminary results, which indicated a possible direct-to-indirect bandgap transition that has not been explored, especially for the InAsSb/GaAsSb SLS with an Sb fraction of 50%. These designs will require more research to understand the advantages involved in the ternary-ternary design, but growing, fabricating, and testing the proposed barrier detector designs will provide steps forward with this research in the future.

7.1.2 Suppression of Surface Leakage Current with Passivation

We investigated passivation techniques on a dual-band LWIR InAs/GaSb pBp barrier detector and a MWIR InAs/InAsSb pn diode to reduce the surface leakage current

seen in these detectors. By using Al_2O_3 and ZnO via atomic layer deposition (ALD), we were able to employ these passivation techniques through fabrication and measure the dark current to understand the surface effects on the fully delineated detector pixels. Results between passivated and unpassivated detectors were compared using variable area diode arrays, and show that both Al_2O_3 ALD film and ZnO ALD treatment reduced the sidewall surface leakage current on these single pixel detectors by at least two orders of magnitude, where the passivated samples showed bulk-limited dark current characteristics over a range of diode sizes from 50 μm^2 to 500 μm^2 under reverse-bias voltage at 77 K. Further optimization to improve the bulk-limited performance at other biases and temperatures is needed, but the techniques used for this research are encouraging to attain bulk-limited performance of small pixel detectors.

7.1.3 Demonstration of an Open-circuit Voltage Photodetector (VocP) Architecture

Transitioning from the material-related challenges to researching the more device-centered aspects of these detectors was crucial to examining the viability of other sensing configurations for future IR detector technology. As part of a large collaborative effort, we re-examined the relative advantages of using the reverse-bias photocurrent of a photodetector versus using the open-circuit voltage under the same conditions. By investigating the detector physics through analytical modeling, fabrication, integration, and test of a VocP detector, we explored the potential of using this architecture for high operating temperature (HOT) small pixels in FPAs. The comparison of the developed models to the measured data support the premise that the open-circuit voltage operation can be modeled using standard diode physics. Further analysis found favorable operating

conditions for the open-circuit voltage detector through noise equivalent temperature difference (NEDT) models using standard radiometric optics for high density FPAs at different integration times and temperatures. The resultant radiometric demonstration of the VocP architecture provided good agreement between the developed model and the measured data over three orders of magnitude in irradiance ranging from 10^{15} – 10^{18} photons/s-cm^2, with capability to go higher. Experimental results have delivered strong evidence that integrating a diode and transistor together to form a new option for IR detection is extremely valuable to the research community. We believe the VocP detector provides a solution to support large format FPAs with small pixel pitch and small capacitor ROICs for HOT MWIR and LWIR operation. Applications that can trade off longer integration times for increased sensitivity and dynamic range will especially benefit from the VocP architecture, ultimately filling a technological void in infrared imaging under HOT MWIR conditions.

To conclude, this research has expanded the fundamental boundaries in infrared detector technology through material system designs and processes, and through the critical role of the detector to readout integrated circuit (ROIC) interface for future advancements toward high-density, HOT FPAs.

7.2 Future Work

Based on the results and conclusions in this dissertation, future studies can take several directions. Specifically, expanding the study on ternary-ternary heterostructure design, optimizing the ALD passivation techniques using Al_2O_3 and ZnO, and exploring

deeper implications of the VocP architecture for future IRFPA development will be explored below.

7.2.1 Investigating Properties of Ternary-Ternary SLS Materials

The immediate results from the ternary-ternary SLS heterostructure material study using Sb fractions of 35% to 57% advances the scientific understanding of these superlattice heterostructure systems by revealing the possibility of MWIR and LWIR ternary-ternary SLS detectors. By simplifying shutter sequencing through fixed Group-V compositions of As and Sb, the proposed designs help realize an alternate solution to the growth challenges faced when developing LWIR detectors. Simulations using the *k·p* modeling tools in NRL MultiBands™ as described in Chapter 3 show several possible combinations of lattice-matched InAsSb/GaAsSb ternary-ternary SLS designs for the MWIR or LWIR regions, where the direct bandgap is in the MWIR region, but a possible indirect bandgap sits in the LWIR region. Future growths using the aforementioned compositions and heterostructure SLS designs would allow us to explore the properties of the ternary-ternary SLS. By measuring the PL, XRD, and lifetime of an epi layer based on the InAsSb/GaAsSb (20ML/15ML) with 50% Sb would be incredibly useful to the community and would establish the viability of the direct-to-indirect bandgap transition observed during the modeling. Simple PL measurements could confirm if both the MWIR bandgap transition and the LWIR bandgap transition are detected. This could also employ a possible way to understand the indirect bandgap properties of SLS detectors where little exploration has been completed.

Lessons learned from the design process of these detectors can also be applied to future studies of p-type SLS LWIR FPAs. With the results, the p-type absorber technology can develop into feasible and valuable enhanced sensing capability for LWIR applications. Specifically continuing the research into the growth, fabrication, and testing phase of the simulated InAs/(In)GaSb binary-binary nBp and the InAsSb/GaAsSb ternary-ternary nBn designs described in Chapter 3 would contribute to the scientific knowledge base significantly by introducing more SLS detectors into the design space.

In particular, the next steps for the nBp detector design would be to passivate the devices to compare the change in the detector performance with the conclusions from the previous results, which would predictably be improved. This would allow for some conclusive evidence to complete the nBp study by showing the improved dark current and quantum efficiency over the pin detector study.

Additionally, steps to complete a design of experiments based on the absorber designs simulated for the ternary-ternary InAsSb/GaAsSb SLS would give this research a more complete conclusion on addressing how p-type absorbers can be leveraged for LWIR applications. The results from the growth, material characterization, fabrication, and test of the InAsSb/GaAsSb ternary-ternary absorber designs and the nBn detector design for this design of experiments would bring valuable knowledge to the IR detector research community.

7.2.2 Quantitative Comparison of ALD Passivation Techniques on LWIR Detectors

The successful studies presented using different passivation techniques show how passivating small pixels can be completed using ALD, specifically with Al_2O_3 and ZnO.

While it would be fair to conclude the ZnO-treated detectors performed better after passivation, each study was conducted on a different detector stack, therefore the two ALD processes would have to be administered on the same detector structure to be properly compared. This can be done most effectively by choosing a barrier detector with a p-type absorber because the shunt resistance due to surface effects is more prominent in p-type materials. The ZnO ALD treatment should also be tested on a fully delineated barrier detector stack because the study in this dissertation only used a pn detector. Completing a comparison study would be beneficial to understand the commercial benefits of ALD passivation and provide a standard to treating the sidewalls of p-type SLS detectors.

Passivating FPAs is an additional direction of study that is needed for p-type SLS barrier detectors. This work solidifies that ALD can be used as a proven passivation technique to improve their performance at the individual pixel level, but effectively passivating an FPA presents additional challenges due to the smaller pixel sizes on larger format arrays. This complicates the deposition of a passivation layer while maintaining pixel pitch and device integrity. Fortunately, ALD is a proven deposition choice for large-area conformal coverage, and Al_2O_3 is a common material system for ALD. The reported approach has a reasonable expectation of success for passivation of future device applications such as LWIR p-type T2SL FPAs.

7.2.3 VocP Test and Measurement

The development of the VocP architecture model and the experimental measurements validating the model resulted in strong evidence that integrating a diode and transistor together can track the irradiance incident on the detector through to the transistor

drain-source current. This is a promising new option for IR detection and is extremely valuable to the research community, but further investigation into several aspects of this architecture is needed to fully understand the physics behind the design and the implications on the overall potential of using this architecture for high operating temperature (HOT) small pixels in FPAs.

Specifically, an experimental demonstration of the NEDT to challenge and compare the models developed for the reverse-bias operation and the open-circuit operation across temperature should be conducted to determine the validity of the analytical model and the claim of the impact on the integration time. The larger question on quantifying the integration time with a small integration capacitor size would prove what tradeoffs there are when operating at open-circuit voltage conditions and how that affects the overall FPA operation.

The measured detector noise discussed in Chapter 5 will translate over to the VocP pixel and will affect the output of the transistor, but it is not known to what extent the noise will influence the overall VocP design. Examining the changes in the open-circuit voltage at the detector while the monitoring the changes in the drain-source current of the transistor will identify this behavior and its impact on the VocP signal. This will be especially important when considering uniformity across an FPA because each individual pixel will be producing a voltage that may prove to be inconsistent throughout the array if several material factors are not addressed such as shunt resistance or material quality.

From a system perspective, tradeoffs will also need to be considered and confirmed experimentally. While the VocP takes advantage of decoupling the detector dark current

from the ROIC integration capacitor versus the incumbent direct-injection operation, the transistor will need to be designed to stay within a specific region that may limit the range of detection. Understanding the dynamic range by measuring the VocP signal over a large range of irradiances and detector operating temperatures will provide answers to these limits and how well they compete with other sensor measurement methods, such as the direct-injection method. Continuing to advance the analytical modeling of both the detector and the ROIC will help bridge design constraints and find optimized configurations for both components of the VocP architecture for future imaging technologies. Overall, maturing this technology will allow for product commercialization and propel exploring the benefits of IR technology forward as more non-invasive sensing techniques are being applied in many aspects of our lives.

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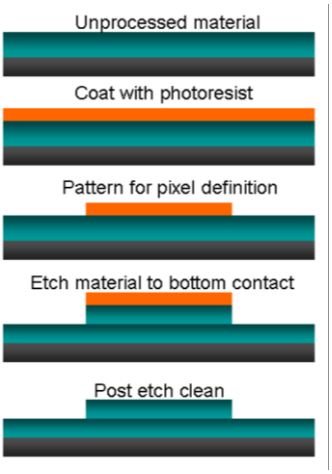
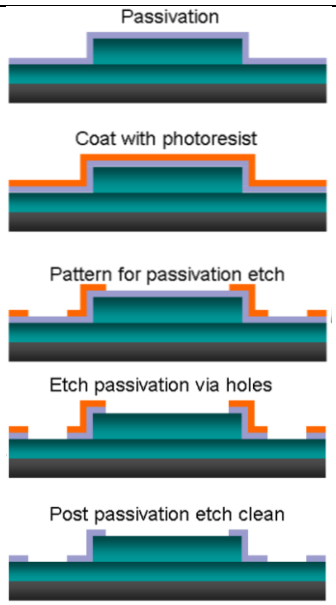
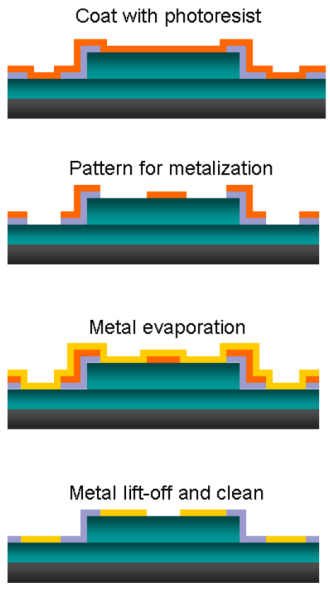
Appendix A. Detailed Fabrication Steps

<table>
<tr><th colspan="3">Abbreviated Single Pixel Detector Fabrication Procedure</th></tr>
<tr>
<td>MESA</td>
<td>
STEP.1. Clean the sample with acetone, methanol, IPA for 1 min each, and heat up at 150C for 5min

STEP.2. Pattern using positive tone resist
1. Spin coat
For >3um mesa = SPR 220: 4000 rpm, 60”, at 500 rpm/sec.
2. Bake at 115 C for 2’
3. Expose for MJB-3 for 40” or ALN02 for 16’’
4. Develop in MF-319 for 2’
5. Inspect under microscope

STEP.3. Etch pattern using ICP
6. Use DC_GAASP Recipe to etch sequentially based on the total thickness, note down the etch rate:
a. Total # of etch steps= (required time for the specific etch*2+1) #30’’ etch, 15’’off
b. This recipe is to avoid the micro-masking
7. Inspect the etch depth using the profilometer,
8. Remove the PR after getting the desired etch with Acteon, Methanol, IPA 1 min each
*The same goes for both the deep etch and shallow etch
</td>
<td> 
</td>
</tr>
</table>

PASSIVATION	STEP.1. Cleaning the sample 1. Remove any PR residues with O2 Ashing for 5' 2. Dip the sample in HCl:H2O (1:10) for 30" STEP.2. Coat with encapsulation method of choice (Si3N4, SiO2, Al2O3) 3. Proceed with the photolithography as stated in previous steps to define the via, STEP.3. Etch the passivation accordingly: 4. If Si3N4 or SiO2 is used, etch with ETC04 using the SiO2 etch recipe; the deposition rate is approximately 200A per minute	
METALIZATION	STEP.1. Pattern using appropriate resist as stated before, STEP.2. Perform HCl dip to prep sample surface STEP.3. Deposit contact metal 1. 500/500/2000 Ti/Pt/Au 2. perform lift-off Alternative Approaches for Photolithography: 1. LOR5A – 4000RPM, 10,000RPM/Sec, 60sec 2. Let the sample sit for 1' before the bake 3. Bake it -180C for 5min 4. Let the sample to cool down for 2' 5. SPR 955 – 4000RPM, 10,000RPM/Sec, 60sec (Thickness was around 0.8um) 6. Bake it – 105C for 1min 7. Let the sample dry for 2' 8. Use the Acetone and MF-319 to clean the backside of the sample (to remove any spill over) 9. Expose 4.5" sec with MJB-3 10. Develop with MFCD-26 for 1min	

Remarks / Notes	
1	Always clean the mask with the solvents before use
2	Let the sample dry for 2' before soft bake, and before development

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