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Superlattice Thin-Film Thermoelectric Material and Device Technologies

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Summary

Superlattice thermoelectric technologies in the Bi_2Te_3 material system can potentially enable efficient thermoelectric refrigeration and air conditioning using high cooling power density superlattice devices as well as lead to compact power conversion devices. We discuss the state of the art in these materials and highlight the state of transition of these materials into device prototypes for both cooling and power conversion. We have determined a $ZT \sim 1.4$ in fully fabricated p–n couples, using p-type Bi_2Te_3/Sb_2Te_3 and n-type $Bi_2Te_3/Bi_2Te_xSe_{3-x}$ superlattices, from heat-to-electrical power conversion efficiency measurements. A concept denoted as High Active-Flux, Low Input/Output Flux (HAF-LIOF) has been developed and validated for the use of the high active heat-flux (200 to 2500 W/cm^2) superlattice devices, with relatively simple heat-exchanger systems, and is applicable for both cooling and power conversion. Superlattice cooling modules with cooling power densities in excess of 150 W/cm^2 at the module level have been demonstrated. The transitioning of high ZT of thin-film materials to improvements in cooling performance has involved solving a series of issues related to the intrinsic superlattice thermoelectric couple as well as optimizing several electrical and thermal interfaces within the p–n couple and between the couple and external interfaces.

49.1 Introduction

The U.S. Department of Defense (DoD) has been supporting the resurgence of the once sleepy field of thermoelectrics during the past decade, since the first set of ideas using nanoscale materials[1–3] were

proposed at the National Thermogenic Workshop in 1992. In particular, the Office of Naval Research (ONR) and the Defense Advanced Research Projects Agency (DARPA) have helped make impressive strides in the materials figure-of-merit, denoted as *ZT*, using nanoscale material concepts. Higher *ZT* of the thermoelectric materials can directly lead to improved efficiencies in both solid-state refrigeration and thermal-to-electric power conversion devices. There have been several reports[4–6] of enhanced *ZT* at various temperature regimes using superlattices, quantum dots, and nanocrystalline inclusions, respectively. In combination with semiconductor technology tools for device fabrication, these materials offer unprecedented advantages such as high cooling power density and high speed cooling/heating in thermal management and high specific power in direct thermal-to-electric power conversion systems. The improvements achieved with these nanoscale thermoelectric materials and their devices are timely for meeting many emerging needs in DoD systems as well as in commercial electronic and optoelectronic systems. As an example, there is an urgent need for compact, high specific power (>1000 W/Kg) portable power sources based on hydrocarbon fuel sources. Similarly, high power density (>5 W/cm^2) and efficient (~20%) direct thermal to electric (DTEC) power conversion sources are required for future Navy vessels. There are hosts of heat sources that could be harnessed in aerospace systems, for propulsion and other needs, where highly efficient and lightweight thermoelectric technologies using advanced nanoscale materials offer new capabilities. Following the lead of DoD, the U.S. Department of Energy[7] is also beginning to explore the advantages of nanoscale thermoelectric technologies for improving the fuel efficiency in automobiles and other ground vehicles.

The superlattice thermoelectric technology developed from its infancy, with U.S. DoD support, is also now being actively considered for the thermal management of advanced microprocessors. As the chip feature sizes shrink from 130 to 90 nm and several circuit innovations are being implemented at the same time, the chips are facing issues of one or more hot spots. These have to be managed just when conventional thermal management components based on state-of-the-art heatsinks are reaching their limits of heat dissipation and the problems are expected to get more severe when there is a move to the 65 nm node in Si-based microelectronics. We have successfully applied[8] the superlattice thermoelectric technology to show a pathway for solving such thermal problems. In the long run, we anticipate similar cooling solutions being able to manage transistor offstate leakage currents for ameliorating power management concerns in advanced computational devices. We have begun to show early success with the superlattice thermoelectric technology for potential applications in cooling IR sensors as well. In an interesting proposal, the lightweight superlattice thermoelectric heat pump is also being considered for futuristic vertical take-off aeronautical concepts.[9] In short, there is a plethora of opportunities for what is appearing to be a fast maturing, nanoscale thermoelectric superlattice technology. The state of the art in materials and device technologies, the possible future directions for the advancement of nano concepts, and the development of unique applications are discussed.

49.2 Superlattice Approach to *ZT* Enhancement

Nanoscale thermoelectric materials, using phonon-blocking/electron-transmitting superlattices in thin-film form,[4] using quantum-dot superlattices in thick-film form,[5] and using nanoscale inclusions in bulk material form,[6] increasingly appear to be the route to achieving enhanced ZT in thermoelectric materials. The first of these developments represented a materials development for the 200 to 400 K range, the second for the 400 to 600 K range, and the third for the 600 to 900 K range.

Certainly, superlattices in other material systems, using the concept of phonon-blocking/electron transmission[10] are less developed for other temperature regimes. We have reported on Si/Ge superlattices that show reduced thermal conductivity both in the cross-plane direction[11] and in the in-plane direction.[12] We have also reported[13] on our preliminary results of thermal conductivity reduction in short period, layered, nonquantum-dot-type PbTe/PbTeSe superlattices. It is reasonable to expect that the PbTe/PbTeSe superlattices, along with Si/Ge superlattices, would offer enhanced *ZT* at mid and high temperatures. The thermal stability of these short period structures, especially in FCC-type

lattice systems, as opposed to that in layered superlattices with periodic Van Der Waals bonds, as in a Bi_2Te_3-material system, have to be examined. Phonon-blocking/electron-transmitting superlattices based on ultra-small-bandgap material combinations in the HgCdTe system, could also be considered for the 80 to 200 K temperature regime.

The thermal conductivity reduction with superlattices, whose lattice thermal conductivity values are well below that of comparable solid solution alloys,[11,14,15] has become well established. However, the physics behind the thermal conductivity reduction mechanism is not yet clear. The thermal conductivity reduction was originally conceived[16] by treating phonon scattering at superlattice interfaces similar to phonon scattering at grain boundary interfaces. Since then, more detailed modeling studies[17–19] of phonon thermal conductivity reduction have been considered. We have observed that the lattice thermal conductivity reduction originates from potential reflection-induced localization of phonon waves[14] in an ever so slightly disordered, from period to period, superlattice similar to localization of light in a disordered medium.[20] This was proposed based on an observed minimum in the lattice thermal conductivity and that highly reflecting superlattice interfaces are likely in the Bi_2Te_3-based material system.[21] Thus, the phenomenon of localization-like behavior of phonons in superlattices has been proposed. We do note that observed theoretical minima, based on wave-particle model for phonons, although occurring at much smaller periods than observed experimentally, have been discussed.[19] We have seen such minima in thermal conductivity in the Bi_2Te_3-based superlattice system,[14] in the Si/Ge-based superlattice system for both cross-plane[10] and in-plane[12] directions, and more recently in the PbTe/PbTeSe-based system[13] as well.

The engineering of thin-film thermoelectric superlattices and quantum-dot superlattices into useful devices can be implemented easily if the electric transport occurs across the superlattice interfaces. This way, planar semiconductor device technology using standard microelectronic tools can be used.[22] However, for efficient cross-plane carrier transport across superlattice interfaces, we need to consider the conduction band offsets in the case of n-type and valence band offsets in the case of p-type materials, respectively,[16] as well as minimization of carrier scattering at interfaces.[21] Thus the combination of (a) lattice thermal conductivity reduction, (b) efficient carrier transport across superlattice interfaces, and (c) reduction or elimination of alloy scattering, has led to the enhanced ZT[4] in the cross-plane direction.

We do anticipate that, in many situations, as with certain sensors or cryo-cooling of electronics using MEMS-like devices,[23] high ZT is required in the in-plane direction as well. Further, if such nanoscale superlattice materials are engineered to produce "bulk-like nano" materials,[24] it is important that higher ZT values be obtained in the in-plane direction as well. So, alternate approaches such as quantum-confinement[25] and/or multivalley effects[26] are required to enhance the Seebeck coefficients. ZT enhancement in Si/Ge superlattices in the in-plane direction[12] has been reported; these superlattices consisted of pure Ge and pure Si, as opposed to Si/Si_xGe_{1-x}, where multivalley degeneracy can be easily achieved using a small amount of lattice-mismatch-induced strain due to the inherent band structure of Ge.[27]

Thus, there is considerable promise for superlattice based phonon-blocking, electron-transmitting structures for ZT enhancement, from cryogenic temperatures to high temperatures such as 600 K. In the following sections, we specifically discuss the superlattice thermoelectric technologies in the Bi_2Te_3-material system. We discuss the state of the art in these materials and highlight the state of transition of these materials into device prototypes for both cooling and power conversion. We have determined a $ZT > 1.4$ in fully fabricated p–n couples, using p-type Bi_2Te_3/Sb_2Te_3 and n-type $Bi_2Te_3/Bi_2Te_xSe_{3-x}$ superlattices, from heat-to-electrical power conversion efficiency measurements. A concept denoted as High Active-Flux, Low Input/Output Flux (HAF-LIOF) has been developed and validated for the use of the high active heat-flux (200 to 2500 W/cm^2) superlattice devices, with relatively simple heat-exchanger systems, and is applicable for both cooling and power conversion. Superlattice cooling modules with cooling power densities in excess of 150 W/cm^2 at the module level have also been demonstrated. Next, we highlight some of our next-generation superlattice materials for medium- and high-temperature applications. In addition, we present our approach to applying the Bi_2Te_3-based superlattice technology with other high-temperature thermoelectric device components for efficient

waste-heat recovery or power conversion. Bi_2Te_3-based superlattice devices can be integrated with n-PbTe/p-TAGS mid temperature bulk devices and n-SiGe/p-SiGe high-temperature bulk devices for obtaining efficiencies approaching 20% using 800 K heat sources.

49.3 Bi_2Te_3-Based Superlattice Materials and Device Technology

The superlattices in the Bi_2Te_3-material system have demonstrated high intrinsic figure-of-merit ($ZT \sim 2.4$ for p-type and almost as high as 1.7 for n-type at 300 K) at the individual thermoelement level. Other advantages include high cooling power density, extremely rapid cooling or heating, and that fully functional devices can be built with 1/40000th of the active-material usage compared to state-of-the-art bulk thermoelectric technology. This has directed us, for the past two years, to develop a viable device module fabrication technology. Not surprisingly, the device and module engineering issues are quite challenging in their own way. The basic p–n couple device development has progressed rather remarkably, as evidenced by a measured ZT of ~2 in the inverted couple mode.[28] The data are shown in Figure 49.1.

The nanoscale superlattices are grown by metallorganic chemical vapor deposition (MOCVD). *In situ* ellipsometry has been used to gain further control over nanometer-scale control of deposition.[29]

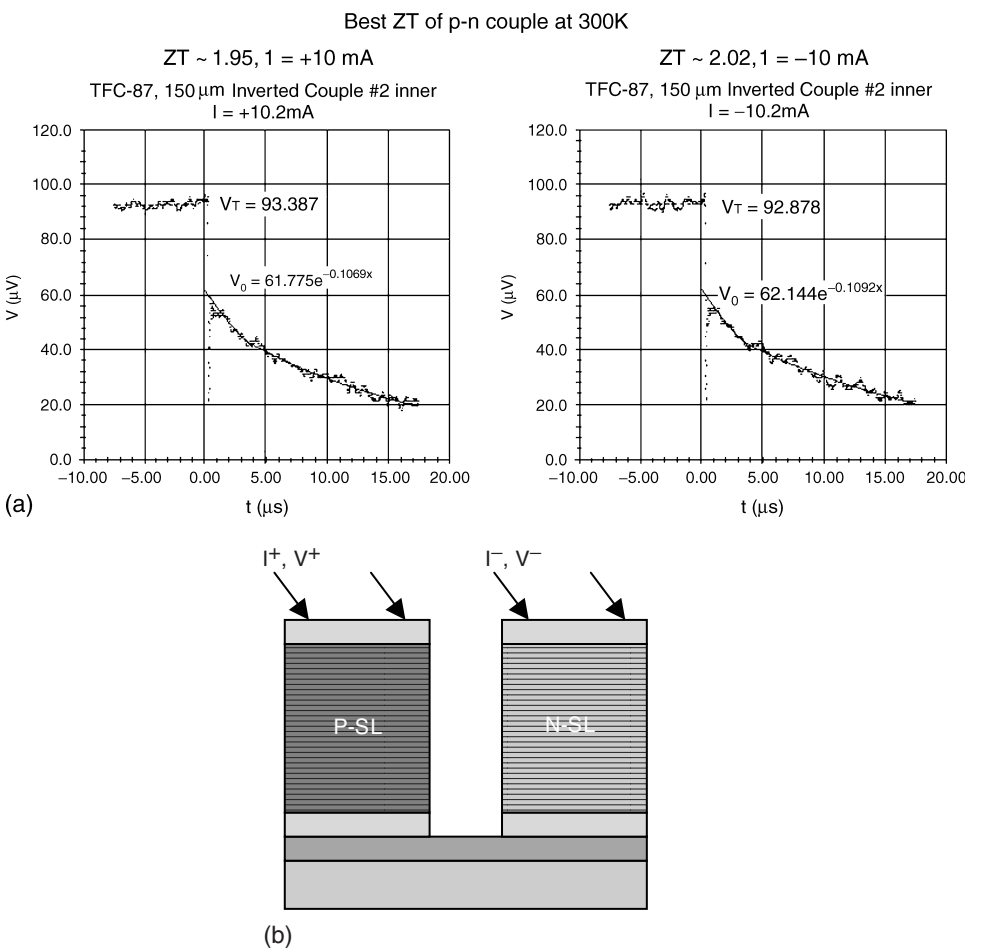

FIGURE 49.1 (a) Best ZT of ~2 in an *inverted* superlattice p–n couple at 300 K, verified with current flow in either direction.[4] (b) The schematic of the inverted couple under test is shown.

The MOCVD process can be scaled to multiwafer growth and for large area growth, similar to that of compound semiconductor space photovoltaic, for enabling low-cost volume production of modules. The fabrication of thin-film modules employs standard semiconductor device manufacturing tools such as photolithography, electroplating, wafer dicing and pick-and-place tools. This allows scalability of the module fabrication from simple modules that can pump a few Watts of heat as shown in Figure 49.2a to multiconnected module arrays as shown in Figure 49.2b.

The module development has faced several challenges. Some of the issues are related to the significant electrical and thermal parsitics in a modular assembly. Some of these are discussed in the following section. Even so, as the technology stands, several applications such as laser thermal management,[30] low profile cryogenic cooling,[31] microprocessor hot spot[32] thermal management, as well as high power density, compact power sources[33] are emerging as attractive in the near term. The relatively inexpensive but microelectronics-type technologies used for the superlattice thin-film device fabrication also lend themselves as suitable for flexible module design as well as for reductions in design cycle time and cost.

The module shown in Figure 49.2a, consisting of an array of four by four p–n couples, has shown a Q_{max} of ~10 Watts. The cooling header area is 0.063 cm^2, thus offering a module cooling power density of over 150 W/cm^2. This is lower than the single p-element heat pumping capability of ~700 W/cm^2[24] due to the packing density associated with the 16 active couples under the common cooling header. The low profile of the module, only about 1 mm and can be as low as 0.1 mm for the entire device, is very attractive for a wide variety of applications including in some complex electronic packages.

Realizing the true intrinsic performance of the p-superlattice and n-superlattice materials, on an average of ~1.8 at 300 K, is a major device optimization problem. In particular, the exact thermal/electrical matching of the p-legs and n-legs, as described in Ref. [34] for maximizing ZT of the couple and hence the COP, as well as minimizing thermal drops across the various device interfaces are significant challenges. Figure 49.3 gives the schematic of the various electrical resistances associated with flip-chip bonded p–n couple.[35] Here, ρ_p and ρ_n are the p and n element Ohmic resistances, respectively, ρ_{cp} and ρ_{cn} are the Ohmic contact resistances at either ends of the p- and n-thermoelements, respectively, ΔR_m is the resistance associated with the metal-interconnecting bar. These resistances have been minimized, effectively, to demonstrate an inverted couple ZT of as much as two at 300 K[28] in Figure 49.1. However, the flip-chip attachment resistance, R_{attach}, has been a significant issue in obtaining large ZT in the fully fabricated couple depicted in Figure 49.3. Note that this fully fabricated couple, as attached to the header and shown in Figure 49.2, has almost all the parasitics associated with a typical module. The impact of the R_{attach} while significant on ZT, has more deleterious effect on the thermal drop, associated with this resistance, during the pumping of the total heat through this interface into the heatsink.

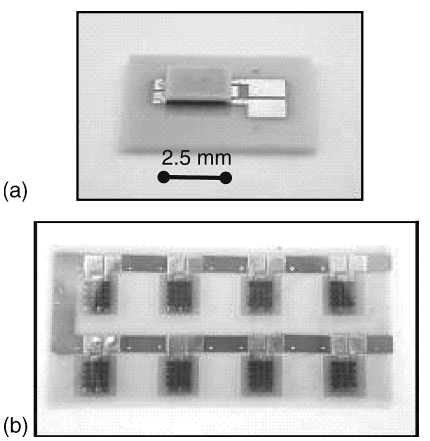

FIGURE 49.2 (a) A 2.5 mm × 2.5 mm cooling module with a measured Q_{max} ~ 10 W and (b) an example of an integrated-array module enabled by semiconductor technology.

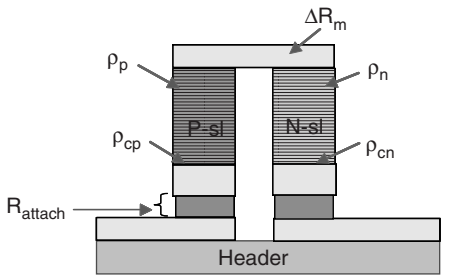

FIGURE 49.3 Schematic of a flip-chip bonded p–n superlattice thin-film couple showing the various electrical device parasitics. (*Source*: Goldsmid, J. 1983. *Electronic Refrigeration*, Pion Publications, New York. With permission.)

The effective ZT of the flip-chip bonded p–n couple shown in Figure 49.3, when the n- and p-legs are thermally/electrically matched, is given by Equation 49.1:

$$ZT \sim \frac{0.5(ZT_p + ZT_n)[\rho_p \cdot lp/a_p + \rho_n \cdot ln/a_n]}{[\rho_p \cdot lp/a_p + \rho_n \cdot ln/a_n + \Delta R_m + 2\rho_{cp}/a_p \cdot + 2\rho_{cn}/a_n + 2R_{attach}]} \tag{49.1}$$

Note that the ZT obtained by Equation 49.1 is under the best of circumstances, when there is good matching between p-legs and n-legs. ZT is generally less, and can be further complicated by the role of various heating associated with the Ohmic parasitics, that are not exactly like standard Joule heating. This has limited our best observed external module-level ZT, as measured by the Harman method, to about 0.65 at 300 K. The cooling ΔT_{max}, which is more dependent on exact thermal/electrical mismatch at no heat load, reflects this ZT at the module level. However, the Q_{max} pumped with the modules, are more easily optimized; this is given by $(\sim 0.5\Pi^2/R_p + 0.5\Pi^2/R_n)$, for a fixed ΔT, by solving for the current that gives maximum heat pumping. This is obtained from the standard energy balance Equation 49.2 shown below.

$$Q = \Pi I - 0.5I^2R - K\Delta T \tag{49.2}$$

Here, Q is heat pumped, Π is Peltier coefficient, I is the current, R is the Ohmic resistance, K is the thermal conductance, and ΔT is the temperature differential under which heat Q is pumped. Work is underway to improve the module level ZT, with careful attention to the various device parasitics as well as appropriate matching of the p-legs and n-legs for both ΔT_{max} as well as for Q_{max} conditions. In addition, a significant attention is being expended on the thermal drop associated with the R_{attach}. Note that the thermal conductance associated with this attachment electrical resistance can be modeled based on standard Weidemann–Franz law, that connects bulk electrical conductivity to thermal conductivity, as applied to electrical interfaces and described by Equation 49.3:

$$K \sim k(a/l) = L_o T \sigma_{attach}(a/l) \sim L_o T(1/R_{attach}) \tag{49.3}$$

Here, L_o is the Lorentz constant, T is the absolute temperature, (a/l) is an *equivalent* aspect ratio of the interface, and σ_{attach} is the electrical conductance of the interface. Such a model has been developed over the past year to explain the cooling performance of the superlattice devices near 300 K, especially at higher operating currents, when both ΠI and I^2R, in Equation 49.2 above, add up to a considerable thermal drop across the interfaces. We obtain this thermal drop, defined as ΔT_{loss}, representing the reduction from intrinsic ΔT, in Equation 49.4:

$$\Delta T_{loss} \sim [L_o T(1/R_{attach})]^{-1}(\Pi I + 0.5I^2R + Q_{pumped}) \tag{49.4}$$

Thus, the ΔT_{loss} is directly proportional to R_{attach} and the problem gets worse as I increases. This relationship has been validated by the good match between the modeled ΔT vs. I, using the intrinsic

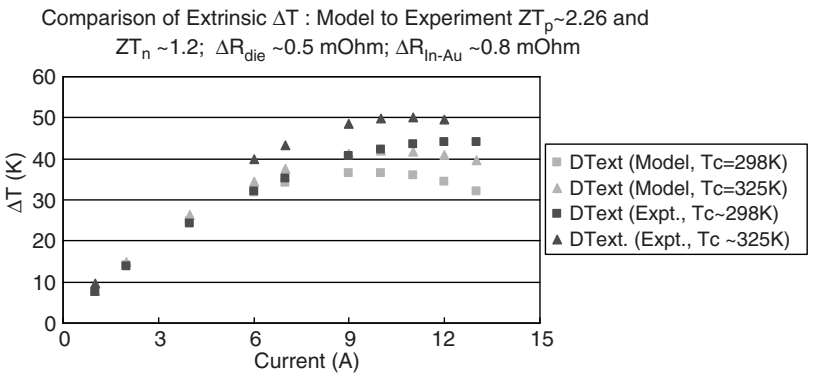

FIGURE 49.4 Comparison of model vs. experimentally measured ΔT vs. I, using a high-performance p-SL inirinsic device with two contacts ($ZT \sim 2.2$), and n-SL device with two contacts ($ZT \sim 1.2$), $\Delta R_m \sim 0.5$ mOhm, and $R_{attach} \sim 0.8$ mOhm. The actual ΔR_m and R_{attach} may be slightly lower than used in the model, as evidenced by the experimental data being higher than the modeled data. Nevertheless, the impact of these parasitic resistances is clear.

p- and n-SL material parameters, their expected thermal mismatch, as well as accounting for the R_{attach}, to the externally observed ΔT. This comparison is shown in Figure 49.4. Note the relatively good agreement at lower currents between modeled and experimental data. We observe that the parameters used for modeling the various parasitics, $\Delta R_m \sim 0.5$ mOhm and $R_{attach} \sim 0.8$ mOhm, are chosen based on the measured sheet resistance of the metal interconnect and the measured attachment resistance (see Figure 49.3). Thus, no aggressive modeling of parasitics was needed to explain the observed external cooling ΔT for the higher ZT materials. Next, we need to bring down the ΔR_m and R_{attach} to levels of $\sim$0.2 mOhm each, to get ΔT_{max} of $\sim$100 K near 300 K operation. These are significant challenges even by advanced semiconductor technology standards.

This device model described above has been increasingly found to be valid from our study of over 300 p–n couples in the last year and has also been successfully applied to explain also some of the low-temperature cooling data[31] seen in p–n couples (described later).

In addition to the various electrical parasitics in a p–n couple module and the thermal drops associated with them, we need to consider heat rejection at the heatsink. This is especially important for high-packing-density cooling device modules, where there is no room for sufficient heat spreading. However, in low-heat flux situations, as often seen in many low-noise electronics or distributed power electronics, we can employ the HAF-LIOF concept.[36] Here, the high cooling power density (~1000 W/cm^2) thin-film thermoelectric devices are integrated in a low packing fraction, such as 0.1 to 10%, to achieve a net outside flux of 1 to 100 W/cm^2, respectively, depending on the thermal management available. This concept is shown schematically in Figure 49.5. Such a concept is also suitable for refrigeration, where heat fluxes are not as high as in chip cooling or as in laser thermal management, as well as in power conversion applications.

49.4 Advanced Cooling Modules for Laser Thermal Management

Thermal management of optoelectronic packages for both long-haul and short-haul fiber-optic communication lasers in the near term as well as for integrating lasers within high density electronic systems requires extremely small-footprint thermoelectric coolers. In addition to a high coefficient of performance (COP) at fairly large temperature differentials, these coolers need to pump large heat-flux levels in excess of 100 W/cm^2 at the module level. The initial modules operated at currents of 10 to 12 A but further device optimization led to lower operating currents. In addition to improving the COP and

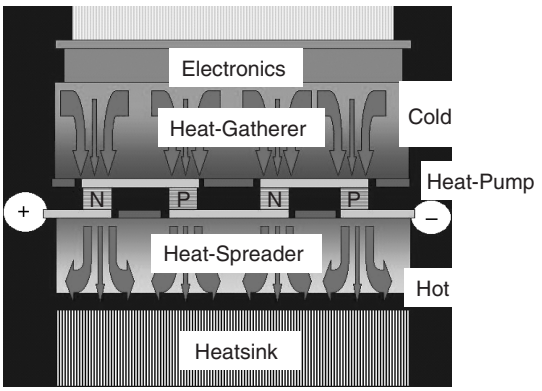

FIGURE 49.5 Schematic of the HAF-LIOF concept to enable the use of high cooling power density thin-film superlattice device elements into low external flux device modules.

power densities, we have been developing high-aspect ratio devices to lower the operating currents significantly. To date, we have p–n couples and modules with I_{max} in the range of 1.5 A with cooling temperature differentials in excess of 35°C and ΔT in excess of 55°C at $T_{hot} \sim 75$°C. The thermoelectric elements employed in these devices are based on p-type Bi_2Te_3/Sb_2Te_3 superlattices and n-type $Bi_2Te_3/Bi_2Te_{2.85}Se_{0.15}$ superlattices.

The smallest module physical dimensions were 1 mm (L) × 2 mm (W) × 1 mm (H). In slightly larger 2 mm × 2 mm × 1 mm size modules, heat pumping capacities of up to 1.8 Watts (Q_{max}) were measured, translating to a cooling power density of 45 W/cm^2 at the module level (Figure 49.6 and Figure 49.7) and 125 W/cm^2 at the couple level. The potential applications for such modules are in laser diode cooling in various small packages such as metal TO cans and some highly integrated optoelectronic packages. A four-die module, capable of providing $Q_{max} > 1$ Watt, will fit quite easily into a TO-46 package and a sixteen-die module capable of over 10 Watt cooling can be accommodated into a TO-5 package. Figure 49.8 displays the aggressive four-die module with a total module area of 1 mm^2 in a TO-46 package.

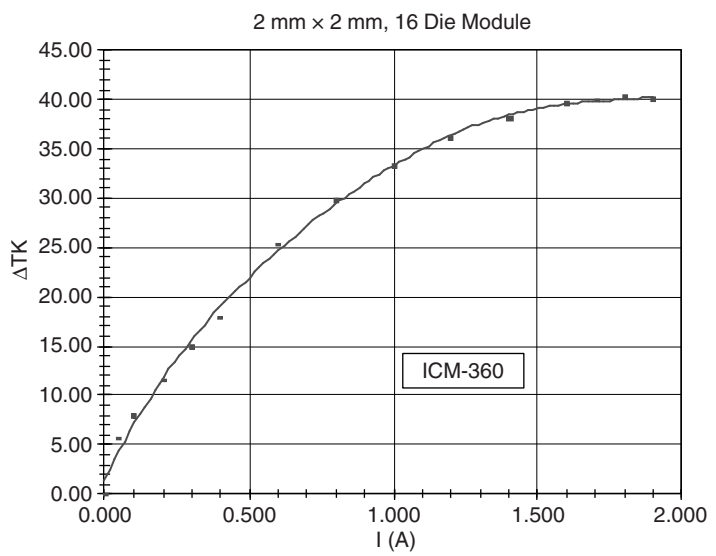

FIGURE 49.6 2 mm × 2 mm module suitable for laser thermal management with a ΔT_{max} of ~40 K.

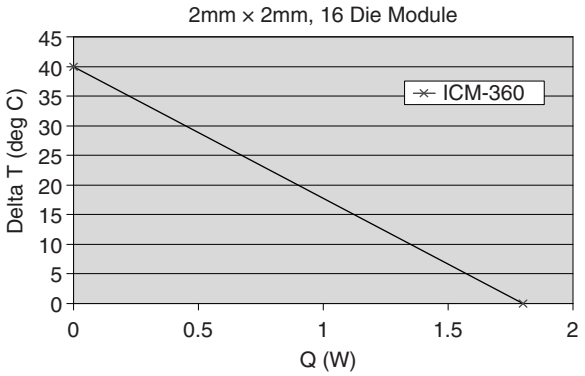

FIGURE 49.7 Load line of a high cooling power, small footprint, 2 mm × 2 mm × 1 mm module with a ΔT_{max} of 40 K and Q_{max} approaching 1.75 Watts.

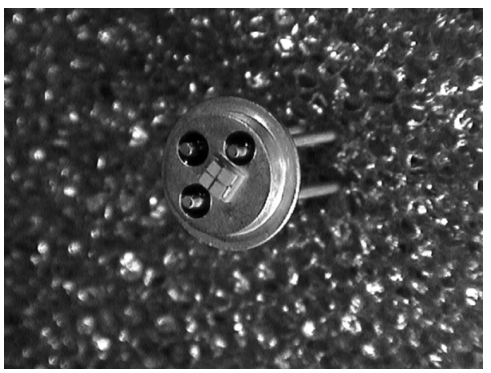

FIGURE 49.8 A high cooling power, small footprint, 1 mm × 1 mm × 1 mm module capable of pumping >1 Watt from laser devices at operating currents of 1 A, as shown above, will allow insertion of lasers into packages being developed for electronics. Thus, it would lead to convergence of packaging between electronics and optoelectronics in some applications.

We believe this work lays the groundwork for further optimization of more efficient and high performance modules for the thermal management of optoelectronic packages for both long-haul and short-haul fiber-optic communication lasers in the near term and for integrating lasers within high density electronic systems.[30]

49.5 Early Reliability Studies with Cooling Modules

In order to exploit the advantages of superlattice technology for optoelectronic applications, device reliability must be established. Of particular interest is the stability and reliability of the superlattice material itself. We are also beginning to characterize the reliability of the superlattice thermoelectric cooling technology, using the toughest power cycling procedures, described elsewhere.[37] We have demonstrated reliability at the material level, evidence of reliability at the individual couple level, and attachment-resistance-dependent reliability in minimodules. We believe as the R_{attach} improves, with proper selection of bonding materials, the module ZT, the ΔT_{max}, and the reliability are all expected to improve hand-in-hand. Standards for such devices are defined in telecommunication industry reliability documents such as GR-468-CORE.[37]

Any study of the material stability of superlattice devices subjected to power cycling should take into account that operating conditions are more severe than those experienced by comparable bulk devices. For example, temperature gradients across thin films in the range of 4 to 8 μm films can exceed 1.0E5 K/cm, two orders of magnitude larger than those found in typical bulk thermoelectric devices. Considering that the superlattice elements also respond thermoelectrically to fast current transients,[4] inevitable in any power-switching test to meet the GR-468-CORE standards, they will experience dramatically larger swings in temperature gradients. In addition, high current superlattice devices with small area contacts can be subjected to high current densities. Superlattice devices can operate at current densities in the range of 1E4 A/cm, at least an order of magnitude larger than similar bulk devices.

With these issues in mind, initial power cycle testing has been performed on relatively simple superlattice couples using $Pb_{37}Sn_{63}$ bonding for flip-chip attachment. No degradation in ΔT was observed after more than 100,000 power cycles, suggesting the intrinsic reliability of the superlattice material. It is an exciting result that such superlattice modules, under optimum attachments even such as developed so far, can withstand temperature switching transients of 100,000 K/cm and there are no fundamental material property changes. It is even more remarkable that we are employing materials with nanoscale structures, of the order of 1 nm, and they show no apparent structural changes. Any structural change would have been identified by lower Peltier voltage (V_o) in ZT measurement[4] from a higher thermal conductivity; no such effects were observed. Any 5% to 10% change in superlattice device stability was in part attributable to the particular attachment metal in the flip-chip attachment process, and seems to be improved with higher temperature attachment metals such as Sn. These studies have indicated the convergence of requirements for both performance and reliability, and relatively low current operation.

49.6 Progress in Cooling Modules at Cryogenic Temperatures

The electronics industry has a need for solid-state cryogenic cooling techniques that can cool targets down to the range of 100 K. Such applications include low noise amplifiers, infrared focal-plane arrays, and high-temperature superconducting electronics. In addition to sustaining a large temperature gradient, these solid-state devices need to be capable of handling large heat fluxes and, in some cases, have a very small height requirement as well. Current bulk thermoelectric devices are limited to a cold-side temperature of about 170 K, are capable of only small heat fluxes, and can have heights in the range of several centimeters. Thin-film nanostructured materials offer the potential to dramatically enhance the cryogenic performance of thermoelectric devices over that of state-of-the-art bulk alloyed materials, especially in combination with microcryogenic cooler concepts.[23] Results are presented on cryo-temperature ΔT measurements performed with superlattice and state-of-the-art bulk devices where, in spite of many device parasitics unique to thin-film devices, the superlattice devices are approaching bulk performance at 125 K. A study of the parasitics involved and their interactions are discussed.

Of particular interest is the effect of the superlattice structure on low-temperature performance. The relative amounts of Bi_2Te_3 to Sb_2Te_3 can be adjusted from ratios of 10 Å/30 Å to 10 Å/60 Å in increments of 10 Å. Since Bi_2Te_3 has a lower bandgap of ~0.15 eV compared to ~0.19 eV for Sb_2Te_3, it is expected that the Bi_2Te_3-rich devices would exhibit better performance at lower temperatures. Sixteen samples of the four superlattice structures were tested for ΔT_{max}. The ΔT was recorded as a function of current and the maximum differential was noted at a specific hot-side temperature, T_H, and then repeated at various T_H down to ~100 K. This maximum, ΔT_{max}, was then plotted as a function of the superlattice structure for three representative hot-side temperatures (Figure 49.9). Although the data suggest that the 10 Å/40 Å structure yields the best performance at all of the temperatures, the error bars belie drawing any definite conclusion.

In spite of the parasitics present in the superlattice mini-modules, as shown by the comparatively large attachment resistance, these devices currently exhibit cooling performance on a par with state-of-the-art bulk materials at 125 K. Figure 49.10 shows a plot of cryogenic cooling for the best superlattice mini-module as compared with state-of-the-art bulk Bi_2Te_3 device. At this stage of development, extrinsic

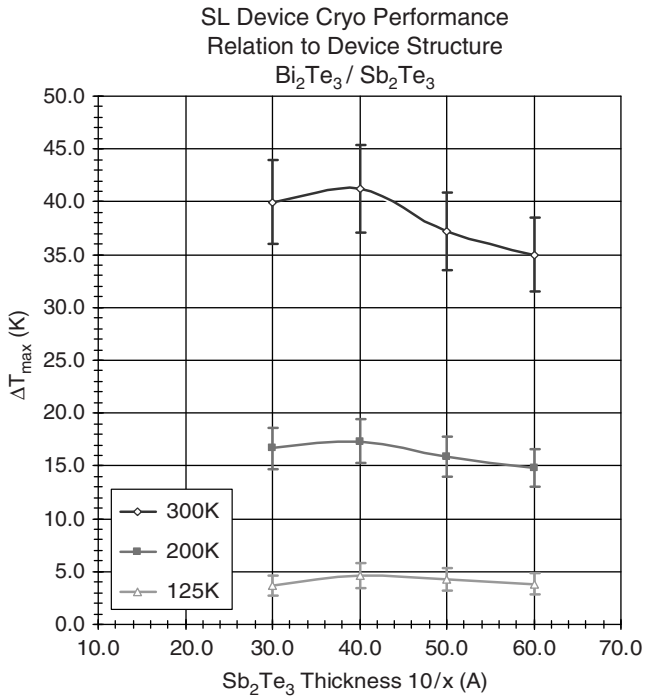

FIGURE 49.9 Graph of ΔT_{max} for various superlattice structures for different hot-side temperatures.[31]

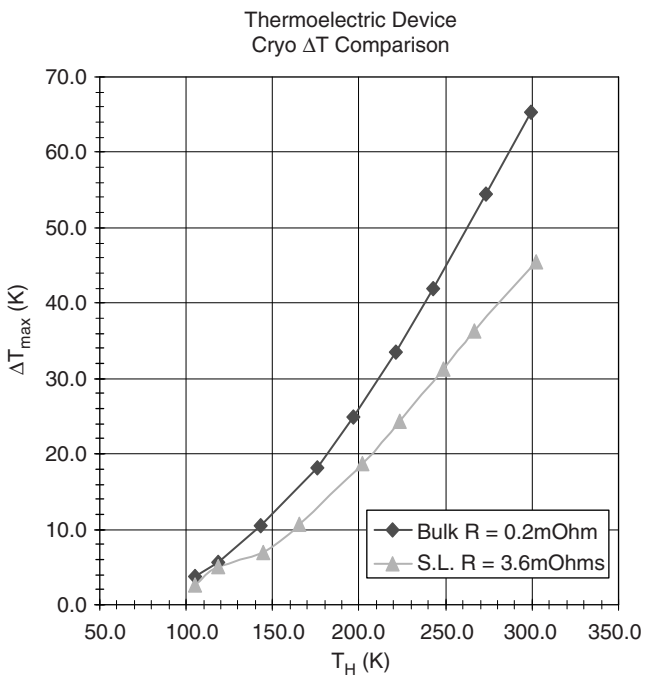

FIGURE 49.10 Superlattice modules, in spite of significant parasitics that are unique to thin-film devices, can offer high cooling power density with similar COP at cryogenic temperatures.

device parasitics dominate intrinsic material properties in practical devices. In order to exploit the potential benefits of bandgap optimization through the use of customized superlattice structures, parasitic attachment resistances must be reduced as much as is practicable. Future work will focus on reducing attachment resistance to the extent possible and then finding the optimal superlattice structure for cryogenic applications.[31]

49.7 Power Conversion Applications

We have also begun to explore the use of the Bi_2Te_3-based superlattice materials for power conversion applications. The full details of the power conversion efficiency attainable with single-stage superlattice devices will be presented elsewhere.[38] However, we do note that early studies of power conversion efficiency with single p–n couples have given a significant correlation with the measured *ZT* in the "inverted" p–n couples[28] by the Harman method. This is shown in Table 49.1 below.

Note that, in power conversion mode, the ΔT across the devices are decided by the external heat-source and heatsink temperatures. Thus, in a series connection of the p- and n-legs, the Seebeck voltages add and, as long as the electrical resistances are such that we can ensure comparable current flow, we can optimize the power device design relatively easily. Thus, unlike in a cooling device, near ΔT_{max}, where the more efficient p-leg can pump on the n-leg when not matched correctly, the power device design is more forgiving. Further, we believe the application of compressive pressure during power testing may also enable the flip-chip resistance, R_{attach}, to come down and thus help achieve an improved *ZT*. In contrast, no such compressive pressures are possible during the "adiabatic" Harman method measurements or under no-load ΔT_{max} measurements. This is expected to lower the R_{attach} and enable a better thermal interface to the eventual heatsink. The application of compressive pressure across the module, between the heat source and the heatsink, is a requirement in power devices for both measurements and during operation.[39]

In addition to improving the efficiency of single-stage superlattice power conversion devices, operating between 300 and 450 K, and thereby offering potential efficiencies in the range of 8 to 10%, multistage power conversion devices[38] can take advantage of larger starting Carnot efficiencies. A schematic of a three-stage, two-wire, segmented device is shown in Figure 49.11. Here, we anticipate a 12 to 16% efficiency using a combination of n-SiGe and p-SiGe alloys, operating as the hot-stage between 600 to 650°C and 400 to 450°C, and n-PbTe and p-TAGS, operating as the mid-stage between 400 to 450°C and 200 to 150°C. The efficiencies depend on material parameters of available bulk materials and the temperature differentials applied across the respective stages. We believe, with the introduction of more recently discovered bulk materials such as filled skutterudites,[40] nanobulk materials,[6,24] and new innovations to SiGe materials,[41] a 20% device conversion efficiency is achievable in the next three years. In addition, advances in superlattices and other nanomaterials for various temperature regimes[4,5,24] could lead to even higher efficiencies in the long term for direct thermal energy conversion.

TABLE 49.1 *ZT* from Power Conversion Efficiency, Measured with Small Temperature Differentials, in p–n Couples

ΔT_{int} (K)	Voc (mV)	Isc (mA)	P_{max} (mW)	Efficiency (%)	ZT at 300 K
8.4	4.59	829	0.95	0.6	1.44
12.5	6.88	1301	2.24	0.9	1.6
17.5	9.63	1670	4.02	1.2	1.41

The Harman Method *ZT* on the same p–n couple, in the inverted mode without thermal matching requirements and the R_{attach}, was about 1.3 at 300 K. Here, the power device was also mounted on a very thick (several mm) split-copper blocks, in contrast to thinner metallization (~30 μm) headers, typically used in modules as shown in Figure 49.3.

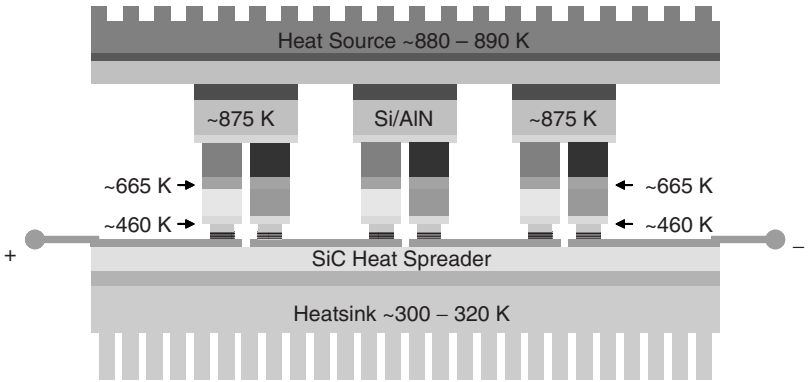

FIGURE 49.11 Schematic of a potentially 20% efficient segmented device operating between 25 and 600°C, the bottom stage can utilize superlattice components described in this review.

49.8 Technology Pull for Near-Term Applications and Future Directions

The transition from the high "intrinsic" *ZT* attainable in thin-film p-type Bi_2Te_3/Sb_2Te_3 and n-type $Bi_2Te_3/Bi_2Te_{3-x}Se_x$ superlattice materials, and the high "extrinsic" *ZT* attainable in their respective thermoelements[4] to module-level performance represents a huge engineering challenge. However, such a transition would enable a plethora of possibilities beyond electronics thermal management to efficient thermal-to-electric power conversion and solid-state refrigeration. Clearly, we believe, there are several emerging applications for the thin-film superlattice thermoelectric technology, in spite of the significant difficulties in realizing the full intrinsic performance of the advanced p-type and n-type superlattices at the module level. Two such applications are in small-footprint optoelectronics cooling[30] and the thermal management of hot spots[8,32] in advanced microprocessors. In addition, highly compact power sources also demand some of the features offered by the thin-film thermoelectric technology. With the progress described here, both power and cooling thermoelectric devices with

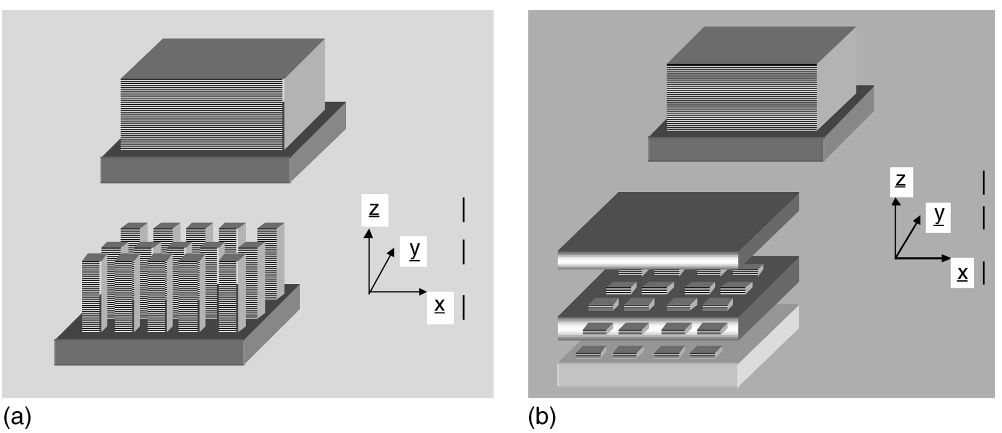

FIGURE 49.12 (a) Transitioning the 2-di superlattice to 1-di quantum-wires using advanced lithography and (b) direct deposition of 2-di superlattices into quantum boxes using self-assembly or other processes, with suitable periodic encapsulation layers for orthogonal quantum confinement. (*Source*: Venkatasubramanian, R., Siivola, E., Colpitts, T., and O'Quinn, B. 2001. U.S. patent pending. With permission.)

thin-film superlattice materials appear to be near-term potential uses. Some of the challenges that remain to be addressed in the full development of this nanoscale thermoelectric-materials technology include optimization of the various electrical and thermal interfaces, both within the p–n couple and between the couple and the external thermal management components.

From the point of view of materials advancement over these superlattices, we anticipate that further improvements can be obtained with both the p-type Bi_2Te_3/Sb_2Te_3 and n-type $Bi_2Te_3/Bi_2Te_{3-x}Se_x$ materials using so called orthogonal quantum-confinement effects in quantum wires and quantum boxes.[42] The quantum confinement of carriers is orthogonal to the heat and current flow and can be implemented with these superlattice materials as shown in Figure 49.12. Here, the heat and electric current flow are along z-axis and the quantum confinement is in the $x-y$ plane. The quantum confinement[25] is expected to lead to a larger electronic density of states, resulting in larger Seebeck coefficients. The Seebeck coefficient enhancement is expected to be isotropic, thus allowing the combined effects of phonon-blocking–electron-transmitting structures with quantum-confinement effects. This approach could result in higher intrinsic material ZT values, enabling it to tolerate more parasitic losses while transitioning to modules. The device technologies that we have developed for two-dimensional layered superlattice materials are also applicable to such quantum-wire and quantum-box material concepts.

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