C1.1 Ohmic contacts to GaN and the III-V nitride semiconductor alloys

S.E. Mohney

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A INTRODUCTION

Ohmic contacts to GaN and the related semiconductors have received considerable attention in the last five years. Ohmic contacts to n-GaN have been far easier to achieve than ohmic contacts to p-GaN, and contact resistivities below 10^{-7} Ω cm^2 have been reported on the n-type semiconductor. The contact resistivities that have been reported for p-GaN are much higher, with recent reports ranging from 10^{-4} Ω cm^2 to the mid 10^{-2} Ω cm^2 range. For ohmic contacts to p-GaN, limiting factors have included difficulties in doping, higher carrier effective mass and possibly higher Schottky barrier heights. Ohmic contacts to n-InN, n-GaInN, n-AlInN and n-AlGaN have also been investigated. Low resistance ohmic contacts generally become easier to achieve as the semiconductor becomes more In-rich and its bandgap becomes smaller, while it is more difficult to make a good ohmic contact as more Al is added to the semiconductor and its bandgap becomes larger.

B OHMIC CONTACTS TO n-GaN

TABLE 1 summarises recent reports of ohmic contacts to n-GaN with contact resistivities below 10^{-4} Ω cm^2. The carrier concentration of the n-GaN is also provided to allow a fairer comparison between studies, since heavy doping promotes carrier transport by tunnelling and lower contact resistivities. The most frequently reported ohmic contacts to n-GaN are variations on the Ti/Al metallisation scheme [1-6], and contact resistivities below 10^{-7} Ω cm^2 have been reported for the Ti/Al/Ni/Au contact when a pre-metallisation reactive ion etch was employed [3]. Many of the low resistance ohmic contacts to n-GaN, including those in the Ti/Al family, involve nitride layers in direct contact with the n-GaN. In many cases, the nitride layers, such as TiN [4,7,8], β-W_2N [9] or a very thin AlN layer [6], have been observed to form through interfacial reactions. Researchers have speculated that the formation of a nitride layer through reaction with GaN causes N vacancies to form in the underlying GaN [1]. These vacancies could result in doping of the GaN and enhanced carrier transport by tunnelling, consistent with the observation of temperature-insensitive contact resistivities in annealed Al/Ti/n-GaN contacts [6]. Somewhat higher contact resistivities have been achieved when nitride layers, such as TiN [10,11] and InN/GaN superlattices [12], are directly deposited on n-GaN. The Ti/TiN [10,13] and Zr/ZrN [10] ohmic contacts present smooth surface morphologies and good long-term thermal stability at 600°C, much more so than the Al-rich contacts [1,14], although the Ti/Al/Ni/Au scheme is reported to exhibit an improvement in surface morphology compared to the Ti/Al contacts [3]. Other approaches to ohmic contact fabrication include implanting Si into the GaN [2,15] and high temperature annealing prior to metallisation [2], in the latter case to promote the formation of N vacancies at the surface of the n-GaN.

C OHMIC CONTACTS TO p-GaN

Achieving low resistance ohmic contacts to p-GaN has been challenging. Even though researchers have made great strides in the p-type doping of GaN, careful processing is needed to maintain high quality p-GaN near the surface of the semiconductor [21]. The most commonly employed metallisation is Ni/Au, although a variety of other ohmic contacts have been investigated, most containing Cr and/or

TABLE 1 Ohmic contacts with contact resistivities less than 10^{-4} Ω cm^2 on n-GaN.

Metallisation	Carrier concentration (cm^{-3})	Processing conditions	Contact resistivity (Ω cm^2)	Ref
Ti/Al (20 nm/100 nm)	~10^{17}	900°C, 30 s	8×10^{-6}	[1]
Ti/Al (35 nm/115 nm)	5×10^{17}	600°C, 15 s	5×10^{-6}	[5]
Ti/Al/Ni/Au (15 nm/220 nm/ 40 nm/50 nm)	4×10^{17}	900°C, 30 s Reactive ion etch of GaN surface prior to metallisation	9×10^{-8}	[3]
Pd/Al (12.5 nm/100 nm)	2.8×10^{17}	650°C, 30 s	1.2×10^{-5}	[16]
Nd/Al (200 nm/200 nm)	1×10^{18}	600°C, 30 s	8×10^{-6}	[17]
Ta/Al (35 nm/115 nm)	7×10^{17}	600°C, 15 s Additional Al overlayer deposited after annealing for TLM measurements	$3 - 6 \times 10^{-5}$	[14]
Ti (20 nm)	$1.5 - 5 \times 10^{17}$	975°C, 30 s Additional Ti/Au layers deposited after annealing	3×10^{-6}	[8]
Ti (150 nm)	7×10^{17}	800°C, 1 min in N_2 900°C, 1 min in Ar Additional Al overlayer deposited after annealing for TLM measurements	4×10^{-6}	[10]
TiN (thickness not reported)	7.4×10^{18}	No anneal	2.5×10^{-5}	[11]
TiN (200 nm)	7×10^{17}	800°C, 1 min	3×10^{-5}	[18]
Ti/TiN (5 nm/200 nm)	7×10^{17}	800°C, 1 min	6×10^{-6}	[10]
Zr/ZrN (20 nm/80 nm)	2×10^{18}	1000°C, 1 min	3×10^{-5}	[10]
Al (150 nm)	7×10^{17}	600°C, 1 - 8 min in Ar/H_2	8×10^{-6} to 1×10^{-5}	[5]
Al (250 nm)	5×10^{19}	No anneal	8.6×10^{-5}	[11]
W (50 nm)	1.5×10^{19}	600 - 1000°C, 1 min	8×10^{-5}	[9]
Ti/Ag (15 nm/150 nm)	1.7×10^{19}	No anneal	6.5×10^{-5}	[19]
Ti/Ni (5 nm/25 nm)	~1×10^{18}	1040°C, 30 s; deposition of Ti performed at 350°C	1.1×10^{-5}	[20]
Ti/Pd/Ni (5 nm/5 nm/25 nm)	~1×10^{18}	990°C, 20 s; deposition of Ti performed at 350°C	4.8×10^{-5}	[20]
Ti/Al (30 nm/200 nm)	$1 - 2 \times 10^{17}$ prior to ion implantation	Ion implantation followed by 1120°C pre-metallisation anneal; no contact anneal	1.0×10^{-5}	[2]
Ti/Au (3 nm/300 nm)	Ion implanted to ~4×10^{20}	No anneal after metallisation	3×10^{-8}	[15]
Ti/Al (20 nm/100 nm)	5×10^{18}	Metal deposited on InN/GaN short period superlattice	6×10^{-5}	[12]

high work function metals such as Ni, Pd, Pt and Au. The contacts are nearly always annealed, although usually not at conditions that result in the excessive consumption of GaN through interfacial reaction with the metallisation. The contact resistivities reported recently are in the low 10^{-4} Ω cm^2 to mid 10^{-2} Ω cm^2 range.

Several approaches to processing the ohmic contacts have been found to result in lower contact resistivities by a factor of about 2 - 3. These procedures include using the post-metallisation anneal to simultaneously activate the Mg dopant, rather than activating the dopant in a separate annealing step [21], using an electrodeposition process for metallisation [22], and annealing in an oxygen-containing environment, which it has been suggested further reduces hydrogen passivation of the Mg dopant [23]. TABLE 2 lists the reported ohmic contacts to p-GaN and their processing conditions whenever contact resistivities below 1 Ω cm^2 have been obtained.

TABLE 2 Ohmic contacts with contact resistivities less than 1 Ω cm^2 on p-GaN.

Metallisation	Carrier concentration (cm^{-3})	Processing conditions	Contact resistivity (Ω cm^2)	Ref
Pt (100 nm)	1×10^{20} (Mg concentration)	No anneal	1.3×10^{-2} measured @ 1 mA	[24]
Ni (100 nm)	1×10^{20} (Mg concentration)	No anneal	1.5×10^{-2} measured @ 1 mA	[24]
Au (100 nm)	1×10^{20} (Mg concentration)	No anneal	2.6×10^{-2} measured @ 1 mA	[24]
Ti (100 nm)	1×10^{20} (Mg concentration)	No anneal	3.5×10^{-2} measured @ 1 mA	[24]
Ni/Au (layer thicknesses not given)	$5 - 6 \times 10^{16}$ (pre-anneal)	750°C, 10 min No anneal of p-GaN to activate dopant prior to metallisation	3.3×10^{-3} measured @ 10 mA	[21]
Pt (layer thicknesses not given)	$5 - 6 \times 10^{16}$ (pre-anneal)	750°C, 10 min No anneal of p-GaN to activate dopant prior to metallisation	1.4×10^{-3} measured @ 10 mA	[21]
Pt/Au (layer thicknesses not given)	$5 - 6 \times 10^{16}$ (pre-anneal)	750°C, 10 min No anneal of p-GaN to activate dopant prior to metallisation	1.5×10^{-3} measured @ 10 mA	[21]
Pd/Pt/Au (layer thicknesses not given)	$5 - 6 \times 10^{16}$ (pre-anneal)	750°C, 10 min No anneal of p-GaN to activate dopant prior to metallisation	2.4×10^{-3} measured @ 10 mA	[21]
Pd/Au (20 nm/500 nm)	9×10^{16}	500°C, 30 s	9.1×10^{-3}	[25]
Cr/Au (50 nm/500 nm)	9.8×10^{16}	900°C, 15 s	$\leq 4.3 \times 10^{-1}$	[26]
Cr/Au (25 nm/200 nm)	1.4×10^{20}	500°C, 1 min (p^+-GaN grown by plasma-assisted MBE)	1.2×10^{-4}	[27]
Ni/Cr/Au (15 nm/15 nm/500 nm)	1×10^{17}	No anneal; increased contact resistivity upon annealing	8.3×10^{-2}	[28]
Ni/Mg/Ni/Si (25 nm/5 nm/ 25 nm/240 nm)	3×10^{17}	400°C, 30 min GaN heated to 400°C for 10 min in vacuum prior to metallisation	9.6×10^{-4}	[29]

D OHMIC CONTACTS TO THE ALLOY SEMICONDUCTORS

Non-alloyed (as-deposited) ohmic contacts to n^+-InN and n^+-$Ga_{0.35}In_{0.65}N$ have been achieved with W [30], Ti/Al [30] and WSi_x [30] metallisations. In addition, Ti/Pt/Au contacts have been prepared on n^+-InN [31]. Compared to Ti/Al and WSi_x, the W contacts exhibited the best thermal stability, with contact resistivities of $<10^{-7}$ Ω cm^2 on $Ga_{0.35}In_{0.65}N$ after annealing at 600°C and 1×10^{-7} Ω cm^2 on InN after annealing at 300°C. When Al is added to the alloy semiconductors and the bandgap is increased, it is more difficult to realise low resistance ohmic contacts. Contact resistivities of 10^{-2} Ω cm^2 have been measured for annealed Ti contacts to n-$Al_{0.5}In_{0.5}N$ [32], and low resistance ohmic contacts have been achieved on AlInN by growing a layer graded from AlInN to pure InN followed by deposition of a WSi_x contact [33]. Contact resistivities as low as 3×10^{-6} Ω cm^2 have been reported for optimised Al/Ti/n-$Al_{0.15}Ga_{0.85}N$/n-GaN contacts for heterostructure devices [34]. However, as more Al-rich alloys are used, achieving low contact resistivities to these materials may present a considerable challenge.

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