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Study of Metal–Dielectric Interface for Improving Electrical Properties and Reliability of DRAM Capacitor

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The interface between a dielectric thin film and a metal electrode is studied to improve reliability as well as electrical properties of the metal–insulator–metal (MIM) capacitor in dynamic random-access memory (DRAM) devices. The interfacial layers between a dielectric thin film and a metal electrode play important functional roles such as increasing the electrical barrier or preventing oxygen defects in high-k dielectrics. By introducing an electrical barrier layer or a sacrificial layer at the metal–dielectric interface for engineering the electronic band, lattice, or dipole, various effects could be confirmed such as the conduction band offset (CBO), bandgap or mismatch modulation for controlling the dielectric loss depending on the AC frequency or leakage current of MIM capacitors. Upon the insertion of Al_2O_3 as an electrical barrier layer, CBO increased because of the band engineering. Further, upon the insertion of TiO_2 as a sacrificial layer at the interface, CBO increased because of the dipole formation at the interface, attributed to the difference in electronegativity. Thus, a robust MIM capacitor for DRAM that maintains a low leakage current and has improved reliability which is realized using the proper combination of interfacial layers.

1. Introduction

The reliability of a dynamic random-access memory (DRAM) capacitor can be determined from the characteristics of the interface between each of its two electrodes and a high-k dielectric thin film between them. Electrical properties such as capacitance and leakage current of a metal–insulator–metal (MIM) capacitor can also be determined from the characteristics of its metal–dielectric interface. An electric potential barrier is formed when a high-k dielectric thin film comes in contact with top and bottom metal electrodes. When a voltage is applied, the electron charge stored at the interface between the electrodes can be rate-limited by such a potential barrier at the metal–dielectric interface or a trap energy level such as an oxygen vacancy in the high-k dielectric thin film. A reaction causing crystal changes in the capacitor due to a difference in the formation enthalpy between the dielectric layer and each electrode may occur between the dielectric thin film and each electrode; such a reaction may considerably change the reliability and electrical properties of the capacitor. Accordingly, manufacturing a capacitor for a semiconductor device by considering the interface characteristics is necessary; moreover, controlling the metal–dielectric interface to suppress the leakage current and thereby improving the reliability of MIM capacitors by introducing various types of interfacial layers between them is important. Studies on the functional layer in DRAM capacitors with respect to criteria such as doping or layer insertion in high-k dielectric films have been previously conducted.[1–4] Moreover, leakage current suppression has mainly focused on the bulk properties of high-k defects such as oxygen vacancies (V_o), grain boundaries, and impurities. The present study covers not only high-k defects but also the role of the interface between the high-k dielectric and the metal electrodes. The excellent electrical performance of TiN-insulator-TiN (TIT) capacitors has already been demonstrated;[5–7] however, some problems have been observed, such as an abnormal current density increase at a negative biasing voltage in stress-induced leakage current (SILC) measurements, as shown in **Figure 1**a. This degradation of current density could be explained using the hole-induced breakdown model.[8–10] The breakage of Zr—O bonds may generate hole traps near the upper electrode interface, which could reduce the Fowler–Nordheim (FN) tunneling area, as shown in Figure 1b. The directional dependence of the leakage current density on the bias voltage is attributed to the different Zr—O bonding status at the interface between the top and bottom electrodes. The easy breakage of Zr—O bonds at the top interface accelerates hole traps because of the applied electric stress after the SILC measurements.

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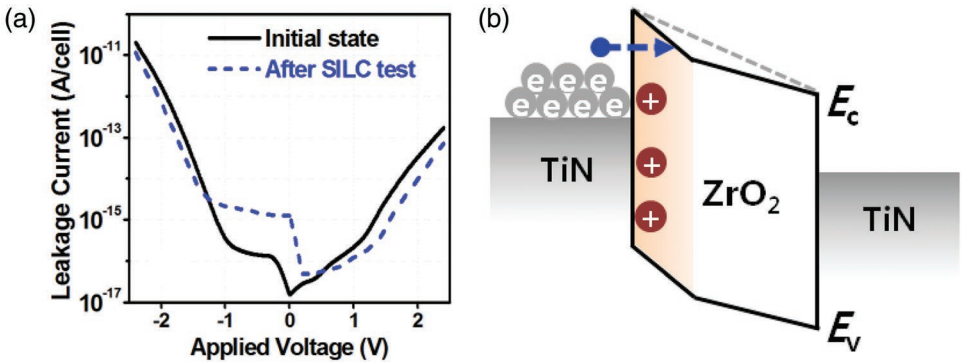

Figure 1. a) *J–V* curves at the initial stage and after the stress-induced leakage current (SILC) test and b) schematic band diagram under negative biasing with hole traps. The electrical data were extracted from nine points in each sample.

The formation of the energy barrier is due to the energy band offset at the interface between the dielectric and electrode of the MIM capacitor. During the manufacturing processes, oxygen from the high-k dielectric thin film may move into the metal electrode, thereby generating dielectric defects at the interface, which cause barrier lowering. Such a barrier lowering can cause an increase in the leakage current and equivalent oxide thickness ($T_{oxeq.}$) of high-k dielectrics. To prevent this issue in MIM capacitors, various functional layers could be introduced at the metal–dielectric interface. In this study, we investigated the effects of the interfacial layer of MIM capacitors fabricated via atomic layer deposition (ALD). X-ray photoelectron spectroscopy (XPS), ultraviolet photoemission spectroscopy (UPS), and spectroscopic ellipsometry (SE) were employed to analyze the electronic band structure to determine the interfacial chemical composition, dielectric bandgaps, and values for the conduction/valence band offsets (CBO/VBO). Electrical properties such as capacitance and leakage current were measured, and the reliability parameters of MIM capacitors, such as D0 (Data 0) retention, were evaluated with the different interfacial layers.

2. Results and Discussion

Various functional layers were introduced at the metal–dielectric interface in the MIM capacitors. The roles of interfacial layers between the high-k dielectric and metal electrodes could be divided into two categories. One is an electrical barrier layer of high-bandgap oxides such as Al_2O_3. The other is a sacrificial layer of metal oxides such as TiO_2. These interfacial layers could act as the CBO and energy band as well as enable lattice mismatch modulation.

A thin film of a high-k dielectric such as ZrO_2 was crystallized after post-thermal processing. The crystalline structure remained unchanged under the insertion of an Al_2O_3 layer of thickness up to 2 Å in ZrO_2 (Figure S1, Supporting information). Crystalline grain boundaries also play an important role in the leakage current path. A shallow trap level can be formed near the conduction band edge within the ZrO_2 bandgap owing to the grain boundary formation between tetragonal (011) ZrO_2 grains. It can be removed by Al substitution at the grain boundary from first-principles calculations (Figure S2, Supporting information). Surface morphology was experimentally confirmed using atomic force microscopy (AFM). A normal AFM image shows the morphology of the crystalline grains and boundaries of the high-k dielectric film. (Figures S3a, Supporting information) The tunneling AFM image (TUNA) shows that the leakage current passes near the valley between crystalline grains as a voltage is applied (Figure S3a,b, Supporting information). Therefore, the continuous leakage current originating from grain boundaries should be controlled. To prevent intrinsic defects in the high-k dielectric thin film and short-circuit leakage path along grain boundaries, an amorphous high-bandgap oxide such as Al_2O_3 was inserted via ALD. By inserting an Al_2O_3 layer in the ZrO_2 film, the tunneling current through the grain boundaries was suppressed (Figure S3c, Supporting information).

A high-bandgap oxide such as Al_2O_3 is inserted as an electrical barrier layer in a ZrO_2 dielectric film; such a structure is called ZAZ and prevents trap-assisted tunneling in the ZrO_2 dielectric film by oxygen defects due to the reaction of the dielectric film and metal electrode.[11–13] An Al_2O_3 thin layer was deposited via ALD in the middle of the ZrO_2 dielectric films. The energy band structure of an MIM capacitor with respect to different dielectric stacks is shown in **Figure 2**. The electronic band was investigated through the ultraviolet–spectroscopy ellipsometry (UV-SE) analysis of the optical bandgap and UPS spectra of the low-binding-energy range for valence band maximum (VBM) estimation; thus, the band diagrams of undoped ZrO_2 and ZAZ dielectric films deposited on a TiN substrate were deduced. The value of CBO increased in the case of a MIM capacitor with an Al_2O_3 electrical barrier layer between ZrO_2 dielectric films. This is attributed to a shift in the Fermi level to a lower level due to holes generated by Al^{3+} doping in the ZrO_2 dielectric film. The CBO value of ZAZ (2.12 eV) is 0.39 eV higher than that of ZrO_2 (1.73 eV). This is because of a positive E_F shift in binding energy (i.e., p-doping effect) caused by the insertion of an Al_2O_3 layer within the ZrO_2 dielectric film.[14,15]

Meanwhile, Al_2O_3 was applied as an ultrathin high-bandgap oxide (UTHB) between the top of the ZrO_2 dielectric and the upper TiN electrode via ALD. A TiO_2 layer inserted between them was applied as a reference. **Figure 3**a shows that the equivalent oxide thickness ($T_{oxeq.}$) decreases and the breakdown voltage increases upon inserting a UTHB layer. This means that the capacitance of the ZrO_2 dielectric thin film with a UTHB layer inserted underneath the upper TiN electrode increased.

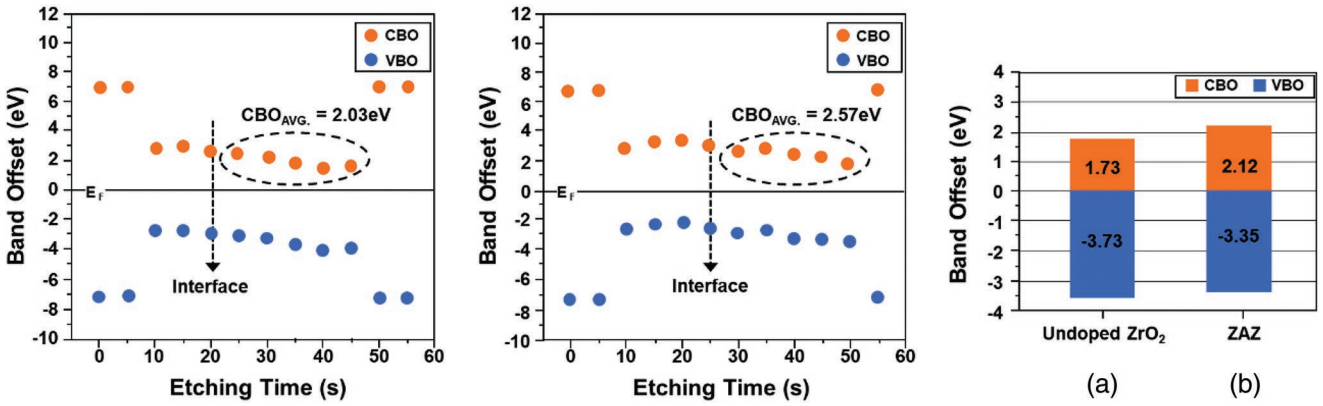

Figure 2. Plot of band offset versus sputtering time of the TiN-insulator-TiN (TIT) stack with different dielectric layers and energy band structure of a metal–insulator–metal (MIM) capacitor with different dielectric stacks: a) ZrO_2 and b) ZAZ. The error range of energy in this model is ±0.05 eV.

As the dielectric film's thickness is reduced, the greater the lattice mismatch between the electrode and dielectric film, the greater is the curvature of nonlinearity due to the increase in the interfacial effect.[16,17] The nonlinearity of capacitance can be expressed as a parabolic function:

$$C(V) = C_0\left(\alpha V^2 + \beta V + 1\right) \quad (1)$$

where C_0 is the capacitance at 0 V and α and β are voltage coefficients. The nonlinearity coefficient (α) is related to Maxwell film stress deformation, which increases with the lattice mismatch.

The nonlinearity coefficient of a UTHB capping dielectric is 93.2% greater than that of a TiO_2 capping dielectric. The difference in lattice parameter between UTHB and TiO_2 can appropriately explain this coefficient change. The difference in the lattice parameter between UTHB and TiN is 57% greater than that between TiO_2 and TiN. Therefore, compared to TiO_2, the nonlinearity coefficient of UTHB is greater; this can increase the capacitance. Figure 3b shows the change in band diagram due to the insertion of UTHB. Because of its own high bandgap, UTHB forms a greater barrier height with the upper electrode than does TiO_2 to prevent the leakage current through the dielectric film. Thus, a higher capacitance and lower leakage could be achieved simultaneously by inserting UTHB between the top of the ZrO_2 dielectric and the upper TiN electrode.

However, UTHB presents one problem, namely, resistance increase. The resistance increase due to UTHB insertion is attributed to the trap generation. The trap is generated by the difference in oxidation numbers of TiO_2 (Ti^{4+}) and UTHB (Al^{3+}). XPS was used to confirm the binding energy at the interface (Figure S4, Supporting information). The chemical bonding change of TiO_2 due to UTHB deposition was observed. As UTHB is deposited, the binding energy of the Ti atom decreases. The decreased oxidation number of Ti leads to a reduction in binding energy.[18] Thus, the oxidation number of Ti at the interface decreases owing to the deposition of UTHB, which has a lower oxidation number than Ti, thereby causing the formation of dangling bonds at the interface. The bonding of oxygen does not show any significant change, indicating that the change is related to metal ions. The resistance failure caused by the trap generation can be confirmed from the reduction rate of capacitance at a high frequency. To quantify the capacitance degradation at a high frequency, the reduction rate of capacitance between 10 kHz and 1 MHz was defined as a dissipation ratio (C_s_DR).

$$C_{s}\_\mathrm{DR} = 1 - C_{s,1MHz}/C_{s,10kHz} \quad (2)$$

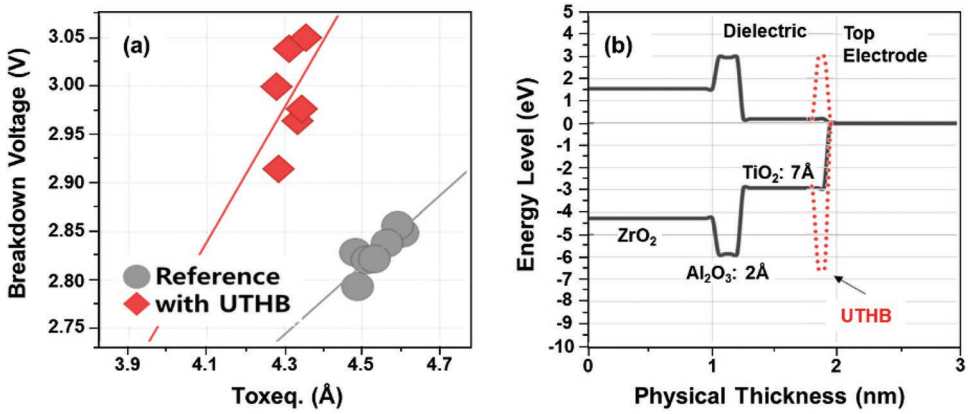

Figure 3. a) $T_{oxeq.}$–breakdown voltage trend and b) band diagram change due to ultrathin high-bandgap oxide (UTHB) application. The electrical data were extracted from nine points in each sample.

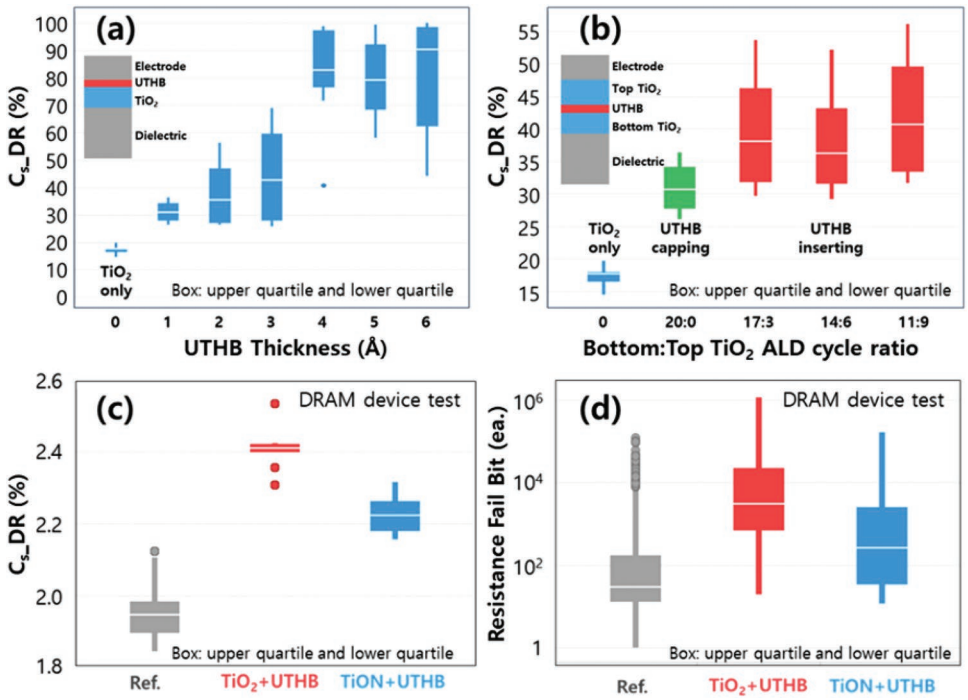

Figure 4. C_s_DR trend according to a) UTHB thickness and b) insertion positions with/without TiO_2 capping layer. c) C_s_DR and d) resistance fail bit according to different capping layers between the dielectric thin film and the upper TiN electrode. The electrical data were extracted from nine points in each sample. Significance level of resistance failure was defined as $p \leq 0.05$ from 1K chips for each condition.

where $C_{s,1MHz}$ and $C_{s,10kHz}$ are the capacitances of the dielectric thin film at 1 MHz and 10 kHz, respectively.

To investigate the origin of trap generation from UTHB and TiO_2, UTHB was deposited on the top of the ZrO_2 dielectric film with varying thicknesses (≈1–6Å) and compared with TiO_2 deposited on the top of ZrO_2 as a reference. **Figure 4**a shows that C_s_DR increases as the thickness of UTHB increases, and when UTHB is deposited at 4 Å or more, C_s_DR does not increase further. C_s_DR is attributable to the electrode resistance or an interfacial trap. In this experiment, a planar MIM structure was used, with the electrode area being considerably greater than its length. Therefore, the electrode resistance could be ignored and the increase in C_s_DR could be related to the interfacial trap. If the bulk trap of the ZrO_2 dielectric is generated by inserting a UTHB layer, C_s_DR should increase without saturation depending on the UTHB thickness. However, C_s_DR was saturated at a thickness of 4 Å; thus, it could be related to the interfacial trap. The insertion of UTHB creates two different interfaces: electrode interface and dielectric interface. Figure 4b shows the C_s_DR trends with and without TiO_2 capping on the top of the ZrO_2 dielectric film. In Figure 4b, "UTHB capping" means that it was deposited without a TiO_2 capping layer and "UTHB inserting" means that it was deposited with a TiO_2 capping layer according to the ratio of UTHB to TiO_2. The C_s_DR of "UTHB inserting" increases compared to that of "UTHB capping." This indicates that the interface between TiO_2 and UTHB generates more traps than that between TiN and UTHB. The interface trap is generated by lattice mismatch, which is related to physical bonding, or the dangling bond, which is related to chemical bonding.[19,20] Regarding the lattice mismatch, the lattice of UTHB is larger than that of TiN and smaller than that of TiO_2. Therefore, the TiO_2/UTHB interface is expected to be physically well matched compared with the TiN/UTHB interface (Table S1, Supporting information); thus, it cannot explain the C_s_DR trends in Figure 4b. Regarding the chemical bonding, TiN and UTHB have the same oxidation number of 3+, whereas TiO_2 has an oxidation number of 4+. The oxidation number difference between TiO_2 and UTHB can generate the interface trap and thus cause an increase in C_s_DR. To reduce the interface mismatch, a TiON capping layer with UTHB was introduced because its oxidation number is more similar to that of UTHB than TiO2. As shown in Figure 4c,d, C_s_DR and resistance failure can be reduced when TiON/UTHB capping is applied compared to TiO_2/UTHB capping. TiO_2 has a higher oxidation number than UTHB and causes an increase in C_s_DR and decrease in Ti binding energy. A TiON film has lower binding energy than TiO_2, implying that the TiON layer could be well matched with UTHB (Figure S5, Supporting information). Most high-k dielectric metal oxides, including TiO_2, ZrO_2 and HfO_2, have an oxidation number of 4+, which does not match with the UTHB oxidation number. The UTHB insertion on the TiO_2 capping layer causes an increase in C_s_DR, whereas the introduction of TiON having an oxidation number similar to that of UTHB reduces C_s_DR up to 44.7%, thereby reducing the resistance failure by 89.5%, as shown in Figure 4c,d.

A MIM capacitor includes a ZrO_2 dielectric thin film between the lower and upper TiN metal electrodes. A sacrificial layer such as TiO_2 was inserted between the ZrO_2 dielectric layer and the upper TiN electrode. The sacrificial layer may function as an oxygen-donating layer that provides oxygen atoms to the upper TiN electrode instead of the dielectric layer during device-manufacturing processes (Figure S6, Supporting

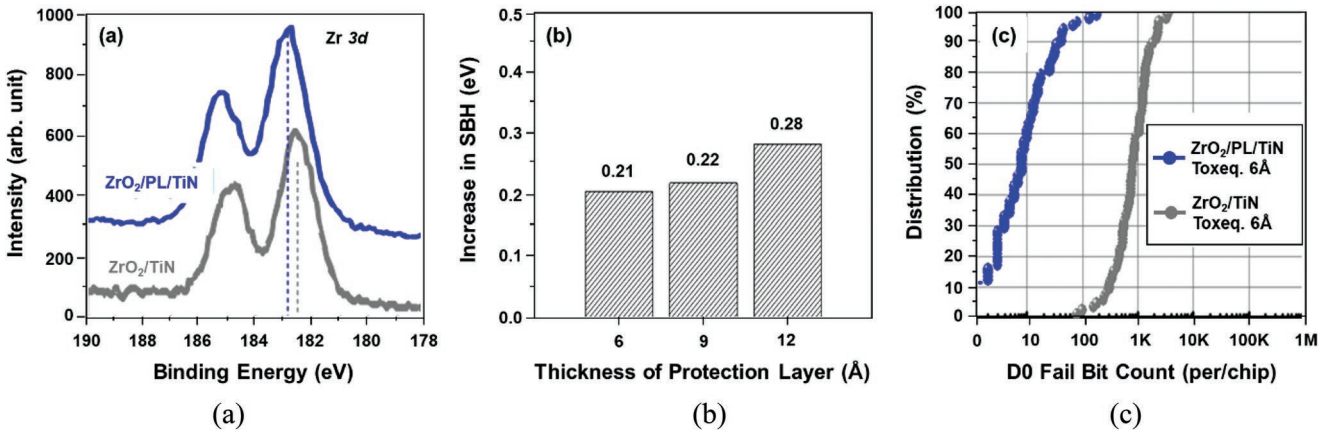

Figure 5. a) Zr 3d X-ray photoelectron spectroscopy (XPS) signal change in ZrO_2 upon insertion of a protection layer (PL) between ZrO_2 and TiN. b) Change in conduction band offset (CBO) (Schottky barrier height) with PL thickness at the top interface. c) D0 fail bit distribution upon insertion of a PL between ZrO_2 and TiN, where $T_{oxeq.}$ denotes equivalent oxide thickness. The error range of XPS energy is ±0.05 eV. Significance was defined as $p \leq 0.05$ from 1K chips for each 8-Gbit sample.

information). The reaction between the ZrO_2 dielectric film and the upper TiN electrode during the post-backend thermal processes as well as the TiN deposition process should be prevented to protect Zr—O bonds in the dielectric film.

As confirmed by SE and UPS analyses, even though the electrical barrier layer at the metal–dielectric interface may not affect the energy band structure of the ZrO_2 dielectric film, it could generate interfacial bonding defects between the dielectric film and the TiN electrode. When the ZrO_2 dielectric thin film comes in direct contact with the TiN electrode, the Ti layer near the interface has a greater charge density than the Zr and O layers near the interface. Thus, the small electric dipole at the interface created by this asymmetric charge distribution reduces the CBO. A sacrificial layer such as TiO_2 between a dielectric and a metal electrode can act as a protection layer (PL) to prevent the reduction of the dielectric film and redistribute the charge density at the interface; thus, the interface dipole moves in the opposite direction, which increases the CBO (Figure S7, Supporting information). To protect the Zr—O bonds of high-k dielectric films, the reaction between the ZrO_2 dielectric film and the top TiN electrode during TiN deposition and the hydrogen incorporation into ZrO_2 during the backend processes should be prevented. First, the oxygen vacancy difference was investigated at the top and bottom interface between the ZrO_2 dielectric film and TiN electrode. Because the bottom TiN electrode was oxidized by oxidants such as O_3 and H_2O during the ZrO_2 ALD process, equilibrium oxygen concentration was achieved at the bottom interface. However, the top TiN electrode was deposited in a deoxidization atmosphere with $TiCl_4$ as the precursor and an ammonia atmosphere, which reduced the oxygen concentration at the top interface.

The CBO according to the oxygen coverage amount at the interface was simulated from first-principles' calculations. The value of CBO increased by 0.6 eV from 35% to 100% oxygen coverage at the interface between tetragonal ZrO_2 and TiN (Figure S8a, Supporting information). As the top interface is expected to have low oxygen coverage, electron tunneling can easily occur when CBO is low under a bias electric field stress. Further, CBO was calculated by inserting TiO_2 as a PL between ZrO_2 and TiN. PL insertion significantly affects the Schottky barrier height by minimizing the reaction between ZrO_2 and TiN and thus increases the CBO up to 0.9 eV under addition of three layers (Figure S8b, Supporting information). Based on the simulation results, the effect of the PL was experimentally evaluated. In XPS analysis, Zr 3d binding energies were compared according to the PL insertion shown in **Figure 5**. The Zr 3d peak is significantly shifted to a 0.5-eV higher binding energy state in a PL-inserted sample (Figure 5a). A lower binding energy can result from bonds with less electronegative elements than oxygen (e.g., N on oxygen sites) or the depletion of oxygen from ZrO_2.[21–23] This means that PL insertion reduced the reaction between ZrO_2 and TiN and thus Zr—O bonds at the interface were protected. The CBO was calculated from the leakage current with measurements at different temperature. As shown in Figure 5b, the CBO value increased with an increase in the PL thickness, which is in agreement with the prior simulation result, but the degree of the CBO increase was only 0.28 eV at PL = 12 Å. This difference in CBO arises from a simulation model assumption. In a model system, we choose 5×1 unit cell of (111) interfaced TiN metal with a 3×1 unit cell of a tetragonal-ZrO_2 surface with (110) orientation. However, it is hypothesized that ZrO_2 is not fully crystallized with (110) orientation and TiN metal is also not a single crystal with (111) interface.

As for the DRAM device performance, the Data 0 (D0) retention characteristic is one of the most important test criteria related to DRAM capacitor reliability. In each cell, the amount of D0 charge written in the MIM capacitor should be retained during the device test operation; if the D0 charge is lost under the device-sensing margin due to the leakage current from the MIM capacitor, it sets to a fail bit at the device read operation. Figure 5c shows the distribution of D0 retention fail bits of a MIM capacitor with and without PL. D0 fail bits were dramatically reduced by up to two orders of magnitude at the same $T_{oxeq.}$ in the case of the MIM capacitor with PL insertion between the ZrO_2 dielectric film and upper TiN electrode. From this result, it was confirmed that the protection of Zr—O bonds at the ZrO_2/TiN interface secured the DRAM capacitor's reliability.

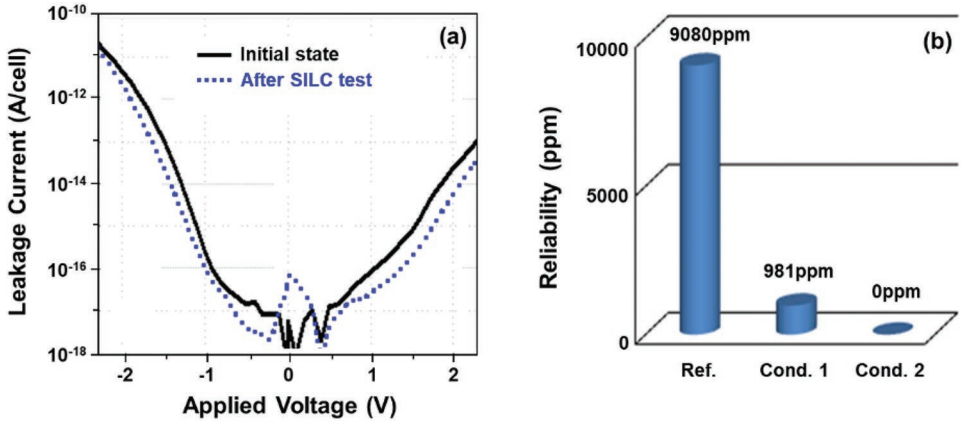

Figure 6. a) *J–V* characteristics initially and after the SILC test with a PL and b) reliability fail-bit rate in package chips with conditions according to PL layers. The electrical data were extracted from nine points in each sample. Significance was defined as $p \leq 0.05$ from 10K 8-Gbit chip samples for each condition.

Figure 6a shows the leakage current density versus biasing voltage (*J–V*) characteristics of the MIM capacitor with PL addition before and after the SILC test. Through PL addition, an abnormal current density increase in the overall range of the biasing voltage compared to the initial measurement was not observed, except under the zero-bias condition. At zero biasing voltage, the trapped electrons in the ZrO_2 dielectric film were measured as a leakage current value during the voltage sweep test. From the viewpoint of DRAM device performance, through such interfacial controls of the MIM capacitor, the D0 fail-bit rates in the mass production reliability test (PRT) after packaging chips dramatically decreased to 0 ppm as the thickness of the PL layers increased from 6 (Condition #1) to 12 Å (Condition #2), as shown in Figure 6b. Thus, a very reliable and robust DRAM capacitor scheme was successfully realized. A function of the sacrificial layer may be to serve as an oxygen-donating layer that provides oxygen atoms to the metal electrode and thus prevent the reduction of the dielectric thin film. The dipole moment resulting from the sacrificial layer at the interface between the high-k dielectric film and the top electrode can also increase the CBO value. Meanwhile, the sacrificial layer may have a double-layered structure comprising the electrical barrier and sacrificial layers. The sacrificial layer may be a conductive layer such as TiO_2, and the electrical barrier layer may be a dielectric layer such as Al_2O_3. In addition, depending on the electronegativity of various metal oxides as sacrificial layers, the greater the difference in the electronegativity between the sacrificial layer and the metal electrode, the greater is the potential barrier formed by the higher dipole moment at the metal–dielectric interface. When a TiO_2 sacrificial layer is replaced with SnO_2, the potential barrier for electrons across the metal–dielectric interface may increase (Figure S9, Supporting information).

Finally, the purposes of the metal–dielectric interfacial layers of the MIM capacitor are summarized in **Figure 7**a. By introducing an electrical barrier layer or sacrificial layer at the interface between the high-k dielectric thin film and the metal electrode for energy band, lattice or dipole engineering, various effects such as CBO, bandgap or mismatch modulation to control the dielectric loss or leakage current could be observed. Electrical barrier layers such as Al_2O_3 could modulate the CBO and lattice mismatch at the interface by changing the energy band structure of the high-k dielectric film. A very thin Al_2O_3 layer in the middle or on top of the high-k dielectric oxide of

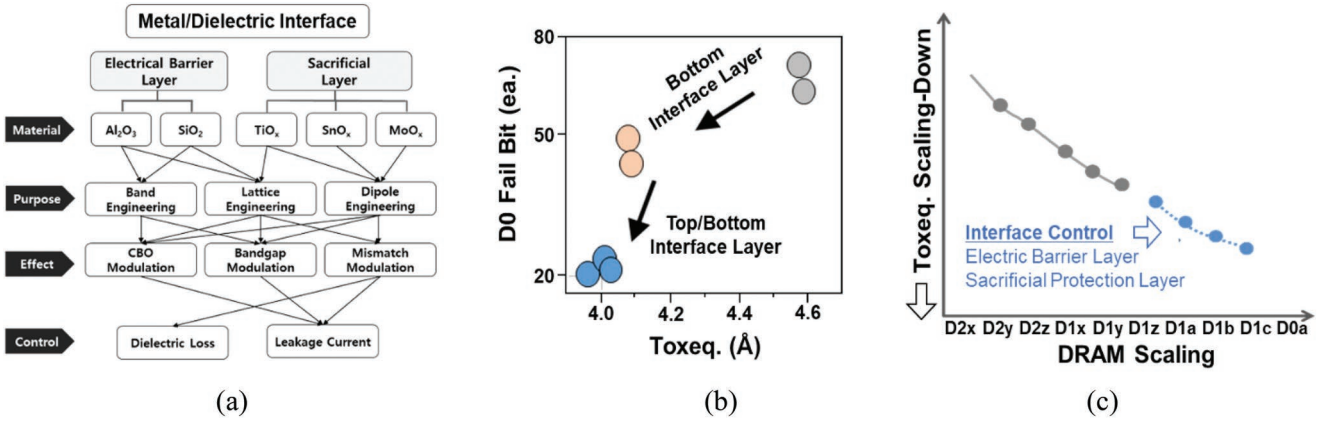

Figure 7. a) Functions of metal–dielectric interface, b) D0 fail bits versus $T_{oxeq.}$ according to the interfacial layers, and c) $T_{oxeq.}$ scale-down of the MIM capacitor via interface control according to DRAM scaling. Significance was defined as $p \leq 0.05$ from 8G cells of 1K chips for each sample.

the MIM capacitor could increase the CBO and thus reduce the leakage current. A sacrificial layer such as TiO_2 could prevent oxygen-deficient defects of the high-k dielectric oxide and also increase the CBO by lowering the valence band maximum (VBM) due to the dipole formation at the metal–dielectric interface. A bottom interfacial layer such as TiO_2 could also reduce the leakage current under a positive bias voltage because it acts as the PL, such as the top interface (Figure S10, Supporting information). As for DRAM device performance and reliability, by combing multi-interfacial layers at both the top and bottom metal–dielectric interfaces for the electrical barrier and sacrificial layers, D0 retention fail bits and the leakage current improved even when the $T_{oxeq.}$ of the MIM capacitor was scaled down, as shown in Figure 7b. Thus, by modulating the metal–dielectric interface using different functional layers between the high-k dielectric thin film and metal electrode, continuous $T_{oxeq.}$ scale-down of the MIM capacitor could be achieved, as the feature size of DRAM has been scaled to the early 10-nm range.

3. Conclusion

Various functional interfacial layers between a high-k dielectric thin film and a metal electrode were studied to improve the D0 retention reliability and electrical properties of the MIM capacitor for DRAM devices. These layers play important roles in not only preventing oxygen defects in high-k dielectrics but also increasing the CBO at the interface between the high-k dielectric thin film and metal electrodes. The leakage current of the MIM capacitor was significantly reduced by modulating the electronic band structure, lattice mismatch, and dipole engineering between them. Through the proper application of the electrical barrier and sacrificial layers in the MIM capacitor, the wafer-level reliability, such as SILC and D0 retention, as well as the package-level reliability related to D0 fail bits were dramatically improved.

4. Experimental Section

Fabrication: ZrO_2 and ZAZ thin films were deposited via ALD using trimethylaluminum and tris(dimethylamino) cyclopentadienyl zirconium (Cp-Zr) as precursors and ozone as the reactant gas at 250 °C. 100-Å-thick ZrO_2 and ZAZ films were used for samples of the grazing-incidence X-ray diffraction (GIXRD), AFM, TUNA, time of flight secondary ion mass spectroscopy (ToF-SIMS), SE, XPS and UPS analysis, while 44-Å-thick ZrO_2 and ZAZ films were used for device samples of the electrical properties such as capacitance and leakage current and reliability such as D0 fail bit. Depth profiling samples using the atomic probe tomography (APT) consisted of 20-Å-thick ZrO2 film and 50-Å-thick ZrO2 lower TiN with and without 7-Å-thick TiO_2. The MOS capacitor structure was consisted with SiGe (800Å)/TiN (30Å)/TiO_2 (3–10Å)/ZrO_2 (68Å)/Interfacial oxide (13Å)/Si substrate. For fabricating the ZAZ layer structure, an Al_2O_3 layer of 1–2 Å thickness was deposited in the middle of the ZrO_2 film, but it was diffused out from the centroid of the ZrO_2 film after post-deposition annealing at 500 °C. For fabricating the interfacial Al_2O_3 layers of 1–6 Å thickness between the top ZrO_2 layer and the upper TiN electrode, trimethylaluminum was used as an Al precursor and O_3 was used as a reactant gas at 350 °C. ALD TiN was deposited as a bottom or an upper electrode using $TiCl_4$ and NH_3 gases at 450 °C. Further, ALD TiO_2 was deposited between the high-k dielectric film and the upper electrode using pentamethylcyclopentadienyl titanium trimethoxide as the precursor and O_3 as the reactant gas at 280 °C. For fabricating ZAZ layer structure, Al_2O_3 layer having thickness range from 1 Å to 2Å was deposited in the middle of ZrO_2 in the separate ALD system, but it was diffused out from the centroid of layer after ALD. For fabricating the interfacial layers of Al_2O_3 having a thickness range from 1 to 6 Å between top ZrO_2 and the upper TiN electrode, trimethylaluminum were used as Al precursors and O_3 was used as a reactant gas. As a bottom or top electrode, ALD TiN having 100 Å thickness was deposited using $TiCl_4$ and NH_3 gases. TiO_2 layers having thickness range from 6 to 12 Å were deposited in the ALD system between ZrO_2 dielectric film and upper TiN electrode using pentamethylcyclopentadienyl titanium trimethoxide precursor and O_3 reactant gas.

Characterization: The tetragonal crystalline ZrO_2 phases were analyzed using the grazing-incidence X-ray diffraction (GIXRD). The incident angle was set at 0.5°, which is slightly larger than the critical angle of a ZrO_2, in order to avoid the diffraction intensity from the interlayer or TiN substrate. At 0.5°, the most diffraction intensity or peaks will come from at the top of the film. An angular resolution was 0.002° in a θ–2θ scan. Surface morphology and image of the confined leakage currents were observed using the AFM and the TUNA, respectively. A Pt—Ir coated tip was used and scan size was 1 µm. Current sensitivity was 1 nA V^{-1} and DC bias voltage was applied from 0 to 10 V. ToF-SIMS equipped with a bismuth liquid metal ion gun was used for the depth profiling of the upper TiN/TiO_2/ZrO_2 samples. The sputtering was performed using an Ar beam (1 keV). The atomic probe tomography (APT) measurements were performed using a LEAP 4000XSi with a pulsed UV laser (λ = 355 nm) and a detector efficiency of 0.57. The chamber pressure was within the range of 10^{-12} to 10^{-11} Torr. The laser pulse energy was set to 100 pJ at a pulse rate of 250 kHz. The VB edge electronic structure and work function of the MIM capacitor were analyzed using XPS and UPS (Thermo Fisher Scientific Co., Theta probe) with an Al Ka X-ray source (1486.6 eV) and helium (I) UV radiation, respectively. For XPS depth profiling, an Ar sputtering process of up to 120 s was performed. To minimize Ar ion bombardment, the Ar ion flux energy was adjusted to a very mild condition of ion acceleration bias at 2 kV and current at 1 µA; no significant generation of Ti metallic states was observed after Ar sputtering.[24] The determination of VBO using XPS analysis was possibly subjected to some degree of deviation induced by the differential charging effect against the real band structures. This may introduce an additional uncertainty at the level of 60.1 eV.[25,26] A rotating analyzer enhanced SE measurement was applied under UV–V illumination using photon energies ranging from 1.5 to 6 eV for determining the optical bandgap of dielectrics. To extract optical properties such as the complex dielectric function and absorption coefficient of the dielectric overlayer with respect to the TiN electrode/substrate, three-phase optical modeling was applied.

Electrical Measurements: For evaluating electrical properties, HP4145 was used to measure *J–V* and SILC and an LCR meter to measure capacitance. D0 retention fail bits were evaluated using wafer-level and package-level test programming tools.

Simulations: To quantitatively understand the band alignment and the role of transition layers, first-principles density functional theory (DFT) calculations[27] were performed based on the generalized gradient approximation method[28] implemented with the projector augmented wave (PAW)[29] pseudopotential using the Vienna ab initio Simulation Package (VASP).[30] Calculations using the Heyd–Scuseria–Ernzerhof (HSE) hybrid functional approach[31] were also performed to improve the bandgap of ZrO_2. To reproduce the experimental bandgap of ZrO_2, the Hartree–Fock fraction (α) was set to 0.32. All calculations were performed using: i) a plane wave cutoff energy of 450 eV; and ii) superlattice structures without vacuum. In our calculations, the rock-salt TiN (111)/t-ZrO_2 (011) stack and t-ZrO_2 (011)/t-ZrO_2 (011) stack that comprises seven TiN layers and seven ZrO_2 layers was considered.

Statistical Analysis: Electrical data such as $T_{oxeq.}$, C_s–DR, and *J–V* characteristics were extracted from nine points in each sample. The D0 fail-bit rate was obtained from 8G cells of ≈0.5–1K chips for each sample. The fail-bit rate of production reliability test (PRT) reliability was obtained from more than 10K chip samples. Continuous variables

are expressed as mean ± 0.05 in 3σ. For normally distributed data sets with equal variances, non-parametric hypothesis testing was performed across groups. In all cases, significance was defined as $p \leq 0.05$. Statistical analysis was conducted using TIBCO Spotfire software or Minitab statistical software.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available in the supplementary material of this article.

Keywords

DRAM, electronic band structure, high-k, MIM capacitor

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