NEUROMORPHIC CHIPS

2D materials–based homogeneous transistor-memory architecture for neuromorphic hardware

Lei Tong[1], Zhuiri Peng[1], Runfeng Lin[1], Zheng Li[1], Yilun Wang[1], Xinyu Huang[1], Kan-Hao Xue[1], Hangyu Xu[2], Feng Liu[3], Hui Xia[2], Peng Wang[2], Mingsheng Xu[4], Wei Xiong[1], Weida Hu[2]*, Jianbin Xu[5], Xinliang Zhang[1], Lei Ye[1]*, Xiangshui Miao[1]

In neuromorphic hardware, peripheral circuits and memories based on heterogeneous devices are generally physically separated. Thus, exploration of homogeneous devices for these components is key for improving module integration and resistance matching. Inspired by the ferroelectric proximity effect on two-dimensional (2D) materials, we present a tungsten diselenide–on–lithium niobate cascaded architecture as a basic device that functions as a nonlinear transistor, assisting the design of operational amplifiers for analog signal processing (ASP). This device also functions as a nonvolatile memory cell, achieving memory operating (MO) functionality. On the basis of this homogeneous architecture, we also investigated an ASP-MO integrated system for binary classification and the design of ternary content-addressable memory for potential use in neuromorphic hardware.

Recently proposed diverse neuron-inspired hardware based on various emerging nanomaterials has effectively advanced neural networks (*1*–*6*), especially for two-dimensional (2D) materials. 2D materials can provide a platform to develop transistor architectures for memory operating (MO)—including field-effect transistors (FETs), tunneling transistors, junction transistors, ferroelectric (FE) transistors, and ferromagnetic transistors—owing to their rich electrostatic control capabilities (*1*, *7*). 2D materials–based FE FETs, FE bipolar junction transistors (BJTs), and FE tunneling transistors exhibit large on-off resistance ratios, fast operation, low power consumption, nonvolatile electronic control, and weight updates under reversible polarization (*1*) because of the strong proximal coupling of FE materials with 2D materials. Therefore, these 2D materials–based FE proximal coupled devices are being intensively investigated for neuromorphic computing (*1*, *4*), in which they are used as memories by dynamically modulating the FE polarization to program the conductivity of superjacent 2D channels (*8*, *9*). Achieving computing tasks requires these memories to be integrated with peripheral circuits, because analog signal processing (ASP) is essential before and after MO (*2*). However, peripheral circuits are generally based on complementary metal-oxide semiconductor (CMOS) transistors, and thus the heterogeneous architectures between memory cells and peripheral circuits lead to their physical separation, making it necessary to consider module integration compatibility issues for chip design (*2*). In addition, an emerging challenge regards how to achieve efficient resistance matching between heterogeneous device architectures as device dimensions are scaling down, which may hinder the pursuit of higher performance and energy efficiency (*10*). Therefore, it is crucial to explore the integration between ASP and MO.

Designing an ASP-MO integrated system with a homogeneous device architecture for peripheral circuits and memory cells offers the potential to relieve the above-mentioned issues, which can also be realized by the mechanism of 2D-FE proximal coupling. On the one hand, FE polarization proximity-induced nonvolatile electronic gating in 2D materials enables the design of nonlinear transistors, including p-n diodes and BJTs (*8*, *11*–*16*). On the other hand, FE polarization can modulate the built-in potential in BJTs (*17*), enabling nonvolatile memory functionalities with an improved on-off resistance ratio. Moreover, the reconfigurable FE polarization domains can seamlessly manipulate arrayed doping domains in 2D materials, showing potential for the fabrication of massive cascaded devices with enhanced compactness. Therefore, a homogeneous, 2D material–based FE proximal coupled BJT architecture is proposed to design peripheral circuits for ASP, as well as nonvolatile memory cells for MO, enabling development of an ASP-MO integrated system.

In this work, seamlessly arrayed periodically polarized $LiNbO_3$ (LNO) domains formed a grating-like structure (fig. S1), which effectively tailored the WSe_2 channels into seamlessly arrayed junctions. ASP, MO, and their corresponding cascade were investigated to demonstrate the success of an integrated system based on the same device architecture, which included a WSe_2 channel crossing three FE domains. Our operational amplifier (OPAMP) was designed for ASP (*18*), and memory cells with encoded synapse weights were cascaded with the OPAMP to demonstrate the applicability in binary classification (*19*). Furthermore, ternary content-addressable memory (TCAM) with a two-transistor-two-resistor (2T2R) configuration was designed with the homogeneous transistor-memory architecture, yielding a ratio of 898.4 between the high-resistance state (HRS) and the low-resistance state (LRS). Such an integrated system architecture could provide a feasible approach to solve the heterogeneous issue and improve neuromorphic applications.

Few-layer WSe_2 flakes were exfoliated and transferred onto LNO to demonstrate the reconfigurable electronic functionalities under FE proximal coupling (WSe_2 characterization and optical images are shown in fig. S1). The basic device functioned as a nonlinear transistor when the domain polarization state was fixed under zero gate voltage (V_g) (Fig. 1A), as the FE proximal coupling induces carrier doping in the WSe_2 (Fig. 1B). This doping mechanism was indicated by the Kelvin probe force microscopy (KPFM) mapping shown in fig. S1C, where the higher (or lower) surface potential induced by the polarization-down (P_d) [or polarization-up (P_u)] domain was in accordance with the p-doping (or n-doping) nature (*8*). Transfer curves for the intrinsic WSe_2 and FE-doped WSe_2 FETs are shown in fig. S1L. The neutral point shifts were 3.8 and −6.2 V for the P_d and P_u domains, respectively, corresponding to a hole doping density of 2.07×10^{12} cm^{-2} and an electron doping density of 3.37×10^{12} cm^{-2}. This doping character induced a built-in potential of ~0.43 eV and a depletion width (w) of 48.25 nm (fig. S1M) (*20*). For a basic n-p-n BJT on the P_u-P_d-P_u domains, current amplifications were measured under the base, collector, and emitter voltage control. The common-base configuration in Fig. 1E showed an average gain of $\alpha = \frac{I_c}{I_e} = 0.979$ (I_c, collector current; I_e, emitter current) for the active region, and the common-emitter configuration in Fig. 1F showed a maximum gain of $\beta = \frac{I_c}{I_b} = 11.2$ (I_b, base current), offering the capability to design analog circuits. More details about signal rectification, amplification, and performance uniformity are shown in figs. S2 to S5.

The basic device could also operate as a nonvolatile memory (Fig. 1C), the mechanism of which differs from those of conventional FE-FET and MemFlash (*1*, *4*, *21*). The FE

[1]Wuhan National Laboratory for Optoelectronics, School of Optical and Electronic Information, Huazhong University of Science and Technology, Wuhan, Hubei 430074, China. [2]State Key Laboratory of Infrared Physics, Shanghai Institute of Technical Physics, Chinese Academy of Sciences, Shanghai 200083, China. [3]School of Power and Mechanical Engineering, Wuhan University, Wuhan, Hubei 430072, China. [4]School of Micro-Nano Electronics, State Key Laboratory of Silicon Materials, Zhejiang University, Hangzhou 310027, China. [5]Department of Electronic Engineering, Materials Science and Technology Research Center, The Chinese University of Hong Kong, Hong Kong, China.
*Corresponding author. Email: wdhu@mail.sitp.ac.cn (W.H.); leiye@hust.edu.cn (L.Y.)

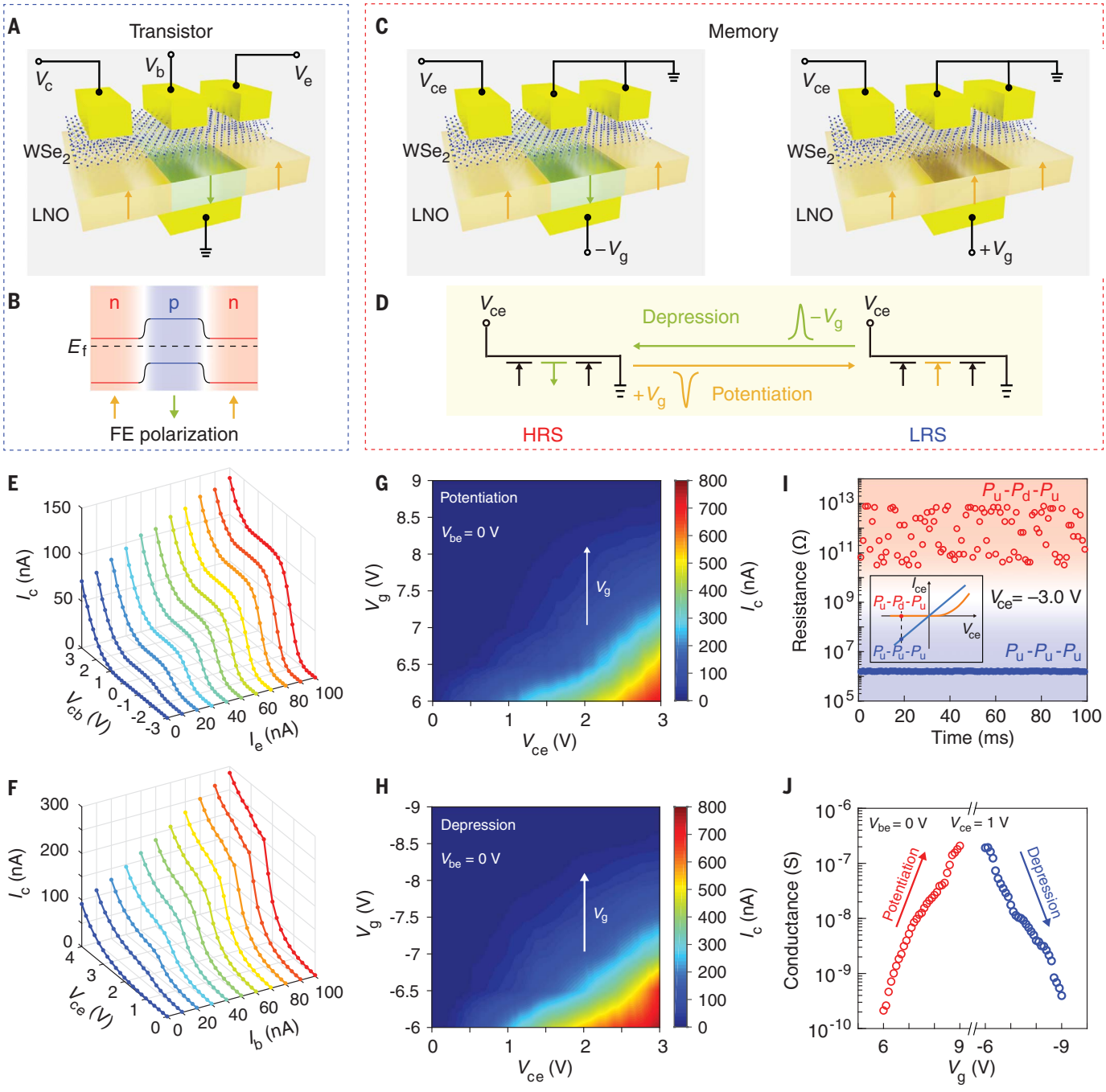

Fig. 1. Basic device and performance mechanism. (**A**) Schematic of the basic device with a homogeneous transistor-memory architecture for nonlinear transistor functionality. (**B**) Mechanism of FE proximity-induced doping in the basic device. E_f, Fermi energy. (**C**) Schematic of the basic device with a homogeneous transistor-memory architecture for the memory functionality. (**D**) Mechanism of potentiation and depression in the basic device, in which the LRS and HRS were controlled by changing the FE polarization state of the base under a positive and negative gate voltage, respectively. (**E** and **F**) Transistor functionality with common-base (E) and common-emitter (F) configuration. (**G**) Current rectification for the potentiation process, for which V_g ranged from 6 to 9 V with a step of 0.5 V. (**H**) Current rectification for the depression process, for which V_g ranged from −6 to −9 V with a step of 0.5 V. (**I**) Channel resistance for the FE polarization state of P_u-P_d-P_u and P_u-P_u-P_u under the driving voltage of V_{ce} = −3 V and V_{be} = 0 V. The inset shows a schematic of the measured current. (**J**) Conductance update for the potentiation and depression with a V_g step of 0.1 V and a width of 1 s. The drive voltages were V_{ce} = 1 V and V_{be} = 0 V.

polarization state was fixed to be P_u for the collector and emitter, and the HRS and LRS were dominated by the built-in potential (*17*), which was controlled by V_g for the base. In the potentiation (or depression) process, a positive V_g from 6 to 9 V (or a negative V_g from −6 to −9 V) changed the FE polarization state for the base to P_u (or P_d), resulting in a low built-in potential with enhanced channel conductance (or a high built-in potential with reduced channel conductance) (Fig. 1D) (*21*, *22*). The mechanism was indicated from

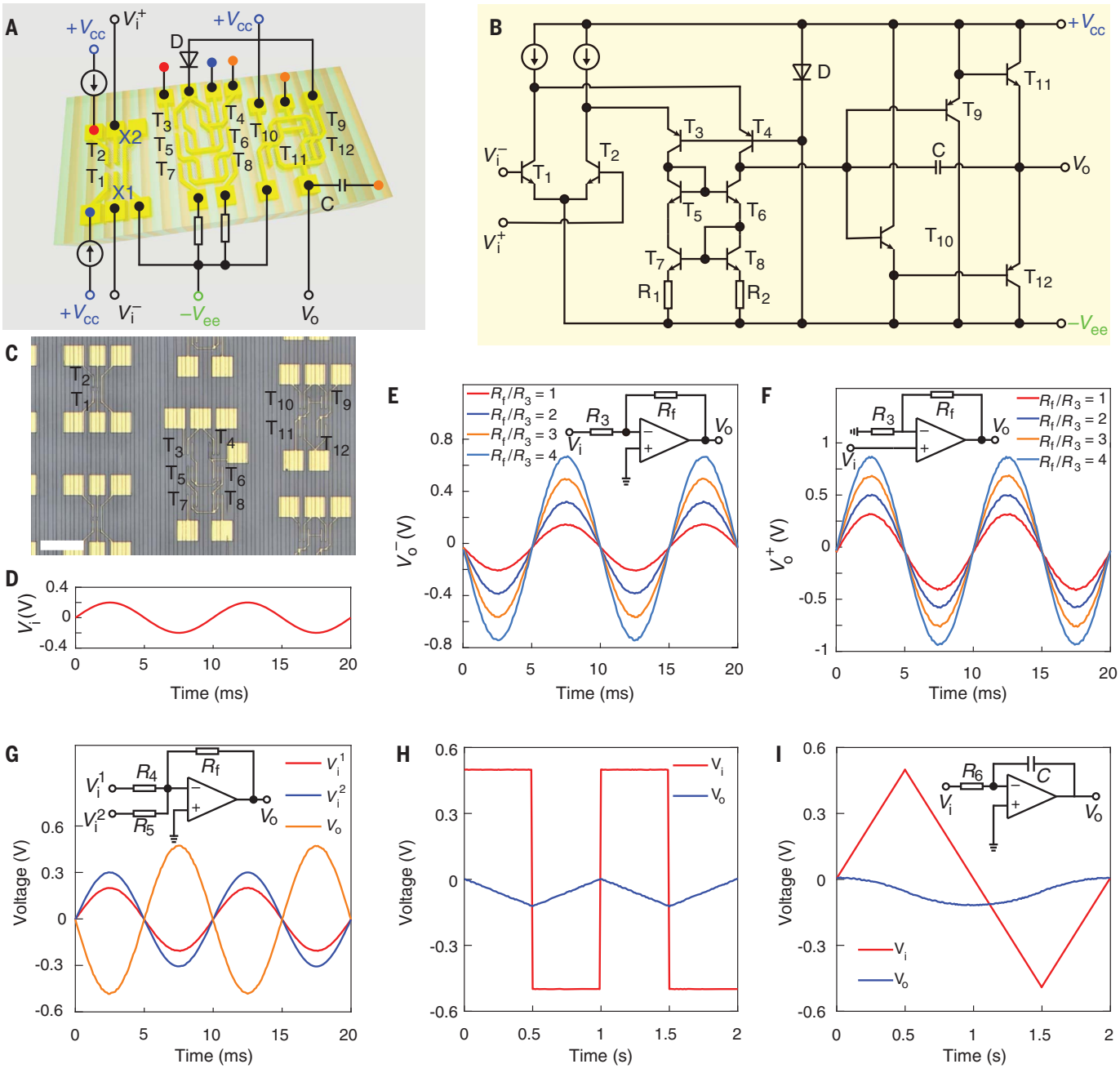

Fig. 2. OPAMP for ASP. (**A** and **B**) Experimental setup (A) and electric circuit (B) of the OPAMP. T_1 to T_{12}, BJTs; D, cascaded diode; C, cascaded capacitance. (**C**) Optical image of the OPAMP. Scale bar, 100 μm. (**D** to **F**) Analog signal inputted at one port (D). Inverted (E) and noninverted (F) output of the OPAMP, with the circuit schematics shown in the insets. (**G**) Analog input and output signals for the addition operation. The inset shows the schematic of the addition calculation. (**H**) Analog integral calculation for a square-shaped input signal and the corresponding triangle-shaped output signal. (**I**) Analog integral calculation for a triangle-shaped input signal and the approximately sinusoidal output signal. The inset shows the schematic of the integral calculation.

the modulated current rectifications under the collector-emitter voltage (V_{ce}) sweep for the potentiation (Fig. 1G) and depression (Fig. 1H) processes, respectively [base-emitter voltage (V_{be}) = 0 V; V_g step of 0.5 V]. This rectification behavior can provide a high resistance ratio between the HRS and LRS. In contrast to the conventional FE-FET structure with the WSe_2 channel placed on a single FE domain (fig. S6), the resistance for the FE polarization state of P_u-P_d-P_u and P_u-P_u-P_u showed an average resistance ratio of ~10^6 under driving voltages of V_{ce} = −3 V, V_{be} = 0 V, and V_g = 0 V (Fig. 1I). Moreover, as an artificial synapse, the conductance update for the potentiation or depression process with a V_g step of 0.1 V under V_{ce} = 1 V and V_{be} = 0 V (Fig. 1J) was encoded as a synapse weight (fig. S7A), and the on-off resistance ratio was ~10^3. The stable memory performance is shown in fig. S7 for measurements of multiple cycles, and the memory performances were compared with those from other studies of diverse memory architectures (table S1). The few-layer WSe_2

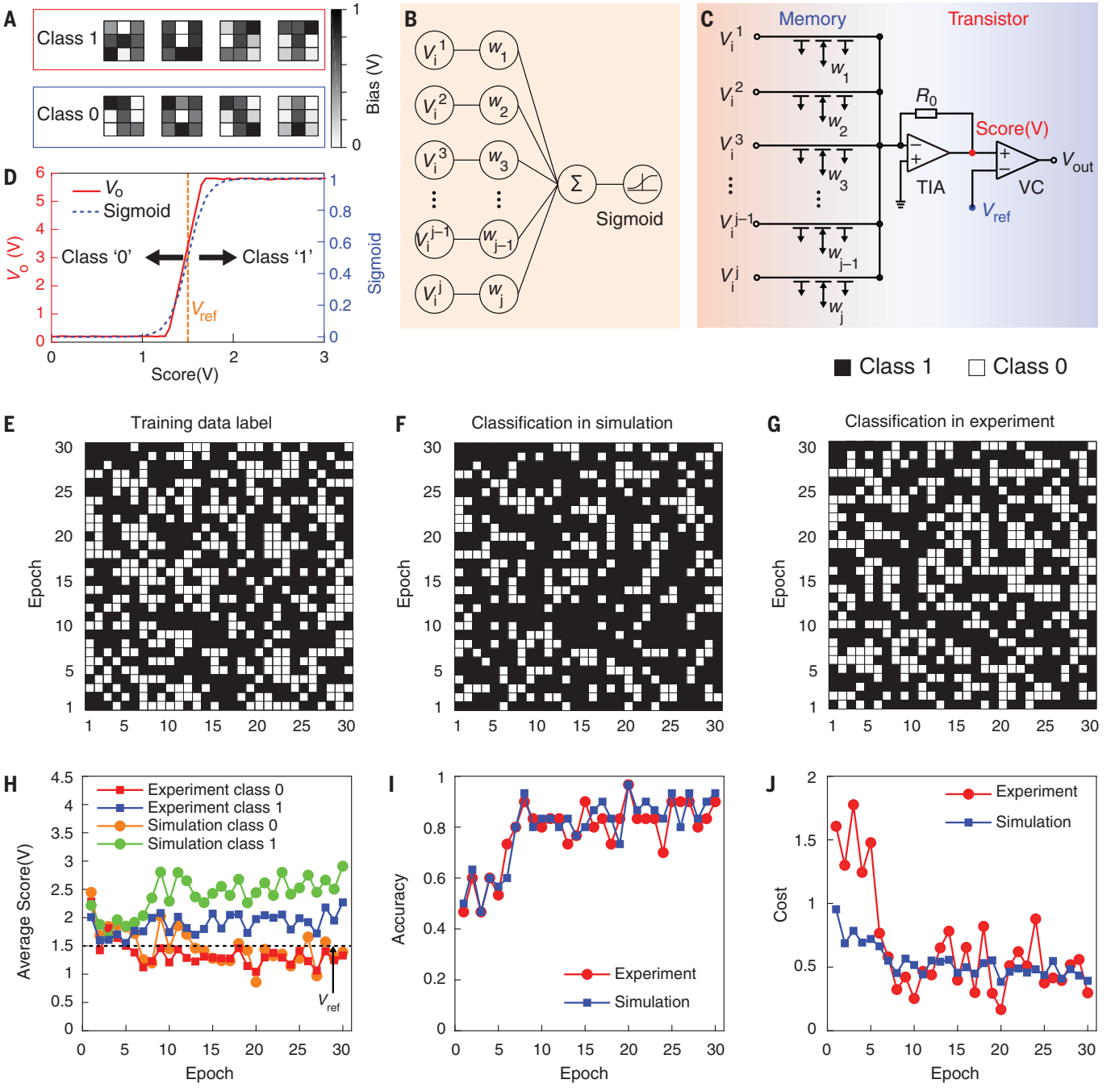

Fig. 3. ASP-MO integration for binary classification. (**A**) Class 1 with letter patterns H, U, S, and T and class 0 with number patterns 2, 0, 2, and 1. (**B**) Schematic of the classification with the sigmoid activation function. (**C**) Schematic of the circuit diagram, where the memory cells were integrated with the TIA and VC. (**D**) Output character of the VC (solid red curve), which was similar to the sigmoid function (dashed blue curve). (**E** to **G**) Training dataset label (E), predicted class in the simulation (F), and predicted class in the experiment (G). (**H** to **J**) Average Score(V) (H), accuracy (I), and cost (J) for the training process in the simulation and experiment.

film grown by chemical vapor deposition was then transferred and patterned on LNO to fabricate an ASP-MO integrated system.

The OPAMP was designed by cascading multiple basic devices for ASP (Fig. 2, A to C) (*18*), with the input electrodes designated X1 and X2. The dc driving voltages were collector voltage (V_{cc}) = emitter voltage (V_{ee}) = 6 V, the resistances were $R_1 = R_2 = 10$ megohms, the capacitance (C) was 1 μF, and the input bias current was varied between 30 and 50 nA to adjust the performance. The OPAMP characteristics were discussed and compared with those of previously reported CMOS-based devices (table S2). We applied an ac input signal $V_i = 0.2\sin 200\pi \times t$ (t, time) (Fig. 2D) at only one input port, and the other port was grounded. The output signal V_o^- was inverted when the signal was input at port X1 (Fig. 2E), the output V_o^+ was noninverted when the signal was input at port X2 (Fig. 2F), and the

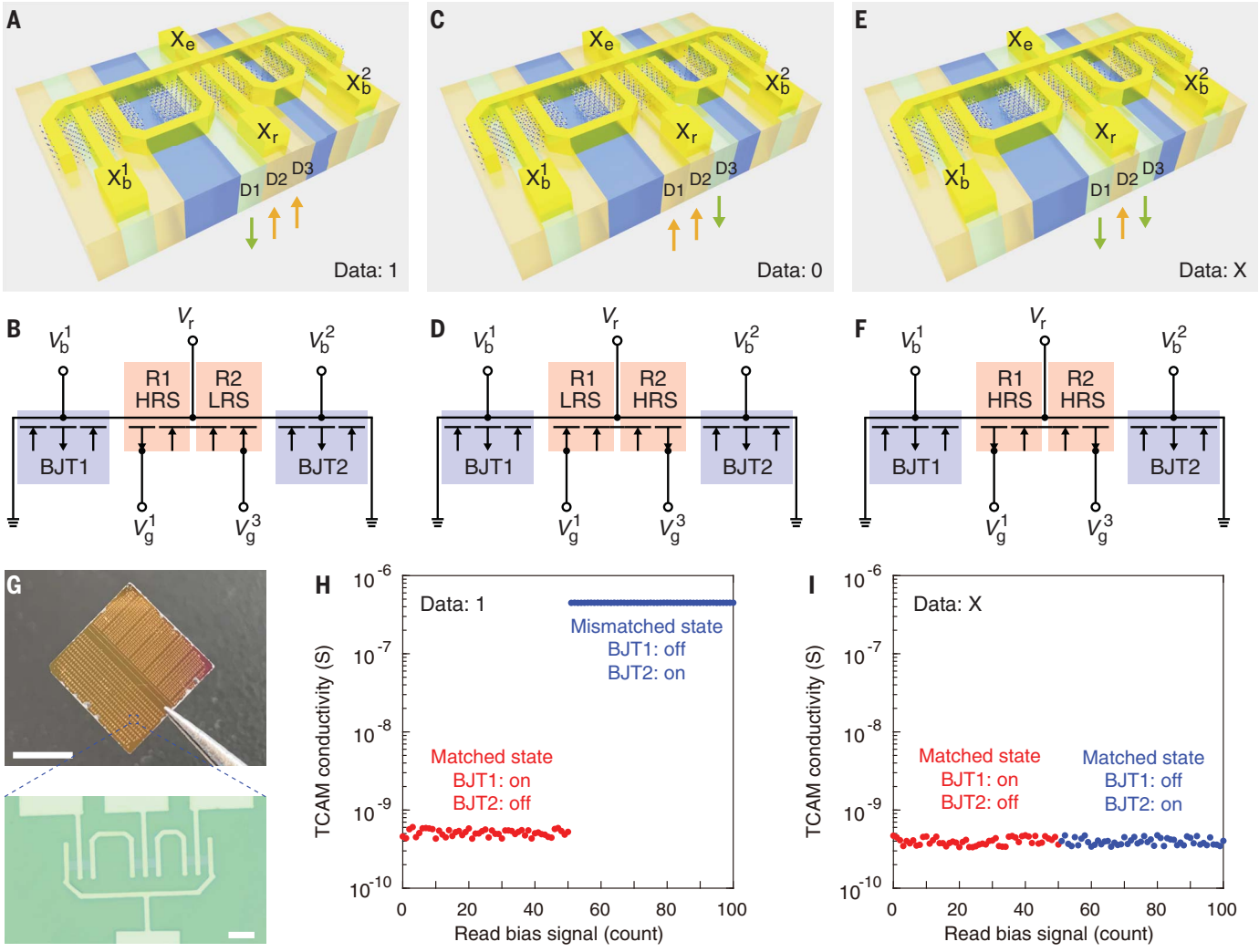

Fig. 4. TCAM cell with a 2T2R configuration based on the homogeneous transistor-memory architecture. (**A** and **B**) Schematics of the TCAM cell with bit data 1. (**C** and **D**) Schematics of the TCAM cell with bit data 0. (**E** and **F**) Schematics of the TCAM cell with bit data X. (**G**) Photograph and optical image of a TCAM cell. Photograph scale bar, 5 mm; optical image scale bar, 20 μm. (**H**) Reading of the TCAM cell with bit data 1. The TCAM cell was in the matched state (or mismatched state) with BJT1 on and BJT2 off (or BJT1 off and BJT2 on). (**I**) Reading of the TCAM cell with bit data X. The TCAM cell was always in the matched state, regardless of whether BJT1 and BJT2 were on or off.

voltage gain was related to the ratio R_f/R_3. For the addition operation, port X2 was grounded, and both input signals were cascaded to port X1, with a resistance (R_f) for negative feedback. The two ac input signals $V_i^1 = 0.2\sin 200\pi \times t$ and $V_i^2 = 0.3\sin 200\pi \times t$ and the output signal V_o are shown in Fig. 2G. Under the condition of $R_f = R_4 = R_5 = 2$ megohms, the output signal was $-V_o = V_i^1 + V_i^2$. When a capacitance was used for negative feedback, the OPAMP achieved the integral calculation with a time constant of $\tau = R_6C = 2$ s ($R_6 = 2$ megohms, $C = 1$ μF). The square input signal V_i and the corresponding integrated output signal $V_o = -\frac{V_i}{RC}t$ are shown in Fig. 2H. The triangle-shaped input signal and the approximately sine wave–shaped integrated output signal are shown in Fig. 2I.

On the basis of the reconfigurable functionalities, the ASP-MO integrated system was used to demonstrate the proof of principle for binary classification (*23*, *24*). The input three pixel–by–three pixel patterns for the letters H, U, S, and T were labeled as class 1, and those for the numbers 2, 0, and 1 were labeled as class 0 (Fig. 3A shows eight randomly selected patterns; and the entire training dataset is shown in fig. S8). The calculation schematic and circuit diagram are shown in Fig. 3, B and C, respectively. The pixels were coded into nine input voltages (V_{ce}) to calculate the weighted average current (Eq. 1) in nine memory cells. The weighted average current was converted into a voltage Score(V) in the transimpedance amplifier (TIA) (*19*, *25*), with a resistance (R_0) of 10 megohms. The nonlinear output voltage (Eq. 2) was processed by the voltage comparator (VC) with a reference voltage (V_{ref}) of 1.5 V, which was similar to the sigmoid function (Fig. 3D)

$$\text{Score(V)} = w_0 + w_1V_i^1 + w_2V_i^2 + w_3V_i^3 + \ldots + w_jV_i^j \quad (1)$$

$$V_{out} = \begin{cases} V_{cc}, & \text{Score(V)} > V_{ref} \\ V_{ee}, & \text{Score(V)} < V_{ref} \end{cases} \quad (2)$$

The drive voltages were V_{cc} (6 V) and V_{ee} (0 V), and the conductance was updated after calculating the cross-entropy cost for each batch, as summarized in fig. S9, C and D. The system was trained for 30 epochs, after which the

pattern label and predicted classes in the simulations and experiments were elucidated (Fig. 3, E to G, respectively). Score(V) is summarized in fig. S9, E and F; the average Score(V) values of classes 0 and 1, which are separated by V_{ref}, are depicted in Fig. 3H. The accuracy and cost are shown in Fig. 3, I and J. The performance was mainly limited by the output characteristics of the VC and the non-negative weight in the hardware. Analogous to conventional FE memristors, this ASP-MO integrated system could be useful for other neuromorphic algorithms, although such investigation is beyond the scope of this work.

TCAM is promising for the parallel search of massive datasets in in-memory computing (*26*, *27*), and TCAM cells with a 2T2R configuration can be constructed on the basis of homogeneous transistor-memory architecture (schematics of the mechanism are shown in Fig. 4, A to F). In our design, the TCAM cell included three WSe_2 channels on nine separated FE domains, with four terminals marked as the emitter electrode (X_e), read electrode (X_r), and base electrodes ($X_b{}^1$ and $X_b{}^2$). Three central domains, designated D1 to D3, formed two memories, with memory R1 across D1 and D2 and memory R2 across D2 and D3. The polarization state of D2 was fixed at P_u; thus, R1 (or R2) was in an HRS when the V_g of –9 V changed D1 (or D3) to P_d and was in an LRS when the V_g of 9 V changed D1 (or D3) to P_u. Moreover, R1 and R2 were connected with two BJT switches, which were switched on (or off) at a base voltage of $V_b{}^1 = V_b{}^2 = 3$ V (or $V_b{}^1 = V_b{}^2 = -3$ V) (Fig. 4, B, D, and F). X_e was grounded, and V_r (5 V) was loaded at X_r for the address search function.

The bit data 1 (or 0) in the TCAM cell was defined when R1 was in the HRS and R2 was in the LRS (or R1 in the LRS and R2 in the HRS). The matched state exhibited a low conductance for the address read at X_r and thus bit data 1 was searched by switching on BJT1 and switching off BJT2 (Fig. 4, A and B). Bit data 0 was searched by switching off BJT1 and switching on BJT2 (Fig. 4, C and D). Otherwise, the TCAM cell was in the mismatched state with a high conductance. For bit data 1, the average conductance was ~0.5 nS (where 1 S = 1 A/V) for the matched state and ~449.5 nS for the mismatched state, with an average conductance ratio $r_c = \frac{C_{high}}{C_{low}} = 899$ (Fig. 4H). The TCAM cell with an unknown bit (designated bit X) was always in the matched state, because both R1 and R2 were in the HRS (Fig. 4, E and F), with an average conductivity of ~0.4 nS (Fig. 4I). The cumulative probability was analyzed in fig. S10.

In addition to binary classification and TCAM design, the basic device should be suitable for various applications, including digital computing (fig. S11) and artificial neural systems with optical sensing abilities (fig. S12) (*28*, *29*). The basic device should also be applicable for the design of analog-to-digital converters, digital-to-analog converters, and analog filters (*2*). The device size can be reduced by scaling down the polarization domain size, which will improve the current gain and integration density. A lower coercive voltage would be helpful for achieving a lower power consumption, which can be attained by reducing the LNO thickness or using other FE materials. Finally, inspired by conventional CMOS-based chips, we have proposed a neuromorphic ASP-MO 3D stacking system derived from 2D integration (fig. S13). The main challenge lies in the growth of wafer-scale, high-quality 2D materials, and recent works have achieved promising breakthroughs to overcome this challenge (*30*). Thus, this homogeneous transistor-memory architecture will help to promote analogous neuromorphic systems on-chip.

REFERENCES AND NOTES

1. C. Liu *et al*., *Nat. Nanotechnol.* **15**, 545–557 (2020).
2. Q. Xia, J. J. Yang, *Nat. Mater.* **18**, 309–323 (2019).
3. L. Danial *et al*., *Nat. Electron.* **2**, 596–605 (2019).
4. D. Ielmini, H. P. Wong, *Nat. Electron.* **1**, 333–343 (2018).
5. W. Zhang *et al*., *Nat. Electron.* **3**, 371–382 (2020).
6. A. Sebastian, M. Le Gallo, R. Khaddam-Aljameh, E. Eleftheriou, *Nat. Nanotechnol.* **15**, 529–544 (2020).
7. M. I. B. Utama *et al*., *Nat. Electron.* **2**, 60–65 (2019).
8. G. Wu *et al*., *Nat. Electron.* **3**, 43–50 (2020).
9. X. Wang *et al*., *Nat. Commun.* **12**, 1109 (2021).
10. P. Kapur, J. P. McVittie, K. C. Saraswat, *IEEE Trans. Electron Dev.* **49**, 590–597 (2002).
11. L. Lv *et al*., *Nat. Commun.* **10**, 3331 (2019).
12. C. Baeumer *et al*., *Nat. Commun.* **6**, 6136 (2015).
13. J.-W. Chen *et al*., *Nat. Commun.* **9**, 3143 (2018).
14. H. Lu *et al*., *Nat. Commun.* **5**, 5518 (2014).
15. N. Park *et al*., *ACS Nano* **9**, 10729–10736 (2015).
16. H. Mulaosmanovic, E. T. Breyer, T. Mikolajick, S. Slesazeck, *Nat. Electron.* **3**, 391–397 (2020).
17. Z. Xiao, J. Song, D. K. Ferry, S. Ducharme, X. Hong, *Phys. Rev. Lett.* **118**, 236801 (2017).
18. D. K. Polyushkin *et al*., *Nat. Electron.* **3**, 486–491 (2020).
19. L. Mennel *et al*., *Nature* **579**, 62–66 (2020).
20. B. Wen *et al*., *ACS Nano* **13**, 5335–5343 (2019).
21. M.-K. Kim, J.-S. Lee, *Nano Lett.* **19**, 2044–2050 (2019).
22. S. Boyn *et al*., *Nat. Commun.* **8**, 14736 (2017).
23. S. Ambrogio *et al*., *Nature* **558**, 60–67 (2018).
24. S. Seo *et al*., *Nat. Commun.* **11**, 3936 (2020).
25. C. Li *et al*., *Nat. Electron.* **1**, 52–59 (2018).
26. K. Ni *et al*., *Nat. Electron.* **2**, 521–529 (2019).
27. R. Yang *et al*., *Nat. Electron.* **2**, 108–114 (2019).
28. L. Tong *et al*., *Nat. Commun.* **11**, 2308 (2020).
29. C. Y. Wang *et al*., *Sci. Adv.* **6**, eaba6173 (2020).
30. X. Xu *et al*., *Science* **372**, 195–200 (2021).
31. L. Tong *et al*., 2D materials-based homogeneous transistor-memory architecture for neuromorphic hardware, version 1.0, Zenodo (2021); https://doi.org/10.5281/zenodo.5163973.

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SUPPLEMENTARY MATERIALS

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2D materials–based homogeneous transistor-memory architecture for neuromorphic hardware

Lei TongZhuiri PengRunfeng LinZheng LiYilun WangXinyu HuangKan-Hao XueHangyu XuFeng LiuHui XiaPeng WangMingsheng XuWei XiongWeida HuJianbin XuXinliang ZhangLei YeXiangshui Miao

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Memory and logic in the same device

Future artificial intelligence applications and data-intensive computations require the development of neuromorphic systems beyond traditional heterogeneous device architectures. Physical separation between a peripheral signal-processing unit and a memory-operating unit is one of the main bottlenecks of heterogeneous architectures, blocking further improvements in efficient resistance matching, energy consumption, and integration compatibility. Tong *et al*. present a transistor-memory architecture based on a homogeneous tungsten selenide-on-lithium niobate device array (see the Perspective by Rao and Tao). Analog peripheral signal preprocessing and nonvolatile memory were possible within the same device structure, promising diverse neuromorphic functionalities and offering potential improvements in neuromorphic systems on-chip. —YS