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Santa Barbara

Ultra High Speed InGaAs / InP DHBT Devices and Circuits

A dissertation submitted in partial satisfaction of the
requirements for the degree of

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in

Electrical and Computer Engineering

by

Zachary M. Griffith

Committee in charge:

Professor Mark Rodwell, Chair
Professor Umesh Mishra
Professor Evelyn Hu
Professor Steve Long

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UMI Number: 3187230

ProQuest Information and Learning Company
300 North Zeeb Road
P.O. Box 1346
Ann Arbor, MI 48106-1346

The dissertation of Zachary M. Griffith is approved:

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Chair

August 2005

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Zachary M. Griffith

Curriculum Vitæ

Zachary M. Griffith

EDUCATION

Bachelor of Science in Electrical Engineering
University of California, Santa Barbara, March 2001
Master of Science in Electrical Engineering
University of California, Santa Barbara, December 2001
Doctor of Philosophy in Electrical Engineering
University of California, Santa Barbara, August 2005

PROFESSIONAL EMPLOYMENT

1999 - 2005 Research assistant, Dept. of Electrical and Computer Engineering, University of California, Santa Barbara
1999, 2000 Summer intern, Conexant Systems Inc., Newbury Park, CA

FIELDS OF STUDY

Major Field: Design and fabrication of highly scaled, ultra high speed InP based double heterojunction bipolar transistors (DHBTs) and small scale circuits.

PUBLICATIONS

Z. Griffith, Y. Dong, D. Scott, Y. Wei, N. Parthasarathy, M. Dahlström, C. Kadow, V. Paidi, M.J.W. Rodwell, M. Urteaga, R. Pierson, P. Rowell, B. Brar, S. Lee, N. Nguyen, and C. Nguyen, "Transistor and Circuit Design for 100-200 GHz ICs", *IEEE Journal of Solid-State Circuits*, vol. 40, no. 10, 2005.

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Abstract

Ultra High Speed InGaAs / InP DHBT Devices and Circuits

by

Zachary M. Griffith

This work examines the efforts pursued through vertical and lateral scaling to increase the bandwidth of InP based DHBTs. Through process development, device performance has improved from lateral scaling and reduced contact resistances. A high-yield 0.5 μm narrow mesa emitter junction technology has been realized. The contact resistivity ρ_c for the emitter, base, and collector layers has been reduced to less than 10 $\Omega \cdot \mu$m^2, a 2:1 improvement. With this base-contact ρ_c and a typical base sheet $\rho_s \cong 600\ \Omega/\square$, the metal-semiconductor transfer length L_t has been reduced to 120 nm, and 0.3 μm base contacts have been realized. This has substantially reduced the extrinsic C_{cb} with minimal increase to the base resistance R_{bb}.

The reductions to the extrinsic capacitive and resistive parasitics allow the active collector thickness T_c to be thinned for increased device bandwidth. To achieve minimum C_{cb}/I_c ratio as T_c is reduced, the maximum current density will increase $J_e = J_{Kirk} \propto T_c^{-2}$. The power density will similarly increase $P = I_c \cdot V_{ce} = J_e A_e \cdot V_{ce}$. Improved device heat-sinking to the high thermally-conductive InP substrate for reduced HBT thermal resistance θ_{JA} (K$\cdot\mu$m^2/mW) must be considered during HBT

design to prevent excessive device self-heating as the operating power density increases. For the device improvements discussed, the follow results have ensued from each collector scaling generation:

T_c = 210 nm $\rightarrow$ f_τ/f_{max} = 276/451 GHz, T_c = 150 nm $\rightarrow$ f_τ/f_{max} = 391/505 GHz,

T_c = 120 nm $\rightarrow$ f_τ/f_{max} = 450/490 GHz, T_c = 100 nm $\rightarrow$ f_τ/f_{max} = 491/415 GHz.

Static frequency dividers were designed and fabricated utilizing an HBT with a collector thickness of 150 nm. The amount of ΔV_{logic} consumed by the parasitic emitter resistance was the scaling limit for these circuits. A dense wiring scheme is utilized to reduce interconnect delays, and the signal integrity was maintained through the use of a low-ε_r, thin-film microstrip environment. Divide-by-2 designs fabricated at GCS and UCSB had a maximum toggle rate of $f_{clk,max}$ = 153 GHz and 142 GHz, respectively.

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1 Introduction

DESPITE formidable progress in CMOS, bipolar transistors remain competitive due to the larger breakdown voltages obtainable and the larger lithographic feature sizes required for a transistor at a given bandwidth. Compared to the SiGe material system, InP heterojunction bipolar transistors (HBTs) have $\approx$ 3.5:1 higher collector electron velocity and $\approx$ 10:1 higher base electron diffusivity. Consequently, at the same scaling generation InP HBTs would have $\approx$ 3:1 greater bandwidth than SiGe HBTs. Today the maturity of advanced silicon processes has enabled SiGe HBTs to be fabricated with 100 nm emitter junctions with minimal extrinsic parasitics, while efforts to aggressively scale InP HBTs are described in this work. With that, SiGe HBTs have demonstrated simultaneous 300 GHz f_τ and 350 GHz f_{max} [1] and 102 GHz static frequency dividers [2], while InP DHBTs from UCSB have obtained simultaneous 450 GHz f_τ and 490 GHz f_{max} [3], 176 GHz power amplifiers with 5-dB power gain [4], and $>$ 150 GHz static frequency dividers [5]. Consequently, the two technologies today have comparable bandwidth,

with SiGe offering much higher levels of integration. Continued bandwidth improvement and increased integration of InP HBTs requires careful consideration be given to scaling laws and limits, and the requirements placed upon transistor design for wideband circuits must be clearly understood [6, 7].

The InP HBTs described in this work utilize a triple-mesa structure. Collector, base, and emitter layers are grown atop of each other and device layers are isolated by mesa formation once electrical contacts have been made. Under bias, the carriers are swept vertically across the emitter, base, and collector by their respective transport mechanisms to realize transistor behavior. The dominant delay associated with the electrons traversing the HBT layers is the base and collector transit times, $\tau_b + \tau_c = \tau_f$. Because mesa HBTs are a vertical transport device, the unity current gain frequency $f_\tau \approx (2\pi\tau_f)^{-1}$ will increase by thinning the active base and collector layers through growth. However, the resistances associated with the ohmic contacts, the link resistances between the contacts and active layers, and the extrinsic base-collector capacitance $C_{cb,ex}$ underneath the base contact (a consequence of the mesa device topology, needed to supply bias to the base terminal of the HBT) must be similarly scaled. If they are not, the maximum oscillation frequency f_{max} will decrease significantly, the C_{cb}/I_c ratio (a digital IC figure of merit for HBTs) will increase, and no benefit from epitaxial scaling will be realized.

This thesis is separated into two parts. The first details design, scaling and fabri-

cation challenges addressed in this work. In Chapter 2 the mesa HBT technology is described. Scaling laws for increasing HBT and digital IC bandwidth, and physical limits to scaling are presented. Advanced process modules for continued increases to HBT bandwidth are briefly discussed – they include collector pedestal implants for reduced C_{cb} and regrown-emitter junctions for reduced R_{ex} and R_{bb}. Chapter 3 summarizes the fabrication efforts undertaken to aggressively scale the mesa HBT footprint and its parasitics. A high-yield 0.5 μm narrow mesa emitter junction technology has been realized. The contact resistivity ρ_c for the emitter, base, and collector layers has been reduced to less than 10 $\Omega \cdot \mu$m^2. With this base-contact ρ_c and a typical base sheet $\rho_s \cong 600\ \Omega/\Box$, the metal-semiconductor transfer length L_t is $\sim$ 120 nm. When combined with i-line stepper lithography having less than 150 nm registration error and collector undercut during mesa formation $\sim$ 150 nm, 0.3 μm base contacts have been realized. This has substantially reduced the $C_{cb,ex}$ with minimal increase to the base resistance R_{bb}. Device performance has thus increased at the same epitaxial scaling generation.

The reductions to the extrinsic capacitive and resistive parasitics have allowed the active collector thickness T_c to be thinned for increased device bandwidth. To achieve minimum C_{cb}/I_c ratio as T_c is reduced, the maximum current density will increase $J_e = J_{Kirk} \propto T_c^{-2}$. The power density will similarly increase $P = I_c \cdot V_{ce} = J_e A_e \cdot V_{ce}$. Improved device heat-sinking to the high thermally-conductive InP

substrate for reduced HBT thermal resistance θ_{JA} (K·μm^2/mW) must be considered during HBT design to prevent excessive device self-heating as the operating power density increases. A barrier to heat flow from the active collector region to the InP substrate is a thin layer of low-thermally conductive $\mathrm{In_{0.53}Ga_{0.47}As}$. This layer provides low contact resistance ρ_c for the InP sub-collector. In this work, this layer has been progressively thinned from 25 nm to 6.5 nm to minimize θ_{JA}, without significantly increasing ρ_c.

The second part of this thesis reports discrete InP DHBT performance and static frequency divider designs from UCSB. Chapter 4 presents many device results of varying collector thicknesses, they include,

T_c = 210 nm $\rightarrow$ f_τ/f_{max} = 276/451 GHz, T_c = 150 nm $\rightarrow$ f_τ/f_{max} = 391/505 GHz,

T_c = 120 nm $\rightarrow$ f_τ/f_{max} = 450/490 GHz, T_c = 100 nm $\rightarrow$ f_τ/f_{max} = 491/415 GHz.

Calibration methods used to make on-wafer and off-wafer network analyzer measurements to 110 GHz are discussed. In addition to demonstrating high bandwidths, these HBTs showed very low-leakage currents $\sim$ 100 pA and could operate to a power density of 20 mW/μm^2 before failure. This is the first work to present such devices. Chapter 5 reports static frequency dividers (digital benchmark circuits for a device technology) designed and fabricated utilizing an HBT with a collector thickness of 150 nm. The devices within the circuits were biased at or close to J_{Kirk} to minimize the dominant gate delay term $\tau = C_{cb}\Delta V_l/I_c$. The amount of logic

swing consumed by the emitter resistance $\Delta V_{parasitic}$ was the HBT scaling limit for these circuits. A dense wiring scheme is used to reduce interconnect delays, and the signal integrity was maintained through the use of a low-ε_r, thin-film microstrip environment. Divide-by-2 designs from UCSB, fabricated at Global Communication Systems (GCS), had a maximum toggle rate of $f_{clk,max}$ = 153 GHz. The same divide-by-2 circuits fabricated at UCSB had a maximum toggle rate $f_{clk,max}$ = 142 GHz.

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2

InP DHBT Theory and Design

INP heterojunction bipolar transistors (HBT) utilizing a mesa topology have been under development at UCSB since 2002. It was pursued as an alternative to the transferred-substrate technology (TS-HBT), where the active collector is defined lithographically after substrate removal and the extrinsic base-collector capacitance $C_{cb,ex}$ can be made small in comparison to the entire C_{cb} of the HBT. However, this process is very complicated and the device yield was low, motivating the mesa structure as an alternative topology for UCSB HBTs.

In this chapter, the mesa HBT technology is described. The carrier delays, resistances, and capacitances are presented, with emphasis on their physical origins from the device topology. From that, the RF HBT figures-of-merit f_τ and f_{max} are introduced. The base and collector transit delays are the dominant contributors to f_τ and f_{max}, but their values do not correlate well to the delays associated with a digital latch, regularly employed as retiming elements and decision circuits. HBT scaling laws are considered here for increased circuit bandwidth. Lastly, device modeling,

scaling limits, and advanced process modules intended to alleviate these limitations are discussed.

2.1 mesa HBT structure

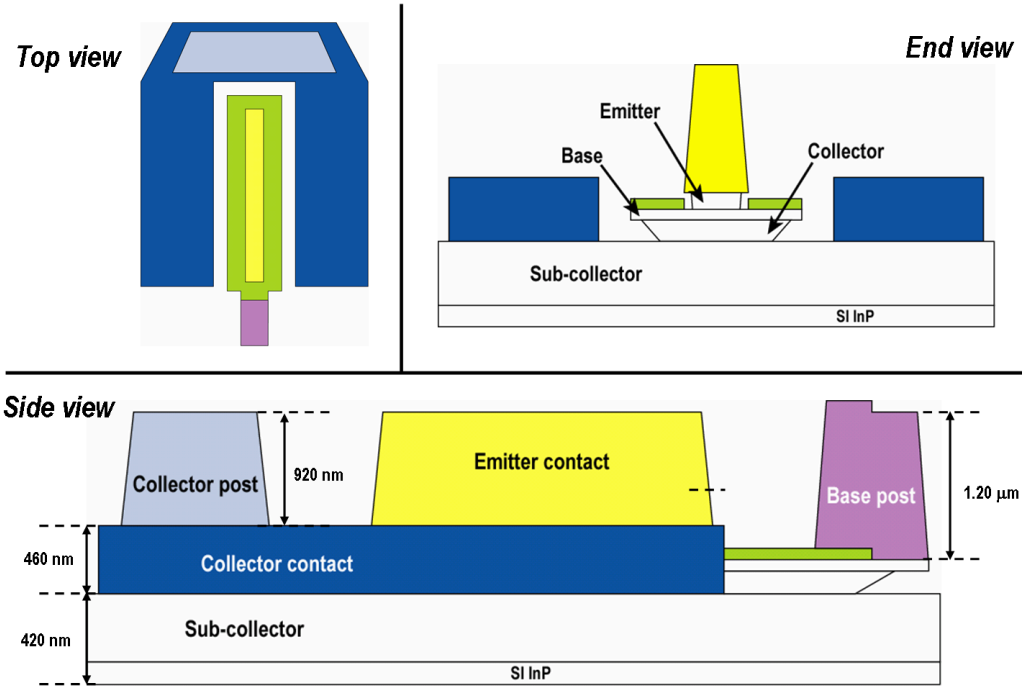

Figure 2.1: Mesa HBT structure w/ self-aligned base contact

The InP HBTs described in this work utilize a triple-mesa structure, shown in Fig. 2.1 and Fig. 2.2. Collector, base, and emitter layers are grown atop of each other and device layers are isolated by mesa formation once electrical contacts have been made. Under bias, the carriers are swept vertically across the emitter, base,

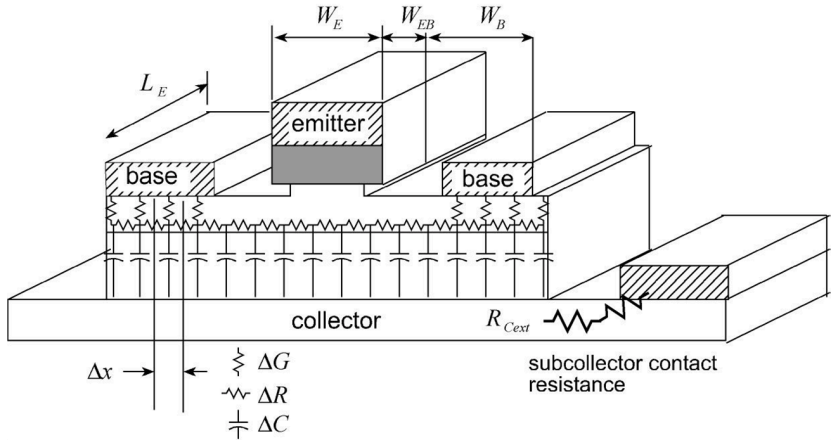

Figure 2.2: Mesa HBT showing distributed device resistances and capacitances

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and collector by their respective transport mechanisms to realize transistor behavior. A metal-semiconductor contact is utilized to electrically link the emitter, base, and collector semiconductor to their respective interconnects. Because the emitter is the top-most layer, its contact can lie above the active region of the device. The base however must be accessed externally through a contact that resides adjacent to the emitter stripe. Spreading resistance underneath the emitter mesa within the intrinsic part of the base is unavoidable. The horizontal gap between the base contact and emitter mesa, and the contact adds additional extrinsic resistances. Furthermore, the base mesa ($W_{mesa} = 2W_{cont} + 2W_{gap} + W_e$) defines the width of the collector

mesa and hence the total C_{cb} of the HBT. Minimizing the base gap and width of the contacts will avoid unwanted increases to R_{bb} and C_{cb}. To ensure this, a self-aligned base contact is employed. After the emitter contact is formed, the emitter mesa is etched down to the base. During the emitter semiconductor etch, an undercut is formed. The undercut serves as a shadow-mask such that the base contact can be deposited overtop the emitter contact and adjacent periphery to contact the base semiconductor, such that only the emitter mesa undercut $\sim$ 50 nm contributes to the base gap resistance. The collector is accessed externally and adjacent to the base. Because the collector is depleted, a thick, highly doped N^+ sub-collector is utilized to provide collector bias. This layer lies underneath the collector mesa, has similar spreading, gap, and contact resistances as described for the base, and is contacted on both sides using a non-self aligned 'horseshoe' like contact. To isolate devices, the sub-collector is etched from the field through to the semi-insulating InP substrate. Further fabrication details are given in Chapter 3 and Appendix B.

2.2 HBT carrier transit times

The time it takes for an electron entering from the emitter to traverse across the base is given by,

$$\tau_b = \frac{T_b^2}{2D_n} + \frac{T_b}{\upsilon_{exit}} \tag{2.2.1}$$

where T_b is the base thickness and D_n is the electron minority diffusivity in the base. Often the T_b/υ_{exit} contribution is ignored by assuming that the electron concentration at the collector side of the base is zero. For a thin base this assumption is not valid and the correction term accounts for how quickly the finite electron concentration exits the base, at a velocity proportional to the thermionic emission velocity $\upsilon_{exit} \sim (2kT/\pi m^*)^{1/2}$ [1]. This transit time calculation assumes uniform composition and doping in the base. To reduce τ_b, a quasi-electric field can be established to accelerate electrons more quickly across the base. Assuming the grading of the base conduction band is linear, Equ. 2.2.1 is rewritten as [2],

$$\tau_b = \frac{T_b^2}{D_n}\left(\frac{kT}{\Delta E}\right)\left[1 - \frac{kT}{\Delta E}\left(1 - \exp^{-\Delta E/kT}\right)\right] + \frac{T_b}{\upsilon_{exit}}\left(\frac{kT}{\Delta E}\right)\left(1 - \exp^{-\Delta E/kT}\right) \tag{2.2.2}$$

where ΔE is the energy difference across the base conduction band. The HBTs presented in this work employ a doping grade producing a $\Delta E \sim 50$ meV. This in turn reduces τ_b by $\sim 50\%$ compared to an ungraded base. Note Equ. 2.2.2 does not consider hot carrier or quasi-ballistic transport in the base due to the abrupt InP/InGaAs emitter-base junction utilized by UCSB HBTs.

Electrons injected from the base into the collector create a displacement current across the junction. The mean delay associated with this current is related to the change in stored base charge (equivalent induced image charge) at the collector side

of the base terminal δQ_{base}, given by

$$\tau_c = \int_0^{T_c} \frac{1 - x/T_c}{\upsilon(x)}\, dx \equiv \frac{T_c}{2\upsilon_{eff}} \tag{2.2.3}$$

where τ_c is the collector transit time, T_c is the collector thickness, and $\upsilon(x)$ and υ_{eff} are the position-dependent and effective electron velocities in the collector drift region.

As electrons enter the collector, they acquire kinetic energy and experience ballistic transport, typically referred to as a velocity overshoot regime. Because of the large energy separation between the Γ-L conduction band valleys (0.55 eV for $\mathrm{In_{0.53}Ga_{0.47}As}$, 0.6 eV for InP), electrons are able to traverse a significant fraction of the collector before attaining sufficient kinetic energy to cause scattering to the higher effective mass, lower velocity L-valley [3, 4]. By modeling the collector velocity as a two-step profile, Equ. 2.2.3 can be written as,

$$\tau_c = \frac{1}{T_c}\int_0^{T_s} \frac{T_c - x}{\upsilon_1}\, dx + \frac{1}{T_c}\int_{T_s}^{T_c} \frac{T_c - x}{\upsilon_2}\, dx \tag{2.2.4}$$

and solved to give,

$$\tau_c = \frac{1}{T_c}\left[\frac{2T_cT_s - T_s^2}{2\upsilon_1} + \frac{(T_c - T_s)^2}{2\upsilon_2}\right] \tag{2.2.5}$$

Because the collector transit time is more heavily weighted on the rate at which δQ_{base} decreases as the displacement current traverses the collector, higher electron velocities near the base are desired. This is shown in the following example. Consider two scenarios: $\upsilon_1 = \upsilon_o$, $\upsilon_2 = \frac{1}{2}\upsilon_o$ and $\upsilon_1 = \frac{1}{2}\upsilon_o$, $\upsilon_2 = \upsilon_o$. Assume the velocity

transition is at $T_s = \frac{1}{2}T_c$. In the first case where the velocity is higher near the base $\upsilon_{eff} = \frac{5}{4}\upsilon_o$, and in the second case where the velocity is lower near the base $\upsilon_{eff} = \frac{7}{4}\upsilon_o$ – an increase of $\sim$ 40%.

2.3 Collector design and maximum current density

As the collector current density is varied, the injected electrons screen the background doping and modify the electric field profile in the collector. To account for this injected charge, Poisson's equation to describe the collector can be written,

$$-\frac{d^2\phi}{dx^2} = \frac{dE}{dx} = \frac{1}{\varepsilon_o\varepsilon_r}\left[qN_c - \frac{J(x)}{\upsilon(x)}\right] \tag{2.3.1}$$

where $\varepsilon_o\varepsilon_r$ is the dielectric constant, N_c the collector doping, $J(x)$ the collector current density, and $\upsilon(x)$ the electron velocity in the collector. Integrating Equ. 2.3.1 to solve for the electric field,

$$E(x) = \frac{1}{\varepsilon_o\varepsilon_r}\int_0^x qN_c - \frac{J(x)}{\upsilon(x)}\ dx \tag{2.3.2}$$

Electrons spread outward as they traverse the collector (current spreading) creating a position dependent current density. In the collector transit time discussion, a step function is used to describe a position dependent electron velocity due to overshoot and scattering. Assuming $J(x)$ and $\upsilon(x)$ to be constant and integrating across the

electric field,

$$\phi_{bi} + V_{cb} \geq -\frac{T_c^2}{2\varepsilon_o\varepsilon_r}\left[qN_c - \frac{J_e}{\upsilon_{eff}}\right] \tag{2.3.3}$$

where ϕ_{bi} is approximately the base bandgap potential difference, V_{cb} is the applied potential difference across the base-collector junction, and T_c is the collector thickness. When this relationship is equal, the current density (injected electrons) modifies the electric field profile such that it is equal to zero at the base-side of the collector, $E(0) = 0$. This is often referred to as the Kirk threshold current density,

$$J_{Kirk} = J_{max} = \frac{2\varepsilon_o\varepsilon_r\upsilon_{eff}}{T_c^2}(\phi_{bi} + V_{cb}) + qN_c\upsilon_{eff} \tag{2.3.4}$$

At higher $J_e > J_{max}$ for an InP-SHBT (InGaAs base and collector), holes are no longer confined to the base as the conduction and valence bands progressively flatten within the collector to a distance T_1, $0 \leq x < T_1$, $E(x) = 0$. This causes the base transit time τ_b and collector-base capacitance C_{cb} to increase, while slightly reducing the collector transit time τ_c. This is the classical definition of the Kirk effect [5]. For an InP DHBT (InGaAs base, InP collector), the valence band discontinuity at the base-collector heterojunction blocks holes from entering the collector region. As J_e exceeds J_{max}, this barrier prevents holes from compensating the excessive electron density and the field will reverse acting as a barrier to the injected collector current. This current barrier will cause a collapse in the current gain and the reduced electron velocity will significantly increase τ_c – a phenomena not experienced by SHBTs.

Higher HBT bandwidths are achieved when J_{max} is increased at a given collector thickness. From Equ. 2.3.4, this can be done by increasing the externally applied V_{cb} and/or increasing the collector doping N_c. When designing an HBT for use in a digital circuit, two bias conditions need to be considered: $V_{cb} = 0, J_e = J_{max}$ and $J_e = 0$. To maximize J_e, the collector doping should be as high as possible, however it should not be so high as to cause depletion layer collapse within the drift collector when there is no current, $E(x = T_c) = 0$. From Equ. 2.3.3 this is satisfied when,

$$N_{c,max} = \frac{2\varepsilon_o\varepsilon_r\phi_{bi}}{qT_c^2} \tag{2.3.5}$$

and Equ. 2.3.4 can be rewritten as

$$J_{max} = \frac{4\varepsilon_o\varepsilon_r\upsilon_{eff}}{T_c^2}(\phi_{bi} + V_{cb}) \tag{2.3.6}$$

At the doping level prescribed by Equ. 2.3.5, J_{max} is $2\times$ higher compared to a collector that is undoped, greatly influencing logic speed through the use of smaller devices at a given operating current I_c.

2.3.1 Correction to account for UCSB base-collector grade

InP DHBTs from UCSB utilize an InGaAs base and InP collector, often referred to as Type-I DHBTs. The conduction band discontinuity between $\mathrm{In_{0.53}Ga_{0.47}As}$ and InP (ΔE_c = 0.26 eV) is removed through a combined transition scheme employing an InGaAs setback layer and chirped-superlattice InGaAs/InAlAs grade [6, 7].

The grade acts to smooth out the energy discontinuity such that there is no effective potential drop across the length of the grade. A dipole electric field is formed between the P^+ base and an N-doped pulse layer inserted to restore the expected field across the graded region, determined from the relationship,

$$N_\delta T_\delta = \frac{\varepsilon_o \varepsilon_r \Delta E_c}{q^2 \cdot T_{grade}} \tag{2.3.7}$$

where N_δ and T_δ are the doping concentration and thickness of the pulse layer. To ensure electrons traverse through the grade and are not reflected, kinetic energy is supplied to them over the setback region. Note, Equ. 2.3.7 does not consider this layer, and the setback potential difference $\Delta\phi_{setback}$ can be a significant fraction of ϕ_{bi}. The amount of kinetic energy needed by the electrons over the setback layer for the employed grade design is not well understood at this time. The InP DHBTs reported in Chapter 4 show no signs of current blocking utilizing a launching energy $\Delta\phi_{setback} \sim$ 0.35 eV. To account for the dipole field across the setback and grade, Poisson's equation is modified,

$$\phi_{bi} + V_{cb} \geq \frac{qN_c T_c^2}{2\varepsilon_o \varepsilon_r} + \frac{qN_\delta T_\delta (T_{setback} + T_{grade})}{\varepsilon_o \varepsilon_r} \tag{2.3.8}$$

From this expression the maximum allowable collector doping to ensure full collector depletion is,

$$N_{c,max} = \frac{1}{T_c^2}\left[\frac{2\varepsilon_o \varepsilon_r}{q}(\phi_{bi} + V_{cb}) - 2N_\delta T_\delta (T_{setback} + T_{grade})\right] \tag{2.3.9}$$

Assuming standard values for $N_\delta = 3 \cdot 10^{18}$ cm^{-3}, $T_\delta = 3$ nm, $T_{setback} = 20$ nm, and $T_{grade} = 24$ nm at $V_{cb} = 0$ V, the dipole field reduces the maximum collector doping by $\sim 2/3$. This is a significant reduction that must be accounted for in design.

An alternative way to determine $N_{d,max}$ and solve for J_{max} is to only consider the portion of the collector between the pulse doping and sub-collector. Poisson's equation solved over this region is,

$$\phi_{bi} - \Delta\phi_{setback+grade} + V_{cb}\frac{T_{InP}}{T_c} \geq -\frac{T_{InP}^2}{2\varepsilon_o\varepsilon_r}\left[qN_c - \frac{J(x)}{\upsilon(x)}\right] \tag{2.3.10}$$

where T_{InP} is the thickness of the InP portion of the collector and the potential difference across the setback and grade is,

$\Delta\phi_{setback+grade} \approx$

$$(\phi_{bi} + V_{cb})\frac{T_{setback}}{T_c} + \frac{qN_\delta T_\delta(T_{setback} + T_{grade})}{\varepsilon_o\varepsilon_r} + \left[qN_c - \frac{J_e}{\upsilon_o}\right]\frac{T_c(T_{setback} + T_{grade})}{2\varepsilon_o\varepsilon_r} \tag{2.3.11}$$

where υ_o is the electron overshoot velocity in the setback and grade. From Equ. 2.3.10, $N_{d,max}$ and J_{max} are,

$$N_{c,max} = \frac{2\varepsilon_o\varepsilon_r \cdot (\phi_{bi} - \Delta\phi_{setback+grade} + V_{cb}(T_{InP}/T_c)}{qT_{InP}^2} \tag{2.3.12}$$

$$J_{max} = \frac{2\varepsilon_o\varepsilon_r\upsilon'_{eff}}{T_{InP}^2}\left(\phi_{bi} - \Delta\phi_{setback+grade} + V_{cb}\frac{T_{InP}}{T_c}\right) + qN_c\upsilon'_{eff} \tag{2.3.13}$$

where υ'_{eff} is used to denote the effective velocity in the InP layer.

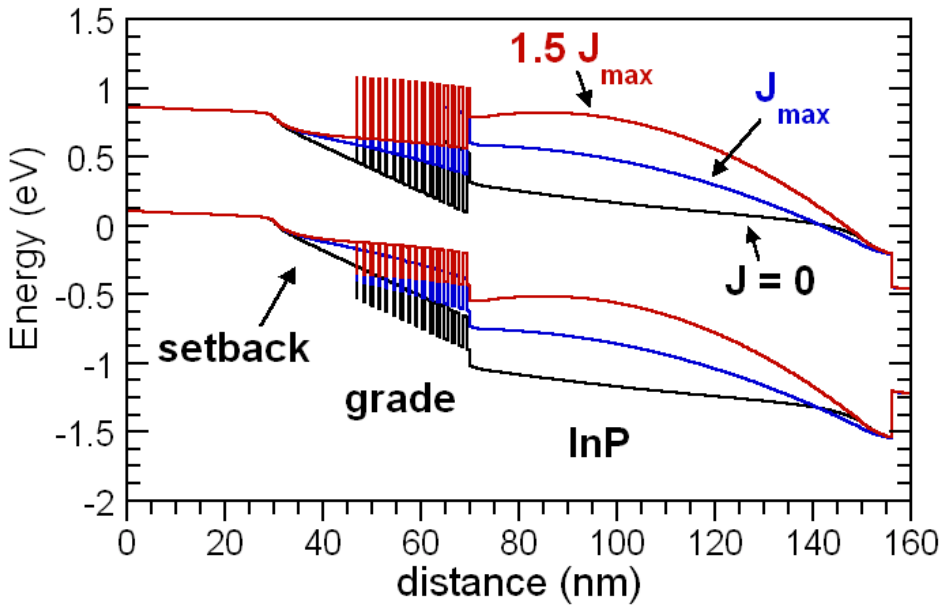

Figure 2.3: Variation of band diagram at V_{cb} = 0, $J = 0, J_{max}$, and $1.5\ J_{max}$

A band-diagram for the base-collector junction is shown in Fig. 2.3 for J_e = 0, J_{max}, and $1.5\ J_{max}$ at $V_{cb} = 0$. Notice from the band-diagram and Equ. 2.3.11, $\Delta\phi_{setback+grade}$ decreases as J_e increases, significantly influencing J_{max} by increasing the potential difference across the InP layer. However, at $J_e > J_{max}$, the reductions to $\Delta\phi_{setback+grade}$ cause a positive potential increase across the grade. At $1.5\ J_{max}$, the field is beginning to reverse in the InP layer, but the potential difference across the grade $\approx \Delta E_c/q$ has become sufficiently large to block electrons and/or reduce their velocity, exacerbating the field reversal at higher J_e. This behavior has been witnessed from fabricated UCSB DHBTs of varying collector thicknesses;

C_{cb} increases slowly, f_τ and f_{max} decrease gradually as J_e exceeds J_{max}. At much higher J_e, the increase of C_{cb} is rapid, and f_τ and f_{max} both roll-off sharply.

2.4 HBT resistance and capacitance

2.4.1 Base-collector depletion capacitance, C_{cb}

With respect to the mesa HBT structure shown in Fig. 2.1, the three components of the collector-base capacitance are,

$$C_{cb} = C_{cb,ex} + C_{cb,gap} + C_{cb,i} \tag{2.4.1}$$

$$C_{cb,ex} = 2\frac{\varepsilon_o \varepsilon_r L_e W_b}{T_c}\ , \quad C_{cb,gap} = 2\frac{\varepsilon_o \varepsilon_r L_e W_{gap}}{T_c}\ , \quad C_{cb,i} = \frac{\varepsilon_o \varepsilon_r L_e W_e}{T_c}$$

where W_b is the width of the base metal-semiconductor junction, $W_{b,gap}$ is the spacing between the base contact and emitter mesa, and W_e and L_e are the width and length of the emitter junction.

2.4.2 Base resistance

The three components that contribute to the base resistance of an HBT are the metal-semiconductor contact $R_{b,cont}$, the gap or link resistance between the base contact and emitter mesa $R_{b,gap}$, and the spreading resistance within the active region where recombination takes place, $R_{b,spread}$. Assuming the base is contacted on both

sides of the emitter,

$$R_{bb} = R_{b,cont} + R_{b,gap} + R_{b,spread} \tag{2.4.2}$$

$$R_{b,cont} = \frac{\sqrt{\rho_c \cdot \rho_s}}{2L_e} \coth \frac{W_b}{L_t}\,, \quad R_{b,gap} = \rho_s \frac{W_{b,gap}}{2L_e}\,, \quad R_{b,spread} = \rho_s \frac{W_e}{12 \cdot L_e}$$

where ρ_c ($\Omega \cdot \mu\text{m}^2$) and ρ_s ($\Omega/\square$) are the specific contact and sheet resistivities of the base, and L_t is the ohmic transfer length equal to $\sqrt{\rho_c/\rho_s}$. Equation 2.4.2 can be rewritten to more clearly show how the base resistance varies with the emitter dimensions and the width of the base mesa,

$$R_{bb} = \frac{1}{2}\frac{\rho_s}{L_e}\left[L_t \coth \frac{W_b}{L_t} + W_{gap} + \frac{W_e}{6}\right] \tag{2.4.3}$$

During HBT fabrication, the base sheet and contact resistivities are monitored using four-point-probe transmission line measurements (TLM) from non-pinched and pinched structures. For each TLM pattern measured, the distance between the probe pads progressively increases such that an excellent linear dependence should be observed for the base resistance versus TLM spacing. A non-pinched TLM structure is shown in Fig. 2.4, where the emitter semiconductor has been removed and the base semiconductor to be measured is exposed, used to extract ρ_c. A pinched TLM structure is shown in Fig. 2.5, where the emitter semiconductor resides atop the base semiconductor, used to determine ρ_s. Why both structures are needed is explained.

By removing the emitter semiconductor, surface states are formed on the exposed base of the non-pinched TLM. For a 30 nm base where the exposed semiconductor

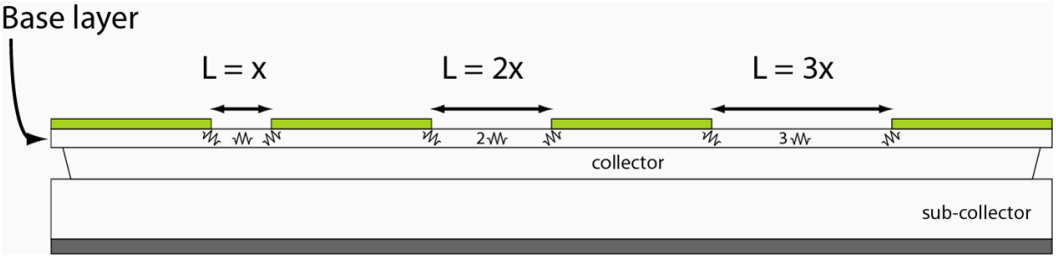

Figure 2.4: Non-pinched TLM structure – the base semiconductor is exposed

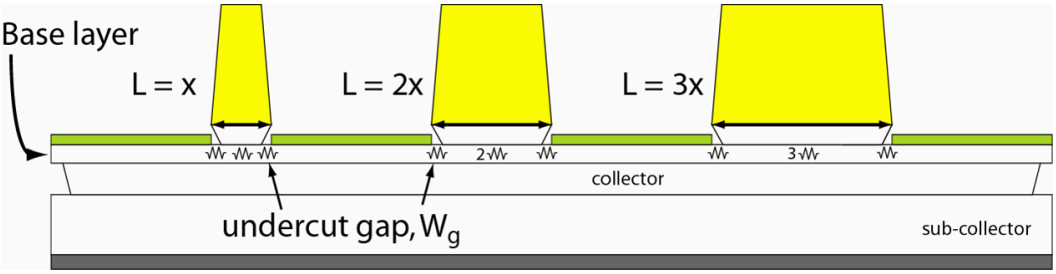

Figure 2.5: Pinched TLM structure – the emitter resides atop the base semiconductor

is doped at $7 \cdot 10^{19}$ cm^{-3}, the surface is depleted by 20%, increasing ρ_s by the same amount. A Pinched TLM does not experience this. However, the undercut formed during the emitter mesa etch introduces an additive gap resistance term to the extrapolated contact resistance, making the extracted ρ_c fictitiously high.

Equations 2.4.4 and 2.4.5 show how the non-pinched and pinched TLMs behave,

$$R_{non-pin} = 2R_{cont} + R'_{slope} \cdot L \tag{2.4.4}$$

$$R_{pin} = 2R_{cont} + 2R'_{gap} + R_{slope} \cdot L \tag{2.4.5}$$

The prime notation is used to identify resistive paths of a depleted surface. From the non-pinched relation, the ohmic transfer length is $L_t = R_{cont}/R'_{slope}$. From the pinched TLM relation, the base sheet resistance is $\rho_s = R_{slope}/W_{TLM}$, where W_{TLM} is the width of the TLM. The contact resistivity can be determined from the relation $L_t = \sqrt{\rho_c/\rho_s}$. Fig. 2.6 shows a plot of measured non-pinched and pinched TLMs from the same wafer.

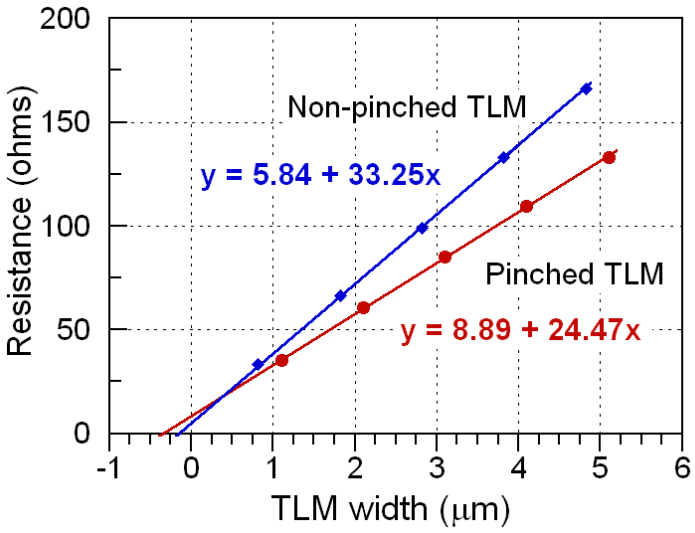

Figure 2.6: Measured TLMs – Pinched and Non-pinched for DHBT 27

The contact resistivities achieved in this work are very low and necessitate the use of this extraction method. Error is further minimized by examining the fabricated TLMs by SEM so as to use their exact dimensions in the extrapolation.

2.4.3 Sub-collector resistance

The contact, gap, and spreading resistances described for the base similarly exist for the sub-collector,

$$R_{cc} = R_{c,cont} + R_{c,gap} + R_{c,spread} \tag{2.4.6}$$

$$R_{cc} = \frac{1}{2}\frac{\rho_s}{L_e}\left[L_t + W_{c,gap} + \frac{W_{cb}}{6}\right]$$

where ρ_c ($\Omega \cdot \mu$m^2) and ρ_s ($\Omega/\square$) are the specific contact and sheet resistivities of the collector, W_{cb} is the width of the collector mesa, $W_{c,gap}$ is the spacing between the collector mesa and contact, L_e is the emitter junction length, and L_t is the ohmic transfer length equal to $\sqrt{\rho_c/\rho_s}$. The exponential term associated with $R_{c,cont}$ can be ignored as the contact is much wider than the L_t associated with the collector contact.

The sub-collector is thick and highly doped to minimize the sheet resistance. The doping cannot be so high as to introduce defects within the growth of the subsequent layers, and making it unnecessarily thick will introduce problems during wafer planarization because it must be etched away in the field in order to isolate devices. HBTs from UCSB typically employ a 300 nm sub-collector doped with Si at $2 \cdot 10^{19}$ cm^{-3}. Non-pinched TLMs are utilized to measure the sheet and contact resistance of the sub-collector. Any TLM surface depletion is ignored because its thickness is much smaller in comparison to the sub-collector.

2.4.4 Emitter resistance

The emitter resistance is dominated by the metal-semiconductor contact, with a small contribution from the tall mesa required for a self-aligned base contact,

$$R_{ex} = R_{ex,cont} + R_{ex,bulk} \tag{2.4.7}$$

$$R_{ex,cont} = \frac{\rho_c}{A_{e,cont}}\ , \quad R_{ex,bulk} = \rho_{bulk}\frac{h_{mesa}}{A_{je}}$$

After the growth of the N^- InP emitter, a 120 nm thick N^{++} InP and InGaAs emitter cap is grown. Because the current transport through the emitter is vertical, standard TLM measurements are not possible. RF parameter extraction is used instead to determine R_{ex}, and the bulk resistivity ρ_{bulk} of the emitter cap can be approximated from sub-collector TLM measurements, typically 3.6 $\Omega \cdot \mu$m. For the 120 nm emitter cap employed in HBTs from UCSB, ρ_{bulk} contributes $\sim$ 0.45 $\Omega \cdot \mu$m^2 to R_{ex}. It is assumed that any surface depletion can be ignored because the emitter junction is much wider and the cap doping is very high. This assumption must be reconsidered when the emitter junction is scaled more narrowly. Nonetheless, if the surface is depleted 50 nm for the 0.5 μm emitter HBTs reported in this work (20% cap depletion), the contribution from ρ_{bulk} would be less than 7 % of the total R_{ex}.

2.5 Transistor figures of merit

The HBT common-emitter unity current-gain cutoff frequency f_τ is,

$$\frac{1}{2\pi f_\tau} = \tau_c + \tau_b + C_{cb} \cdot (R_{ex} + R_c) + \frac{\eta kT}{qI_e}(C_{cb} + C_{je}) \tag{2.5.1}$$

where τ_c and τ_b are the collector and base transit times, C_{cb} and C_{je} are the depletion capacitances for the collector and emitter, R_c and R_{ex} are the resistances of the collector and emitter, and $(\eta kT/qI_c)^{-1}$ is the transconductance of the HBT.

The HBT maximum oscillation (unity power-gain) frequency is,

$$f_{max} = \sqrt{\frac{f_\tau}{8\pi(RC)_{eff}}} \tag{2.5.2}$$

dependent upon the HBT f_τ and a general time constant RC_{eff} that includes the effects of the distributed base-collector network, the emitter and collector resistances, and the device transconductance g_m [8]. When the base resistance is much larger than the emitter and collector resistances, their effects become secondary and only the distributed base-collector network needs to be considered. Furthermore, the components of C_{cb} should only consider the resistance in its path when determining the charging time constants. Utilizing the definitions for C_{cb} and R_{bb} from Equ. 2.4.1 and 2.4.3,

$$f_{max} = \sqrt{\frac{f_\tau}{8\pi(R_{bb}C_{cb})_{eff}}} \tag{2.5.3}$$

and

$$(R_{bb}C_{cb})_{eff} = C_{cb,i}R_{bb} + C_{cb,gap}(R_{b,cont} + R_{b,gap}/2) + C_{cb,ex}(R_{b,cont,0}||R_{b,cont,1}) \tag{2.5.4}$$

where the collector-base capacitance underneath the emitter stripe $C_{cb,i}$ is charged through the entire base resistance, and the gap capacitance $C_{cb,gap}$ between the emitter mesa and base contact is charged through ($R_{b,cont} + R_{b,gap}/2$). The extrinsic collector-base capacitance $C_{cb,ex}$ underneath the base contact is charged by currents traversing vertically through the contact above it, having a resistance $R_{b,cont,0} = \rho_c/(2 \cdot L_e W_b)$. If the collector mesa has been undercut during fabrication, a parallel charging path is formed by currents traversing laterally through the base contact (semiconductor sheet resistance ignored) in the region associated with the undercut W_u. This path has a resistance $R_{b,cont,1} = \rho_s L_t \cdot \coth(W_u/L_t)/2L_e$, and $R_{b,cont,0}$ is equal to $\rho_c/(2 \cdot L_e(W_b - W_u))$

2.6 Device modeling

This section describes the two modeling schemes most often used to characterize InP HBTs from UCSB. The first technique makes use of the measured S-parameters of the HBT in order to extract their electron transit time, resistances, and capacitances to create a hybrid-π equivalent circuit. It is an accurate, simplified representation of an HBT compared to the true distributed nature of RC elements within

the device. The second device modeling technique utilizes a bias dependent, highly detailed, equation based physical model of the HBT geometry for use in circuit designs.

2.6.1 Small-signal equivalent circuit modeling

Fig. 2.7 shows the hybrid-π equivalent circuit for an HBT. It is a modified voltage controlled current source where the RC elements of the device are placed between their respective nodes. The extraction procedure for determining the model components from S-parameter measurements at different bias currents is discussed.

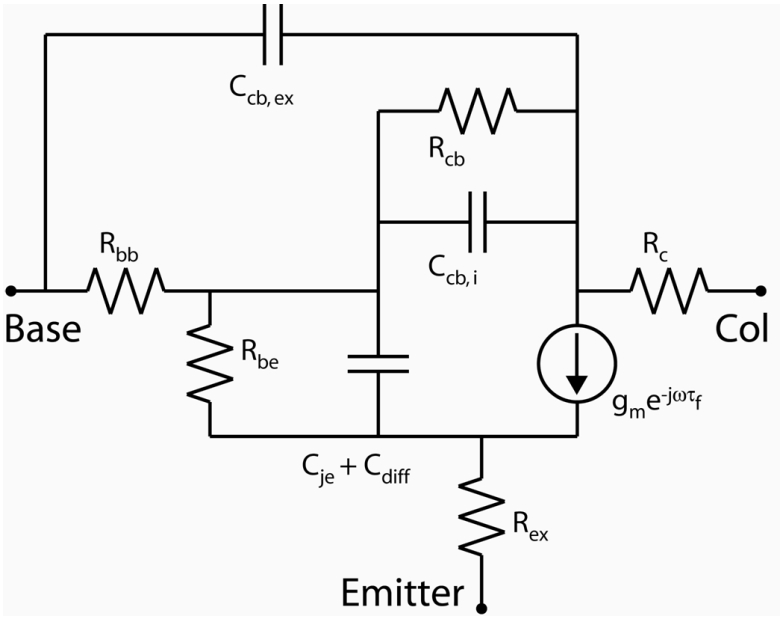

Figure 2.7: Hybrid-pi equivalent circuit HBT model

The device transconductance g_m, input diffusion capacitance C_{diff}, and input resistance R_{be} are given by,

$$g_m = \frac{qI_e}{\eta kT} \tag{2.6.1}$$

$$C_{diff} = g_m \cdot \tau_f \tag{2.6.2}$$

$$R_{be} = \frac{\beta}{g_m} \tag{2.6.3}$$

$\beta = \partial I_c / \partial I_b$ is used for RF modeling and determined from the low frequency value of h_{21}. From this, $R_{ex} + R_{bb}/\beta$ and η can be determined at low frequencies by plotting,

$$Re(Y_{21})^{-1} = R_{ex} + \frac{R_{bb}}{\beta} + \frac{\eta kT}{qI_e} \tag{2.6.4}$$

for various bias currents. The intercept at $1/I_e = 0$ gives $R_{ex} + R_{bb}/\beta$, leaving η to be found from a $Re(Y_{21})^{-1}$, $1/I_e$ pair.

The collector-base conductance $1/R_{cb}$ and total collector-base capacitance C_{cb} can be determined from the real and imaginary parts of Y_{12} from the network expression at low frequencies,

$$Y_{12} = \left(\frac{1}{R_{cb}} + \omega^2 (C_{be} + C_{cb,i}) C_{cb,i} R_{bb} \right) + j\omega (C_{cb,i} + C_{cb,ex}) \tag{2.6.5}$$

For the mesa HBT structure discussed in this work, it is fair to assume a ratio of extrinsic to intrinsic collector-base capacitance, $C_{cb,ex}/C_{cb,i}$ of three at this point in

the modeling. Once the remaining circuit elements are determined, a more accurate value for each can be found.

The total delay τ_{ec} electrons experience through the HBT is,

$$\frac{1}{2\pi f_\tau} = \tau_c + \tau_b + C_{cb} \cdot (R_{ex} + R_c) + \frac{\eta kT}{qI_e}(C_{cb} + C_{je}) \tag{2.6.6}$$

It is assumed that f_τ has been extracted from h_{21} at the different bias currents, and C_{cb}, R_{ex}, and g_m have already been determined. The collector resistance R_c is small and to first order can be determined from extracted TLM measurements and the geometry of the HBT. From that, $\tau_f = \tau_c + \tau_b$ and C_{diff} can be determined from the $1/I_e = 0$ intercept, leaving C_{je} to found from a $(1/2\pi f_\tau)$, $1/I_e$ pair.

The base resistance is determined by comparing the real part of Y_{11} of the measured HBT data to the equivalent circuit from the following relation,

$$Re(Y_{11}) \cong \frac{1}{R_{be}} + \omega^2(C_{je} + C_{diff})^2 \cdot R_{bb} \tag{2.6.7}$$

Through the hybrid-π model, R_{bb} can be adjusted to make the quadratic frequency dependence of $Re(Y_{11})$ match the measured trend. On the Smith chart, S_{11} should be similarly monitored. Once determined, the R_{bb}/β contribution to Equ. 2.6.4 is known. At low frequencies R_{be}, R_{ex}, and g_m may need adjustment in order for h_{21}, S_{11} (Smith chart), and $Re(Y_{21})$ to be in agreement with the measured HBT. Also, R_{bb} influences the curvature S_{11} undergoes as the frequency increases. It should be 'fine-tuned' so that $Re(Y_{12})$ and S_{11} are well matched between the measured and

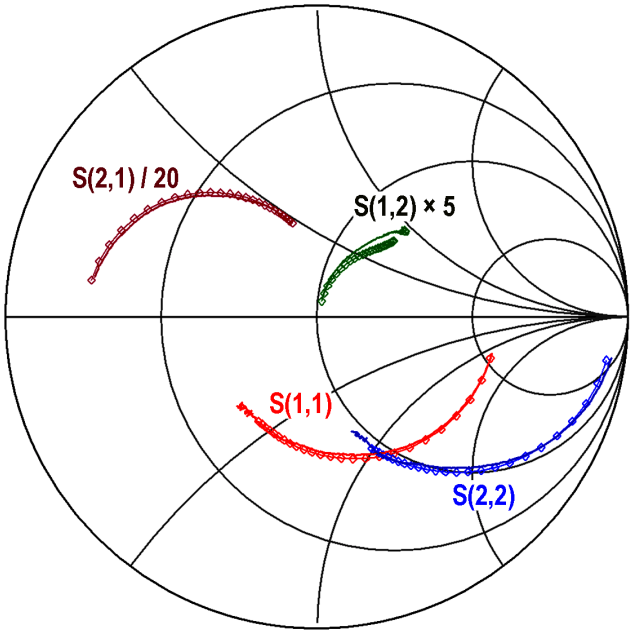

Figure 2.8: Measured (solid line) and simulated S-parameters (data points) of the HBT and hybrid-π equivalent circuit

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modeled data over the same frequency sweep.

Before the model can be finished, more precise values of $C_{cb,i}$ and $C_{cb,ex}$ need to be found. Returning to Equ. 2.6.5, there is a quadratic frequency dependence that is only influenced by $C_{cb,i}$. Similarly, Mason's unilateral gain U is only influenced by $C_{cb,i}$. By simultaneously monitoring $Re(Y_{12})$ and U, $C_{cb,i}$ can be adjusted while keeping the total C_{cb} constant to match well the measured and modeled data.

Fig. 2.8 shows on a Smith chart measured HBT S-parameters (DHBT 27, reported in Chapter 4) and those of its equivalent circuit. Overall, the S-parameters, Y-parameters, h_{21} and U are in very good agreement with the real and modeled data.

The deviation in S_{12} is believed to be due to substrate mode coupling contributing to the reverse transmission of the measurement. The f_τ and f_{max} of the hybrid-π equivalent circuit was consistent with the value extrapolated for the HBT.

2.6.2 Large-signal HBT modeling

The small-signal hybrid-π equivalent circuit has shown to be an effective way to characterize an HBT. However, this model is of limited use in circuit design because its accuracy is poor when the bias currents and voltages vary from those associated with the modeled HBT. The second modeling scheme discussed utilizes a non-linear npn-BJT based SPICE model for circuit designs. It is a highly detailed equation based physical model, where the exact dimensions of the device footprint, epitaxial thicknesses, bulk and contact resistivity, base electron diffusivity, and electron velocity in the collector are all considered.

Fig. 2.9 shows the mathematical large signal HBT model. Within the SPICE model, the resistive and capacitive terms have been set to zero and replaced external to the HBT. The length, width, and contact resistivity of the emitter are passed parameters to determine the junction area A_{je}, R_{ex}, $R_{b,spread}$, C_{je}, and $C_{cb,i}$. The base contact width, base contact resistivity, and collector undercut are passed to determine the collector mesa width, $R_{b,cont}$, $R_{c,spread}$, and $C_{cb,ex}$. The base and collector gap resistances R_{gap}, the collector-base gap capacitance $C_{cb,gap}$ associated with the

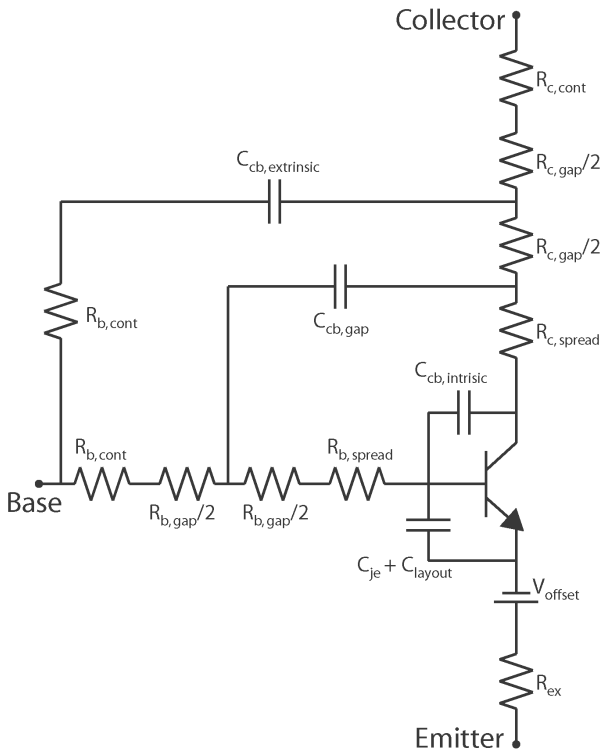

Figure 2.9: Distributed parasitics of mathematical device model

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emitter-base undercut, and collector contact resistance $R_{c,cont}$ are fixed parameters within the model and vary only with emitter length. Lastly, the thickness of the base and active collector can be varied as well. These eight input parameters of the HBT model associated with the device footprint are the most significant in determining its peak bandwidth and are sensitive to process variance. The remaining HBT parameters within the model are determined from TLM measurements and epi design from previously fabricated devices. Lastly, an external potential drop has been added to

the emitter terminal, external to the device, to account for the additional ~ 150 mV V_{be} required to bias the abrupt InP/InGaAs base-emitter junction utilized by UCSB HBTs.

The simulated RF characteristics of the large signal HBT model are very similar to its fabricated counterpart, assuming the required input parameters of the model are consistent with the extracted values from TLM measurements and small-signal RF extraction. In the instances where variation is observed between the large signal model and small signal equivalent HBT circuit, adjustments can be made to the large signal model to increase its accuracy. It does not account for variations in C_{cb} as the collector potential V_{cb} is varied, nor does it consider how the HBT behaves for a given collector thickness when it is operated beyond its maximum current density, J_{max}. To correct for these limitations, the normalized C_{cb} within the model is adjusted by the expected amount, as observed from measured devices of the same collector thickness. If C_{cb} varies significantly as V_{cb} changes (typical in current mode logic (CML) circuit design), then a weighted average is used. An additional point – the low-current breakdown voltages BV_{CEO} and BV_{CBO} are often not as relevant in comparison to the high J_e low-voltage HBT operation required for high f_τ, f_{max} and low C_{cb}/I_c ratio. A *safe operating area* (SOA) should instead be considered for the device associated with the maximum power density the HBT can support before failure at a given J_e. Such a plot requires many transistor measurements be

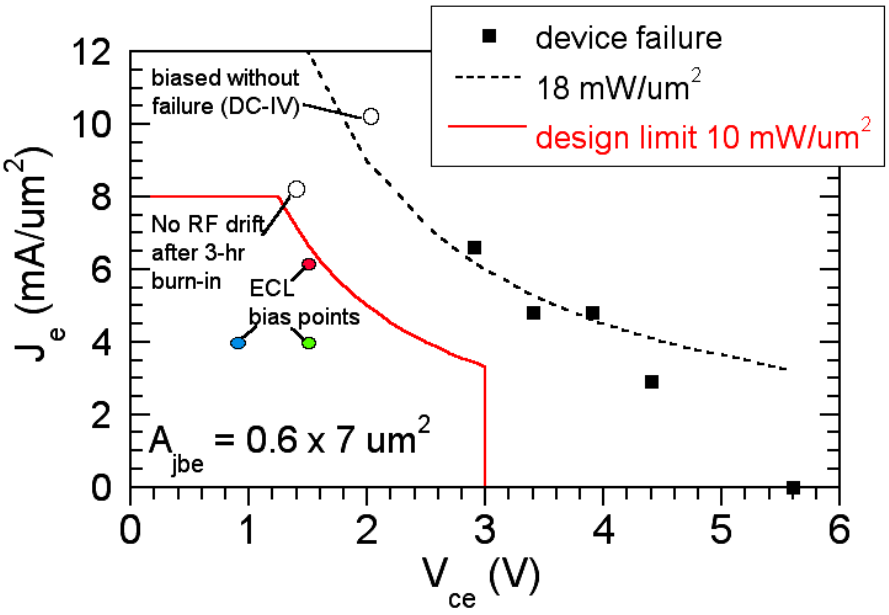

Figure 2.10: InP DHBT safe operating area plot – 150 nm collector, 30 nm base

taken from similar devices to the point of failure. Taking into account that the shunt heat-sinking path through the emitter will not contribute as significantly in large ICs compared to discrete HBT measurements, a *safe operating area* is determined and is shown in Fig. 2.10.

The large signal model described here was employed in static frequency divider designs utilizing emitter coupled logic (ECL) and CML topologies. There was excellent agreement between the maximum simulated circuit performance and that measured from fabricated circuits. These results are discussed in Chapter 5 and Chapter 6.

2.7 HBT delays within digital ICs

While the HBT figures-of-merit f_τ and f_{max} describe the maximum bandwidth attainable for a single device, they are of limited value in predicting the speed of logic, mixed-signal, or optical transmission ICs. A regularly cited digital figure-of-merit for a device technology is a static frequency divider. It is a master-slave (M-S) flip-flop consisting of two series connected latches that are clocked out of phase 180°. To generate the $f_{clk}/2$ frequency division, the differential output of the flip-flop is inverted and connected to the input such that the circuit changes state on the rising edge of the clock cycle. Because M-S flip-flops are utilized as retiming elements for data synchronization, their maximum toggle rate often limits circuit bandwidth. For this reason, static dividers are a more realistic benchmark circuit in comparison to the narrow-band operation of dynamic frequency dividers and ring oscillators.

The propagation delay through the latch is dependent upon the combined charging times of the capacitances in the signal path. By modeling the latch as an n-port linear network having no inductors, the method of open circuit time constants (MOTC) can be used to evaluate the time constants associated with the pole coefficients a_n of the system. Note, MOTC does not determine the coefficients b_n

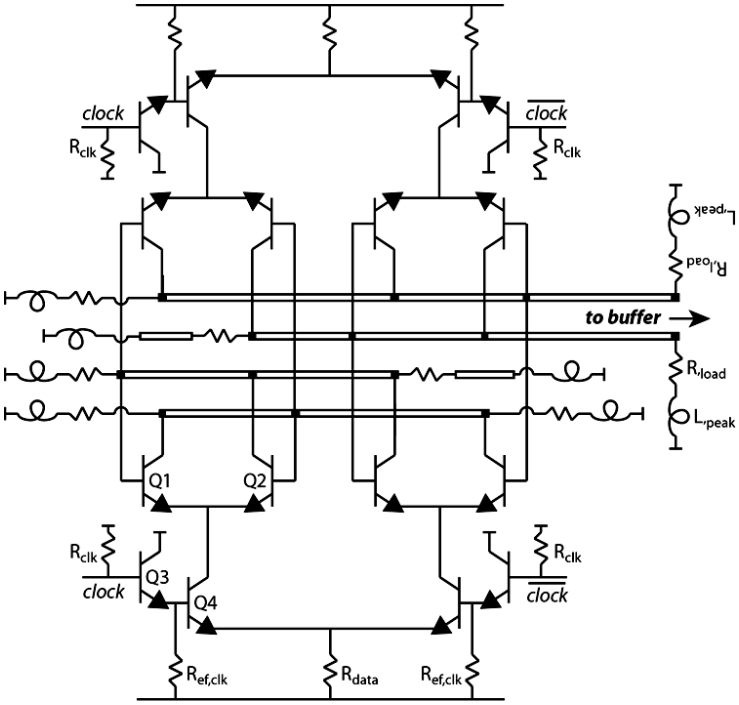

Figure 2.11: Schematic of CML static frequency divider

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associated with the zeros. The transfer function for such a network is given by,

$$\frac{V_{out}}{V_{in}} = \left[\frac{V_{out}}{V_{in}}\right]_{midband} \left(\frac{1 + b_1 s + b_2 s^2 + \cdots b_n s^n}{1 + a_1 s + a_2 s^2 + \cdots a_n s^n}\right) \tag{2.7.1}$$

In order to utilize MOTC, the passive and active components of the network must behave linearly. To satisfy this requirement, the HBT transconductance g_m and diffusion capacitance C_{diff} of those devices operating as part of a differential pair (where the voltage across the base emitter junction is $\approx \Delta V_{logic} >> kT/q$) are modified,

$$G_{m,\, large-signal} = \frac{\Delta I_o}{\Delta V_{be}} \approx \frac{1}{R_{Load}} \tag{2.7.2}$$

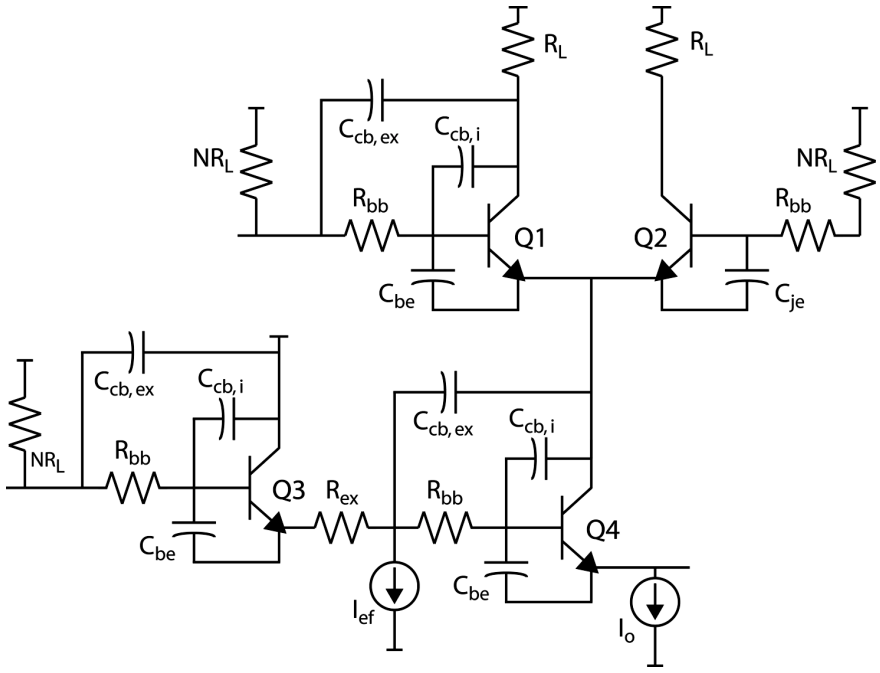

Figure 2.12: Delay path and capacitors charged during clock transition

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$$C_{diff,\ large-signal} = G_m \cdot (\tau_b + \tau_c) \tag{2.7.3}$$

Similar linearization is required of the base-emitter depletion capacitance C_{je},

$$C_{je,\ large-signal} = \frac{1}{V_1 - V_2} \int_{V_1}^{V_2} C_{je}(V)\, dV \tag{2.7.4}$$

To simplify the analysis, the network is considered to only have a single dominant pole a_1, and the zeros are ignored. The coefficient a_1 is,

$$a_1 = R_{11}^0 C_1 + R_{22}^0 C_2 + R_{33}^0 C_3 + \cdots R_{nn}^0 C_n \tag{2.7.5}$$

where R_{nn}^0 is the effective resistance across the terminals of C_{nn} while treating all

other capacitances as open circuits. The propagation delay is typically defined as the time required to charge the output node when the input is toggled. Assuming a $(1 - \exp(-t/\tau))$ charging behavior, $T_{prop} = a_1 \ln(2)$. However, to the level of accuracy of the assumptions used in the analysis, linear node charging with time is assumed and $T_{prop} = a_1/2$.

Fig. 2.11 shows a schematic of a two-level CML flip-flop configured as a static frequency divider. The schematic is redrawn in Fig. 2.12 to show the significant resistive and capacitive elements encountered in the signal path, for the determination of the propagation delay,

$$\begin{aligned} 2T_{prop} \;\cong\; & N(\Delta V_{logic}/I_o)C_{cb3} \;+\; R_{bb}C_{cbi3} \\ & +\; [2(R_{ex3} \;+\; 1/g_{m3}) \;+\; (\Delta V_{logic}/I_o)]C_{cb4} \;+\; 2C_{cbi4}R_{bb4} \\ & +\; (C_{je4} \;+\; I_o\tau_f/\Delta V_{logic})(R_{bb4} \;+\; R_{ex3} \;+\; 1/g_{m3}) \\ & +\; [C_{je2} \;+\; C_{je1} \;+\; (I_o\tau_f/\Delta V_{logic})](\Delta V_{logic}/I_o) \\ & +\; (N \;+\; 1)(\Delta V_{logic}/I_o)C_{cb1} \;+ R_{bb1}C_{cbi1} \end{aligned} \tag{2.7.6}$$

The devices are operating in the following modes: Q3 emitter-follower, Q4 common-emitter, Q1 common-base, and Q2 cut-off. N denotes the fan-out of identically connected gates in a larger circuit. As shown in Equ. 2.7.6, the base and collector transit times play a relatively minor role in logic speed, in comparison to their strong contributions to f_τ. The most significant delays in the latch are from charg-

ing the depletion capacitances over the logic swing, $(C_{je} + C_{cb})\Delta V_{logic}/I_o$, where $\Delta V_{logic}/I_o = R_L$. To minimize these capacitive delays, small devices should be used operating a current density J_e close to J_{Kirk}.

It is not evident from the gate delay expression, but R_{ex} has a large indirect effect on the maximum toggle rate. Consider the differential pair in Fig. 2.13, where R_{ex} is present. The differential switching current is described by,

$$I_{c1} - I_{c2} = I_o \tanh\left[\frac{q(V_1 - V_2)}{2kT} - \frac{I_{e1} - I_{e2}}{2} \cdot R_{ex}\right] \tag{2.7.7}$$

With no R_{ex} present, the current is completely switched when $V_1 - V_2 = 6kT/q$. For non-zero values of R_{ex} at a fixed current I_o, the output characteristics for $I_{c1} - I_{c2}$ begin to progressively lean over as R_{ex} is increased. When the voltage drop across R_{ex} is $6kT/q$, more than $10kT/q$ potential difference is needed to switch the currents. If we assume an HBT junction temperature rise of $\sim 60°$C when these devices operate in a larger circuit, the potential difference required to switch only the base-emitter junction is $\sim$ 187 mV. Typically, $V_1 - V_2 = \Delta V_{logic}$ = 300 mV for ECL and CML based latches. This leaves 113 mV $\approx 4kT/q$ of voltage headroom to account for $I_o R_{ex}$ = $\Delta V_{parasitic} \cong J_e \rho_c$, and digital noise margin (due to signal ringing on the interconnect bus) in order to regenerate the logic state on the 'hold' stage of the latch.

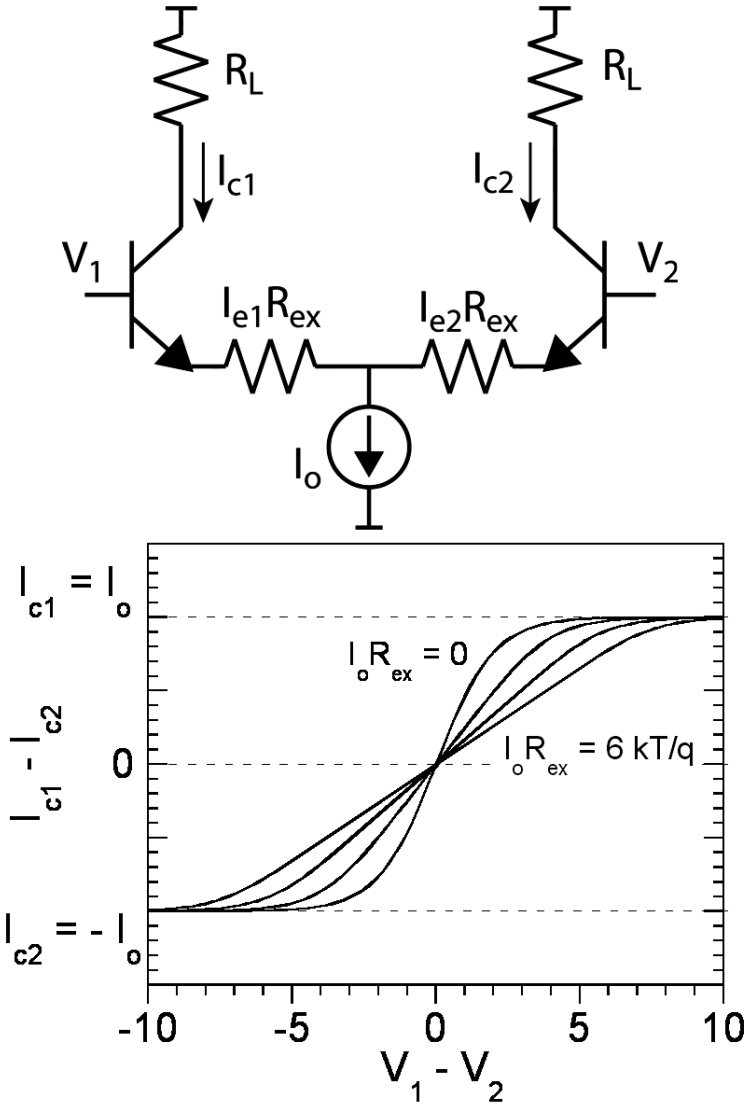

Figure 2.13: Current flow of a differential pair in the presence of emitter resistance – $I_o R_{ex} = 0, 2kT/q, 4kT/q,$ and $6kT/q$. $V_1 - V_2$ is normalized to kT/q.

Table 2.1: Summary of simultaneous parameter scaling for a γ:1 increase in HBT and circuit bandwidth

key device parameter	required change
collector depletion layer thickness	decrease γ:1
base thickness	decrease $\sqrt{\gamma}$:1
emitter-base junction width	decrease γ^2:1
collector-base junction width	decrease γ^2:1
emitter depletion thickness	decrease $\gamma^{1/2}$:1
emitter contact resistivity, ρ_{ex}	decrease γ^2:1
emitter current density	increase γ^2:1
base contact resistivity – if contacts lie above B-C junction	decrease $\sim \gamma^2$:1
base contact resistivity – if contacts do not lie above B-C junction	unchanged
bias currents and voltages	unchanged

2.8 HBT scaling principles

The previous section reviewed the relevant HBT transit and RC delays associated with discrete device performance and those of a digital latch. In order to improve HBT as well as analog and digital IC speed, all significant capacitances and transit times must be simultaneously reduced by an appropriate amount corresponding to an intended γ:1 increase in bandwidth [10]. This is done while maintaining constant all resistances, the operating voltages and current I_c , and transconductance $g_m = qI_c/\eta kT$ – i.e. I_c and $g_m \propto \gamma^0$. These associated scaling laws are discussed and reviewed here.

Reducing the collector depletion layer thickness T_c by $\gamma : 1$ and base thickness T_b by $\gamma^{1/2}$:1 reduces τ_f (and C_{diff}) by the required proportion. Consequently how-

ever, increases to C_{cb} and R_{bb} result. Reducing the emitter and collector junction areas in proportion to γ^2:1 will result in the desired γ:1 reduction in C_{cb}. The intrinsic base resistance $R_{b,spread}$ underneath the emitter is reduced by $\gamma^{3/2} : 1$, but $R_{b,gap}$ has increased by $\gamma^{1/2} : 1$ and the horizonal contact resistance $R_{b,cont}$ by $\gamma^{1/4} : 1$. At the 0.6 μm emitter junction scaling generation, scaling for a $\gamma : 1$ increase in bandwidth would result in R_{bb} as a whole remaining unchanged. For higher orders of HBT scaling, the contribution due to $R_{b,gap}$ is significant for thin bases due to the exposed, depleted surface having a much higher effective sheet resistance by $\sim$ 60%. Increased base doping would be required to keep R_{bb} constant. If the base ohmic contacts lie above the collector-base junction, their width must be reduced γ:1 to obtain the requisite reduction in C_{cb}; this necessitates a γ^2:1 reduction in the base contact resistivity $\rho_{v,b}$. If the contacts do not lie above the same semiconductor junction associated with the active collector region, their resistivity need not be scaled as aggressively, if at all.

With constant I_c, but with the emitter junction area reduced in proportion to γ^2:1, the emitter current density J_e increases $\gamma^2 : 1$. This is feasible and expected within the limits imposed by the Kirk effect, as $J_{\text{Kirk}} \propto 1/T_c^2 \propto \gamma^2$. Because the emitter resistance R_{ex} must remain constant in the presence of a γ^2:1 reduction in emitter junction area A_{je}, the normalized emitter contact resistivity $\rho_{ex} = R_{ex}A_e$ must be reduced rapidly, with $\rho_{ex} \propto 1/\gamma^2$. Because operating J_e increases in proportion

to the bandwidth squared, the maximum reliable power density associated with a *safe operating area* (previously discussed) P/A_e=$J_eV_{ce}$$\propto \gamma^2 V_{ce}$ is a more significant applied voltage limit than the low-current breakdown voltages BV_{CEO} or BV_{CBO}. The scaling limits of BV_{CEO} and BV_{CBO} with collector thickness are not clear for the type of base-collector grade utilized in this work. Trade-offs between grading design and performance, and breakdown are given in the next section.

Scaling requirements for the emitter depletion thickness T_{eb} are not easily summarized here and beyond the scope of this work. Detailed analysis of the need for scaling T_{eb} is reported in [10] and briefly summarized. The total emitter-base capacitance C_{je} is given by,

$$C_{je} = C_{je1} + C_{je2} = \frac{\kappa_1 L_e W_e}{T_{eb}} + \kappa_2 T_{eb} T_b I_c \tag{2.8.1}$$

Examination of C_{je} in conjunction with the imposed scaling laws shows that C_{je1} is reduced $\gamma^2 : 1$ and C_{je2} is reduced $\gamma^{1/2} : 1$ (where κ_1 and κ_2 are constants that are unchanged), suggesting that T_{eb} need not be scaled. This is not a reasonable and accurate statement. Consider the increase in stored mobile electron charge under bias across T_{eb} for the same I_c within a $\gamma^2 : 1$ narrower emitter. The potential drop associated with the electron quasi-Fermi level energy across T_{eb} will increase and modify the ideality factor N from the relationship $I_c \propto \exp^{qV_{be}/NkT}$,

$$N = 1 + \frac{1}{q}\frac{\partial(\Delta E_{fn,eb})}{\partial V_{be}} \tag{2.8.2}$$

where $\Delta E_{fn,eb}$ is the change in quasi-Fermi energy at the base-edge of the emitter and the increase in N beyond unity is due to the modulation of $\Delta E_{fn,eb}$ by V_{be} – this neglects effects from the abrupt emitter-base junction utilized in this work. To keep such changes small and prevent N from increasing at higher J_e operation, T_{eb} must be reduced as the current density increases. The emitter depletion layer thickness need not be scaled as rapidly as that of the collector, but it is reasonable to suggest T_{eb} be scaled $\gamma^{1/2} : 1$. Consequently C_{je} becomes progressively less significant with scaling. These scaling laws are summarized in Tab. 2.1.

Lastly, reductions to device thermal resistance need to be considered [15]. For discrete HBTs, a significant fraction of the heat generated in the collector is removed through the base and into the emitter metal – behaving as an effective shunt path in parallel with the substrate. In large integrated circuits, the heat-sinking through the emitter is much less effective and should not be considered. From the scaling laws, the thermal resistance normalized to the emitter junction area $\theta_{JA}A_{je}$ must be reduced in proportion to the square of the circuit bandwidth $\gamma^2 : 1$. Removing layers between the collector and substrate that are of low thermal conductivity is imperative, and substrate thinning could be beneficial. These are general guidelines, as there is no clear approach how to keep the junction temperature constant through subsequent scaling generations.

Consider specifically the impact of this scaling on ECL and CML logic speed.

With a γ:1 scaling, the collector thickness T_c is reduced γ:1, the current density increased γ^2:1, and the dominant delay $C_{cb}\Delta V_{logic}/I_c$ reduced γ:1. The parasitic voltage drop $R_{ex}I_c = \rho_{ex}J_e$ remains constant only because ρ_{ex} is reduced rapidly, being proportional to $1/\gamma^2$.

2.9 HBT scaling limits and solutions

From the HBT scaling laws, in order to increase circuit bandwidth, the transit times and capacitances of the device must be reduced while maintaining constant resistances, currents, and g_m. This is realized by thinning the base and collector layers, narrower emitter and collector junctions, increased operating current density, and reduced contact ρ_c and sheet ρ_s resistivities.

Thinner base and collector epitaxial layers can be achieved through growth. The base sheet resistance is $\propto T_b^{-1}$, and to keep it unchanged the bulk resistivity (ρ_{bulk}, Ω·cm) must be decreased through increased base doping. As the doping approaches $7 \cdot 10^{19}$ cm^{-3}, the hole mobility decreases and the doping-mobility product remains relatively constant. InP DHBTs from UCSB utilizing a 30 nm base and doping grade from $7 - 4 \cdot 10^{19}$ cm^{-3} have a $\rho_{bulk} \cong 18\ \Omega{\cdot}\mu$m. Thinner bases with higher doping are being investigated (T_b = 20 nm, $8 - 6 \cdot 10^{19}$ cm^{-3}), with initial results showing a 20% reduction in ρ_{bulk}.

As the collector is thinned, the increased electric field enables higher operating current densities. For InP DHBTs, the grade employed to removed the conduction band discontinuity between the InGaAs and InP must continue to be effective. This has been satisfied in existing designs by removing only the InP contribution from the collector. Eventually, the InGaAs setback layer will be a significant fraction of the total collector such that the increased electric field across it will reach $E_{critical}$ before doing so in the larger bandgap InP layer, and the benefit of increased collector breakdown voltage will be negated. At the scaling node associated with this condition, thinning the setback and grade would be needed. It is not clear how the grade should be scaled, however scaling the setback is simple. As discussed in §2.3, the electrons entering the collector from the base require additional kinetic energy, supplied by the setback layer, before entering the grade. Existing results from measured HBTs suggests that a setback potential difference as low as $\Delta\phi_{setback} \cong 0.28$ eV ($T_{setback} = 15$ nm, $T_{grade} = 24$ nm, $T_c = 120$ nm) is adequate. Thus, as the collector is scaled, the setback should be thinned to maintain a similar value of $\Delta\phi_{setback}$. Experiments are underway to better understand the limits of this grading scheme. These scaling issues aside, UCSB InP DHBTs have demonstrated current densities ~ 18 mA/μm^2 before showing signs of current blocking from the setback/grade *or* thermal effects.

Emitter contacts as narrow as 0.4 μm can be achieved through standard opti-

cal lithography and evaporated metal-liftoff techniques. As the contact is scaled, advanced photoresist processes are needed to resolve smaller features using i-line stepper lithography. Even with such features, the height of the contact will be limited by the aspect ratio attainable from the e-beam metal evaporator. An electroplated emitter contact, or one formed through metal-sputtering and dry-etch, are alternative ways of producing tall, straight, narrower features. For these narrower contacts, the undercut of the emitter mesa becomes increasingly difficult to control. Dielectric sidewall spacer processes allow for very thin emitter semiconductor layers, minimizing the undercut during mesa formation. Furthermore, the spacer eliminates the need for evaporated self-aligned base contacts, where instead electroplating or metal-sputter dry-etch processes are used. These advanced processes are under development and are discussed in [12, 13].

Narrower collector junctions require narrower base contacts. A minimum width $\sim L_t$, the ohmic transfer length, should be maintained to prevent exponential increases to the contact resistance $R_{b,cont}$. As L_t is scaled to less than 0.3 μm, these thin, narrow contacts have unwanted resistance and inductance that influence HBT performance. Furthermore, circuits employing these narrow contacts are very difficult to yield in a manufacturing environment.

The underlying theory of metal-semiconductor junction contact resistance is reviewed in Appendix A. Through the appropriate choice of metal workfunction and

highly doped semiconductor, field-emission will be the dominant transport mechanism across the junction, having an electron tunneling probability $\propto \exp(\phi_{barrier}^{1/2} \cdot W_{depletion})$ where $\phi_{barrier}$ is the barrier energy and $W_{depletion}$ is the resulting depletion width at the inferface. Invarient of the metal employed, the Fermi level at the semiconductor surface will be influenced by residual surface contamination due to a combination of surface states, native oxides, and metal-semiconductor diffusion at the interface. Preparation techniques to minimize their presense have been developed, where exceptionally low values of contact resistance $\rho_c \approx 6\ \Omega \cdot \mu\text{m}^2$ values have been achieved. At this scaling node, the resulting transfer length is $\sim$ 100 nm. Contacts this narrow are not realistic. In order to satisfy the scaling requisites for the collector junction, a collector pedestal process has been under development for use in III-V HBTs.

The emitter contact resistivity is influenced by the same metal-semiconductor issues as for the base. Because the semiconductor layer contacted for the emitter is the last one grown, defects due to lattice strain from excessively high doping or growth of lattice-mismatched, narrow-bandgap In-rich InGaAs can be utilized. The increased doping reduces the depletion width, while the narrower bandgap semiconductor maintains a lower energy barrier for electrons, as the penalty is less severe to the contact resistance if contamination or oxides are present at the surface. Emitter contact resistivity to N^+ $\text{In}_{0.85}\text{Ga}_{0.15}\text{As}$ as low as 7 $\Omega \cdot \mu\text{m}^2$ has been achieved in

this work. Similar contacts to the N^+ $\mathrm{In_{0.53}Ga_{0.47}As}$ sub-collector have achieved ρ_c $\sim 4\,\Omega\cdot\mu\mathrm{m}^2$ utilizing a different surface treatment before contact deposition. Adjustments are being made to the emitter photoresist lithography steps so as to achieve comparable results. It is not clear how ρ_c can be further reduced. Advanced materials engineering may be beneficial. Regrown emitter junction HBTs have been under development at UCSB as an alternative, where the ohmic contact is much larger than the emitter junction for reduced access resistance.

2.9.1 Collector pedestal implant – reduced C_{cb}

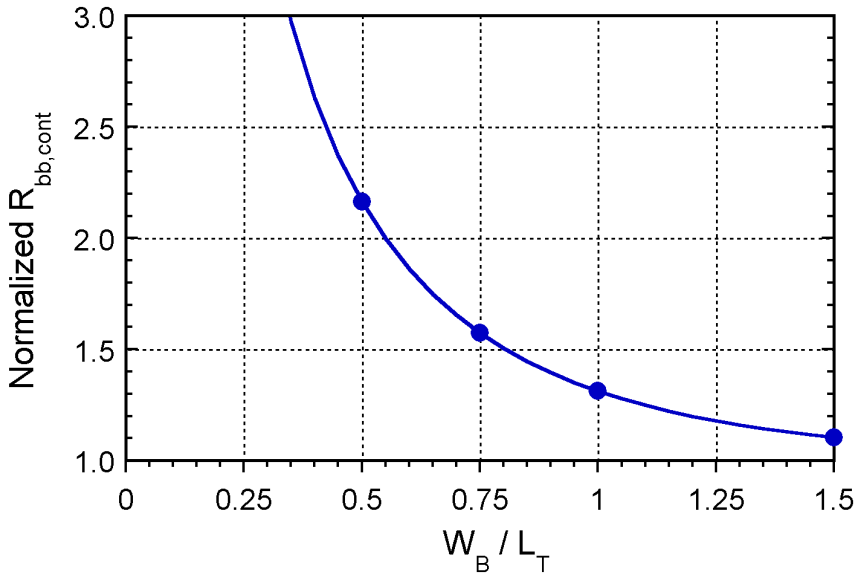

Figure 2.14: Variance of the contact resistance (normalized to $\frac{\sqrt{\rho_c\rho_c}}{2L_e}$) as the base contact is scaled

For the HBTs reported in Chapter 4, the emitter and collector junctions are 0.6 μm and 1.3 μm wide, and the base contact W_b has been scaled on the order of the ohmic transfer length L_t. Preserving this ratio as the emitter is narrowed entails similar scaling of the collector mesa through narrower base contacts. Fig. 2.14 shows how with further scaling $R_{b,cont}$ increases exponentially as the W_b is scaled. In addition, base contacts less than 300 nm present challenges in process design for high yield fabrication, where non-negligible bulk metal resistance exists along the length of the contact.

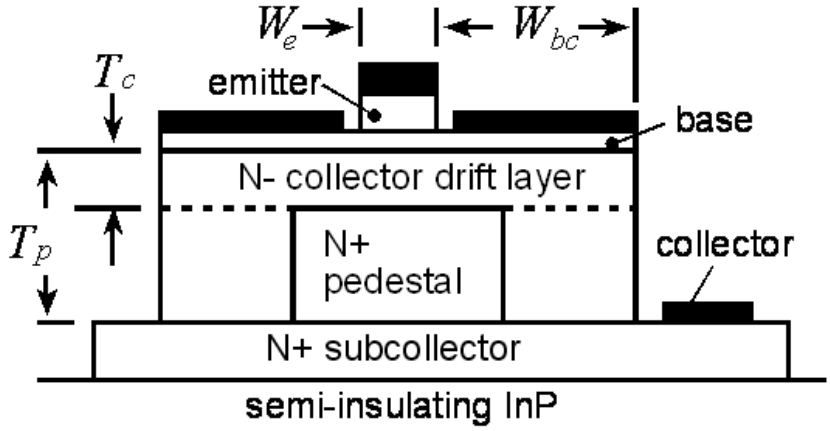

Figure 2.15: Pedestal process schematic

Closely following the SiGe device structure described in [14], an implanted collector pedestal can be used to reduce the extrinsic collector-base capacitance $C_{cb,ex}$ of the HBT. This is realized by first growing the sub-collector and an undoped layer

$\sim$ 200 nm thick. A patterned N^+ pedestal is then implanted through the undoped layer, employing approximately the same geometry as the intended emitter. This provides a sink for electrons from the collector to sub-collector. The remaining active layers are grown and the HBT is formed, utilizing the standard UCSB mesa HBT footprint already described. Fig. 2.15 shows a cross-section of the intended device structure. The intrinsic C_{cb} is unchanged, however $C_{cb,ex}$ is significantly reduced by the added height of the depleted pedestal layer underneath the base contact and the large base pad interconnect used. The lowered A_{jc}/A_{je} associated with the pedestal HBT aliviates the need for narrower base contacts, permitting them to be wider at a given level of device performance for increased HBT yield. Initial results of this work are reported in [15].

2.9.2 Emitter junction regrowth

Collector pedestal processes address neither emitter contact nor base resistivity scaling limits. Again, closely following the SiGe device structure, there is under development an HBT process flow in which a T-shaped emitter is formed by regrowth whose ohmic contact is much larger than the emitter junction. This is achieved by first growing a template where the sub-collector, collector, and intrinsic base layers are grown. Two additional layer are included, an extrinsic base that provides a highly conductive link between the contact and intrinsic base, and a multi-layer InP/InAlAs

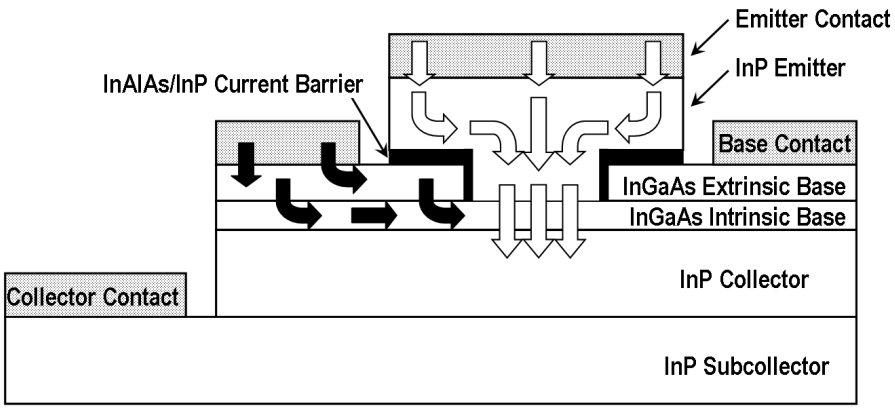

Figure 2.16: Regrown-emitter process schematic

current barrier that prevents unwanted carrier injection between the emitter and extrinsic base. Once the template is grown, an emitter window is patterned and etched through to the intrinsic base. This defines the geometry of the emitter junction. The emitter and cap layers are then growth across the wafer surface. Lastly, device fabrication ensues in the same manner as a mesa HBT, where the emitter contact deposited is larger than the active junction underneath it. The reductions of emitter resistance through an increased contact/junction area ratio is an attractive alternative to materials engineering for reduced emitter access resistance because it also permits an extrinsic base region of $N_A > 10^{20}$ cm^{-3} doping where the total extrinsic and intrinsic thickness of 100 nm significantly reduces the base resistance R_{bb}. Initial results of this work are reported in [16].

2.10 HBT scaling efforts in this work

The carrier transit times, and the resistive and capacitive delays associated with the InP mesa HBT topology have been discussed. To increase device bandwidth and reduce digital IC gate delay, the footprint must be physically scaled vertically and laterally to reduce the C_{cb}/I_c and A_{jc}/A_{je} ratios of the HBT. The base and emitter contact resistivities ρ_c must be reduced to maintain simultaneously high f_τ *and* f_{max}, and decrease the dominant gate delay $C_{cb} \cdot (R_L + R_{bb})$. Limits to scaling the device footprint have been clearly outlined as well.

Chapter 3 reports the efforts undertaken to scale the HBT for increased bandwidth. Improved surface preparation before ohmic contact deposition has reduced the emitter, base, and collector ρ_c by 2:1. Advanced photolithography processes have demonstrated with high yield, 0.5 μm emitter junction HBTs. Also, because the base ρ_c has been reduced to $\sim 6\ \Omega \cdot \mu\text{m}^2$, the ohmic transfer length is sufficiently small to allow contacts as narrow as 0.3 μm wide, significantly reducing the extrinsic C_{cb} of the HBT. Other process changes have been pursued and are reported. The HBT has been scaled to the physical barriers allowable for maximum f_τ and f_{max}, and minimum C_{cb}/I_c ratio without utilizing the pedestal implant or emitter regrowth modules. Device results employing this footprint, the fabrication improvements, and many different collector thicknesses have demonstrated record bandwidths and are reported in Chapter 4.

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3

HBT scaling and process improvements

CHAPTER 2 discussed the importance of vertical and lateral scaling of the HBT in order to produce devices having simultaneously increasing f_τ and f_{max}, and lower C_{cb}/I_c ratio. At the time this work began (November 2002), the mesa HBT process at UCSB [1] was still in its infancy and based closely on the transfered-substrate HBT (TS-HBT) process flow [2], [3]. The transition from to mesa device topology was motivated by the following issues with the transferred substrate process.

The dominant failure mechanism associated with the TS-process have to do with the substrate removal steps. After the device and circuit formation is complete, BCB coats the wafer and vias are etched for the subsequent electroplating of a 5 μm thick ground plane. At this point a GaAs or AlN carrier wafer was soldered against the ground plane. Often the BCB cracks because of the high temperature and pressure experienced by the wafer from the soldering bonder, or pockets of air get trapped between the InP host and carrier wafer. In the areas where this occurs, device and

circuit yield is zero. The final step requires the InP host to be etched away. Sometimes during this etch, the NiCr resistors are attacked because their SiN protection layer has formed cracks or voids earlier in the process. Circuits using these resistors would not bias correctly.

Device heat-sinking must be considered as the active HBT layers are scaled because the operating power density increases proportional to the device bandwidth squared. In the TS-topology, heat generated in the HBT is removed from the collector contact and Si_3N_4 dielectric on the emitter contact. Both of these heat-sinking mechanisms have high thermal resistance. The triple-mesa topology alleviate this issue because heat generated in the collector can be removed into the high thermally conductive InP substrate.

For the TS-HBT process, device interconnects are deposited before and after the InP host wafer is removed. Electrical connection between them is required. To make this possible and have passivated HBTs, the passivation dielectric (polyimide) is pattern-etched leaving the device encapsulated while clearing the field. This requires the device interconnect metal climb ~ 0.8 μm over the device encapsulation. The metal at the interconnect step coverage sites is thin and necessitates a much lower maximum operating current density (mA$/\mu$m) for them.

By using a mesa HBT topology the first two issues are avoided, greatly improving HBT performance and yield. Other failure mechanisms associated with emitter-

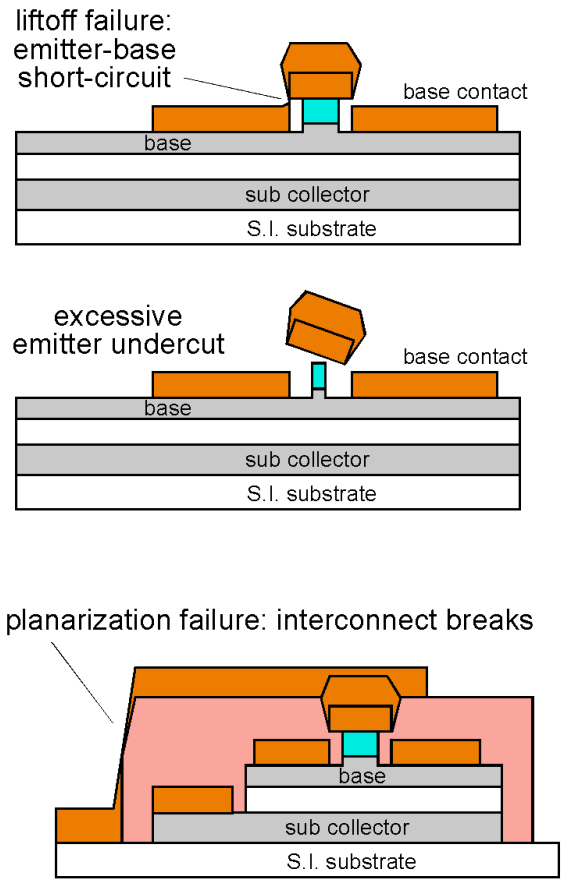

Figure 3.1: Failure mechanisms that limit yield for mesa HBTs

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base lift-off short-circuits, excessive emitter semiconductor undercut, and metal interconnect step coverage fractures and current handling were still unresolved, as shown in Fig. 3.1. Because of these mesa process limitations, discrete device yield was poor for highly scaled devices with emitter widths less than 0.7 μm, and for those with a collector to emitter mesa width ratio less than three. For circuits us-

ing larger device features, the yield was poor for transistor counts greater than 100 HBTs. As this chapter will report, numerous fabrication improvements and changes have been made to the mesa HBT process flow for increased device scaling and increased circuit yield employing such devices. HBT and circuit results from this process will be reported in Chapter 4 and Chapter 5, respectively.

3.1 Improved metal-semiconductor contact deposition

Contact related resistances have a significant impact on HBT and circuit speed, and through each subsequent HBT scaling generation a γ^2 decrease is required of the emitter and base contact resistivities ρ_c for a γ increase in bandwidth. The ρ_c associated with the metal-semiconductor junction (discussed in Appendix A) is made smaller through the appropriate choice of interfacial metal contacting a semiconductor of low bandgap, having minimal surface oxides or contamination. The following sub-sections discuss the extensive efforts undertaken to improve the quality of the emitter and base contacts for reduced ρ_c.

3.1.1 Indium rich InGaAs contact layers

Non-alloyed ohmics are utilized for contacting the collector, base, and emitter. Because the emitter cap layers are grown last, all preceding layers grown should be closely lattice-matched to InP for minimal defect related strain. $\mathrm{In_{0.53}Ga_{0.47}As}$ has a

similar lattice constant as InP, where the bandgap energies are 0.72 eV and 1.35 eV respectively. It is utilized as the base material to form the base-emitter heterojunction to InP. Also, the lower bandgap associated with $\mathrm{In_{0.53}Ga_{0.47}As}$ produces lower values of contact resistance compared to InP at similar doping levels. Therefore, it is utilized as the N^+ emitter cap layer and sub-collector contact layer. For some of the devices reported in this work, the emitter cap is step-graded from $\mathrm{In_{0.53}Ga_{0.47}As}$ to the more narrow bandgap $\mathrm{In_{0.85}Ga_{0.15}As}$ with increased doping from $3 \cdot 10^{19}$ cm^{-3} to $6 \cdot 10^{19}$ cm^{-3}. Some improvement in ρ_c for the emitter contact was observed for these changes, but the data suggests that the emitter ρ_c is more sensitive to surface preparation and metal source quality.

3.1.2 Surface preparation before metal deposition

The most significant reductions observed for the emitter, base, and collector ρ_c came through improved semiconductor surface preparation prior to metal deposition. In the past HBT work from UCSB [3, 4], an oxygen plasma etcher had been used to clean the surface, but it simultaneously bombards the surface with energetic ions and likely damaged the surface. An alternative surface preparation technique was pursued to concurrently remove scum after photolithography development, not damage the surface, and strip away surface oxides prior to metal deposition.

Studies by Driad *et al.* [5] showed that an ultra-violet ozone treatment (UV-

ozone) is an effective way of cleaning a surface of organic and non-organic materials. UV-ozone also produces an oxide film which passivates the defective surface layers associated with the native oxides of InP and InGaAs, and device processing. They go on to report that after a ten minute UV-ozone treatment, the stoichiometric composition at the surface is restored. Based on this understanding of UV-ozone treatments and its affect on InP and InGaAs, the following surface preparation scheme was devised.

After photoresist development, the sample is treated for 10 minutes in UV-ozone to etch away any remaining scum and to oxidize the surface. Prior to loading into the E-beam evaporator for the base and collector contact deposition, the sample is dipped into a diluted NH_4OH solution to strip this oxide. The sample is dried immediately thereafter to prevent the re-formation of an oxide layer, leaving the surface with a minimal number of defects and associated surface states. This process cannot be used before the emitter deposition however, because NH_4OH reacts with SPR-955 and ruins the emitter photoresist lithography. A diluted HCl dip and short water rinse is used instead.

3.1.3 Thin interfacial Pd layer to the P$^+$ InGaAs base

Contacts to P^+ $\mathrm{In_{0.53}Ga_{0.47}As}$ while varying the interfacial Pd thickness, anneal temperature, and anneal time were investigated by Chor *et al.* [6]. Their detailed

analysis describes how Pd reacts with GaAs and InGaAs, diffusing through the interfacial oxides and disperses them uniformly away from the surface. X-ray diffraction studies showed that the *as deposited* Pd forms As-rich Pd_xGa_yAs phases at room temperature. After a high temperature anneal, the Pd forms Ga-rich Pd_xGa_yAs phases. Invariant of whether the sample is annealed, there is no evidence of an oxide-related species present at the metal-semiconductor interface. Oxide-free surfaces are not similarly witnessed when Ti is the interfacial metal. The dominant reaction between Ti and GaAs results in the formation of Ti_xAs_y and $Ga_xTi_yO_z$. These species change little when annealed and the interfacial oxides are still present.

While a UV-ozone treatment combined with NH_4OH dip have shown to be extremely effective in removed scum and surface oxides, some native oxides return to the semiconductor surface in the time it take to dry the NH_4OH dipped sample and load it into the E-beam evaporator. Because the lowest value of contact resistance to a semiconductor is achieved from an oxide-free surface, ohmic contact experiments to P^+ and N^+ InGaAs were performed at UCSB varying the interfacial Pd thickness, the anneal temperature, and the anneal time. For P^+ InGaAs, the lowest base ρ_c came from a Pd/Ti/Pd/Au contact 2.5/17/17/65 nm and no annealing. The contact resistance increases $\sim$ 50% after a 60 second anneal at 300°C. For N^+ InGaAs, no improvement was observed when an interfacial layer of Pd was used. When annealed, ρ_c would increase. A Ti/Pd/Au contact produced the lowest value of emitter

Table 3.1: Summary of InP HBT ohmic contact progress. Note, for these HBTs a base doping grade is employed and the values listed below reflect the doping value of the semiconductor the metal makes contact to.

Process date	Apr 03	Oct 03	Mar 04	Mar 04	Oct 04	Jan 05	Jan 05
DHBT	19b	mHBT	22b	24	25	26	27
Emitter ρ_c, $\Omega \cdot \mu$m^2	15	20	10.1	7.2	7.8	10.4	8.4
Cap style	InGaAs	InAs	In-rich	InGaAs	In-rich	In-rich	In-rich
Cap doping, cm^{-3}	$3{\cdot}10^{19}$	$3{\cdot}10^{19}$	$3{\cdot}10^{19}$	$3{\cdot}10^{19}$	$5{\cdot}10^{19}$	$5{\cdot}10^{19}$	$6{\cdot}10^{19}$
Base ρ_c, $\Omega \cdot \mu$m^2	20	14	9.6	6.1	6.2	3.8	4.6
Doping, cm^{-3}	$8{\cdot}10^{19}$	$4{\cdot}10^{19}$	$7{\cdot}10^{19}$	$8{\cdot}10^{19}$	$7{\cdot}10^{19}$	$7{\cdot}10^{19}$	$7{\cdot}10^{19}$
Collector ρ_c, $\Omega \cdot \mu$m^2	12	N/A	5.4	5.5	4.0	5.8	8.4
InGaAs contact, nm	12.5	25	12.5	10	8.5	8.5	6.5

contact resistance $\sim 8\ \Omega \cdot \mu$m^2, showing little variance before and after annealing.

For the N^+ sub-collector contact, the interfacial Pd cannot be used because its diffusion depth (even for thin Pd layers $\sim$ 2.5 nm) would exceed the thickness of the InGaAs layer. An effective contact to InP would result and its larger bandgap would greatly increase ρ_c. Regardless, low resistance ohmic contacts $\sim 6\ \Omega \cdot \mu$m^2 have been realized through a combination of good surface preparation and a Ti/Pd/Au contact to InGaAs layers as thin as 6.5 nm.

Tab. 3.1 summarizes the measured values of emitter, base, and collector contact resistance for different device process runs. The base and collector ρ_c were deter-

mined through standard transmission line measurement (TLM) extraction. Accuracy was ensured through visual inspection of the TLM dimensions with the FEI SEM. The emitter ρ_c was determined through either the 'fly-back' method or RF parameter extraction. Reproducibly, the emitter contact ρ_c is less than 10 $\Omega \cdot \mu$m^2, and the base and collector contact ρ_c is less than 6 $\Omega \cdot \mu$m^2. For DHBT 27, the collector ρ_c increased to 8.4 $\Omega \cdot \mu$m^2. This can be attributed to the thickness (6.5 nm for reduced device thermal resistance) of the InGaAs sub-collector contact layer. Even though non-alloyed contacts are utilized, there is a non-zero diffusion depth associated with the interfacial titanium layer. It is suspected Ti is beginning to penetrate through the InGaAs portion of the sub-collector, creating a mixed contact to InGaAs and the larger bandgap InP, and an increased ρ_c would be expected.

3.2 Advance lithographic scaling, device formation

When this work began, the Nanofabrication Research Facility at UC Santa Barbara had introduced many new tools – they included an E-beam evaporator (E-beam 4), Panasonic ICP etcher, local-alignment system to the GCA i-line photolithography stepper, and high-resolution low-voltage FEI Sirion SEM. Because device and circuit yield for the mesa HBT process was poor, many changes were required in order to yield devices with increased bandwidth and circuits employing such devices.

The new tools were utilized to find permanent solutions to the fabrication yield limiters – E-beam 4 provides improved metal lift-off profiles, the Panasonic ICP etcher offers consistent etch rates and profiles, the local alignment system of the stepper produces alignment registration errors of less than 150 nm, and the FEI SEM can inspect in detail the accuracy of all process steps. This section reports the existing problems at each step of the process and how they were corrected.

3.2.1 Emitter lithography and scaling

The narrowest device feature is the emitter contact. The emitter lithography from the transferred substrate process, and first generation mesa HBT process utilized a combination of SPR-950 by Shipley and CEM-365iS (contrast enhancement material) by ShinMicroSi photoresist process. CEM acts as a bleachable solution which is initially opaque, but becomes nearly transparent upon exposure. After spin-coating the soft-baked positive resist (changed to SPR-955 for the current process) with CEM, the pattern is exposed. The exposed areas of the sample are bleached more heavily, creating an in-situ contact mask. This results in an increased contrast level for the photomask pattern and smaller features can be realized. For the CEM to be effective, it must sit on the wafer for $\sim$ 60 seconds before being spun so that the pre-baked resist properly interacts with it. If CEM does not interact long enough with the photoresist, the increased contrast of the pattern will not be realized and a

poorer liftoff profile will result. This step had not been well documented and understood. This resulted in process deviation and is why an increased number of emitter short-circuits were experienced over time in the transferred substrate process [4]. Metal 'spikes' at the top of the emitter contact and metal 'strands' at the bottom of the contact were no longer present through the improved emitter lithography when combined with the use of the new e-beam evaporator tool (E-beam 4). Emitter contacts as narrow as 0.5 μm (0.4 μm emitter junction width), with high yield $\sim$ 100 % have been realized.

3.2.2 Base lithography and scaling

The base and collector semiconductor underneath the base contact represents the extrinsic base-collector capacitance ($C_{cb,ex}$) of the device. It is a consequence of the mesa device topology and is needed to supply bias to the base terminal of the HBT.

Processing limitations associated with the base contact must be clearly understood before it can be scaled to prevent the base contact resistance from increasing excessively. If we assume the minimum metal-semiconductor overlap required is equal to the transfer length L_t (typically 120 nm for the current process), an additional width due to the alignment registration error of the photolithography stepper, and the base-collector undercut during mesa formation adds to the minimum contact width. In general, the alignment error is 100 nm for the base contact and the

base-collector undercut is 100 nm. Therefore, the minimum base-contact widths fabricated for HBTs at UCSB is $W_{b,min} = W_{error} + L_t + W_{undercut} \approx 300$ nm.

A negative photoresist (PR is removed during development where not exposed) is required for the base lithography step to ensure that all unexposed photoresist is removed from underneath the emitter undercut before the self-aligned base contact is deposited. The photoresist used for this step had always been AZ-5214 by Clariant. Because AZ-5214 is susceptible to excessively undercutting the pattern during development, and the pattern focus would drift across the wafer, the base contact was often ragged and difficult to scale. A different photoresist was needed and nLOF (negative lift-off film)-2020 by Clariant was pursued. Through experiments, this negative resist demonstrated a high depth of focus for small features and little pattern undercut during development. This improved lithography step when combined with the new E-beam evaporator (E-beam 4) has produced narrow base contacts less than 300 nm wide without any liftoff artifacts remaining on the contact.

The process improvements to the emitter and base contact lithography and deposition were adopted amongst the remaining process steps. The stepper local-alignment feature is employed on all nine lithography steps before device passivation. In the event that the lithography fails, new advanced strippers like 1165 by Shipley and AZ-300T by Clariant can cleanly remove all unwanted PR without compromising surfaces where ohmic contacts are to be deposited. After six months of

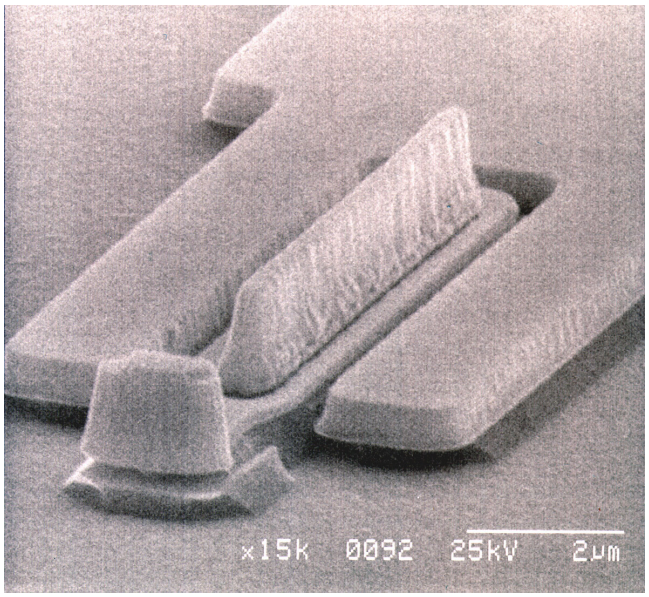

Figure 3.2: Angled SEM of an HBT before passivation

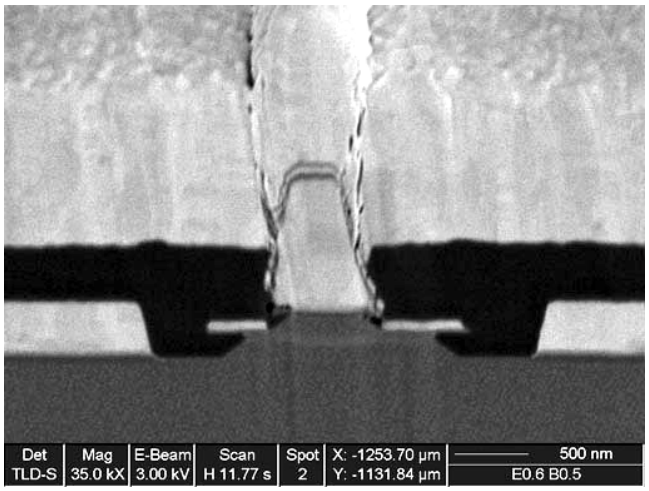

Figure 3.3: Cross-sectional SEM of an HBT after passivation and interconnect metal

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changes and amendments to the device formation part of the process flow, Fig. 3.2 and Fig. 3.3 show a profile and cross-sectional SEM of the updated HBTs from UCSB.

3.3 Old device passivation and interconnect process

The first mesa HBTs from UCSB utilized the transferred-substrate passivation and interconnect scheme. However, differences in device topology required some changes be made. For the TS-HBT process, the devices are isolated once the InP wafer is etched away. Mesa HBTs are isolated after the 300 nm sub-collector in the field is etched away and 100 nm of semi-insulating InP removed. Compared to TS-HBTs, the polyimide passivation thickness needs to be 400 nm taller for mesa devices.

The device interconnects for the TS-process employed a microstrip wiring environment. This was possible because a ground plane is generated before the carrier wafer is bonded and InP host wafer removed. This is not possible for mesa HBTs. Instead, a coplanar waveguide environment (CPW) is used for its simplicity, where low ε_o air and high ε_r = 12.8 InP sit above and below the interconnects. The large difference in dielectric constant and the thick substrate make this CPW environment vulnerable to radiative losses and parasitic substrate modes, making network ana-

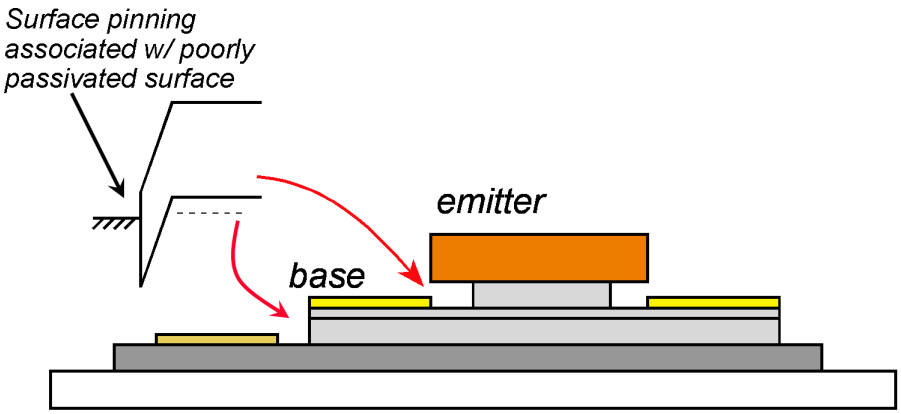

Figure 3.4: Device cross-section showing leakage paths for poorly passivated surfaces

lyzer measurements of high bandwidth HBTs difficult.

The following subsections discuss the passivation and interconnect scheme used in the old process flow and why they needed to be changed. Section §3.4 will detail how the required changes were carried out.

3.3.1 Polyimide passivation

InP and InGaAs surfaces that are exposed to the ambient environment or poorly passivated typically experience Fermi level pinning $\approx$ 200 meV below the conduction band edge (Fig. 3.4). For the exposed portion of the P^+ base, the surface pinning depletes $\sim$ 5 nm of the top surface (when $N_A \cong 7 \cdot 10^{19}$ cm^{-3}). When the base is thin (less than 40 nm), this depletion depth significantly increases the base resis-

tance. For the N^- emitter and drift collector, the exposed surfaces will no longer be fully depleted of mobile carriers and a leakage path is formed.

The original passivation of InP HBTs at UCSB used polyimide by HD Microsystems. It is applied as a liquid onto a substrate and then thermally cured leaving a smooth and rigid film across the wafer surface. When properly applied, all semiconductor surfaces will be encapsulated and the device leakage currents will be small. Through numerous small area HBT process runs, the Gummel curves showed variability in the leakage currents for the base I_b and collector I_c at moderate base-collector offset voltages. It was suspected that either the polyimide was not a well-behaved passivation material, or the polyimide was not filling in against the active device junctions. Cross-sectional SEMs of regrown emitter junctions (work pursued by D. Scott and Y. Wei) that were passivated in polyimide showed that the dielectric was not filling in well against the junctions and air filled voids remained. Mesa HBTs were assumed to be experiencing the same problem. Because the type of polyimide used was quite viscous and most likely the reason void-filling difficult, a more effective spin-on dielectric was pursued. Referencing other high-frequency $\mathrm{In_{0.53}Ga_{0.47}As}$/InP HBT results in the published literature, all used benzocyclobutene (BCB) to passivate devices. This was pursued on future device runs and explained in §3.4.3.

3.3.2 Interconnect step coverage

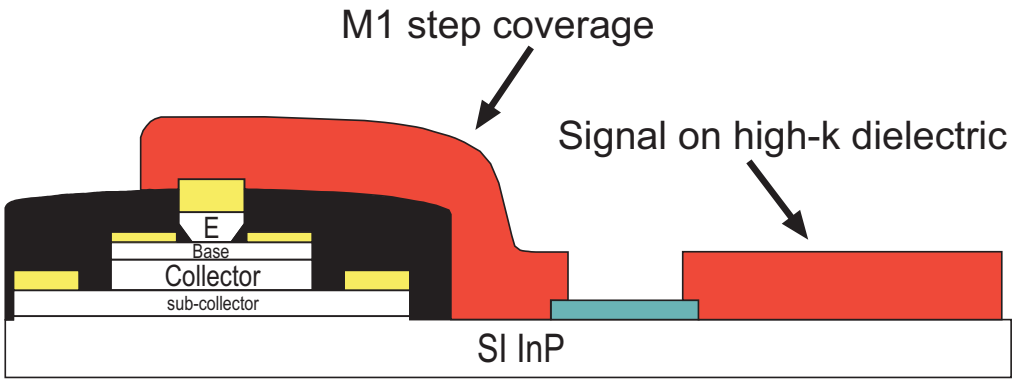

Figure 3.5: Old HBT process after passivation and Metal-1 interconnect

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The first mesa HBT process used polyimide for device passivation that was patterned to leave islands around the device. This was necessary for the TS-process in order to use collector metal for both the contact and as interconnect metal, however it is not necessary for the mesa topology. The mesa HBT height compared to the TS-HBT is 400 nm taller due to the sub-collector and isolation depth, and Metal-1 interconnect must climb 1.2 μm, (0.8 μm for the TS-process) to electrically contact the HBT. As Metal-1 in both processes is $\approx$ 1 μm thick, step-coverage is a greater concern for mesa devices. Fig. 3.5 and Fig. 3.6 show a drawing and SEM of the HBT after the patterned polyimide etch and Metal-1 deposition, where the large

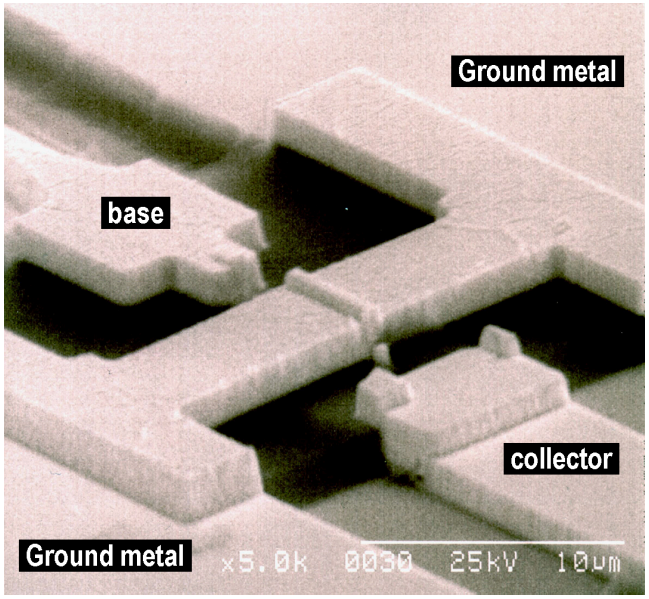

Figure 3.6: Old device interconnect scheme showing tall Metal-1 step-coverage

interconnect step can be observed.

In addition to the step-coverage issues with the wiring, substrate mode coupling to the CPW wiring [8] is exacerbated by having them rest on the ε_r = 12.8 InP substrate. The CPW guided mode propagates at the interface between the two dielectric media with a phase velocity υ_g that exceeds the TEM wave in the higher ε_r InP substrate υ_d. This condition causes energy from the guided CPW wave to be radiated into the substrate. For constructive interference, the radiated wave and the guided CPW wave should have the same propagation constant along the direction of the CPW transmission line. This requirement restricts the propagation direction of the

radiated wave to a semicone of angle θ, given by

$$\cos\theta = k_g/k_d = (\varepsilon_{eff}/\varepsilon_r)^{1/2} \tag{3.3.1}$$

where k_g and k_d are the propagation constants of the guided and radiated waves. Thus, energy transfer from the CPW mode into the substrate causes attenuation of the guided wave.

When the substrate thickness is finite and comparable to the dielectric wavelength, reflections from the back-side air-dielectric interface influence the behavior of the CPW structure. These are referred to as surface wave or substrate modes. In the frequency ranges where the propagation constants of the surface waves approach or exceed the CPW mode, the two modes are phase matched and interact strongly such that significant dispersion and radiative losses can occur. To prevent this condition from being satisfied, the operating frequency should not exceed that associated with the lowest order TE_o and TM_o substrate modes. This is the case when the substrate height $h < 0.12\lambda_d$, where λ_d is the wavelength in the substrate. For a 635 μm thick InP substrate (typically used in this work) where the CPW lines rest, the lowest order TE_o and TM_o substrate modes are excited at $\sim$ 20 GHz. Consequently, measurement of HBTs having several hundred GHz bandwidth is very difficult in this wiring environment. To alleviate the parasitic mode coupling, the interconnects should be suspended above the InP substrate using a low ε_r dielectric. By doing so, less signal energy is coupled into the substrate reducing the parasitic effects.

3.4 New device passivation and interconnect process

With the device fabrication updates completed for the front-end and issues associated with the passivation and interconnects well understood, changes to the mesa HBT back-end could go forth. Realizing that polyimide did not consistently passivate the HBTs well, BCB was pursued as an alternative. Experiments were undertaken to learn how to adequately prepare the HBT surfaces, how BCB should be etched and how quickly to etch it, and how well the suspended metal interconnects would adhere to the planarized BCB surface. Furthermore, these new process steps would need to maintain their physical and electrical integrity to the end of the process where MIM (metal-insulator-metal) Si_3N_4 capacitors and additional BCB cures are required to produce circuits. All of these associated experiments were pursued concurrently.

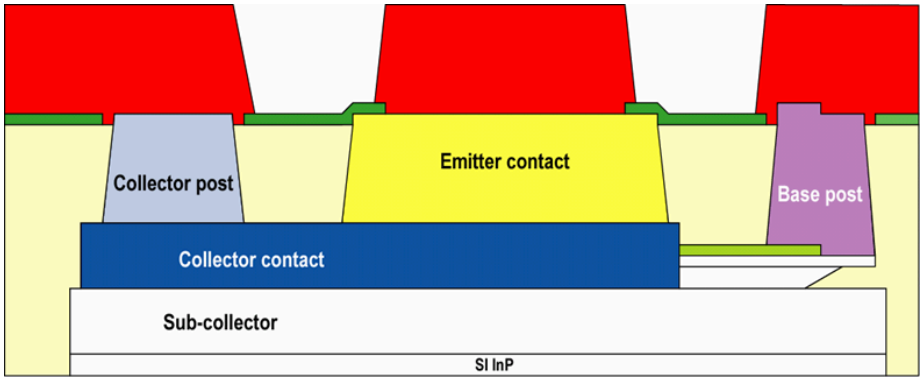

Figure 3.7: Updated HBT cross-section after passivation and Metal-1 interconnect

3.4.1 Interconnect posts for a planar wiring environment

Fig. 3.7 shows a cross-section of the desired HBT process after device passivation and interconnects. In order to have a suspended wiring environment above the substrate, two modifications are required before the devices can be passivated and the wafer planarized. The incorporation of a collector post that is of equal height to the tall emitter contact and base post is needed. This will allow the three HBT terminals to be contacted from the suspended surface, compared to the polyimide passivated HBT (Fig. 3.6) where the collector signal line rests on the collector contact. A similar interconnect post is added to support resistors because they must reside on the substrate for heat-sinking purposes and will be buried underneath the dielectric. To realize both the collector and resistor post without adding unnecessary steps, the order of the process flow was modified.

After the base-collector mesa formation etch, the collector contact is typically deposited. Instead, the device isolation etch is performed and the resistors are deposited on the semi-insulating substrate. At this point, metal is deposited that simultaneously contacts the collector and the resistors. Even with the semiconductor height difference between the collector and resistors, the wide focus range available from nLOF-2020 (photoresist used for collector contact lithography) makes this simultaneous deposition possible. Lastly, a $\sim$ 0.8 μm tall post is deposited on the collector contact and separately a $\sim$ 1.2 μm tall post is deposited on the resistor

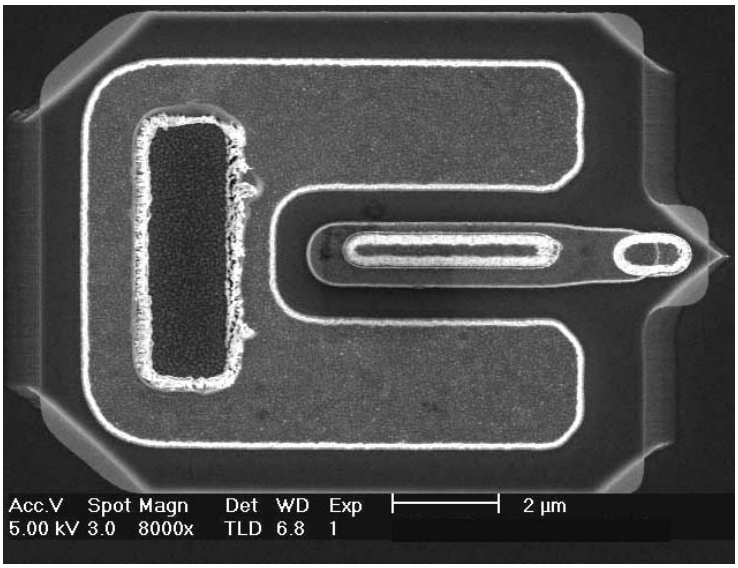

Figure 3.8: SEM, top view – 0.6 μm emitter width, 1.3 μm collector mesa width

contact for Metal-1 interconnection.

Because of the processing experience that had accrued overtime, introducing these steps and changes required little new process development. A close-up SEM of this modified mesa device is shown in Fig. 3.8. Compared to Fig. 3.2, there is a collector post and the collector contact resides inside the device isolation etch border. This border is approximately 1 μm on all sides to ensure the contact does not exceed the mesa edge. A circuit SEM of a divide-by-2 circuit interconnect bus is shown in Fig. 3.9 – showing the devices, collector interconnect metal, resistors, and interconnect posts. The wafer is ready for device passivation and planarization.

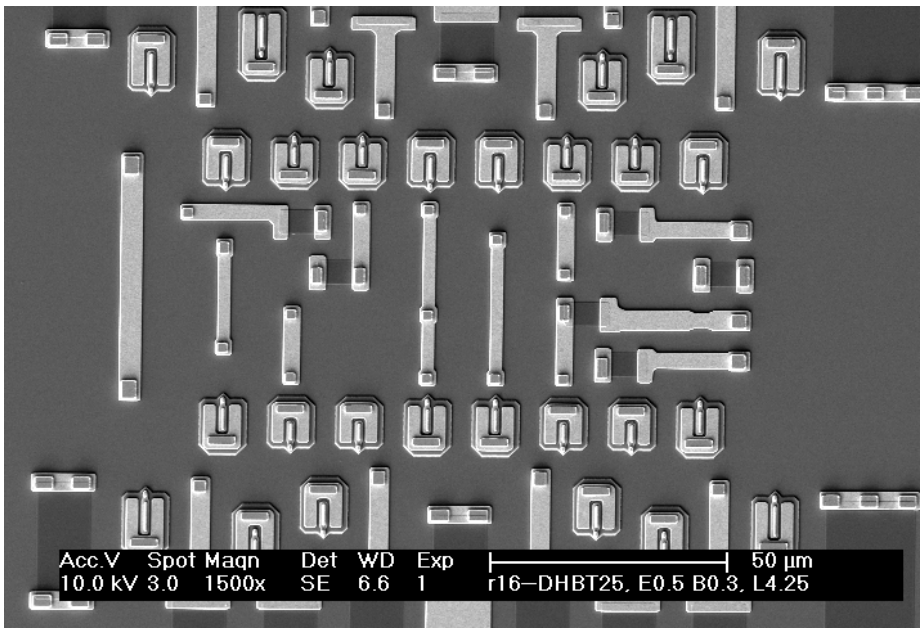

Figure 3.9: SEM of divider core before device passivation and metal interconnects

3.4.2 Metal adhesion to the spin-on dielectric surface

Experiments were performed to learn how well metal interconnects adhered to a spin-on dielectric surfaces. Polyimide was deposited and cured on many test samples, and the surfaces were prepared differently. In the cases where interconnects were deposited directly on the polyimide surface, all of the metal peeled away during lift-off. This was also observed for samples having 400 nm of polyimide etched away to roughen the deposition surface and increase adhesion. The surface preparation that was found to be effective involved etching 400 nm of dielectric from the surface and then depositing 100 nm of Si_3N_4 over the samples before depositing in-

terconnect metal. After lift-off and needle probing, the metal did not show any signs of peeling or deformation.

One RF HBT process run was completed using polyimide passivation and raised interconnects. After the polyimide etchback and Si_3N_4 deposition, vias were etched to expose the HBT contacts. Because of unforeseen problems associated with the polyimide etch-back, not enough was removed and / or the via etch was not deep enough. A thin layer of polyimide is thought to have remained over the contacts, such that HBT yield was limited by open-circuits or a large emitter resistance was present during the measurement. This was noted for future process runs. Nonetheless, while HBT performance was poor, the interconnects maintained their integrity after numerous probings.

3.4.3 BCB passivation

The height from the substrate floor to the top of the device interconnect posts is ≈ 1.8 μm. A benzocyclobutene by DuPont (*BCB 3022-35*) was chosen for its low viscosity and because it could be spun-on uniformly at a thickness of ~ 2 μm. Before it could be utilized for HBT passivation, experiments were performed to determine how the wafer surface should be prepared before coating with BCB, how it should be etched, and the preferred manner of inspection to ensure all of the interconnect posts are exposed.

There were no instructions accompanying the BCB suggesting how the semiconductor surface should be prepared. Understanding the importance of removing surface oxides for minimal leakage currents, the same surface preparation for the base and collector contact deposition was attempted – a 10 minute UV-ozone treatment, followed by a 10 second diluted NH_4OH:H_2O 1:10 dip, and N_2 dried with no water rinsing. The wafer was immediately coated with BCB. To be certain it filled in well against the HBT junctions, it rested on the surface for 30 sec before being spun to a final thickness of ~ 2 μm. Lastly, the sample was quickly loaded into the Nanofabrication facility 'Blue Oven' to prevent oxygen from contaminating the uncured BCB.

The Panasonic inductively coupled plasma etcher (ICP) was utilized for BCB etching. Through trial and error experimentation using Si dummy wafers, a CF_4:O_2 50:200 sccm (1000 W power) recipe was determined to be most useful. The BCB etch rate associated with this recipe was $\sim$ 250 nm / minute and it left the surface smooth.

During the etching experiments it was discovered that there is a BCB height difference of $\sim$ 200 nm from the center of the sample (thicker) to the edge (thinner). This amount of non-uniformity was within the processing limits and attempts to remove it were not pursued. Because there was no laser monitoring system in the ashing chamber of the ICP and excessive overetching would ruin the sample, an

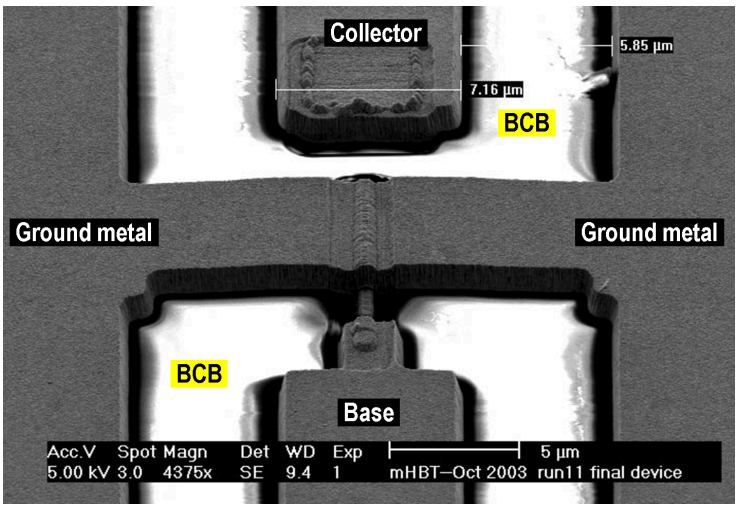

Figure 3.10: Planar device interconnect scheme: metal interconnect on 1.7 μm of BCB above InP substrate

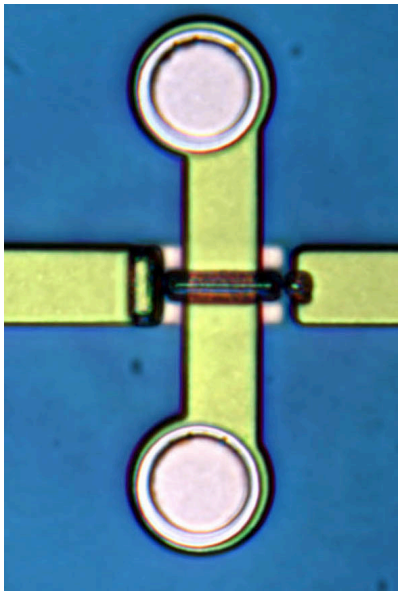

Figure 3.11: IC micrograph photo of device within test structure after passivation

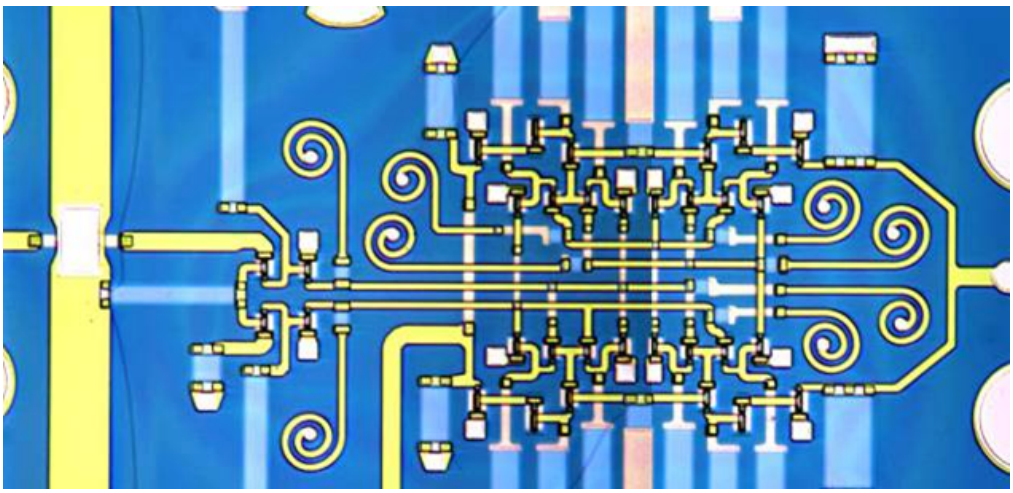

Figure 3.12: IC micrograph photo of a static frequency divider interconnect bus after Metal-1 interconnect

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iterative etching scheme was used. Once the BCB is cured, 300 nm is blanket etched in the ICP and then inspected at low-voltage in the FEI SEM to confirm that all of the interconnect posts are exposed. If they are not and BCB remained, an additional 100 nm is etched and inspected again. This is repeated until 300 nm of the posts are exposed.

As with the planar wiring environment, the transition from polyimide to BCB was straight forward with few problems. The Si_3N_4 interconnect adhesion layer was well behaved and the metal liftoff profile was clean. An SEM of a completed HBT after BCB passivation and interconnect deposition is shown in Fig. 3.10, and an optical photograph is shown in Fig. 3.11. Fig. 3.12 shows the same divider interconnect bus from Fig. 3.9 after Metal-1 deposition and MIM capacitor formation without

any evidence of BCB degradation.

3.5 Thin-film microstrip for mesa HBTs

A coplanar waveguide environment (CPW) was used for mesa HBTs for simplicity, because devices could be tested after the first layer of interconnect metal is deposited. If not properly designed, CPW is susceptible to the excitation of parasitic modes (shown in Fig. 3.13) that can corrupt transistor and circuit measurements. To suppress each of them, additional processing steps are needed: ground vias for microstrip modes, wafer thinning for substrate modes, and ground straps for slot modes. Also, multiple ground breaks in complex ICs introduces ground return inductance to various parts of the circuit and must be considered during design.

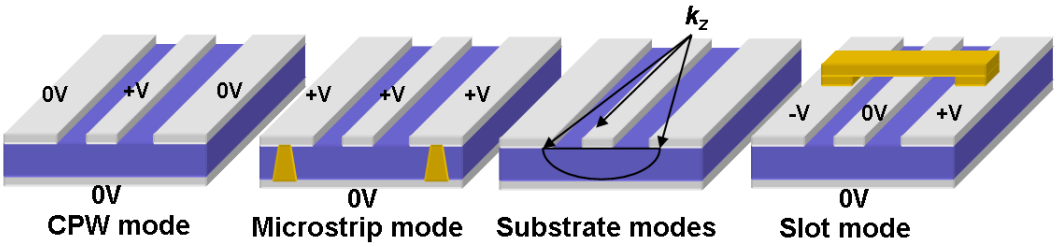

Figure 3.13: Coplanar wiring environment – showing the CPW and parasitic modes

CPW substrate modes are not easily suppressed at higher frequencies $>$ 20 GHz, and their presence makes vector network analyzer (VNA) calibration and subsequent S-parameter measurements difficult to achieve. The Thru-Reflect-Line (TRL)

method is most commonly used to calibrate the HP 8510C VNA at UCSB before HBT testing [7]. This method does not require accurate characterization of all of the calibration standards. The TRL calibration utilizes two transmission line standards – the 'Thru' standard and the 'Line' standard. The line standard differs from the Thru line by an electrical length ΔL, related to the frequency span being examined. The Reflect standard is satisfied through the use of an open or short circuit termination.

From the measured calibration standards, the reflection coefficient Γ of the Reflect and propagation constant of the Line standard are determined. The only parameter that must be precisely known is the characteristic impedance Z_o (typically 50 Ω) of the Line standard,

$$Z_o = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \tag{3.5.1}$$

This characteristic impedance is the reference impedance for the calibrated measurements, having a magnitude and phase associated with it – i.e. both real and imaginary parts. Resistive losses at low frequency and skin effect losses are $\propto \sqrt{\omega}$. The effect of surface impedance (skin effect) on β however tends to decrease at higher and higher frequencies. These resistive losses can be accurately modeled within an electromagnetic (EM) simulator such that a complex impedance correction can be applied to the TRL calibration, and the measured S-parameters converted to a reference impedance of 50 Ω as expected by the VNA [9].

Energy coupled into the semiconductor in the form of substrate modes appears

as an effective conductance G, altering the effective Z_o. This is not accounted for well in the EM simulation and hence cannot be applied to the complex impedance correction. As the frequency increases, higher order TE and TM substrate modes will be excited (appearing as resonances on the Smith chart) and Z_o will diverge further away from $50\ \Omega$. The TRL calibration will not be effective and the accuracy of the S-parameter measurements will poor. Unless the wafer is thinned to less than 125 μm ($f_{cutoff} \sim$ 100 GHz), an alternative wiring environment is needed in order to lessen the parasitic substrate modes, and have accurate VNA calibration and device measurements.

The transferred-substrate HBT process is very difficult, however by soldering the host wafer to a carrier and removing the substrate, a ground plane is formed and a thin-film microstrip wiring environment can be used. Because the dielectric height between the signal line and ground plane is $\sim$ 5 μm, parasitic modes ($f_{cutoff} >$ 500 GHz) will not be excited at the frequencies HBTs and circuits are tested. Radiative probe-to-probe coupling though has interfered with device measurements at frequencies greater than 200 GHz. Unable to use the style of microstrip from the transferred-substrate process, an inverted microstrip interconnect scheme was conceived – shown in Fig. 3.14, where the ground plane is the top-most layer of metal. After Metal-1 is deposited and capacitors are formed, posts $\sim$ 3.5 μm tall are electroplated or evaporated. BCB of the same thickness is spun, cured, and etched back

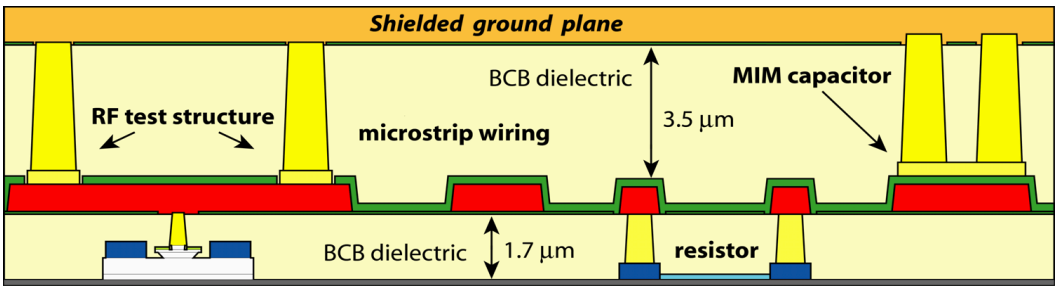

Figure 3.14: Cross-section of the mesa HBT process, showing its thin-film microstrip wiring environment

to reveal the posts. Lastly, the ground plane is formed.

From a circuit design standpoint, using thin-film microstrip is advantageous as well because it is more predictable and easier design in to. Ground straps required for CPW to maintain ground plane continuity are not needed and Metal-1 can be used solely for signal interconnects. Amplifier design is simplified through the use of microstrip because 2-D and 3-D electromagnetic simulators like Momentum by Agilent can more accurately predict the impedance of signal lines, along with the capacitance and inductance of various structures. The thin-film dielectric between the ground plane and signal line permits the interconnects of digital and mixed-signal circuits to be placed more closely together without compromising signal integrity, thus decreasing the wiring parasitics and delays. Lastly, the ground plane shields the core parts of amplifiers and digital circuits of interference from the probed input and output signals.

The final point is of particular importance for discrete HBT measurements. By shielding the signal lines from the probe pad to the device, probe-to-probe coupling can be significantly reduced. On-wafer TRL VNA calibration structures (discussed in Chapter 4) allow the HBT test structure to use long signal lines between the probe pad and terminal of the device (where the reference plane is set). The increased distance has reduced probe-to-probe coupling effects. Through the combined use of the long signal lines for increased probe spacing, inverted microstrip where the ground plane shields the signal lines, and shielded probes where the signal line is covered by a ground plane until the edge of the probe [6], excellent VNA measurements of HBTs should be possible to 300 GHz with minimal parasitic substrate mode coupling due to the large probe pad.

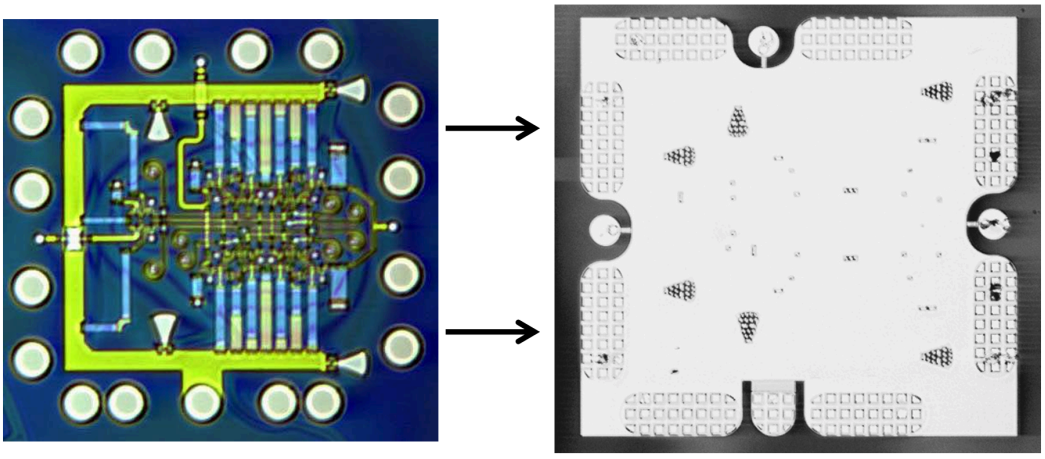

Figure 3.15: Fabricated divide-by-2 before and after final ground-plane metalization

This inverted microstrip is employed as the wiring environment for the static frequency dividers reported in Chapter 5 and proved to work well. Fig. 3.15 shows a divider circuit before and after ground plane deposition. Device results are not available at this time.

3.6 Process challenges for UCSB metamorphic DHBTs

Even though InP DHBTs have demonstrated higher bandwidths and breakdown voltages compared to SiGe HBTs at similar levels of scaling, the high cost and low breakage strength of InP substrates have hindered it acceptance beyond low-volume, commercial manufacturing environments. Metamorphic growth of InP-based DHBTs on GaAs substrates has been investigated as a means of accessing the properties of InP in a GaAs manufacturing environment with lowered costs. For these devices to be useful in high speed circuit applications, a low C_{cb}/I_c ratio (high J_e) is necessary, requiring the device operating temperature be addressed during device design [11]. Because the metamorphic buffer layer can have a significant impact on the thermal resistance of the HBT [12], InP is used as the buffer for its higher thermal conductivity. While these buffer layers are capable of removing the strain associated with the 3.8% lattice mismatch between GaAs and InP, InP buffers cannot suppress defects in the growth of the device layers to the low levels observed with graded ternary buffers [13]. However, the thermal resistance of mHBTs using low thermally conductive ternary buffer layers (InP = 68 W/K-m, InAlAs = 9.9 W/K-m, InGaP = 15 W/K-m) is such that these devices when biased at current densities required for high bandwidth would exhibit several 100°C self-heating [14].

Cross-sectional TEM (transmission electron microscopy) images of the mHBT epitaxy from the results to be reported [15] are shown in Fig. 3.16 and Fig. 3.17.

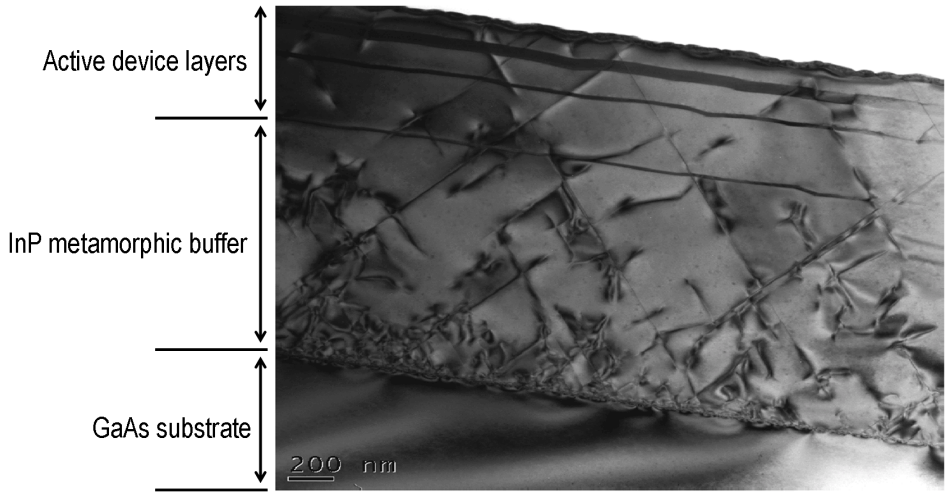

Figure 3.16: Observed InP metamorphic buffer defects from epitaxy growth

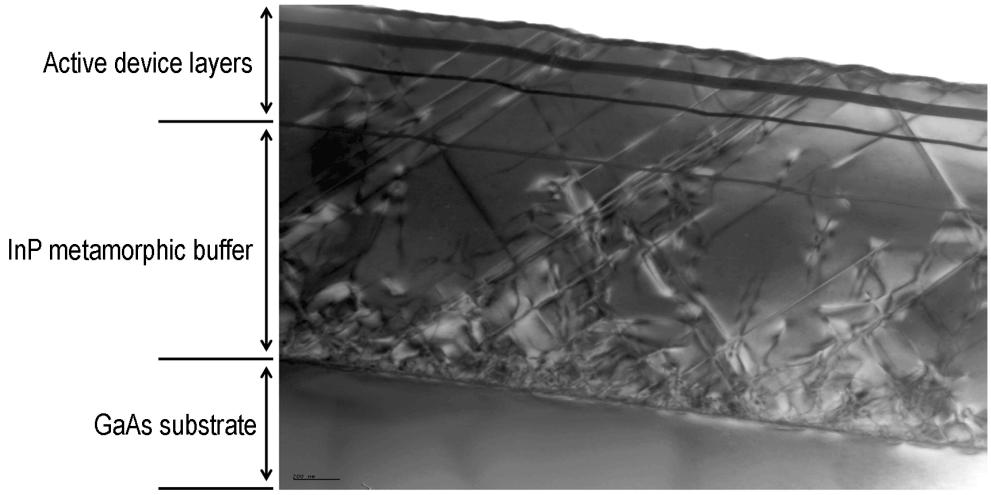

Figure 3.17: Observed InP metamorphic buffer defects–different location

There is a defect density per unit length emitter of 5-6 $/\mu$m [16], which results in 35-45 defects for a 0.5×7 μm^2 mHBT. Despite this, the transistor yield is similar to that observed for lattice-matched HBTs (LM-HBT, where the host wafer is InP) from UCSB. Thus the present data does not support any conclusion that the defect density from the InP metamorphic buffer impacts transistor performance or yield.

The primary research on metamorphic HBTs from UCSB was conducted by Dr. YoungMin Kim, and results from that work have been reported in [12] and [17]. They discuss in detail the thermal resistance of a number of metamorphic buffer schemes, along with RF performance of small area DHBTs. The process used to fabricate these older mHBTs is the same as discussed in §3.3, where limitations associated with device scaling and passivation lessened their performance.

The surface morphology of the mHBT is very rough compared to LM-HBT growths. For LM-HBTs having a low defect density and smooth surface, the wet-etch behavior is easily observed and can be well controlled. The surface roughness associated with mHBTs however makes observing the semiconductor wet-etch difficult. Consequently, an underetch or overetch of a mesa features can happen unintentionally. In the case of an underetch, semiconductor material remains above the layer that is to be revealed. Because the wet-etch chemistry used to remove InP and InGaAs is highly selective, an underetch of the preceeding layers would prevent subsequent layers from etching where material remained and the process run would

be ruined. Excessive emitter undercut is undesired because it would create a larger gap underneath the emitter contact between the emitter mesa and base contact. This larger gap unnecessarily increases the base resistance and reduces f_{max}.

The process improvements reported in §3.2.1, §3.2.2, and §3.4 to scale the HBT footprint, passivate the device in BCB, and raise the interconnects from the substrate were adopted for future mHBT process runs. The inability to determine when the InGaAs and InP etches ended was still of concern. §3.6.1 and §3.6.2 will discuss the additional process-step employed to reduce base-leakage and increase mHBT device yield.

3.6.1 Difficulties etching the emitter mesa

Through a series of experiments it was discovered that during the emitter semiconductor wet-etch in the mHBT process, the InP in the field is completely etched away, but N^- material surrounds the emitter mesa – shown in Fig. 3.18 and Fig. 3.19. In some places, what appears to be InP strands protrude beyond the emitter undercut and touch the self-aligned base contact. While contacting this metal did not impair device performance significantly, base-leakage currents were higher and yield suffered because of the raised base metal on the N^- semiconductor short-circuiting to the emitter contact. Sometimes this metal could be 'burned-off', where in some instances a V_{be} greater than the device turn-on $\sim$ 0.8 V would be required. However,

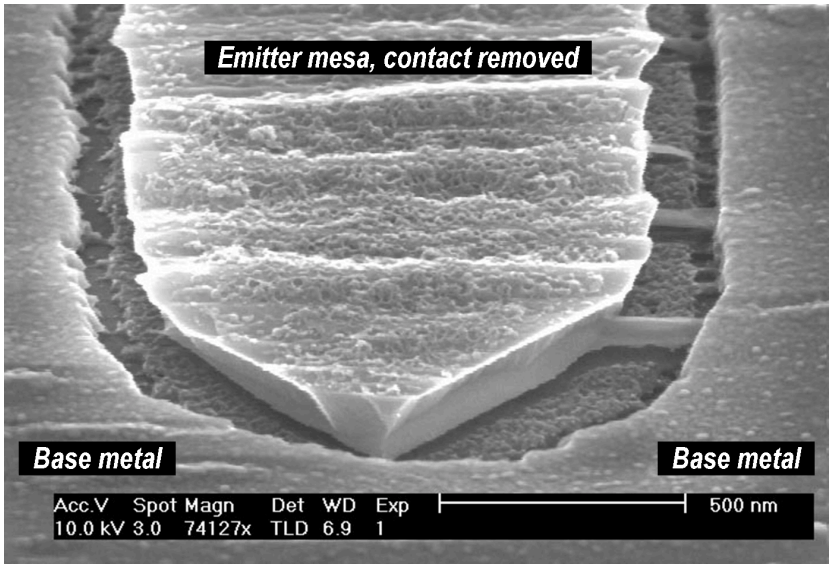

Figure 3.18: Inspection of emitter mesa after wet-etching. Note, the emitter contact has been removed

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if circuits were pursued, they would not bias properly.

It is suspected that during the growth transition from the InGaAs base to InP emitter, Ga and/or As is unintentionally incorporated in the initial layers of the emitter. If there is a thin layer of InAsP or InGaAsP above the base, the semiconductor etch-rate would become slow for these materials because of the wet-etch solution being used. Furthermore, the etch-rate of this material would be even slower around the emitter mesa where the wet-etch solution circulates less. This is most likely why the base semiconductor is exposed in the field and the emitter mesa is surrounded by this N^- material. Rather than correcting the epitaxial growth at this time, a dielectric sidewall spacer solution was pursued.

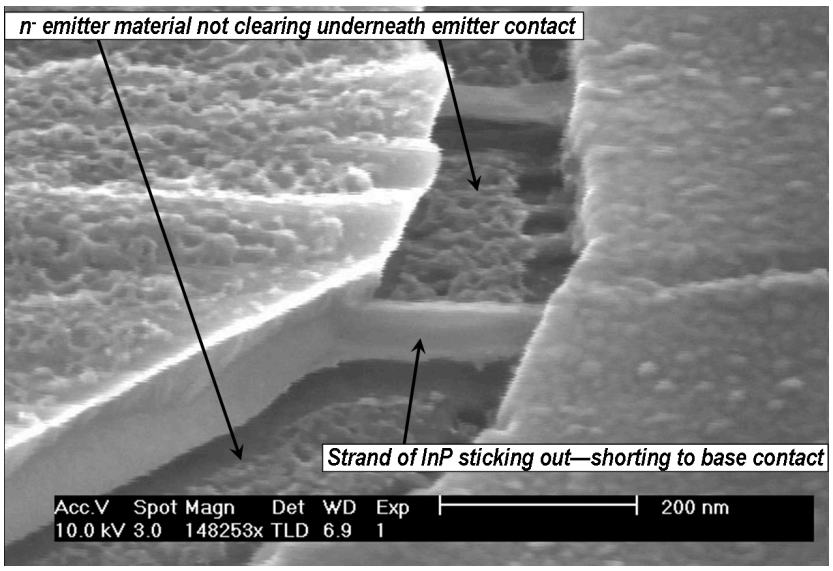

Figure 3.19: Inspection of the N^- semiconductor between the etched emitter mesa and self-aligned base contact

3.6.2 SiO_2 dielectric sidewall solution

Dielectric sidewall spacers around the emitter contact of InP HBTs has been investigated as a means of electrically isolating the emitter and base contact in more advanced device processes. The same type of dielectric spacer is used here for a different purpose for mHBTs to increase the spacing between the base contact and any residual material associated with the emitter undercut. Fig. 3.20 shows the process steps involved in fabricating the sidewall and are described here.

After the emitter contact is formed, 100 nm of SiO_2 is deposited on the wafer by plasma enhanced chemical vapor deposition (PECVD). The wafer is then etched anisotropically by reactive ion etch (RIE) using a CF_4:O_2 gas mixture. This etch

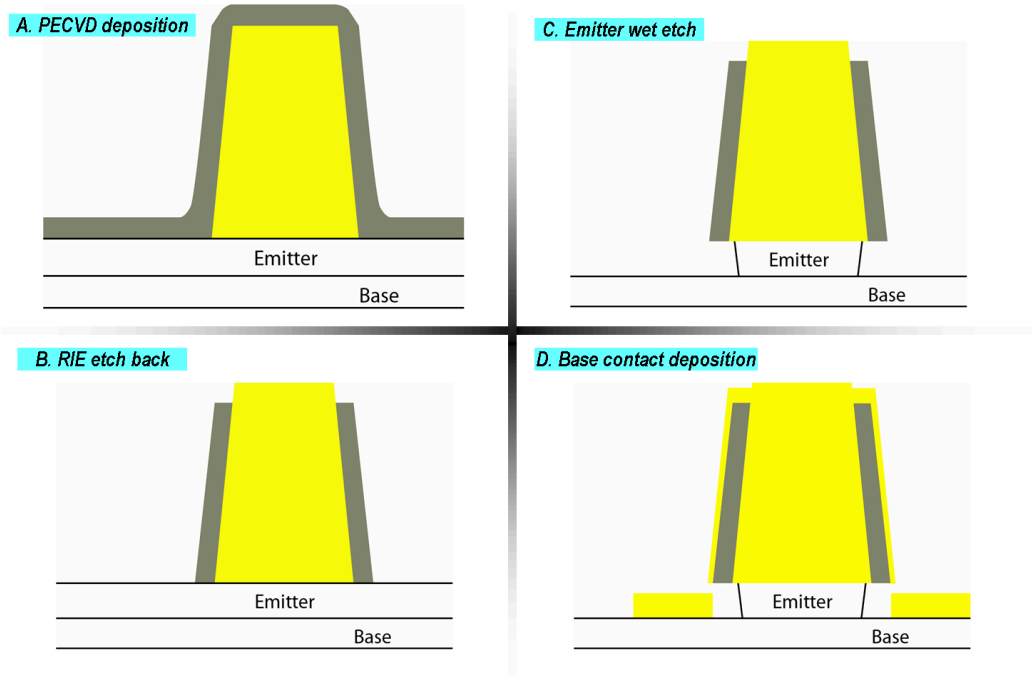

Figure 3.20: Process flow for emitter dielectric sidewall spacer

removes SiO_2 from the field and leaves an 80 nm sidewall around the emitter contact. The emitter mesa is wet-etched. Lastly, the self-aligned base contact is deposited with an additional 80 nm spacing from the emitter mesa edge.

A cross-sectional SEM of the mHBT shown in Fig. 3.21, where the dielectric sidewall and emitter undercut are highlighted. While this sidewall alleviates the emitter mesa etching issues, the base gap resistance $R_{b,gap}$ between base contact and emitter mesa is $\sim 2.5\times$ higher due to the spacer. Separating process-related issues from growth-related issues when measuring mHBT electrical performance is im-

perative to understanding the differences between mHBTs and their lattice-matched counterpart. The results in Chapter 4 will reveal that the DC and RF performance of mHBTs and LM-HBTs is very similar.

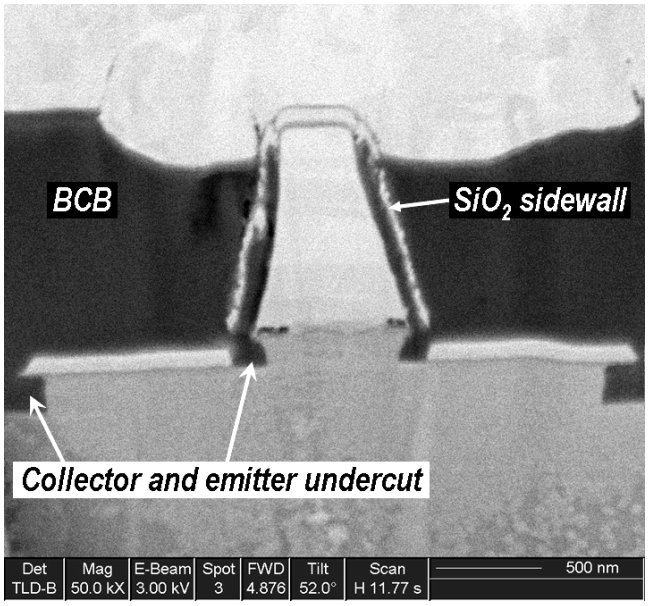

Figure 3.21: Cross-sectional SEM of an mHBT after passivation and device interconnect

3.7 Summary

This chapter reports the efforts undergone in order to create a high frequency InP DHBT process with increased bandwidth and high yield. Process steps have been added to support small-scale circuits. Chapter 4 reports recent RF HBT results from UCSB using this updated process. Static frequency dividers have been yielded as well and are reported in Chapter 5. The final process-flow is given in Appendix B.

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4

InP DHBT Device Results

THIS chapter reports discrete device results for InP DHBTs fabricated from UCSB – a continuation of the research by M. Dahlström [9]. Combined with the new HBT process reported in Chapter 3, the device epitaxy was designed to simultaneously increase f_τ and f_{max}, and reduce the C_{cb}/I_c ratio for use in small-scale digital integrated circuits. Thermal resistance, emitter resistance, and base resistance are the key barriers to HBT scaling. As the DHBT results are reported, there will be a discussion of the intended use of the device, what changes were made to the layer structure compared to its predecessor, along with measured DC and RF results.

4.1 VNA calibration methods

Accurate and repeatable on-wafer two-port device measurements require a well characterized measurement environment. For the HBTs reported in this work, their bandwidths far exceed the DC-110 GHz frequency span covered by typical com-

mercial vector network analyzers (VNA). Modules are available for testing at higher frequencies, however device data in these frequency bands are not needed to determine the f_τ, f_{max}, and C_{cb}/I_c of an HBT. Furthermore, the challenges associated with achieving accurate measurements $>$ 110 GHz are beyond the scope of this work.

Before measurements can commence, a two-port VNA calibration is required so as to place the measurement reference planes precisely at the input and output of the device-under-test (DUT). In an on-wafer measurement environment, this requires stripping from the measurements the contributions from delays and losses associated with microwave cabling, the wafer probes, and the on-wafer transmission line network that the DUT is embedded within. A VNA calibration is performed by measuring a set of defined calibration standards. From the S-parameter measurements of these standards, a set of error correction coefficients are determined and used to calibrate the VNA and subsequent measurements. A discussion of the derivation and formulation of the error correction terms is complicated and not included – however, the following references [1, 2, 3, 4] provide detailed mathematical derivation of various VNA calibration schemes.

There are two approaches available to realize the VNA calibration standards – invariant of the calibration method used. The first is realized by utilizing a calibration substrate different from the DUT. Such substrates are commercially available and

are effective in calibrating a VNA from DC-110 GHz. These substrates are typically fabricated using thin-film processes on alumina, where coplanar waveguide (CPW) is the wiring environment employed. Because the calibration is designed to place the measurement reference planes at the wafer-probe tips, this method is often referred to as a *probe-tip* or *off-wafer* calibration. This approach is commonly used for on-wafer DUT measurements and offers the advantage of having well-characterized, precision calibration standards. There are two drawbacks however associated with using a calibration substrate that is different from the DUT.

The probe spacing between the calibration standards is of a distance where electro-magnetic field coupling between port 1 and port 2 is experienced. If the coupling is constant and the same for all standards measured during the calibration, their effects are less severe. At frequencies > 50 GHz, this is not a reasonable expectation. Increasing the signal-line spacing between the probe-pad and terminals of the device would lessen the effects of the fringing fields. However, for a probe-tip calibration, the effects of the embedding structure (probe-pad and signal lines) must be removed from the measurement so that the S-parameter measurements only contain data about the device – i.e. the reference planes are moved from the probe-tips to the device terminals. An approximate approach often used to account for the device test structure is to measure the open-circuit network capacitance of the structure without a device present and subtracting it from device measurements using

S-parameter simulation software. Because HBTs having very high bandwidths have little capacitance, this approach can generate considerable error. Also, this approach ignores the series resistance and inductance of the embedding network, both having values that effect high bandwidth devices.

A more precise determination of the electrical characteristics is done by measuring both the open *and* short-circuit test structures, and subtracting the measured Y-parameters and Z-parameters, respectively, of these networks from measurements of the DUT [5]. This approach is conditioned upon the physical length of the embedding network being small relative to the propagation wavelength at the measurement frequency. De-embedding the entire test structure this way is particularly attractive because it removes any residually generated human error due to mis-interpretation of the lumped equivalent circuit from the open and short-circuit structures. An additional comment: as already mentioned, there are limits as to the length of the signal lines in the embedding network in order to suppress port-to-port fringing fields. Recently, probes have become commercially available where a shielded ground-plane covers the signal line of the probe [6] until the tip is reached–used in the measurements of DHBT 27, to be discussed. Typically, probe-to-probe coupling causes the device Unilateral power gain to progressively roll-off at greater than -20dB/dec for frequencies beyond 50 GHz. By removing the fringing field transmission between port 1 and port 2, their effects are removed from the S-parameter measurements –

increasing the accuracy of device characterization.

The second way of realizing the calibration standards is to design them custom to the process associated with the DUT on the same wafer. Using this approach, calibration standards can be realized in the same embedding network used by the DUT and the measurement reference planes can be placed at the device terminals. Also, unlike with probe-tip calibrations, the signal lines can be made longer to reduce fringing fields. The trade-off of this approach is that the realization of precision calibration standards repeatably on the substrate over numerous process runs may be challenging and require some post-processing of the S-parameter data to account for such deviations between the expected and realized calibration standard values. At higher frequencies however, these deviations have less and less effect on the measurements of the device.

There are a number of different VNA calibration methods that could be utilized to calibrate the system. The calibrations differ in the standards that are measured, and in the assumptions made regarding the standards for determining the error-corrections terms. The calibration methods are named according to the standards that are measured in the method; they include Short-Open-Line-Thru (SOLT), Thru-Reflect-Line (TRL), Line-Reflect-Match (LRM), and Line-Reflect-Reflect-Match (LRRM). In this work, TRL (probe-tip and on-wafer) and LRRM (probe-tip) techniques are used for VNA calibration, and are briefly reviewed.

The LRRM method [2] is well suited for two-port VNA calibration in a coaxial measurement environment where the desired frequency span to be tested is large. An example would be a DC-110 GHz single sweep on an Agilent 8510XF VNA system. The accuracy of the standard models used in the calibration need not be known to a high level of accuracy. The models expected include two independent reflect standards – a dual one-port device made up by two identical, isolated loads with a reflection coefficient Γ_{r1} for Reflect '1'and Γ_{r2} for Reflect '2'. To assure independent measurements, a non-ideal open-circuit and non-ideal short-circuit should be used in the determination of Γ_{r1} and Γ_{r2}. The Match standard is modeled as a resistor R having a series inductance L, where R must be known (and have a similar value as the Line impedance) and L is determined from the calibration. The Line standard provides a fixed value of electrical delay.

Unlike the LRM calibration method where two known and electrically identical Match standards are needed (for Port 1 and 2), the additional Reflect used by LRRM eases this condition and increases the accuracy of the calibration. An additional benefit is that all LRRM standards can be realized with a fixed probe-to-probe spacing, lessening fringing field effects. Note, the LRRM calibration is generally not an available technique in VNA hardware (like the Agilent 8510C and 8510XF systems used for HBT testing in this work), however it can be implemented into the VNA through the use of commercially available controller software [8].

Like the LRRM calibration, the TRL calibration does not require an accurate characterization of all of the calibration standards. The calibration uses two transmission line standards – one designated as a 'Thru', and the other 'Line'. The Line standard differs from the Thru by some electrical length ΔL. The Reflect standard may be an open or short circuit termination.

The solution for the error terms in a TRL calibration is over-determined, and the reflection coefficient associated with the Reflect standard and the propagation constant of the Line standard can be determined from calibration measurements. The only parameter that must be accurately known is the characteristic impedance Z_o of the Line standard. This Z_o becomes the reference impedance for the calibrated measurements and it is important to remember that this impedance has frequency dependent real and imaginary parts. Methods are described in [7] how this frequency dependence of the characteristic impedance is accounted for and corrected in the device measurements.

An often cited disadvantage of the TRL method is that one Line standard can only cover a 1:8 frequency span, with the ideal ΔL being a $\lambda/4$ wavelength at the center of the span. As such, multiple Line standards are required to cover larger frequency ranges, and low frequency standards take up large amount of die area. Multiple Line standards may also be utilized to provide measurement redundancy in a given band. Interested readers are referred to [1, 3, 7] for a complete discussion of

the TRL calibration method.

4.2 150 nm collector, 30 nm base – DHBT 19b

At the time this work began (September 2002), the best reported HBT result from UCSB (DHBT 17) was fabricated in the old UCSB process with a 200 nm collector and 30 nm base, exhibiting a 282 GHz f_τ and $>$ 400 GHz f_{max} [10]. The yield was $<$ 10% and DC current gain $\sim$ 15. Also, the collector doping was chosen such that a voltage offset of V_{cb} = 0.3 V was required to fully deplete the collector at low J_e. The measured thermal resistance and emitter resistance for these devices suggested that digital circuit bandwidth would benefit from thinning the collector from 200 nm to 150 nm in order to operate the HBTs at higher current densities.

A device layer structure was conceived (DHBT 19b), intended for use in emitter-coupled-logic (ECL) static frequency divider circuit design. The full layer structure and simulated band-diagram [11] for the device are given in Tab. 4.1 and Fig. 4.1, respectively. It utilizes a 150 nm collector and 30 nm base, with a projected J_{Kirk} = 3 mA/μm^2 at V_{cb} = 0.0 V and J_{Kirk} = 6 mA/μm^2 at V_{cb} = 0.6 V. The InGaAs sub-collector contact layer was thinned from 25 nm to 12.5 nm for reduced thermal resistance. Also, ECL divider designs require the collector be fully depleted at V_{cb} = 0.0 V, therefore the collector doping was chosen to ensure this. Two wafers were

Table 4.1: Layer structure DHBT 19b – 150 nm collector, 30 nm base

Thickness (nm)	Semiconductor Composition	Doping (cm^{-3})	Description
40	$In_{0.53}Ga_{0.47}As$	$3 \cdot 10^{19}$:Si	Emitter cap
80	InP	$3 \cdot 10^{19}$:Si	Emitter cap
10	InP	$8 \cdot 10^{17}$:Si	Emitter
30	InP	$3 \cdot 10^{17}$:Si	Emitter
30	InGaAs	$5 - 8 \cdot 10^{19}$:C	Base
20	$In_{0.53}Ga_{0.47}As$	$3 \cdot 10^{16}$:Si	Setback
24	InGaAs / InAlAs	$3 \cdot 10^{16}$:Si	B-C grade
3	InP	$3 \cdot 10^{18}$:Si	Delta doping
103	InP	$3 \cdot 10^{16}$:Si	Collector
25	InP	$1.5 \cdot 10^{19}$:Si	Sub-collector
12.5	$In_{0.53}Ga_{0.47}As$	$2 \cdot 10^{19}$:Si	Sub-collector
300	InP	$2 \cdot 10^{19}$:Si	Sub-collector
Substrate	Semi-Insulating InP		

ordered with this design from IQE and attempts to process the new divider mask set began. Because of process difficulties associated with forming devices, it was concluded that circuits would not be functional when the process was completed. Efforts were pursued to correct the HBT fabrication process steps.

After six months the device formation updates were completed. Two samples were fabricated using two different mask sets – one for devices, the other for circuits. The device mask set was processed to check device performance and yield as it contained narrower device footprints on the reticle that are more difficult to yield. On this mask set, HBTs could be measured after Metal-1 interconnect deposition – something not possible with the divider mask set. A screening of the device wafer

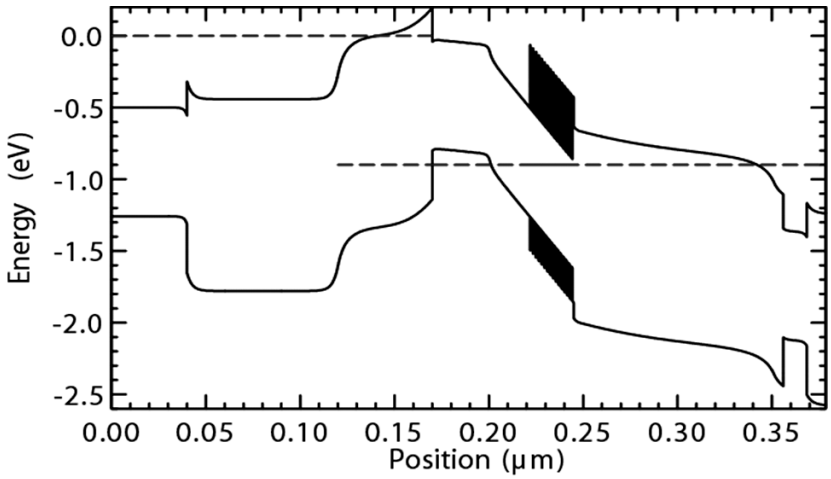

Figure 4.1: Simulated band-structure DHBT 19b – V_{be} = 0.9 V, V_{cb} = 0.0 V

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showed that yield was $\sim$ 100% for HBTs of all dimensions (emitter junctions as narrow at 0.4 μm), with little variation in DC and RF performance amongst them.

Fig. 4.2 shows the common-emitter $I-V$ curves and Gummel characteristics for DHBT 19b. The devices can sustain a maximum operating power density $P_{max} >$ 18 mW/μm^2, there is no evidence of current blocking at $J_e > 12$ mA/μm^2, $V_{cb} = 0.0$ V and the ideality factors for the base n_b and collector n_c are similar to other InP DHBTs [10] from UCSB. Tab. 4.2 summarizes the measured electrical characteristics for the device.

Fig. 4.3 shows the measured microwave gains h_{21} and Mason's unilateral gain U at the bias associated with peak f_τ and f_{max}. A maximum 370 GHz f_τ and 459 GHz f_{max} were extrapolated from two different devices of exact dimension at J_e

Table 4.2: Summary of electrical characteristics, DHBT 19b

			emitter	base		collector		ideality			
DHBT	β	BV_{CEO}	ρ_c	ρ_s	ρ_c	ρ_s	ρ_c	n_b	n_c	f_τ	f_{max}
19b	11	5.6	15	603	20	12.9	12	1.55	1.05	370	459
		Volts	ρ_c, $\Omega \cdot \mu$m^2 and ρ_s, Ω/sq							GHz	

= 8.3 mA/μm^2 and V_{cb} = 0.3 V. Measuring two devices was necessary because the DC-50 GHz device test structures utilizing an *on wafer* Thru-Reflect-Line (TRL) network analyzer calibration showed strong resonances beyond 20 GHz (likely due to parasitic substrate modes), but less so in W-band (75-110 GHz). Consequently, the DC-30 GHz data was taken from a device utilizing a short-pad test structure requiring a *probe-tip* TRL network analyzer calibration. The measured values of f_τ and f_{max} for both DHBTs were the same and consistent with simulated values from device modeling.

While this HBT performance showed significant improvements in yield compared to DHBT 17, the device β was lower than expected and J_{Kirk} was much higher. It was believed that the device passivation scheme combined with high base doping was responsible for the low β. The J_{Kirk} was high because the pulse doping in the collector was inadvertently grown 50% higher than specified. Complications pertaining to the growth of the pulse doping have since been resolved.

Three projects were pursued after the DHBT 19b measurements were completed – all discussed thoroughly in Chapter 3. The first was to reduce the device

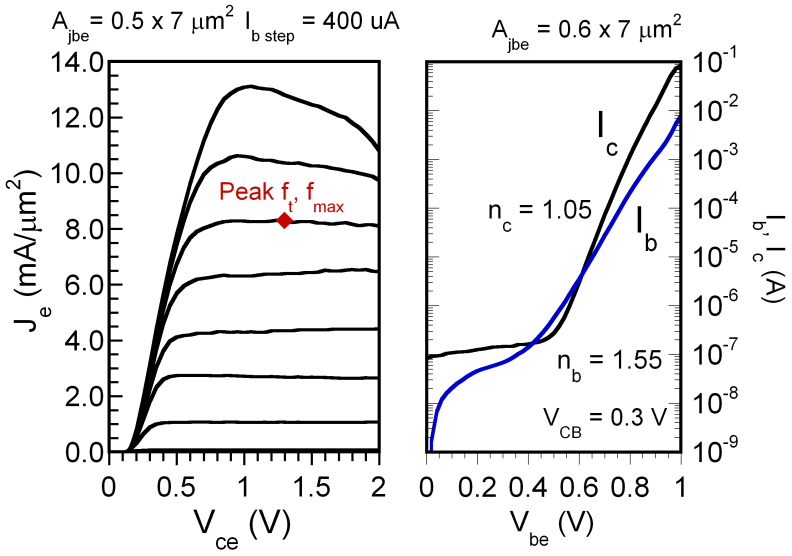

Figure 4.2: Common-emitter I-V and Gummel characteristics, DHBT 19b

leakage currents. This involved transitioning from polyimide to BCB as the passivation dielectric. It also permitted the device interconnects to be suspended above the high $\varepsilon = 12.8$ InP substrate. Second, corrections were needed to the back-end of the process. The circuit wafer previously mentioned (processed concurrently with DHBT 19b devices) failed to yield devices or circuits because of problems associated with forming the inverted microstrip wiring environment. Lastly, from the device data measured from DHBT 19b, static frequency dividers were designed with an intended $f_{clk,max} > 150$ GHz. To do so, a simple design-kit was generated that included safe operating curves based on the maximum operating power density of

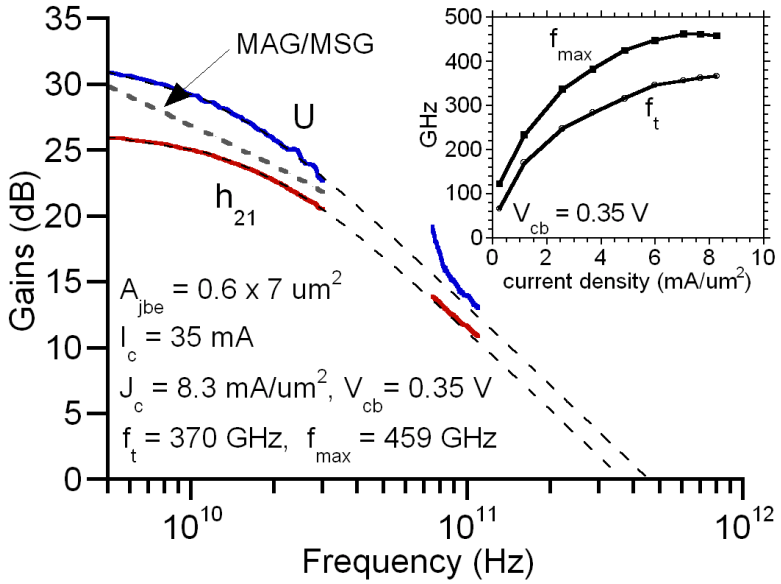

Figure 4.3: Measured microwave gains, DHBT 19b – Peak f_τ, f_{max}

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the HBTs and a plot of the dependence of C_{cb}/I_c with varying V_{cb} and J_e.

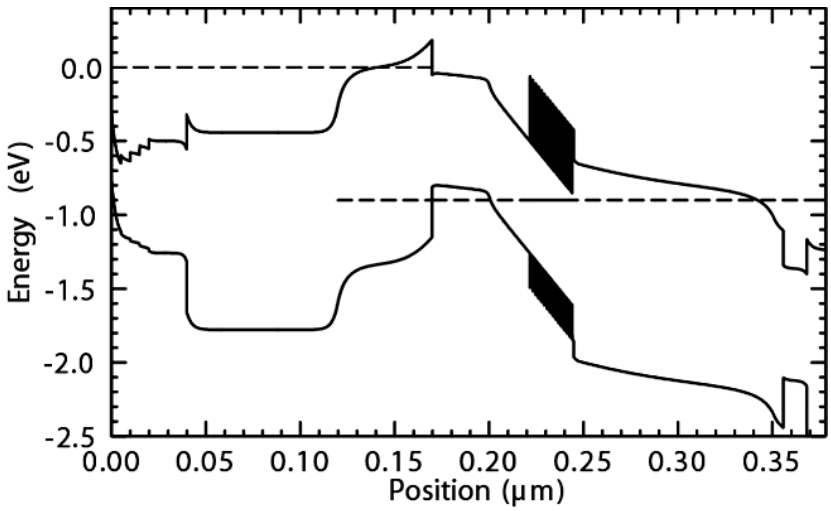

Figure 4.4: Simulated band-structure DHBT 22 – V_{be} = 0.9 V, V_{cb} = 0.0 V

4.3 150 nm collector, 30 nm base – DHBT 22

This wafer, like DHBT 19b, has a 150 nm collector and 30 nm base. There are two significant differences with DHBT 22 – the emitter cap is step-graded from $\mathrm{In_{0.53}Ga_{0.47}As}$ to the narrower bandgap In-rich $\mathrm{In_{0.85}Ga_{0.15}As}$ for reduced emitter ρ_c, and the doping grade in the base is reduced from $8 \rightarrow 5 \cdot 10^{19}$ cm^{-3} to $7 \rightarrow 4 \cdot 10^{19}$ cm^{-3}. In addition to these changes, all of the process modifications discussed in Chapter 3 (BCB passivation, raised interconnects, inverted-microstrip wiring) were employed for device and circuit formation. Static frequency dividers were yielded and are discussed in Chapter 5.

The full layer structure and simulated band-diagram for the device are given

Table 4.3: Layer structure DHBT 22 – 150 nm collector, 30 nm base

Thickness (nm)	Semiconductor Composition	Doping (cm^{-3})	Description
5	$In_{0.85}Ga_{0.15}As$	$> 3 \cdot 10^{19}$:Si	Emitter cap
15	$In_xGa_{1-x}As$	$3 \cdot 10^{19}$:Si	Emitter cap
20	$In_{0.53}Ga_{0.47}As$	$3 \cdot 10^{19}$:Si	Emitter cap
80	InP	$3 \cdot 10^{19}$:Si	Emitter
10	InP	$8 \cdot 10^{17}$:Si	Emitter
80	InP	$5 \cdot 10^{17}$:Si	Emitter
30	InGaAs	$4 - 7 \cdot 10^{19}$:C	Base
20	$In_{0.53}Ga_{0.47}As$	$2.5 \cdot 10^{16}$:Si	Setback
24	InGaAs / InAlAs	$2.5 \cdot 10^{16}$:Si	B-C grade
3	InP	$3 \cdot 10^{18}$:Si	Delta doping
103	InP	$2.5 \cdot 10^{16}$:Si	Collector
10	InP	$1.5 \cdot 10^{19}$:Si	Sub-collector
12.5	$In_{0.53}Ga_{0.47}As$	$2 \cdot 10^{19}$:Si	Sub-collector
300	InP	$2 \cdot 10^{19}$:Si	Sub-collector
Substrate	Semi-Insulating InP		

in Tab. 4.3 and Fig. 4.4, respectively. The collector doping was slightly reduced compared to DHBT 19b, with the projected J_{Kirk} = 3 mA/μm^2 at V_{cb} = 0.0 V and J_{Kirk} = 6 mA/μm^2 at V_{cb} = 0.6 V. Fig. 4.5 shows the common-emitter $I-V$

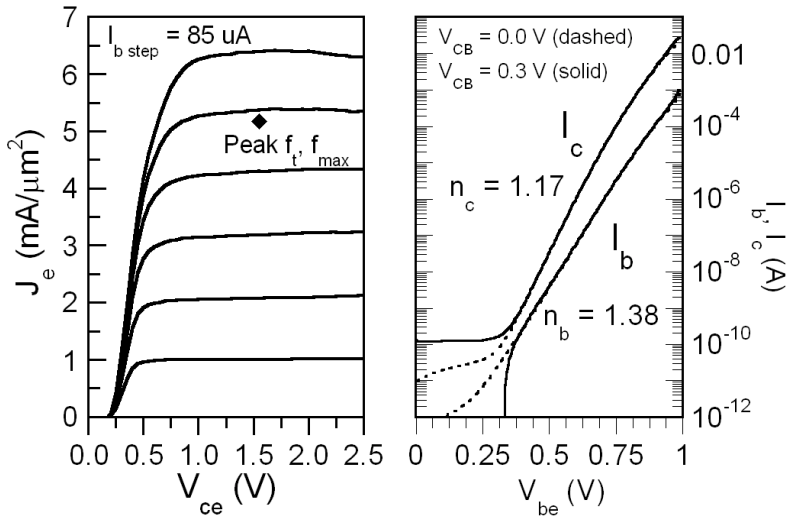

Figure 4.5: Common-emitter I-V and Gummel characteristics, DHBT 22

curves and Gummel characteristics for DHBT 22. The devices behave as expected with no signs of gain-compression or current blocking at P = 15 mW/μm^2, and the Gummel curves show normal ideality factors for the base n_b and collector n_c. Tab. 4.4 summarizes the measured electrical characteristics for DHBT 22.

DC-50 GHz RF measurements were carried out after performing a *probe-tip* Line-Reflect-Reflect-Match (LRRM) calibration on an Agilent 8510 XF network analyzer. An on-wafer open circuit pad structure identical to the one used by the

Table 4.4: Summary of electrical characteristics, DHBT 22

			emitter	base		collector		ideality			
DHBT	β	BV_{CEO}	ρ_c	ρ_s	ρ_c	ρ_s	ρ_c	n_b	n_c	f_τ	f_{max}
22	36	5.1	10.1	564	9.6	11.9	5.4	1.38	1.17	391	505
		Volts	ρ_c, $\Omega \cdot \mu$m^2 and ρ_s, Ω/sq							GHz	

devices was measured after calibration in order to de-embed this associated capacitance from the device measurements. Fig. 4.6 shows the measured microwave gains h_{21} and Mason's unilateral gain U at the bias associated with peak f_τ and f_{max}. A maximum 391 GHz f_τ and 505 GHz f_{max} were extrapolated at J_e = 5.17 mA/μm^2, V_{cb} = 0.6 V, and C_{cb}/I_c = 0.51 ps/V. A small-signal $hybrid-\pi$ equivalent circuit of

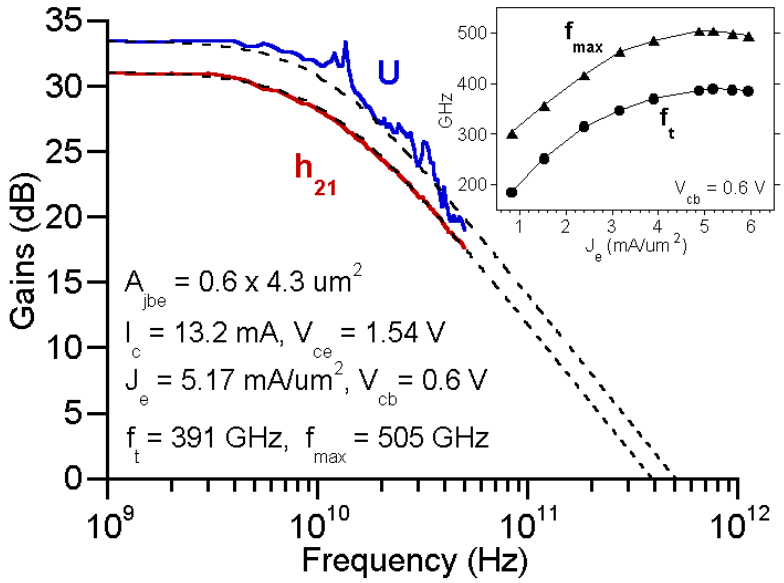

Figure 4.6: Measured microwave gains, DHBT 22 – Peak f_τ, f_{max}

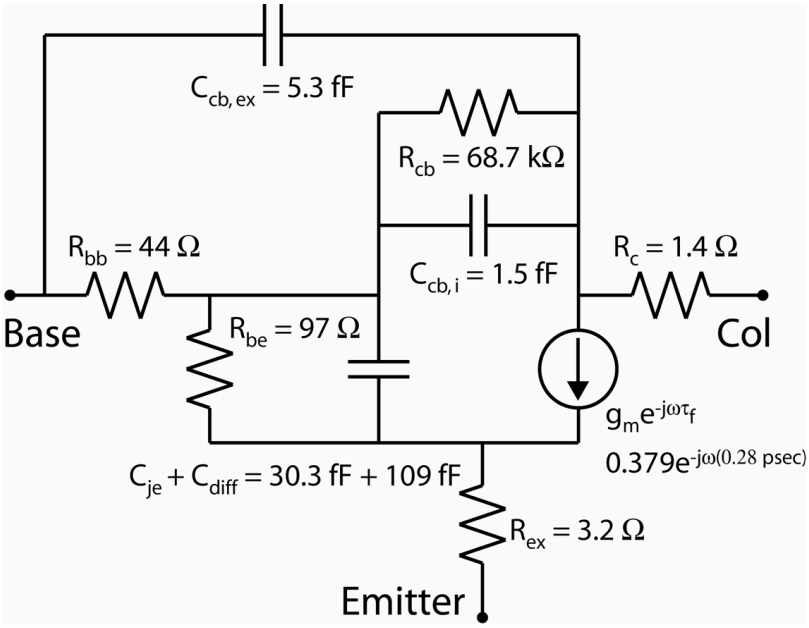

Figure 4.7: Hybrid-π model, DHBT 22 – Peak f_τ, f_{max}

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the device at peak f_τ and f_{max} is shown in Fig. 4.7.

Inspection of the measured data shows DHBT 22 improved when compared to DHBT 19b. The device leakage currents were reduced by more than 100$\times$ for both the base I_b at low V_{be} and the collector I_c as low $V_{cb,offset}$. This can be attributed to a reduction in the amount of semiconductor surface pinning through the use of BCB. Device β increased by more than was anticipated from the reduction in base doping, likely due to reduced surface leakage from around the N^- emitter periphery. Lastly, the emitter and base contact resistivity ρ_c were reduced by $\sim$ 40% through the combined use of the In-rich InGaAs emitter cap layer, and improved surface preparation

and metalization source quality – previously discussed in detail in Chapter 3. These results reflect the betterment in HBT performance from layer structure and fabrication changes. Also, the yield remained high and circuits with transistor counts of 28 (divide-by-2) and 56 (divide-by-4) were realized on the same wafer.

Further attempts to improve the process-flow ceased and scaling of the epitaxial layers was pursued. The remaining sections report device results from different DHBT layer structures utilizing the new UCSB HBT process.

4.4 210 nm collector, 35 nm base – DHBT 24

DHBT 24 was designed by M. Dahlström and Z. Griffith for use in InP DHBT based power amplifier designs by V. Paidi operating at $\sim$ 200 GHz. The designs and layout were done utilizing the old UCSB HBT device and circuits process (discussed in Chapter 3) because of time restrictions, and results of this work have been reported in [14]. The full layer structure and simulated band-diagram for the device are given in Tab. 4.5 and Fig. 4.8, respectively. The collector doping was selected for a J_{Kirk} = 1.5 mA/μm^2 at V_{cb} = 0.0 V and J_{Kirk} = 3.5 mA/μm^2 at V_{cb} = 0.8 V.

While the amplifier results demonstrated 8.3-dBm output power at 176 GHz with 4.5-dB associated power gain, device and circuit performance suffered because of processing complications that increased the emitter and base contact resistance ρ_c. That caused f_{max} to be $\sim$ 35% lower than projected. Devices were fabricated again using the new process (improved ohmic contacts, and BCB passivation) to show that the HBTs could operate at much higher bandwidths for the same material.

Fig. 4.9 shows the common-emitter $I-V$ characteristics for DHBT 24. The device is well behaved with no evidence of gain-compression or current blocking due to thermal effects until $P >$ 14 mW/μm^2, and the Gummel curves showed expected ideality factors for the base n_b = 1.40 and collector n_c = 1.10. Tab. 4.6 summarizes the measured electrical characteristics for the device.

DC-40 GHz RF measurements were carried out after performing a *probe-tip*

Table 4.5: Layer structure DHBT 24 – 210 nm collector, 35 nm base

Thickness (nm)	Semiconductor Composition	Doping (cm^{-3})	Description
30	$In_{0.53}Ga_{0.47}As$	$3 \cdot 10^{19}$:Si	Emitter cap
110	InP	$3 \cdot 10^{19}$:Si	Emitter
10	InP	$8 \cdot 10^{17}$:Si	Emitter
40	InP	$5 \cdot 10^{17}$:Si	Emitter
35	InGaAs	$5 - 8 \cdot 10^{19}$:C	Base
20	$In_{0.53}Ga_{0.47}As$	$1.5 \cdot 10^{16}$:Si	Setback
24	InGaAs / InAlAs	$1.5 \cdot 10^{16}$:Si	B-C grade
3	InP	$3 \cdot 10^{18}$:Si	Delta doping
163	InP	$1.5 \cdot 10^{16}$:Si	Collector
50	InP	$1.5 \cdot 10^{19}$:Si	Sub-collector
10	$In_{0.53}Ga_{0.47}As$	$2 \cdot 10^{19}$:Si	Sub-collector
300	InP	$2 \cdot 10^{19}$:Si	Sub-collector
Substrate	Semi-Insulating InP		

Table 4.6: Summary of electrical characteristics, DHBT 24

			emitter	base		collector		ideality			
DHBT	β	BV_{CEO}	ρ_c	ρ_s	ρ_c	ρ_s	ρ_c	n_b	n_c	f_τ	f_{max}
24	21	6.9	7.2	446	6.1	12.6	5.5	1.40	1.10	276	451
		Volts	ρ_c, $\Omega \cdot \mu m^2$ and ρ_s, Ω/sq							GHz	

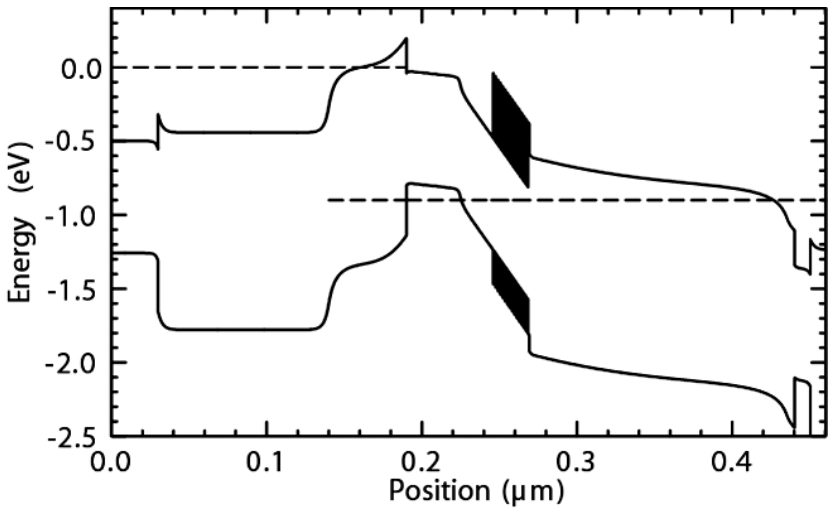

Figure 4.8: Simulated band-structure DHBT 24 – V_{be} = 0.9 V, V_{cb} = 0.0 V

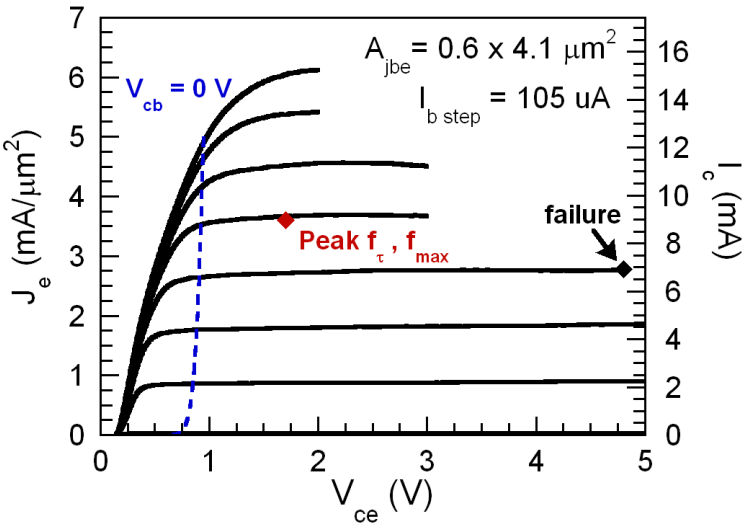

Figure 4.9: Common-emitter I-V characteristics, DHBT 24

Thru-Reflect-Line (TRL) calibration on an Agilent 8510C network analyzer. An on-wafer open circuit pad structure identical to the one used by the devices was measured after calibration in order to de-embed this associated capacitance from the device measurements. Fig. 4.10 shows the extrapolated microwave gains h_{21} and Mason's unilateral gain U at the bias associated with peak f_τ and f_{max}. A maximum 276 GHz f_τ and 451 GHz f_{max} were measured at J_e = 3.48 mA/μm ^{2} and V_{cb} = 0.8 V. A small-signal $hybrid-\pi$ equivalent circuit of the device at peak f_τ and f_{max} is shown in Fig. 4.11.

Improvements observed in device performance between DHBT 19b and DHBT 22

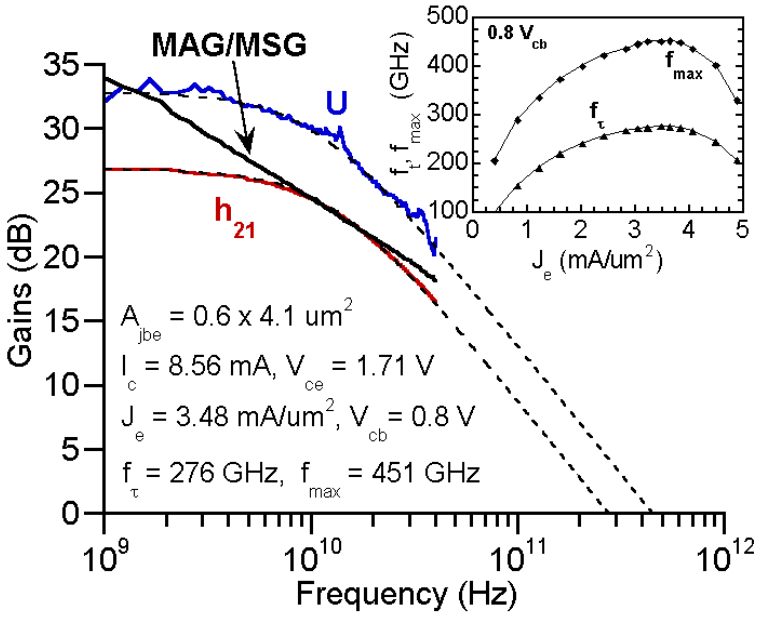

Figure 4.10: Measured microwave gains, DHBT 24 – Peak f_τ, f_{max}

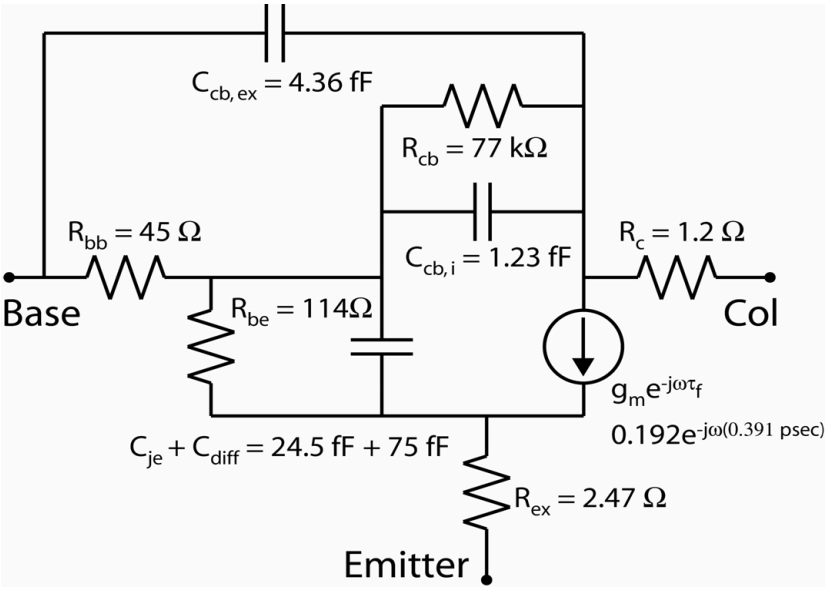

Figure 4.11: Hybrid-π model, DHBT 24 – Peak f_τ, f_{max}

(§4.2, §4.3) were similarly observed for DHBT 24. Between old and new UCSB HBT process, peak β increased from 14 to 21, base and collector leakage currents were reduced $\sim 100\times$, and f_τ / f_{max} increased from 220 / 290 GHz to 275 / 451 GHz.

4.5 100 nm collector, 30 nm base – DHBT 25 and 26

Two HBT layer structures utilizing a 100 nm collector and 30 nm base were designed to investigate the effectiveness of the chirped-superlattice base-collector grade at higher current densities and produce devices with high f_τ without significant reductions to f_{max}. The InGaAs contribution to the sub-collector has been thinned from 12.5 nm to 8.5 nm for reduced thermal resistance θ_{JA}, while maintaining low collector contact ρ_c.

For Type-I DHBTs to operate effectively at high J_e, the energy barrier to electron transport in the collector associated with the conduction band discontinuity between InGaAs and InP must be removed. The DHBTs designs and results discussed in the previous sections (DHBT 19b §4.2, DHBT 22 §4.3, DHBT 24 §4.4) employed a 47 nm transition region (20 nm setback, 24 nm grade, 3 nm pulse doping) between the base and InP portion of the collector and was effective at suppressing current blocking. As the collector thickness T_c is scaled, the ternary materials associated with the setback and grade will occupy a greater portion of the collector and the device operating temperature will increase rapidly at moderate base-collector voltages V_{cb} [15]. Two approaches to reduce them from the collector are pursued.

The conduction-band potential drop across the setback layer associated with

launching electrons into the grade is [4],

$$\Delta\phi_{setback} = (V_{cb} + \phi_{bi})\frac{T_{setback}}{T_c} + \frac{qN_\delta T_\delta T_{setback}}{\varepsilon_o\varepsilon_r} + \frac{(qN_c - \frac{J(x)}{v_{eff}})T_c T_{setback}}{2\varepsilon_o\varepsilon_r} \tag{4.5.1}$$

For the device designs with a 210 nm and 150 nm T_c, the collector setback thickness $T_{setback}$ = 20 nm produced an electrostatic potential drop across this region $\Delta\phi_{setback} \approx$ 0.370 and 0.378 eV, respectively. Scaling to 100 nm collector thickness with a 20 nm $T_{setback}$ would give $\Delta\phi_{setback} \approx$ 0.442 eV. Based on the previous results and effectiveness of the grade for the values of $\Delta\phi_{setback}$ utilized, the setback was thinned to 15 nm and the grade unchanged (42 nm transition) to make $\Delta\phi_{setback} \approx$ 0.332 eV for DHBT 25.

Invariant of the setback thickness, a pulse-doping is required to suppress the change in the conduction band quasi-field at the InP interface within the collector when a chirped-superlattice grade is used in order to remove the ΔE_c discontinuity, and is determined from the following relationship [3,4],

$$N_\delta T_\delta = \frac{\varepsilon_o\varepsilon_r \cdot \Delta E_c}{q^2 T_{grade}} \tag{4.5.2}$$

The second device design explored (DHBT 26) employs the same layer structure and doping values as DHBT 25, but the setback is further thinned to 10 nm and the base-collector grade has been reduced by 2:1 (25 nm transition) with the pulse doping adjusted to produce a $\Delta\phi_{setback} \approx$ 0.338 eV.

Table 4.7: Layer structure DHBT 25 / 26 – 100 nm collector, 30 nm base

Thickness (nm)	Semiconductor Composition	Doping (cm^{-3})	Description
5	$In_{0.85}Ga_{0.15}As$	$> 5 \cdot 10^{19}$:Si	Emitter cap
15	$In_xGa_{1-x}As$	$4 \cdot 10^{19}$:Si	Emitter cap
20	$In_{0.53}Ga_{0.47}As$	$3 \cdot 10^{19}$:Si	Emitter cap
80	InP	$3 \cdot 10^{19}$:Si	Emitter
10	InP	$1 \cdot 10^{18}$:Si	Emitter
40	InP	$8 \cdot 10^{17}$:Si	Emitter
30	InGaAs	$4 - 7 \cdot 10^{19}$:C	Base
15	$In_{0.53}Ga_{0.47}As$	$9 \cdot 10^{16}$:Si	Setback
24 / 12	InGaAs / InAlAs	$9 \cdot 10^{16}$:Si	B-C grade
3	InP	$2.75 \ / \ 5.5 \cdot 10^{18}$:Si	Delta doping
58 / 75	InP	$9 \cdot 10^{16}$:Si	Collector
10	InP	$1.5 \cdot 10^{19}$:Si	Sub-collector
8.5	$In_{0.53}Ga_{0.47}As$	$2 \cdot 10^{19}$:Si	Sub-collector
300	InP	$2 \cdot 10^{19}$:Si	Sub-collector
Substrate	Semi-Insulating InP		

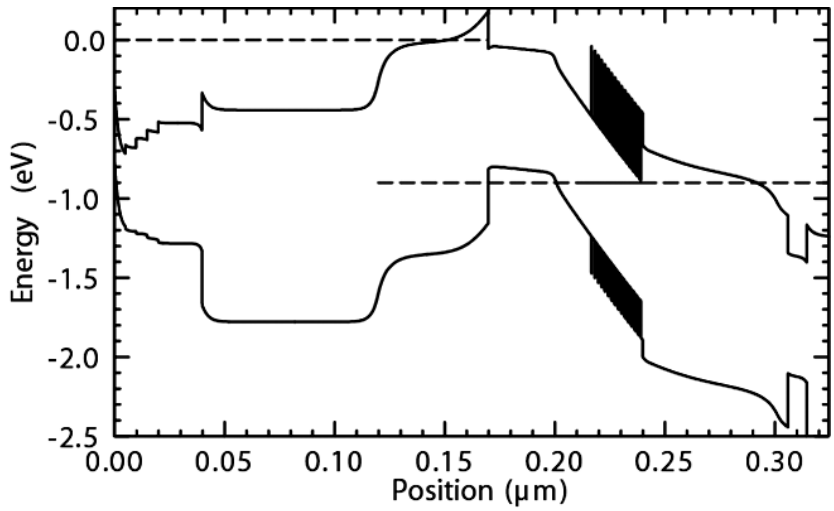

Figure 4.12: Simulated band-structure DHBT 25 – V_{be} = 0.9 V, V_{cb} = 0.0 V

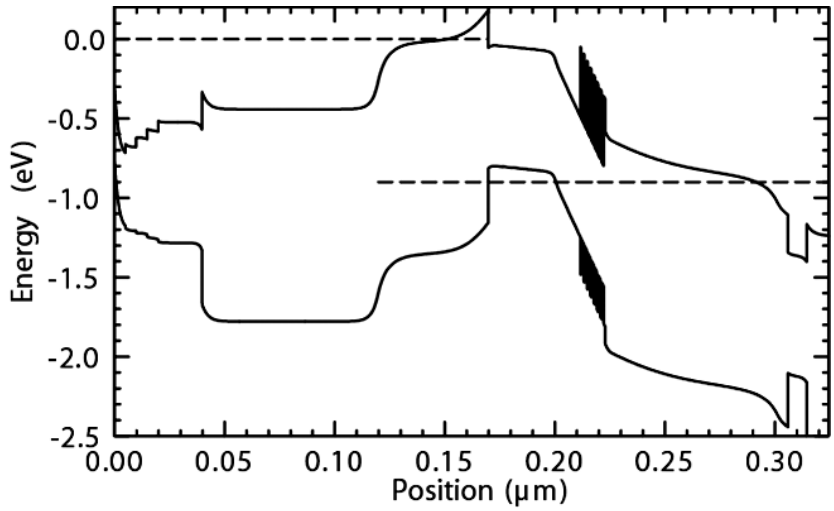

Figure 4.13: Simulated band-structure DHBT 26 – V_{be} = 0.9 V, V_{cb} = 0.0 V

The layer structures and simulated band-diagrams for DHBT 25 and DHBT 26 are given in Tab. 4.7, Fig. 4.12, and Fig. 4.13, respectively. The collector doping was

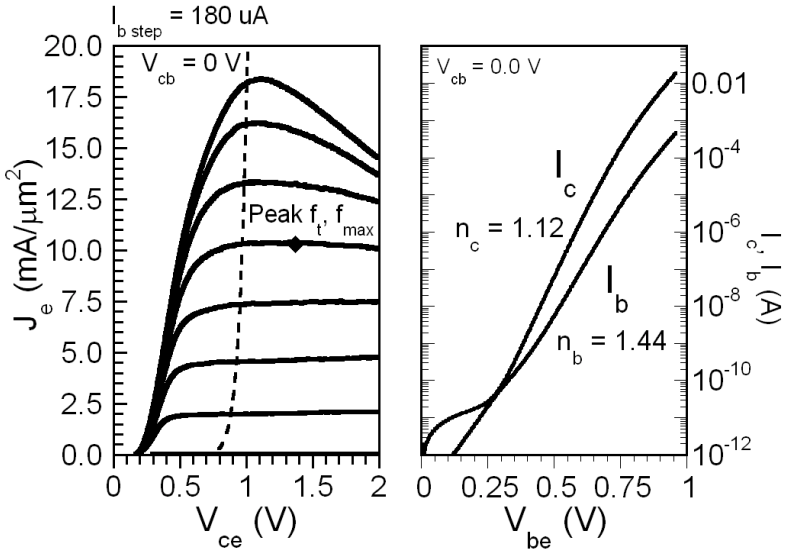

Figure 4.14: Common-emitter I-V and Gummel characteristics, DHBT 25

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specified for a projected J_{Kirk} = 5 mA/μm^2 at V_{cb} = 0.0 V and J_{Kirk} = 12.5 mA/μm^2 at V_{cb} = 0.6 V.

Fig. 4.14 and Fig. 4.15 shows the common-emitter $I-V$ curves and Gummel characteristics for DHBT 25 and DHBT 26, respectively. The devices behave normally with no evidence of gain-compression or current blocking until $J_e >$ 9 mA/μm^2, and the Gummel curves show expected ideality factors for the base n_b and collector n_c.

DC-42 GHz RF measurements were carried out after performing a *probe-tip* Thru-Reflect-Line (TRL) calibration on an Agilent 8510C network analyzer. An on-wafer open circuit pad structure identical to the one used by the devices was

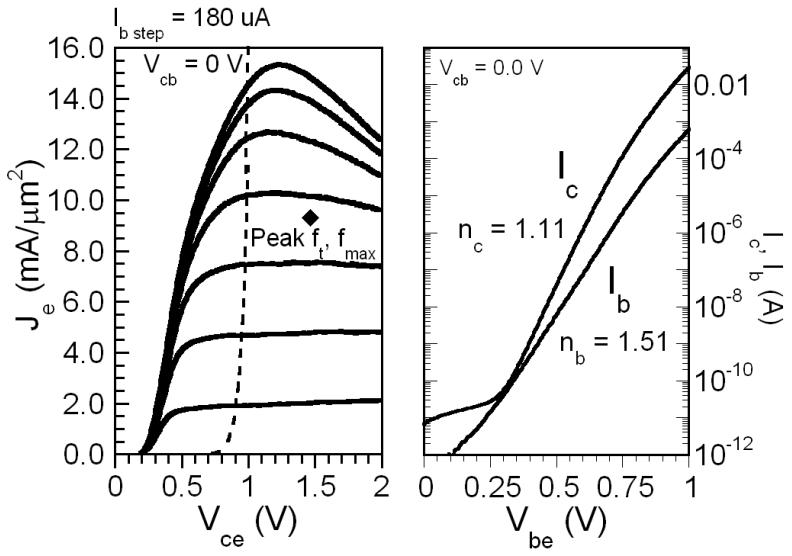

Figure 4.15: Common-emitter I-V and Gummel characteristics, DHBT 26

measured after calibration in order to de-embed this associated capacitance from the device measurements. Fig. 4.16 shows the measured microwave gains h_{21} and Fig. 4.17 shows Mason's unilateral gain U at the bias associated with peak f_τ and f_{max}, respectively for DHBT 25. A maximum 491 GHz f_τ and 415 GHz f_{max} were extrapolated at J_e = 10.3 mA/μm ^{2} and V_{cb} = 0.4 V. Fig. 4.18 shows the measured microwave gains h_{21} and Fig. 4.19 shows Mason's unilateral gain U at the bias associated with peak f_τ and f_{max}, respectively for DHBT 26. A maximum 465 GHz f_τ and 416 GHz f_{max} were extrapolated at J_e = 8.53 mA/μm ^{2} and V_{cb} = 0.4 V.

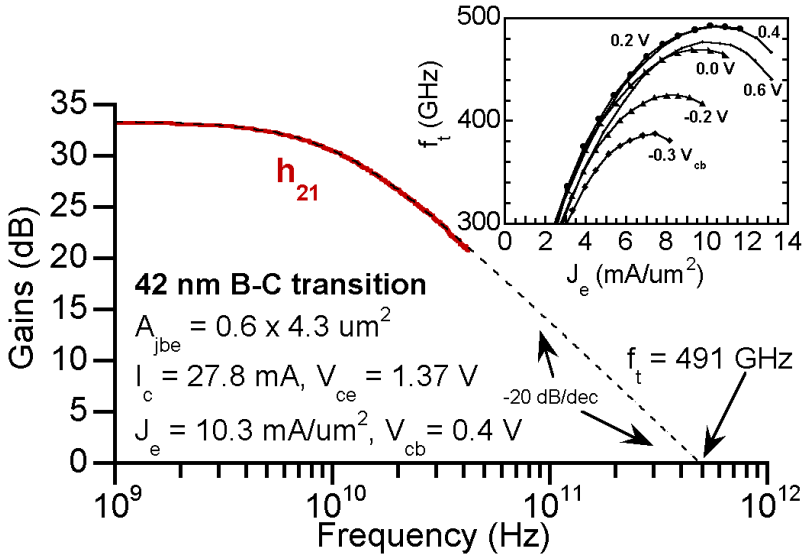

Figure 4.16: Measured microwave gains, DHBT 25 – Peak f_τ

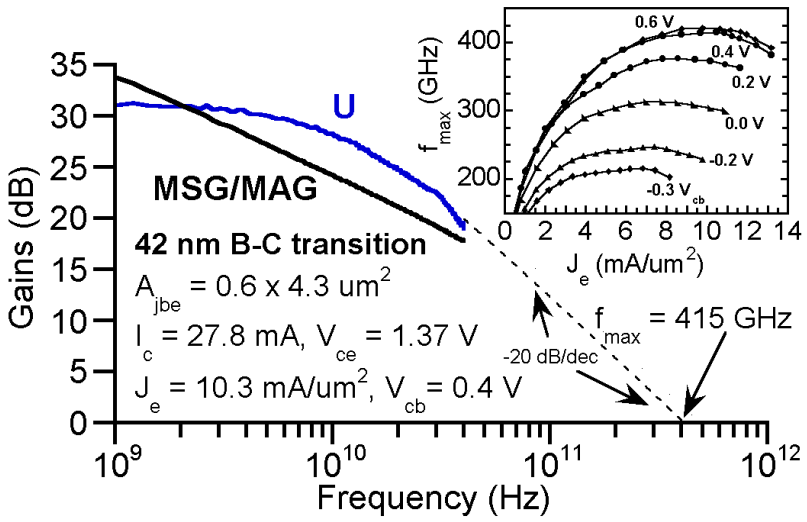

Figure 4.17: Measured microwave gains, DHBT 25 – Peak f_{max}

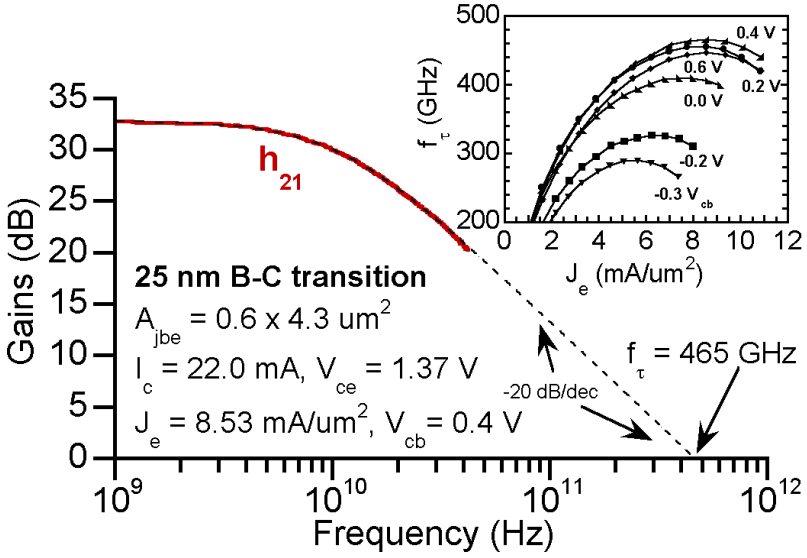

Figure 4.18: Measured microwave gains, DHBT 26 – Peak f_τ

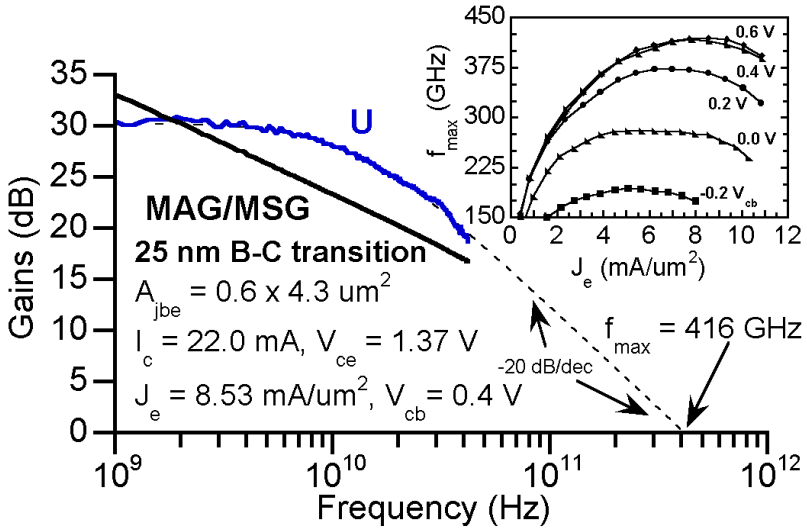

Figure 4.19: Measured microwave gains, DHBT 26 – Peak f_{max}

Table 4.8: Summary of electrical characteristics, DHBT 25 and 26

			emitter	base		collector		ideality			
DHBT	β	BV_{CEO}	ρ_c	ρ_s	ρ_c	ρ_s	ρ_c	n_b	n_c	f_τ	f_{max}
25	41	3.1	7.8	629	6.2	12.9	4.0	1.44	1.12	490	415
26	47	3.1	10.4	616	3.8	13.3	5.8	1.51	1.11	465	416
		Volts	ρ_c, $\Omega \cdot \mu$m^2 and ρ_s, Ω/sq							GHz	

4.5.1 Comparison of the proven grade *vs* the thinned grade

Thermal resistance θ_{JA} and device junction temperature were measured by the method of Liu [17] (at different V_{cb} (Fig. 4.20) to vary the field distribution and power dissipation in the InGaAs setback, ternary grade, and InP layers of the collector) through the following relationship,

$$\delta V_{be}|_{fixed\ I_c} = \frac{dV_{be}}{dT}\frac{dT}{dP}\frac{dP}{dV_{ce}} = -\phi \cdot \theta_{JA} \cdot I_c \cdot \delta V_{ce} \tag{4.5.3}$$

where ϕ is the thermal-electric feedback coefficient (V$/^\circ$C) and θ_{JA} ($^\circ$C$/$mW) the device thermal resistance. Because InGaAs, InAlAs, and InP have substantially different thermal resistivities, variation of θ_{JA} with V_{cb} and J_e is expected. Tab. 4.9 and Fig. 4.21 shows θ_{JA} (from I_c = 15 mA, J_e = 5.8 mA$/\mu$m^2) for varying V_{cb} and the temperature rise at different bias points. Note that the change in thermal feedback coefficient, ϕ has adjusted to account for the difference in operating current density. Also, the collector junction may be considerably hotter than the emitter junction due to the emitter interconnect metal, and the high thermal resistance of the InGaAs base.

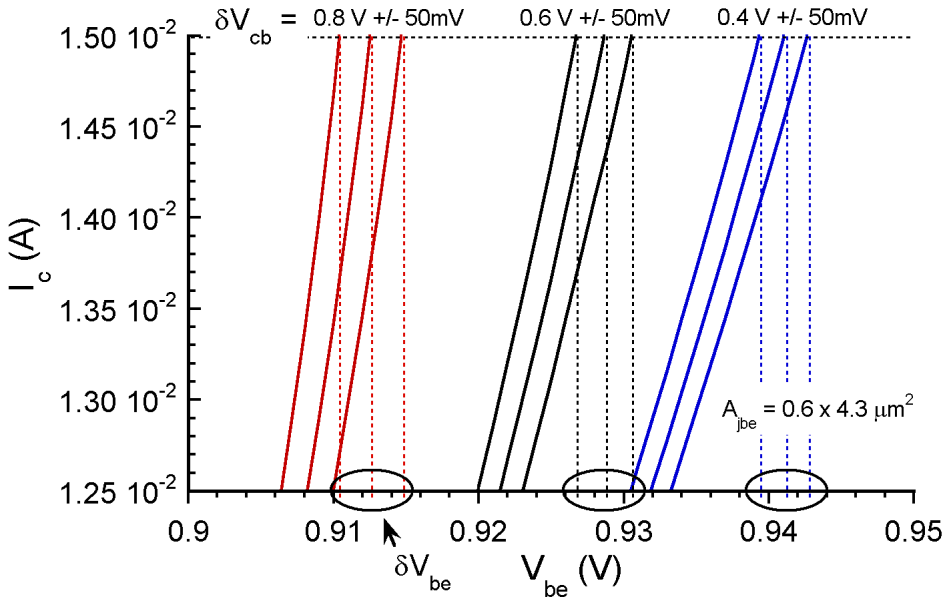

Figure 4.20: Change in V_{be} associated with differences in operating temperature for changes in V_{ce} ($\delta V_{ce} = \delta V_{be} + \delta V_{cb}$), keeping I_c constant. The Gummel measurement technique is used to acquire device thermal data.

Fig. 4.22, Fig. 4.23, and Fig. 4.24 show a direct comparison of the two HBTs. The hybrid-π equivalent circuit shows that the devices have similar values of resistive and capacitive parasitics – therefore, the disparity in DHBT performance is directed at the differences between the B-C grades. The common-emitter I-V curves from Fig. 4.22 are comparable for $J_e \leq 9$ mA/μm^2. At higher J_e, the 25 nm transition device (DHBT 26) suffers from current blocking (validated by the increase in C_{cb} witnessed in Fig. 4.24), while the 42 nm transition device (DHBT 25) behaves normally until $J_e \geq 18$ mA/μm^2. The negative differential resistance observed for both HBTs is due to device self-heating.

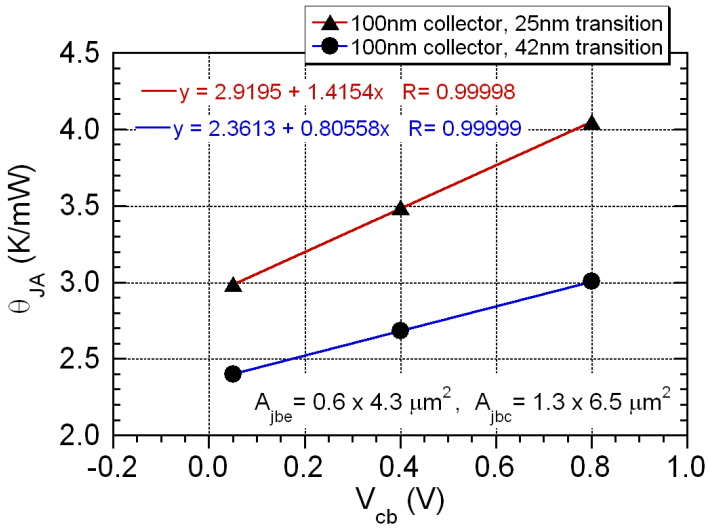

Figure 4.21: Variance of thermal resistance θ_{JA} with changing collector potential V_{cb}

The inability of the 25 nm transition devices to operate well at higher J_e is most likely due to imperfect design, or possibly more fundamental issues regarding the design of the graded layers. Upon closer examination of the energy band diagram, the setback is too thick for the pulse doping and grade used. The potential difference $\Delta\phi$ over the setback and grade for the 25 nm transition is the same as for the 42 nm transition, however this results in the electric field being much higher at the base-end of the collector and less strong in the InP. Electrons entering the collector will scatter more closely to the base and the effective electron velocity may be significantly reduced. The electron velocity associated with transport in the higher effective mass L-valley will modify the electric field in the InP more quickly as the current density

Table 4.9: Thermal resistance and device operating temperature – $A_{je} = 0.6 \times 4.3\ \mu\text{m}^2$

DHBT 25, 42 nm transition $\theta_{JA} = 2.3613 + 0.8056 \cdot V_{cb}$ (K/mW)			DHBT 26, 25 nm transition $\theta_{JA} = 2.9195 + 1.4154 \cdot V_{cb}$ (K/mW)		
V_{ce} (V)	J_e (mA/μm ^{2})	ΔT (K)	V_{ce} (V)	J_e (mA/μm ^{2})	ΔT (K)
2.5	9.61	242	2.5	8.60	304
2.5	7.40	179	2.5	7.12	247
2.0	14.49	271	2.0	14.90	386
2.0	13.66	253	2.0	12.33	311
2.0	12.36	226	2.0	10.90	272
1.11	18.41	153	1.23	15.30	176
1.37	10.30	105	1.37	8.53	111

is increased. Consequently, the Kirk threshold and field reversal will occur at a lower J_e when compared to the 42 nm transition HBT. This also explains why the thermal resistance is lower for the 42 nm transition because electrostatic potential drop is much less in the setback and grading layers of the collector at moderate to high J_e.

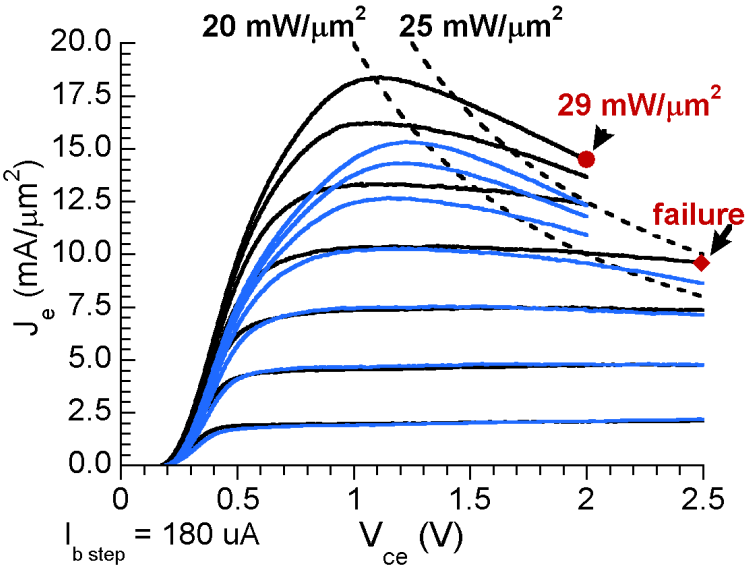

Figure 4.22: High-power density common-emitter curves – 42 nm transition (DHBT 25) black, 25 nm transition (DHBT 26) blue

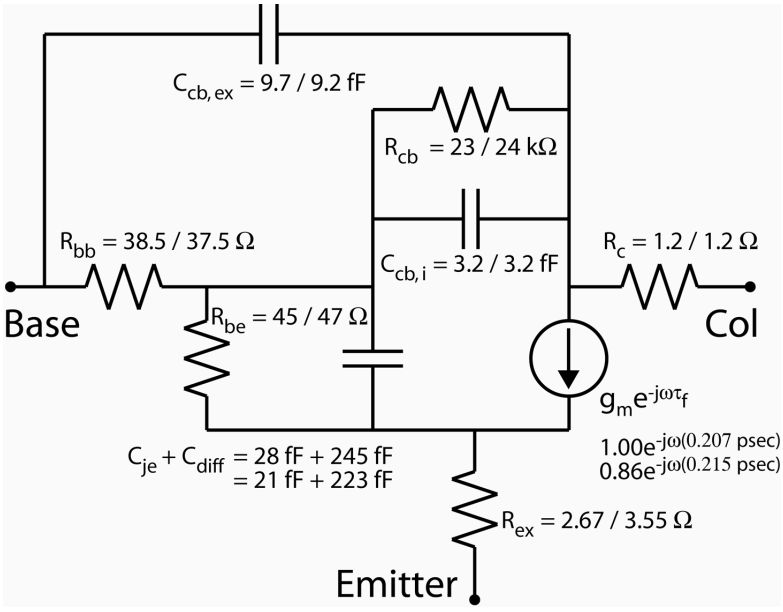

Figure 4.23: Hybrid-π models, 100 collector, 42 / 25 nm transitions – Peak f_τ, f_{max}

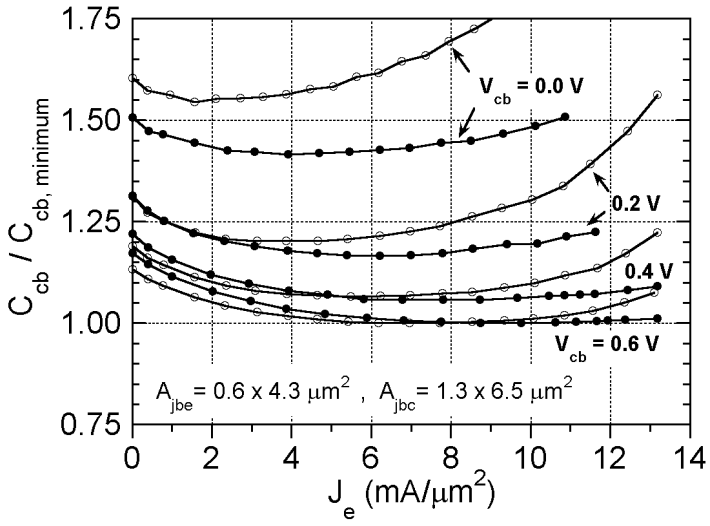

Figure 4.24: Comparison of C_{cb} vs J_e and V_{cb} for both 100 nm collector devices– 42 nm transition (DHBT 25) filled, 25 nm transition (DHBT 26) hollow

Table 4.10: Layer structure DHBT 27 – 120 nm collector, 30 nm base

Thickness (nm)	Semiconductor Composition	Doping (cm^{-3})	Description
5	$In_{0.85}Ga_{0.15}As$	$> 5 \cdot 10^{19}$:Si	Emitter cap
15	$In_xGa_{1-x}As$	$4 \cdot 10^{19}$:Si	Emitter cap
20	$In_{0.53}Ga_{0.47}As$	$3 \cdot 10^{19}$:Si	Emitter cap
80	InP	$3 \cdot 10^{19}$:Si	Emitter
10	InP	$8 \cdot 10^{17}$:Si	Emitter
40	InP	$5 \cdot 10^{17}$:Si	Emitter
30	InGaAs	$4 - 7 \cdot 10^{19}$:C	Base
15	$In_{0.53}Ga_{0.47}As$	$3.25 \cdot 10^{16}$:Si	Setback
24	InGaAs / InAlAs	$3.25 \cdot 10^{16}$:Si	B-C grade
3	InP	$2.75 \cdot 10^{18}$:Si	Delta doping
78	InP	$3.25 \cdot 10^{16}$:Si	Collector
5	InP	$1.5 \cdot 10^{19}$:Si	Sub-collector
6.5	$In_{0.53}Ga_{0.47}As$	$2 \cdot 10^{19}$:Si	Sub-collector
300	InP	$2 \cdot 10^{19}$:Si	Sub-collector
Substrate	Semi-Insulating InP		

4.6 120 nm collector, 30 nm base – DHBT 27

The device results from DHBT 25 having a collector thickness $T_c = 100$ nm confirmed that the base-collector grade can support current densities $J_e >$ 15 mA/μm^2 without showing degradation to HBT performance from current blocking or thermal effects. They showed that in scaling the collector T_c from 150 nm to 100 nm, f_{max} had decrease by the same amount f_τ increased and the C_{cb}/I_c ratio was unchanged. This suggests that for the device footprint utilized, the collector to emitter area ratio (a measure of extrinsic C_{cb}) is excessive at 100 nm collector T_c.

Based on the measured data for DHBT 22 (150 nm T_c) and DHBT 25 (100 nm

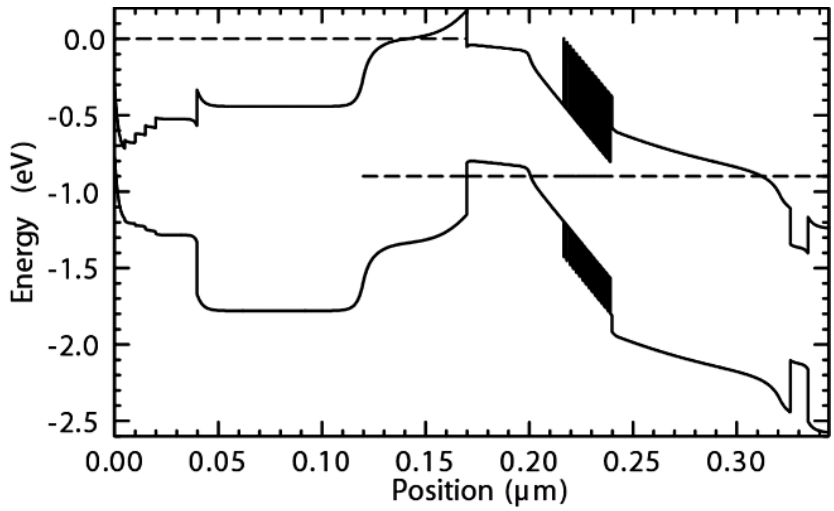

Figure 4.25: Simulated band-structure DHBT 27 – V_{be} = 0.9 V, V_{cb} = 0.0 V

T_c), an InP DHBT layer structure employing a 120 nm thick collector and 30 nm base was ordered from IQE with a projected f_τ and $f_{max} > 450$ GHz. The InGaAs contribution to the sub-collector has been thinned from 8.5 nm to 6.5 nm for reduced thermal resistance θ_{JA}, while maintaining low collector contact ρ_c. The device design was intended for use in 150 GHz static frequency divider designs consuming only half the power (150 mW per latch) as those results to be reported in Chapter 5. The collector doping was selected so that the extrinsic portions of the collector beyond where electrons traverse is fully depleted at 0.0 V_{cb} with a projected J_{Kirk} = 3 mA/μm^2 and at V_{cb} = 0.6 V, J_{Kirk} = 7 mA/μm^2.

Fig. 4.26 and Fig. 4.27 show the common-emitter $I - V$ curves and Gummel

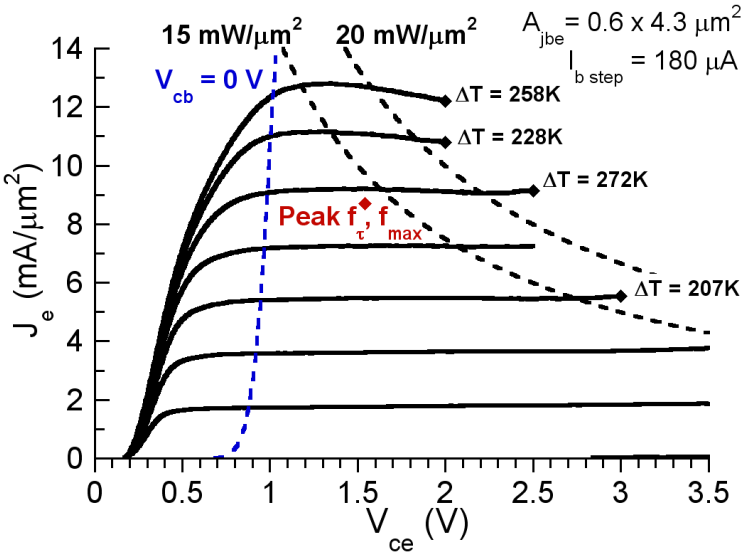

Figure 4.26: Common-emitter current-voltage characteristics, DHBT 27

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characteristics for DHBT 27. The device is well behaved with no evidence of gain-compression or current blocking at $J_e > 12$ mA/μm^2, and the Gummel curves show expected ideality factors for the base n_b and collector n_c. Thermal resistance θ_{JA} and device junction temperature were measured at different V_{cb} to vary the field distribution and power dissipation in the InGaAs setback, ternary grade, and InP layers of the collector. The thermal measurement techniques are the same as described in §4.5, Equ. 4.5.3, and Fig. 4.20. Variation of θ_{JA} with V_{cb} is shown in Fig. 4.28, where $\theta_{JA} = 2.6561 + 1.0878 \cdot V_{cb}$ (°C/mW). Superimposed on Fig. 4.26 are contours of constant power density (mW/μm^2) and the respective increase in temperature ΔT at

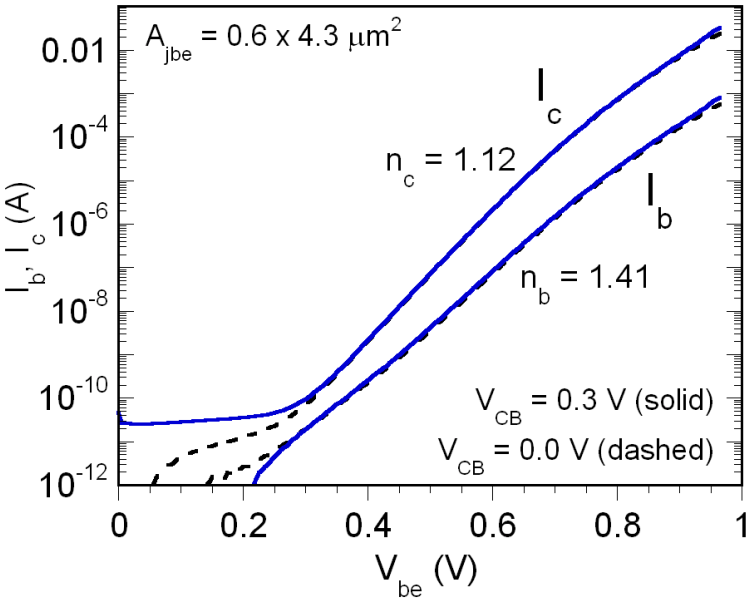

Figure 4.27: Gummel characteristics, DHBT 27

different operating points.

DC-110 GHz RF measurements were carried out after performing a *probe-tip* Line-Reflect-Reflect-Match (LRRM) calibration on an Agilent 8510 XF network analyzer. On-wafer open and short circuit pad structures identical to those used by the devices was measured after calibration in order to de-embed their associated

Table 4.11: Summary of electrical characteristics, DHBT 27

			emitter	base		collector		ideality			
DHBT	β	BV_{CEO}	ρ_c	ρ_s	ρ_c	ρ_s	ρ_c	n_b	n_c	f_τ	f_{max}
27	40	3.9	8.4	610	4.6	12.1	8.4	1.41	1.12	450	490
		Volts	ρ_c, $\Omega \cdot \mu$m^2 and ρ_s, Ω/sq							GHz	

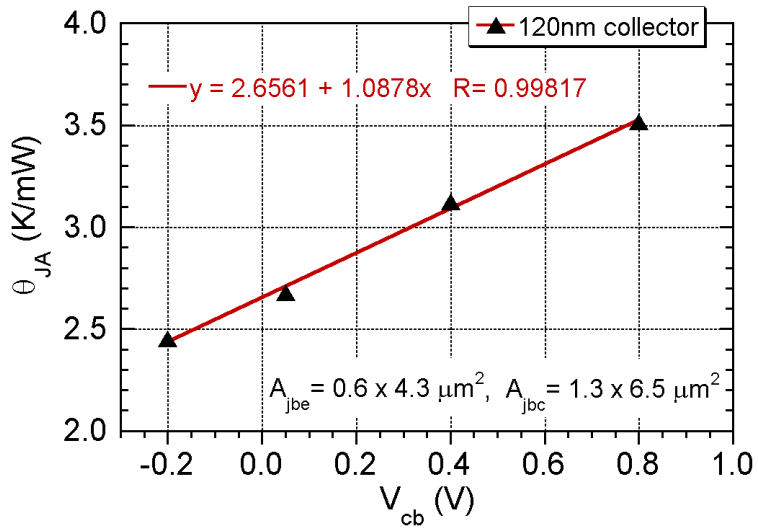

Figure 4.28: Variance of thermal resistance θ_{JA} with changing collector potential

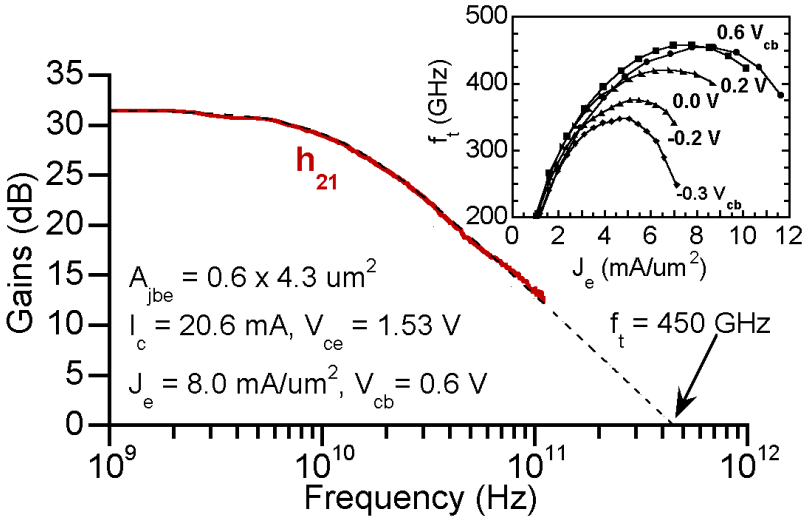

Figure 4.29: Measured microwave gains, DHBT 27 – Peak f_τ

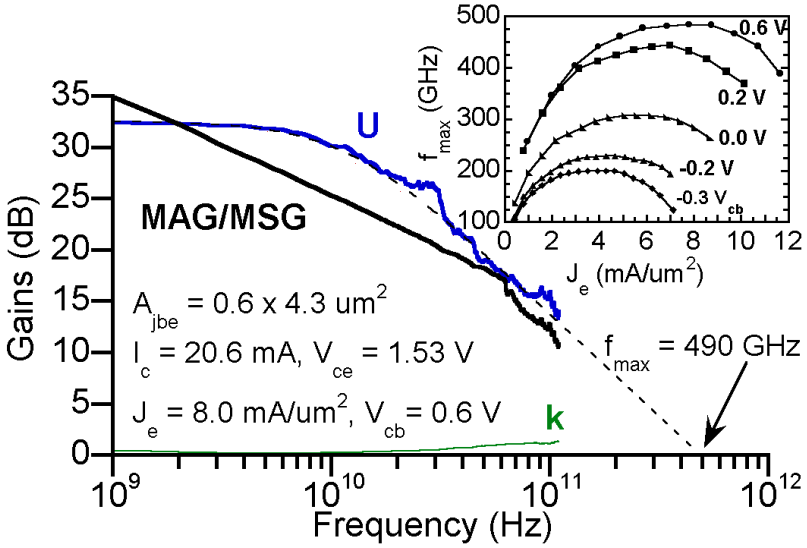

Figure 4.30: Measured microwave gains, DHBT 27 – Peak f_{max}

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parasitics from the device measurements. Fig. 4.29 shows the measured microwave gains h_{21} and Fig. 4.30 shows Mason's unilateral gain U at the bias associated with peak f_τ and f_{max} respectively for DHBT 27. A maximum 450 GHz f_τ and 490 GHz f_{max} were measured at J_e = 8.0 mA/μm^2, V_{cb} = 0.6 V, and C_{cb}/I_c = 0.37 ps/V. A small-signal $hybrid-\pi$ equivalent circuit of the device at peak f_τ and f_{max} is shown in Fig. 4.31.

The variation of C_{cb} versus J_e and V_{cb} for use in current mode logic (CML) circuit design is shown in Fig. 4.32, where switching endpoints for devices from the CML static frequency divider schematic are shown (Fig. 4.33). Lines connecting the switching endpoints have been superimposed to act as a guide. At the indicated bias

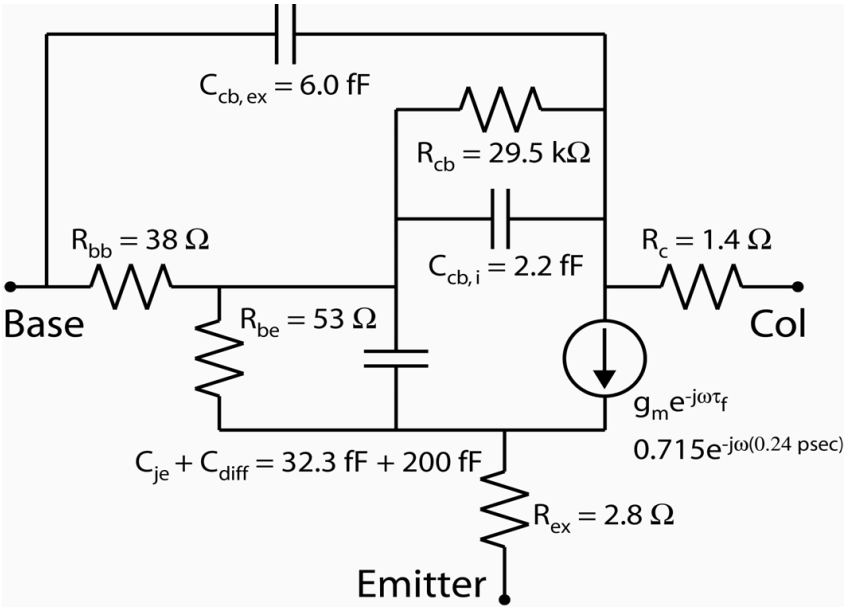

Figure 4.31: Hybrid-π model, DHBT 27 – Peak f_τ, f_{max}

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points, data steering devices (Q1,Q2) have a minimum $C_{cb}/I_c \approx 1.6$ ps/V, emitter follower devices (Q3) $C_{cb}/I_c \approx 0.57$ ps/V, and clock steering devices (Q4) $C_{cb}/I_c \approx 0.67$ ps/V. Some of the bias points have been selected beyond J_{Kirk} for reduced C_{cb}/I_c ratio. While C_{cb} may be increasing, inspection of the microwave gains versus J_e and V_{cb} (Fig. 4.29, Fig. 4.30) shows that the initial roll-off of f_τ and f_{max} is soft, suggesting that the initial field collapse in the setback layer of the base-collector interface does not significantly impact the forward delay τ_f of the HBT. Because of this, the selection of a smaller device size for a J_e slightly above J_{Kirk} will increase the maximum toggle rate of the latch. At J_e substantially above J_{Kirk}, the field will reverse in the collector setback and grade. The forward delay will increase rapidly –

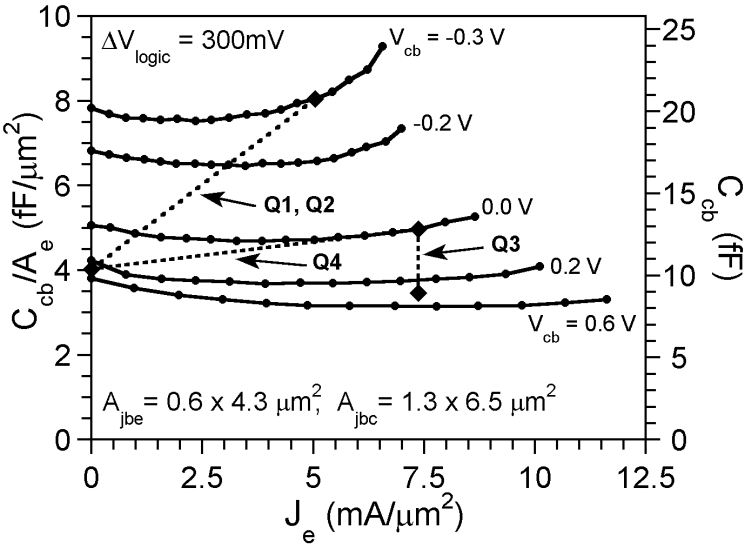

Figure 4.32: Comparison of C_{cb} vs J_e and V_{cb}, DHBT 27, labeled to show the corresponding device switching endpoints within a CML divider schematic Fig. 4.33. Lines connecting the switching endpoints have been superimposed to act as a guide.

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this is when the roll-off of both f_τ and f_{max} becomes significant, and digital circuit speed will suffer.

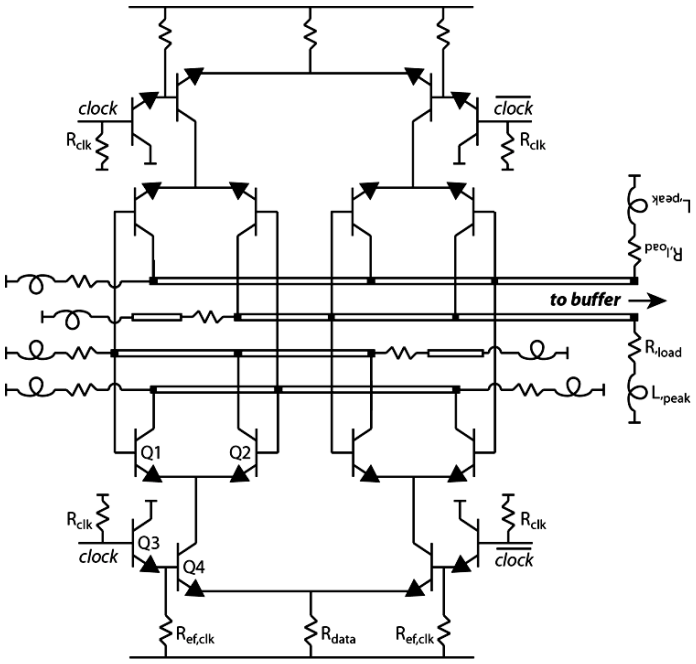

Figure 4.33: Schematic of current mode logic (CML) static frequency divider

Table 4.12: Layer structure *metamorphic* DHBT – 200 nm collector, 30 nm base

Thickness (nm)	Semiconductor Composition	Doping (cm^{-3})	Description
10	InAs	$3 \cdot 10^{19}$:Si	Emitter cap
30	$In_{0.53}Ga_{0.47}As$	$3 \cdot 10^{19}$:Si	Emitter cap
80	InP	$3 \cdot 10^{19}$:Si	Emitter
10	InP	$8 \cdot 10^{17}$:Si	Emitter
30	InP	$3 \cdot 10^{17}$:Si	Emitter
30	InGaAs	$4 \cdot 10^{19}$:C	Base
20	$In_{0.53}Ga_{0.47}As$	$3 \cdot 10^{16}$:Si	Setback
24	InGaAs / InAlAs	$3 \cdot 10^{16}$:Si	B-C grade
3	InP	$3 \cdot 10^{18}$:Si	Delta doping
153	InP	$3 \cdot 10^{16}$:Si	Collector
25	$In_{0.53}Ga_{0.47}As$	$2 \cdot 10^{19}$:Si	Sub-collector
375	InP	$2 \cdot 10^{19}$:Si	Sub-collector
20	InP	undoped	buffer
20	InAlAs	undoped	buffer
1500	InP	undoped	metamorphic buffer
Substrate	Semi-Insulating GaAs		

4.7 metamorphic DHBTs

Processing challenges associated with the old UCSB HBT process and those specific to metamorphic InP HBTs (mHBT) lessened the DC and RF performance of these devices. This section reports the latest mHBTs results from UCSB employing the device formation improvements discussed in Chapter 3.

The full layer structure and simulated band-diagram for the device are given in Tab. 4.12 and Fig. 4.34, respectively. The HBT design is similar to the devices reported in [10] (DHBT 17), having a 200 nm collector and 30 base. The collector

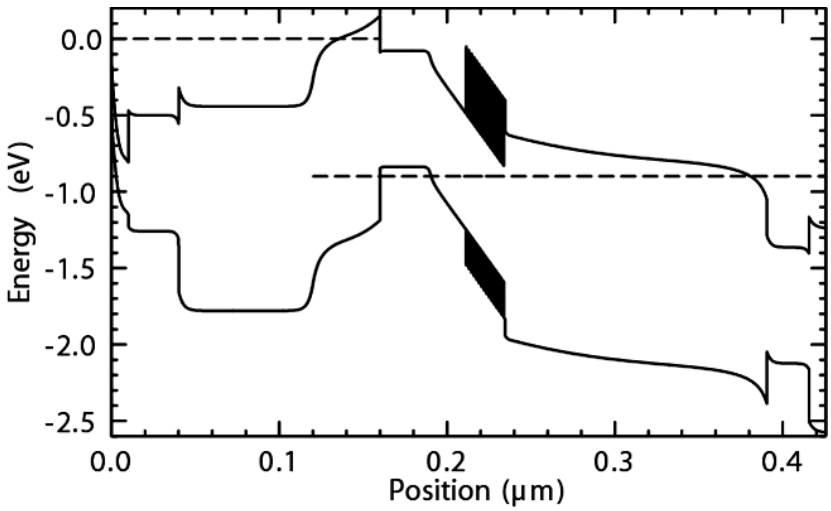

Figure 4.34: Simulated band-structure mHBT – V_{be} = 0.9 V, V_{cb} = 0.0 V

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design is identical, but the base doping is constant at $4 \cdot 10^{19}$ cm^{-3} without any conduction band grading. Compared DHBT 17, τ_b is expected to be higher (slightly lower f_τ), and the necessary dielectric sidewall spacer around the emitter contact will increase the gap resistance $R_{b,gap}$ between the base contact and emitter mesa (lower f_{max}).

Fig. 4.35 shows well-behaved common-emitter $I - V$ characteristics for the metamorphic HBTs. Gummel characteristics for the mHBT and a lattice-matched InP HBT (LM-HBT, active layers grown on lattice-matched InP substrate) are superimposed and shown in Fig. 4.36. Compared to the LM-HBT, the mHBT has similarly low collector leakage currents $\sim$ 100 pA, with like collector ideality fac-

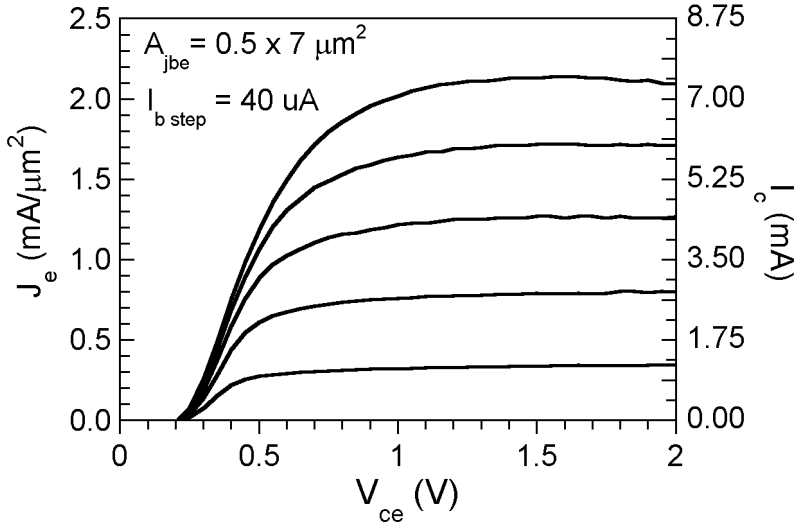

Figure 4.35: Common-emitter current-voltage characteristics, mHBT

Table 4.13: Summary of electrical characteristics, mHBT

			emitter	base		collector		ideality			
	β	BV_{CEO}	ρ_c	ρ_s	ρ_c	ρ_s	ρ_c	n_b	n_c	f_τ	f_{max}
mHBT	35	5.7	20	814	14	—	—	1.68	1.24	268	339
		Volts	ρ_c, $\Omega \cdot \mu$m^2 and ρ_s, Ω/sq							GHz	

tors n_c. The increased base ideality factor n_b for the mHBT is because of the residual N^- InAsP or InGaAsP surrounding the emitter mesa. This creates a small leakage path, but once the base-emitter junction is turned on ($V_{be} > 0.8$ V, $I_c > 100$ μA), the n_b of the mHBT is similar to the LM-HBT. Tab. 4.13 summarizes the measured electrical characteristics for the device.

DC-30, 75-110 GHz RF measurements were carried out after performing an *on*

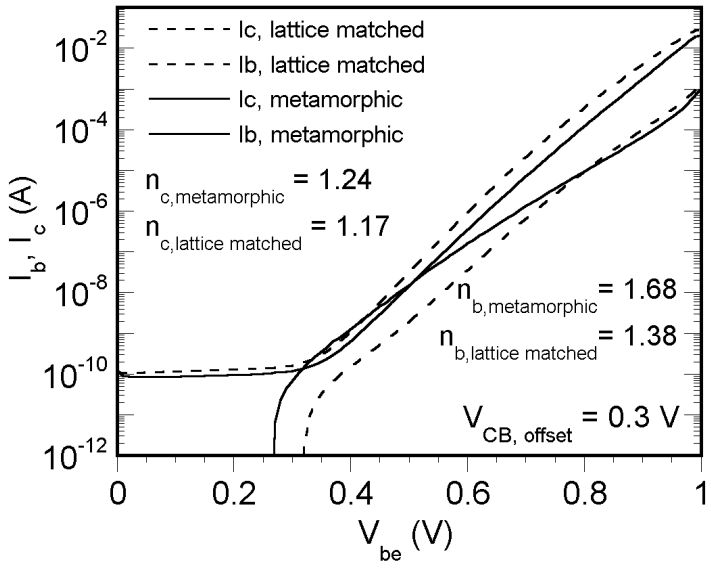

Figure 4.36: Gummel curves – comparing metamorphic and lattice-matched DHBT characteristics

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wafer Thru-Reflect-Line (TRL) calibration on an Agilent 8510C network analyzer. Fig. 4.37 shows the measured microwave gains h_{21} and Mason's unilateral gain U at the bias associated with peak f_τ and f_{max}. A maximum 268 GHz f_τ and 339 GHz f_{max} were extrapolated at J_e = 2.9 mA/μm ^{2} and V_{cb} = 0.8 V. These values of f_τ and f_{max} measured were consistent with simulated values from device modeling. The normalized thermal resistance R_{th} = 10.1 °C·μm^2 /mW and the device experiences an emitter junction to ambient temperature increase ΔT = 51°C when biased at peak f_τ, f_{max}.

These results demonstrated for the first time that InP metamorphic DHBTs can

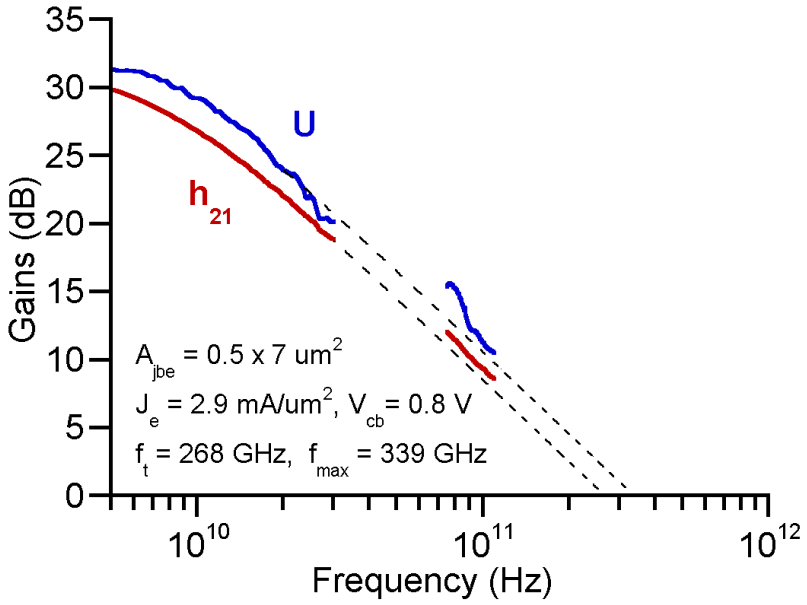

Figure 4.37: Measured microwave gains for 200 nm collector metamorphic DHBT – Peak f_τ, f_{max}

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demonstrate electrical equivalence compared to InP DHBTs grown on a lattice-matched substrate. Thermal measurements of the mHBT show only a small increase in θ_{JA} due to the 1.5 μm thick InP buffer grown on the GaAs substrate. A thorough discussion with supporting experimental data of the thermal resistance of InP mHBTs from UCSB have been reported in the following publications – [19, 20, 21].

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5

Static frequency divider results

STATIC frequency dividers were designed and simultaneously fabricated at Global Communication Semiconductors (GCS), UCSB, and Rockwell Scientific (RSC). This chapter discribes the measurement systems required to test divider circuits to 150 GHz and the results from each firm.

A schematic of the emitter coupled logic (ECL) divide-by-2 circuit is shown in Fig. 5.1. The divider interconnect bus is doubly-terminated by the load resistors R_L to make the interconnects short and keep the wiring delays small. Because the parasitic voltage drop $\Delta V_{parasitic} \cong J_e \rho_c$ across the emitter resistance limits the maximum toggle rate and the HBTs utilized in the designs could support higher current densities J_e, a lower load resistance is utilized such that larger devices operating at higher currents I_c are used in order to reduce the major delay $\tau = C_{cb} \Delta V_{logic} / I_c$, where ΔV_{logic} is maintained at 300 mV. A peaking inductor is added in series with R_L to decrease the transition time of the changing logic state on the bus. To keep the capacitive loading on the signal bus low, an output buffer using small devices

restores the output signal so that it can be measured off-chip. Lastly, thin-film dielectric microstrip wiring is employed for the circuit interconnects because of its predictable characteristics, controlled impedance, and reduced line coupling at very high frequencies. The circuit lay-out was varied to produce many versions, where the HBT junction areas were adjusted slightly so as to realize the fastest possible divider circuit associated with the other fixed design parameters. The maximum simulated toggle rate was 168 GHz.

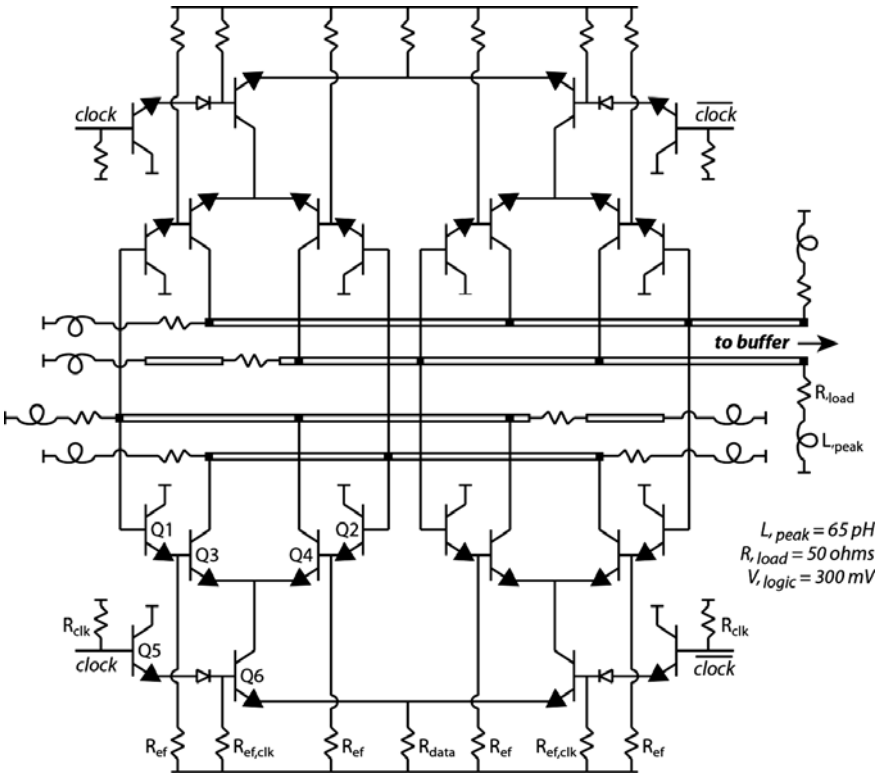

Figure 5.1: Circuit diagram of ECL static frequency divider w/ design details

5.1 Static divider testing and measurement equipment

Testing of divide-by-2 and divide-by-4 circuits took place at UCSB and the Mayo Foundation Special Purpose Processor Development Group. After circuit fabrication was complete, wafers were brought to UCSB for an initial screening to investigate yield, and to test divider functionality from DC to 110 GHz. Non-phase locked signal sources beyond 110 GHz are available at UCSB and divider testing possible, however a functional divide-by-2 beyond 110 GHz requires the output signal be down-converted for spectrum analyzer measurement. Because the down-convert mixer does not have a pre-selector, all intermixing products of the RF and LO signal are visible. When combined with the cabling losses, it is difficult to determine if a divide-by-2 is functioning correctly.

A program milestone required that a 150 GHz divider be produced. It was the responsibility of the Mayo Foundation to repeat the divider measurements of the participating contractors. Since testing beyond 110 GHz was not feasible for divide-by-2 circuits, the self-oscillation frequency of many dividers was determined. Those with the highest self-oscillation frequency were identified and tested further at the Mayo Foundation.

When the circuit bias is adjusted to achieve its maximum clock rate $f_{clk,max}$, the divider may begin operating in a dynamic mode. To be certain the divider is static, the circuit is toggled at low frequency at the same bias associated with $f_{clk,max}$.

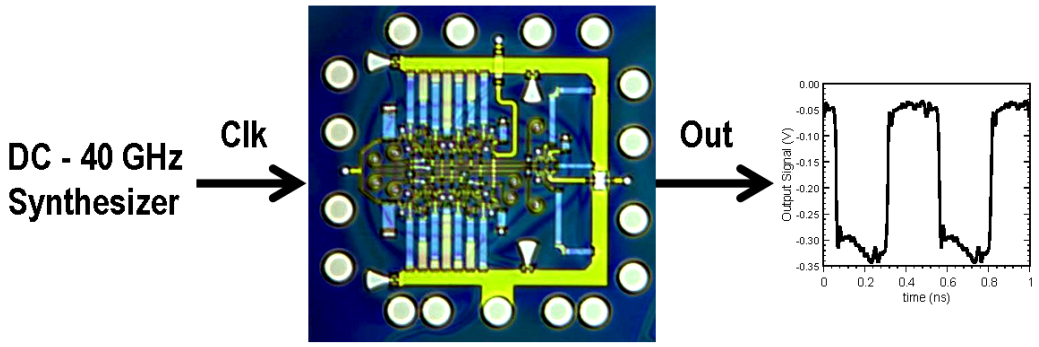

Figure 5.2: DC-40 GHz divider testing

Fig. 5.2 shows the measurement setup for testing between DC-40 GHz. The synthesizer signal is delivered directly on-wafer.

Fig. 5.3 shows the measurement setup for divider testing from 50-75 GHz (V-band) and 75-110 GHz (W-band). For V-band measurements, the synthesizer drives a frequency tripler for testing between 50-75 GHz, and the signal is delivered on-wafer using a WR-15 waveguide coupled probe. For W-band measurements, the synthesizer drives a 20-40 GHz amplifier, whose output drives a frequency tripler for testing between 75-110 GHz, and the signal is delivered on-wafer using a WR-10 waveguide coupled probe.

Fig. 5.4 shows the measurement setup for divider testing from 110-136 GHz. A backward-wave-oscillator (BWO) produces the source signal without any frequency multiplication that is delivered on-wafer using a WR-06 waveguide coupled probe.

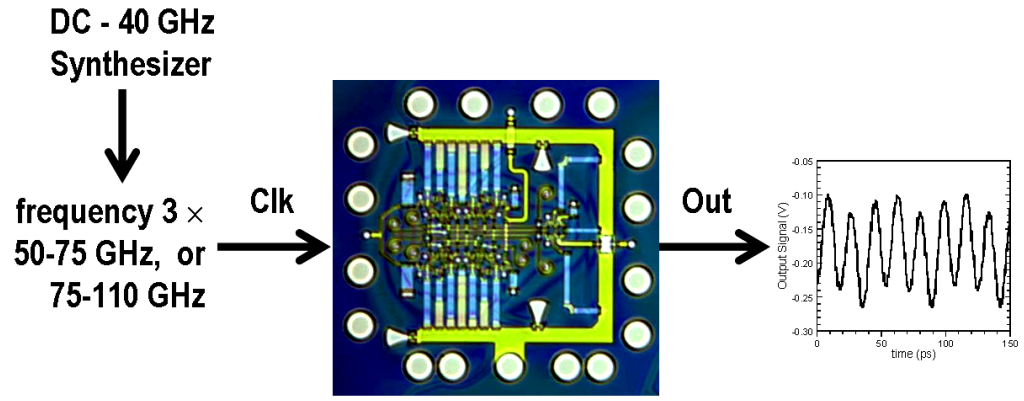

Figure 5.3: 50-75 and 75-110 GHz divider testing

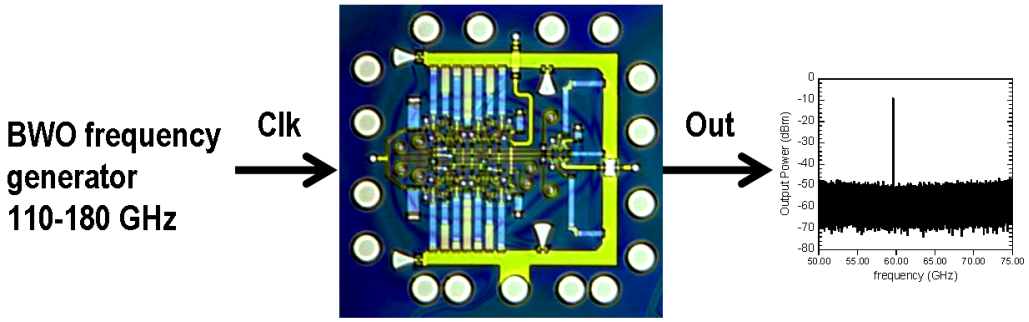

Figure 5.4: 110-136 GHz divider testing

The output spectrums from DC-50 GHz and 50-75 GHz were monitored simultaneously to ensure that the measured $f_{clk}/2$ is the fundamental signal and not harmonic content associated with a failing divider operating in an $f_{clk}/3$ or $f_{clk}/4$ state.

Fig. 5.5 shows the measurement setup for divider testing from 136-156 GHz. A

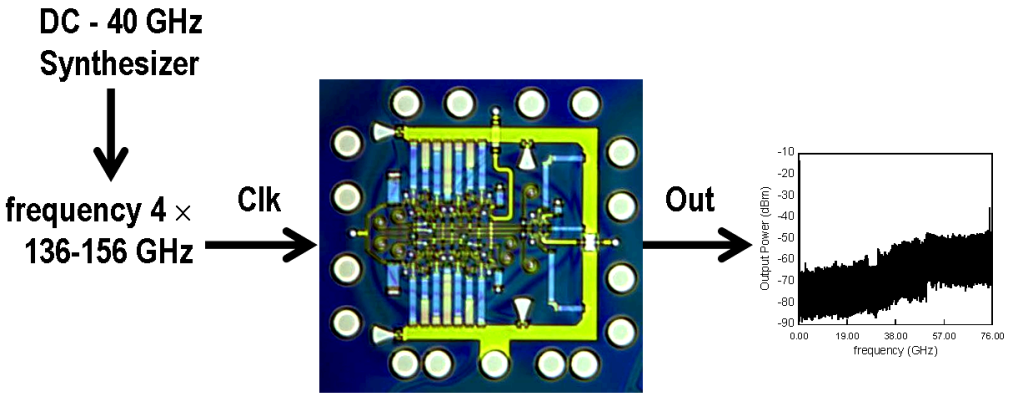

Figure 5.5: 136-156 GHz divider testing

phase-locked synthesizer signal is quadrupled using a Virginia Diode (VDI) doubler chain, and the source signal is delivered on-wafer using a WR-05 waveguide coupled probe. As with the 110-136 GHz testing, the output spectrums from DC-50 GHz and 50-75 GHz were monitored simultaneously to ensure that the measured $f_{clk}/2$ is the fundamental signal.

Table 5.1: Key device parameters of the 118.7 GHz static divider

	units	Q1, Q2	Q3, Q4	Q5	Q6
A_e	μm^2	0.5 × 4	0.5 × 4	0.5 × 5	0.5 × 5
J_e	mA/μm^2	5.0	6.0	4.0	4.8
V_{cb}	V	0.0	0.6	0.6	0.6
f_τ	GHz	220	235	255	255
f_{max}	GHz	150	265	260	260

5.2 GCS manufactured dividers

5.2.1 First wafer lots, October 2003–excessively high C_{cb}

The first completed circuit wafers from GCS demonstrated working dividers. RF device measurements showed that the base-collector capacitance C_{cb} was twice as high as specified at 0.0 V_{cb}, suggesting that the collector was severely undepleted. Upon investigation, it was discovered that the growth of the pulse doping layer in the collector was excessive and the reason for the excessive C_{cb}. This problem has since been resolved. For discrete HBT measurements, the V_{cb} potential could be increased to more fully deplete the collector and improve device bandwidth. This could not be done within the divider circuits and their bandwidth suffered. However, circuit testing was promising. Divide-by-2 and divide-by-4 circuits operating from 2 to 111 GHz were demonstrated. These were the first such circuits to operate beyond 100 GHz [1]. The fastest dividers were identified and the wafer was sent to the Mayo Foundation.

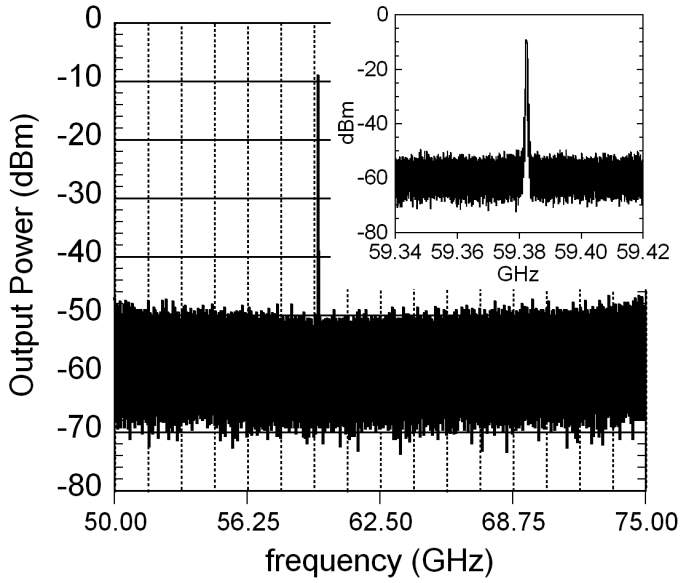

Figure 5.6: GCS fabricated divide-by-2 output spectrum, f_{clk} = 118.70 GHz, f_{out} = 59.35 GHz

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Testing at higher frequencies demonstrated increased circuit bandwidth. The fastest divide-by-2 circuit had a maximum toggle rate of 118.7 GHz. Excluding the output buffer, the circuit consumed 620 mW within the divider core. The output spectrum at $f_{clk}/2$ = 59.38 GHz is shown in Fig. 5.6. Tab. 5.1 summarizes the discrete RF performance of different HBTs within the circuit (Fig. 5.1) at their respective bias conditions. The fastest divide-by-4 circuit had a maximum toggle rate of 115.72 GHz. The output spectrum at $f_{clk}/2$ = 28.93 GHz is shown in Fig. 5.7.

Sensitivity measurements were performed from f_{clk} = 3 to 118.70 GHz on the divide-by-2 circuit (Fig. 5.8). The self-oscillation frequency of the divider was

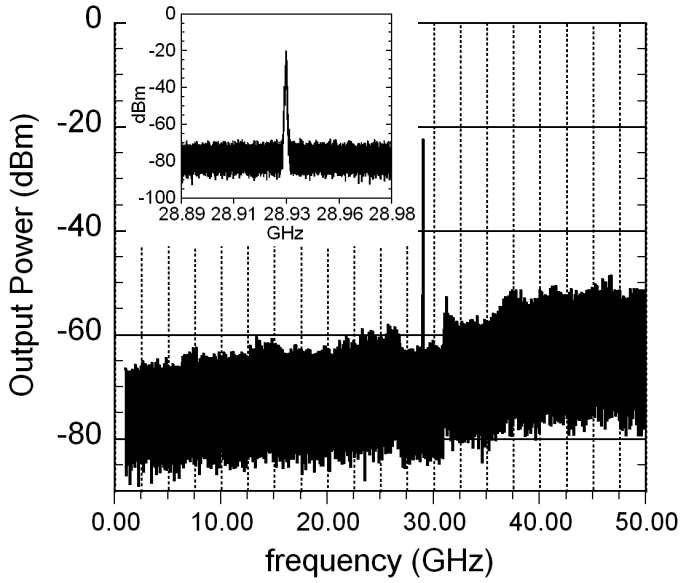

Figure 5.7: GCS fabricated divide-by-4 output spectrum, f_{clk} = 115.72 GHz, f_{out} = 28.93 GHz

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75 GHz. The discontinuity between V-band and W-band testing is due to the minimum input power requirements of the W-band frequency tripler. Circuit results were summarized and reported in [2].

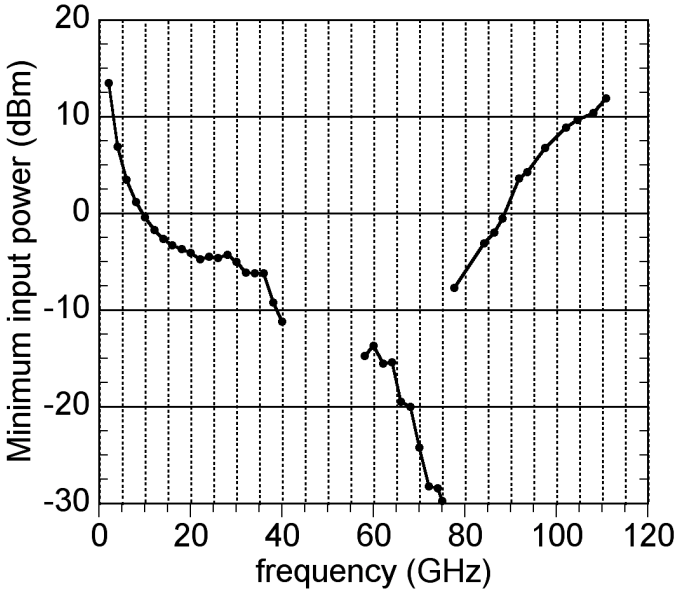

Figure 5.8: Sensitivity plot of 118.7 GHz divide-by-2

Table 5.2: Key device parameters of the 150 GHz static divider

	units	Q1, Q2	Q3, Q4	Q5	Q6
A_e	μm^2	0.5 $\times$ 5	0.5 $\times$ 4	0.5 $\times$ 6	0.5 $\times$ 5
J_e	mA/μm^2	4.0	6.0	3.3	4.8
C_{cb}/I_c	ps/V	0.99	0.59	0.86	0.59
V_{cb}	V	0.0	0.6	1.7	0.6
f_τ	GHz	260	301	280	301
f_{max}	GHz	268	358	280	358

5.2.2 Good wafer lots, February 2004–150 GHz dividers

Excessive base-collector capacitance C_{cb} lessened the maximum clock rate of the first batch of circuits. The InP DHBT growth inaccuracies were resolved and static frequency dividers were fabricated again at GCS.

Divide-by-2 and divide-by-4 circuits were clocked as low as 3 GHz to show they are fully static in nature – the output waveform at $f_{clk}/2$ = 1.5 GHz is shown in Fig. 5.9. Measurements continued with most of the dividers operating to f_{clk} = 112 GHz. Divide-by-2 testing at UCSB ceased. Further divide-by-4 testing continued, utilizing GUNN oscillator sources operating to 140 GHz. A maximum toggle rate of $f_{clk,max}$ = 137 GHz was demonstrated, where the output spectrum at $f_{clk}/4$ = 34.25 GHz is shown in Fig. 5.10.

The fastest dividers were identified and circuit testing continued at the Mayo Foundation under the supervision of UCSB and Rockwell Scientific. Attempts to test divide-by-4 circuits did not reveal any operating beyond f_{clk} = 137 GHz. The

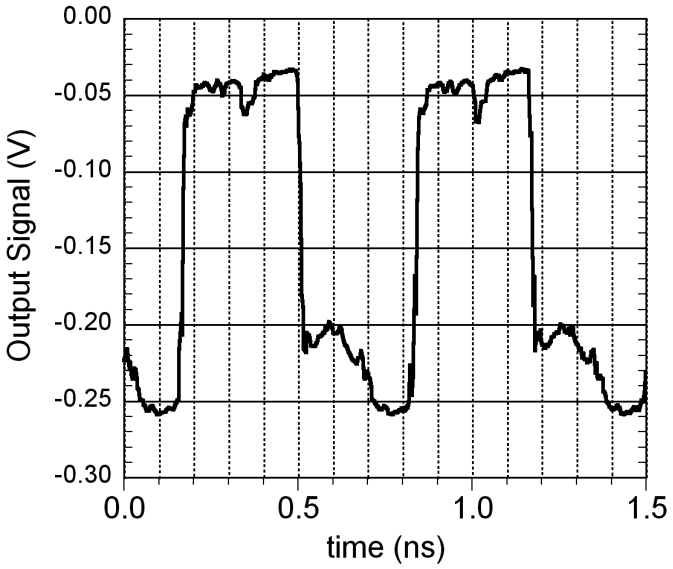

Figure 5.9: GCS divide-by-2 output waveform, f_{clk} = 3 GHz, f_{out} = 1.5 GHz

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maximum toggle rate of the divide-by-4 was not limited by the input stage, rather the second stage did not operate as fast as designs had predicted. This was confirmed by testing separately the second divider stage. Configured as a divide-by-2, it only showed an $f_{clk,max}$ = 72 GHz.

Divide-by-2 circuits demonstrated an f_{clk} = 150 GHz. The signal power delivered on-wafer was $\sim$ 11 dBm. The output spectrum at $f_{clk}/2$ is shown in Fig. 5.11. As the toggle frequency increased to 152 GHz, the divider operated correctly. However, the output power at $f_{clk}/2$ reduced by $\sim$ 8 dBm. At higher frequencies, no output signal was visible. The platten where the wafer rested was reduced in tempera-

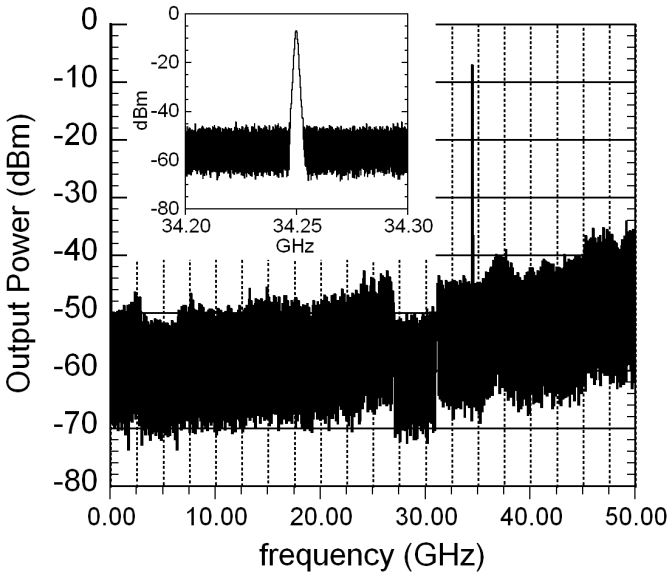

Figure 5.10: GCS fabricated divide-by-4 output spectrum, f_{clk} = 137 GHz, f_{out} = 34.25 GHz

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ture from 25°C to 20°C. Returning to 152 GHz, the $f_{clk}/2$ output signal increased by $\sim$ 10 dBm due to the reduction in wafer temperature. f_{clk} was increased to 153 GHz and the divide-by-2 demonstrated the correct $f_{clk}/2$ output spectrum at 76.5 GHz, shown in Fig. 5.12. Excluding the output buffer, the circuit consumed 595 mW from the divider core. Testing at higher frequencies was not attempted. Sensitivity measurements were performed from f_{clk} = 3 to 153 GHz on the divide-by-2 (Fig. 5.13). The self-oscillation frequency was 87 GHz.

The maximum simulated and measured f_{clk} of the divide-by-2 are in good agreement – simulated $f_{clk,max}$ = 168 GHz, measured $f_{clk,max}$ = 153 GHz. Excessive de-

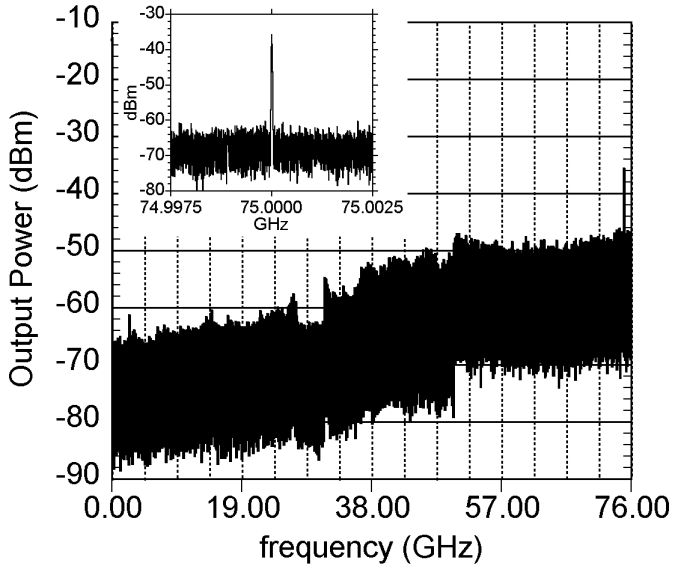

Figure 5.11: GCS fabricated divide-by-2 output spectrum, f_{clk} = 150 GHz, f_{out} = 75 GHz at T = 25°C

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vice self-heating associated with clock-level emitter followers (Q5, Fig. 5.1) limited divide-by-2 bandwidth beyond 152 GHz, such that cooling was required to increase the toggle rate. Because these designs did not employ a level-shift diode between Q5 and Q6, the additional V_{be} voltage drop required for correct Q6 bias was applied by an external supply at the base of Q5. This significantly increased the power density under DC operation in Q5 – J_e = 3.3 mA/μm^2, V_{ce} = 2.7 V, $P \approx$ 9 mW/μm^2. At 150 GHz f_{clk}, input signal power required for the divider to function was $\sim$ 11 dBm. Recall, the clock signal is applied to the divider single-ended, thus the toggle voltage $V_{clk} \approx$ 1.1 V$_{p-p}$ appears at the base of Q5. Therefore, the peak maximum power dissipated in Q5 is as high 11 mW/μm^2. Under these operating conditions, the HBTs

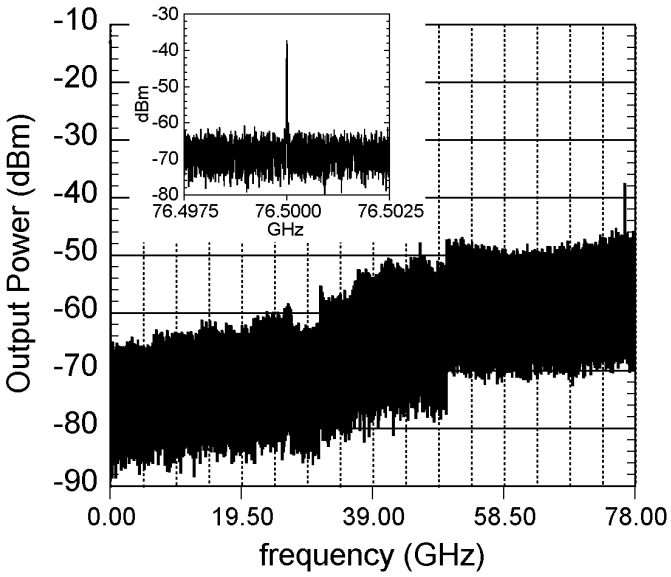

Figure 5.12: GCS fabricated divide-by-2 output spectrum, f_{clk} = 153 GHz, f_{out} = 76.5 GHz at T = 20°C

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experience significant device self-heating and are unable to operate at higher bandwidths. This was not considered in detail at the time of design.

In addition to this divide-by-2 result, other firms have demonstrated static frequency dividers operating beyond 150 GHz. HRL has reported a divide-by-8 circuit operating to 151.2 GHz [4] utilizing a CML topology. In order to achieve this bandwidth, a -30°C stream of air cooled the surface of the wafer during testing. Vitesse has reported a divide-by-2 circuit operating to 152.05 GHz [5] utilizing an ECL topology. Northrop Grumman has reported a divide-by-2 circuit operating to 153.0 GHz [6] utilizing a CML topology.

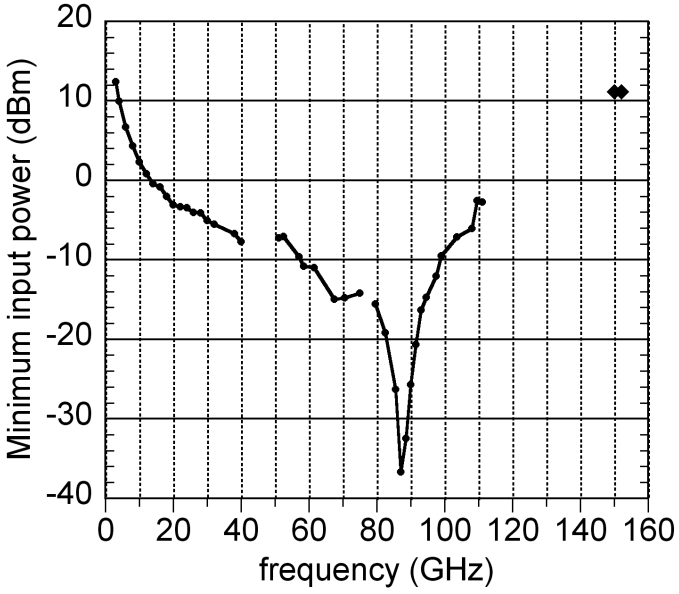

Figure 5.13: Sensitivity plot of 150 GHz divide-by-2

5.3 UC Santa Barbara manufactured dividers

Static frequency dividers were fabricated at the UCSB Nanofabrication Facility with a projected maximum clock rate $f_{clk} > 160$ GHz. These circuit designs were similar to those fabricated at GCS because the HBT base and collector designs were the same. Circuit layout changes were necessary because of differences between the processes.

The new UCSB circuits process was utilized to fabricate divide-by-2 and divide-by-4 circuits. Discrete device yield was high $\sim$ 100%, however circuit yield was low (less than 5%) because of complications associated with the formation of the M1-ground plane interconnect posts, and BCB etching before depositon of the ground plane. This was confirmed during circuit testing. In most instances a waveform at f_{clk} was observed, indicating that more than one load resistor was not properly terminated to the ground plane.

Amongst the functional dividers, they were clocked as low as 4 GHz to show they are fully static in nature. The output waveform at $f_{clk}/2$ = 2.0 GHz is shown in Fig. 5.14. Measurements continued, with divide-by-2 and divide-by-4 circuits operating to f_{clk} = 113 GHz (Fig. 5.15). Circuit testing continued at the Mayo Foundation under the supervision of UCSB and Rockwell Scientific. A divide-by-2 circuit with a maximum toggle rate $f_{clk,max}$ = 142 GHz was demonstrated. The output spectrum at $f_{clk,max}/2$ = 71 GHz is shown in Fig. 5.16, where the signal power delivered on-

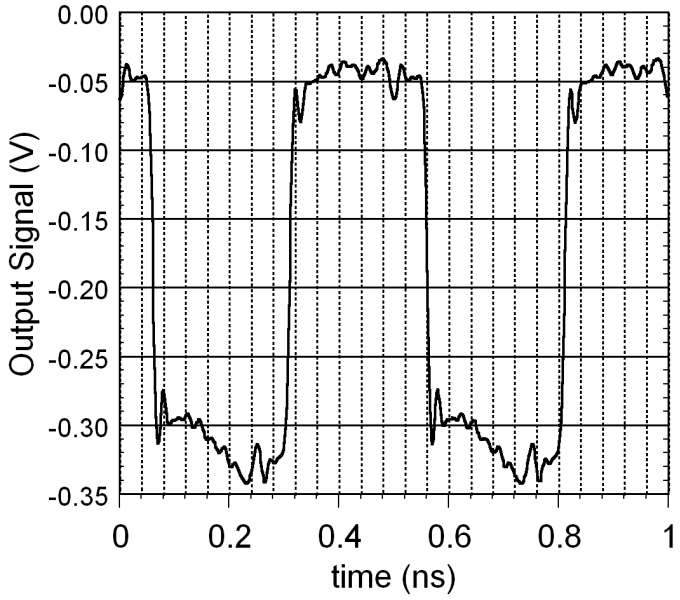

Figure 5.14: UCSB divide-by-2 output waveform, f_{clk} = 4 GHz, f_{out} = 2 GHz

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wafer was $\sim$ 11 dBm. Excluding the output buffer, the circuit consumed 800 mW within the divider core. At higher frequencies, the divider failed, operating in a divide-by-3 or divide-by-4 state. Sensitivity measurements were performed from f_{clk} = 4 to 142 GHz. The self-oscillation frequency was 84 GHz. Because of time restrictions, divide-by-4 circuits were not tested at higher frequencies.

The maximum toggle rate of the dividers was lower than projected. Compared to GCS, the UCSB HBT process produces much lower values of emitter and base contact resistance. This is reflected in the RF device measurements. Peak HBT f_τ / f_{max} from the 150 GHz GCS divider wafer was 301/358 GHz, whereas peak

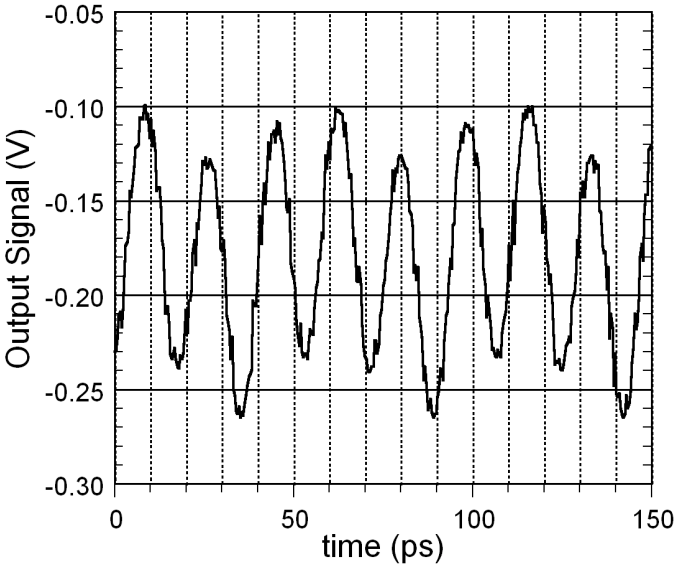

Figure 5.15: UCSB divide-by-2 output waveform, f_{clk} = 113.1 GHz, f_{out} = 56.55 GHz–the highest available sampling scope measurement

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HBT f_τ / f_{max} from the 142 GHz UCSB divider wafer was 391/505 GHz. For all divider designs, the HBTs within the circuit are biased closely to $J_e = J_{Kirk}$ for minimum C_{cb}/I_c ratio. An error while processing the UCSB dividers resulted in the sheet resistance of the resistors being 20% lower than specified in the designs, significantly increasing the operating current density for some of the HBTs. From Fig. 5.1, devices Q3-Q6 were affected little. However, the bias current I_{ef} of the emitter followers on the data level (Q1,Q2) exceeds I_{Kirk} by $\sim$ 40%. This causes C_{cb} for Q1 and Q2 to increase significantly and explains why the UCSB divider performance suffers compared those fabricated at GCS.

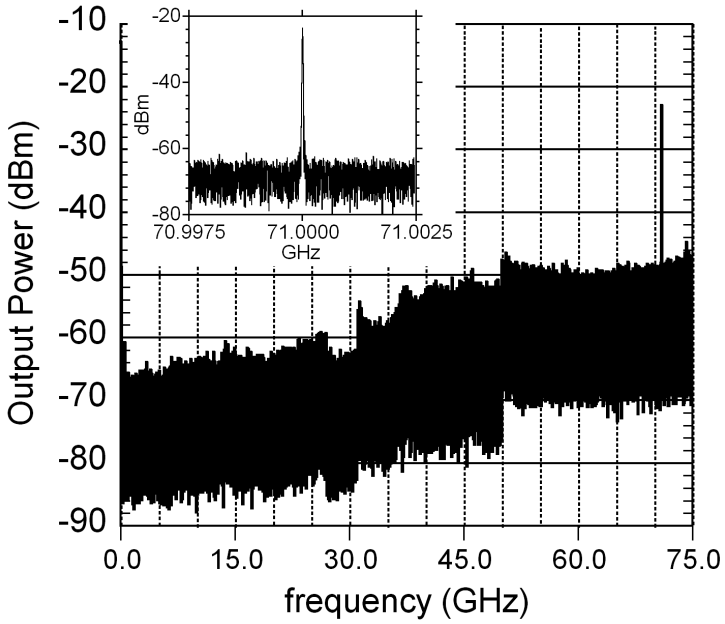

Figure 5.16: UCSB fabricated divide-by-2 output spectrum, f_{clk} = 142 GHz, f_{out} = 71 GHz

5.4 Rockwell Scientific manufactured dividers

The divider circuits from GCS and UCSB were realized in a standard-mesa HBT technology, utilizing evaporated contacts, metal lift-off, and a self-aligned base contact. These device features are key limiters to the yield of circuits with high transistor counts. Processes are being development at Rockwell Scientific (RSC) to eliminate these failure mechanisms from the device formation steps. The new process involves electroplating the emitter and base contacts, and using a dielectric sidewall around the emitter. The sidewall provides electrical isolation between the emitter and base.

The process is described in detail in [8]. Static frequency dividers were demonstrated in the early phases of this technology. The circuit designs were similar to the dividers produced by GCS and UCSB.

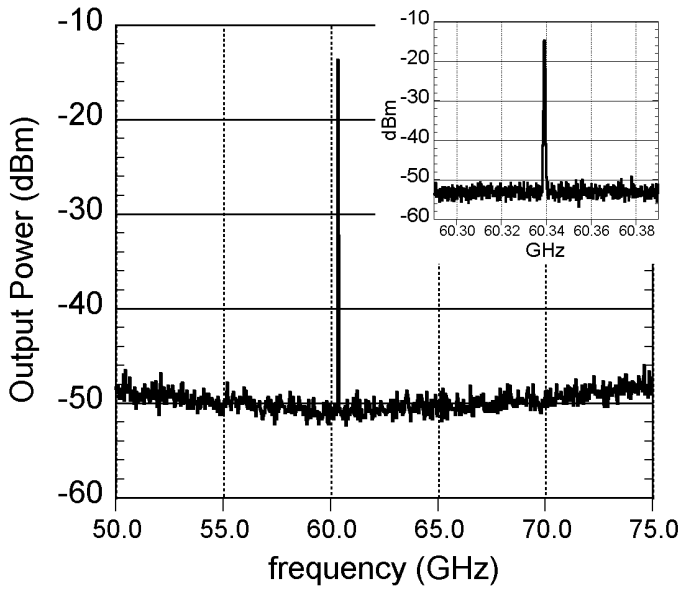

Figure 5.17: RSC fabricated divide-by-2 output spectrum, f_{clk} = 120.68 GHz, f_{out} = 60.34 GHz

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Divide-by-2 circuits were clocked as low as 4 GHz to show they are fully static in nature. Measurements continued to f_{clk} = 111 GHz. The fastest dividers were identified and the wafer was sent to the Mayo Foundation. Testing at higher frequencies demonstrated increased circuit bandwidth. The fastest divide-by-2 circuit had a maximum toggle rate of 120.68 GHz. The output spectrum at $f_{clk}/2$ = 60.34 GHz is shown in Fig. 5.17.

Circuit performance for these dividers was slower than those from GCS and UCSB because of increased parasitics associated with RSC process. Significant improvements have since been made. Device and circuit results from this technology having increased bandwidth will be reported in the future.

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6 Conclusions

6.1 Accomplishments

6.1.1 Process development

The HBT fabrication process underwent many changes in order to increase device bandwidth and yield, and they are summarized. The local-alignment feature of the GCA i-line photolithography stepper was well characterized, generating reproducible alignment error within $\pm$ 0.15 μm of the target feature. This allowed the extrinsic base-collector mesa to be reduced by 2:1 when compared to HBTs from UCSB prior to this work. Through the combined use of advanced photoresist processes and the new E-beam evaporator (E-beam-4), metal spikes and artifacts associated with metal liftoff are no longer present. This increased the HBT yield of 0.5 μm wide emitter junctions to 100%. Improved semiconductor surface preparation prior metal deposition of the device contacts was explored for reduced contact resistance. Through the combined use of an UV-ozone plasma treatment and di-

luted NH_4OH dip to the sample before loading into the evaporator, a 2:1 reduction in all contact resistances has been observed. The dielectric passivation material was changed from polyimide to BCB, reducing the HBT leakage currents for the base and collector by 100×. A collector post feature was added so that during the BCB passivation etch-back, once the collector, base, and emitter contacts were exposed, the etching would stop. Because the wafer is now planarized and the contacts exposed, interconnects can be deposited and step-coverage issues are avoided. Process steps associated with the formation of the thin-film microstrip wiring environment were modified from the original process reported by S. Krishnan [1]. Tall posts are now formed after the second layer of interconnect metal. BCB is deposited, etched back to reveal the interconnect posts, and the ground plane is evaporated. Through the utilization of these process changes, InP HBTs and circuits employing them have been demonstrated. The results are summarized in the following sections.

6.1.2 HBT results

Tab. 6.1 summarizes discrete InP DHBT DC and RF performance for the layer structures investigated. Progressive scaling of the high thermally resistive ternary layers from the collector, combined with reductions to the emitter and base resistance allowed f_τ and f_{max} to increase and remain simultaneously high as the collector was thinned from T_c = 210 nm to 100 nm. The bias conditions associated

Table 6.1: Summary of electrical characteristics for all HBTs fabricated in this work – from April 2003 to January 2005, listed sequentially. **Bold** listed values of f_τ and f_{max} indicate record performance for InP-DHBTs at the time of measurement and publication.

	thickness			emitter	base		collector			
DHBT	col / base	β	BV_{CEO}	ρ_c	ρ_s	ρ_c	ρ_s	ρ_c	f_τ	f_{max}
19b	150 / 30	11	5.6	15	603	20	12.9	12	**370**	**459**
mHBT	200 / 30	35	5.7	20	814	14	—	—	**268**	**339**
22	150 / 30	36	5.1	10.1	564	9.6	11.9	5.4	**391**	**505**
24	210 / 35	21	6.9	7.2	446	6.1	12.6	5.5	276	451
25	100 / 30	41	3.1	7.8	629	6.2	12.9	4.0	**490**	**415**
26	100 / 30	47	3.1	10.4	616	3.8	13.3	5.8	465	416
27	120 / 30	40	3.9	8.4	610	4.6	12.1	8.4	**450**	**490**
	nm		Volts	ρ_c, $\Omega \cdot \mu$m^2 and ρ_s, Ω/sq					GHz	

with peak f_τ and f_{max} were well below a bias where device self-heating affected performance. For future InP DHBT designs, higher operating power densities can be tolerated as the collector thickness, device footprint, and emitter and base resistivities are scaled for increased bandwidth. Fig. 6.1 summarizes the device f_τ and f_{max} from different HBT manufacturers as of July 2005.

6.1.3 150 GHz ECL static frequency dividers

InP HBTs from UCSB were measured and modeled for use in static frequency divider designs having a toggle rate $>$ 150 GHz. HBTs having a collector thickness of 150 nm were utilized. The devices were sized to operate at a current density $J_e \approx J_{Kirk}$ to minimize the C_{cb}/I_c ratio of the device. However, the devices were

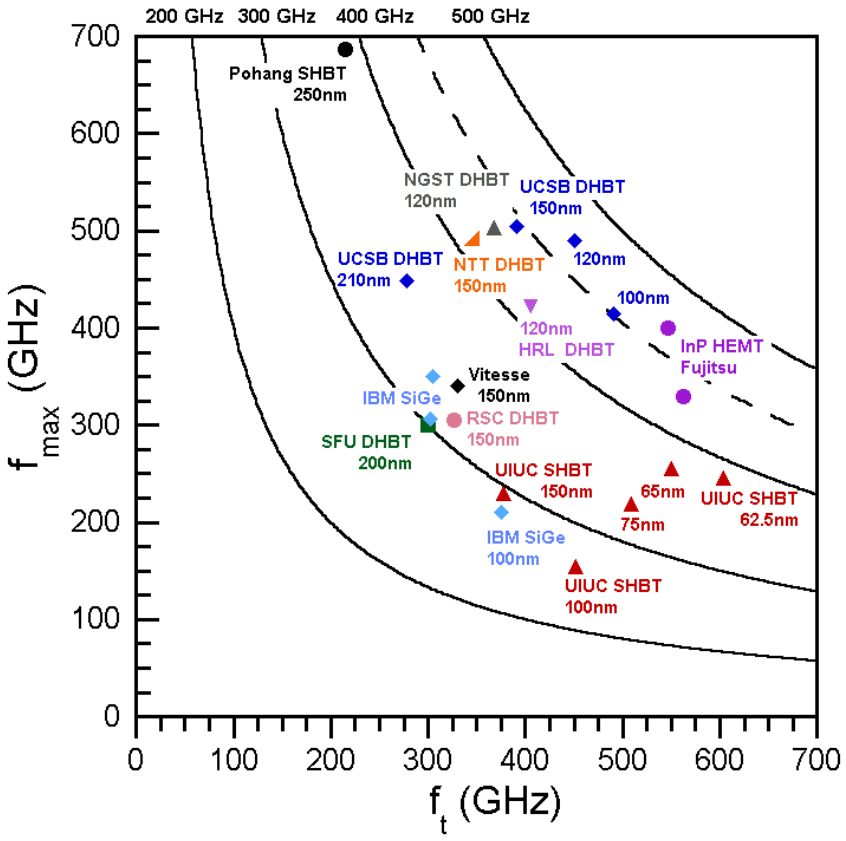

Figure 6.1: Summary of f_τ and f_{max} performance from various HBT manufacturers at the collector thickness cited – updated June 2005

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not scaled so small to where the parasitic voltage drop across the emitter resistance $\Delta V_{parasitic}$ becomes a significant fraction of ΔV_{logic}. Because there was no power budget assigned for the designs, emitter coupled logic was used for reduced gate delay when compared to the current mode logic topology. The maximum simulated toggle rate was 168 GHz.

These circuit designs were fabricated independently at GCS, UCSB, and Rock-

well Scientific (RSC). The GCS and UCSB process makes use of a mesa HBT technology, whereas the RSC process is more advanced and intended to produce circuits having $>$ 10,000 HBTs. A 153 GHz divide-by-2 was demonstrated from GCS. A 142 GHz divide-by-2 was demonstrated from UCSB. This is a 63% increase in $f_{clk,max}$ compared to the previous dividers from UCSB. Lastly, a 120.8 GHz divide-by-2 was demonstrated from RSC while the process was in its infancy.

Other firms have demonstrated static frequency divider operating to 150 GHz. At the time this work began (April 2003), the maximum toggle rate for a static frequency divider in an InP and SiGe material system were 100 GHz and 86 GHz [3] respectively. Today (June 2005) the maximum toggle rate for a static frequency divider in an InP and SiGe material system is 153 GHz (this work) and 102 GHz [4] respectively.

6.2 Future work

For InP DHBTs to gain wider acceptance, more circuits utilizing these devices need to be demonstrated. The circuits must operate at higher frequencies where SiGe HBTs cannot similarly compete. InP HBT circuits consuming less power than could be realized in SiGe at similar bandwidths are needed as well. Attempts to demonstrate such circuits have been attempted and are reported here.

6.2.1 150 GHz CML static frequency dividers

A new set of static frequency dividers operating at 150 GHz were designed utilizing HBTs with a 120 nm collector for increased operating current density J_e and reduced C_{cb}/I_c ratio. Unlike the divider designs that employed emitter coupled logic (ECL), the new designs utilize current mode logic (CML), shown in Fig. 6.2. The power consumption associated with the CML topology is significantly less than ECL because the emitter followers have been removed (and their respective operating

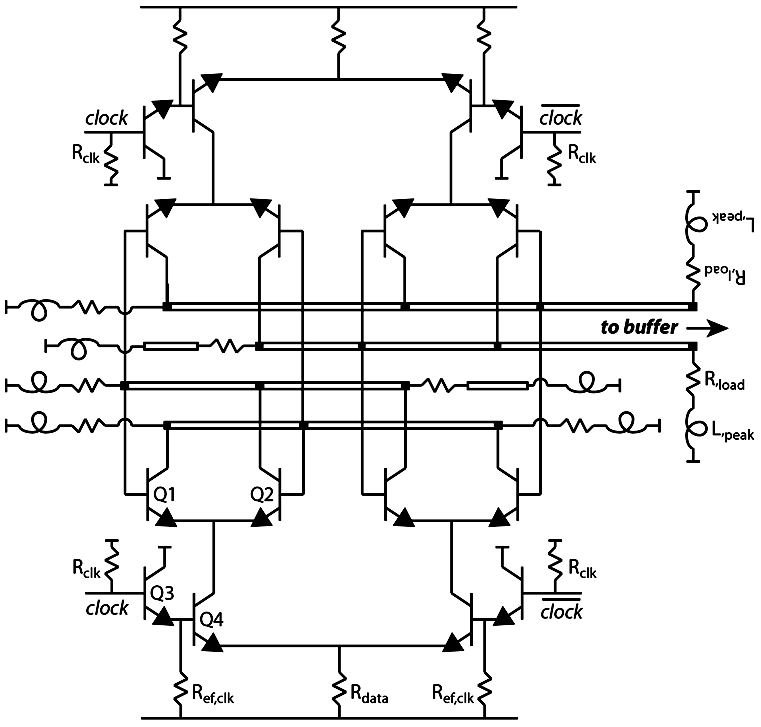

Figure 6.2: Circuit diagram of current mode logic (CML) static frequency divider

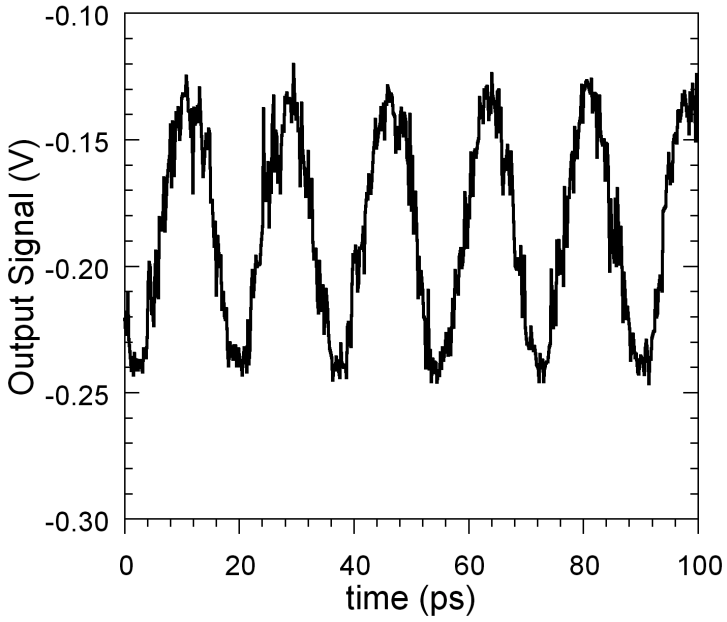

Figure 6.3: CML divide-by-2 output waveform – $f_{clk,max}$ = 112.5 GHz, f_{out} = 56.25 GHz

currents) from the data level, such that only devices Q1 and Q2 remain (Fig. 6.2). Devices throughout the circuit are sized to either operate at a J_e slightly above J_{Kirk} (reduced C_{cb}/I_c ratio), or to a point where the voltage drop across the emitter resistance ($\Delta V_{parasitic}$) is not excessive.

Initial circuit results have been demonstrated. The dividers were fabricated at RSC utilizing their dielectric sidewall spacer process. Divide-by-2 circuits were toggled from f_{clk} = 4 GHz to an $f_{clk,max}$ = 112.5 GHz (Fig. 6.3). Excluding the output buffers, the circuit consumed 212 mW. Testing at higher frequencies has not been pursued. The source-free self-oscillation frequency (no signal applied) was

$\sim$ 78 GHz. This suggests that the divider could operate as high as 125 GHz. Circuit performance was slower than projected because a 150 nm thick was used, not 120 nm as designed for. This increases the C_{cb}/I_c ratio for Q1 and Q2 (Fig. 6.2) because of the lower J_{Kirk} associated with thicker collectors, and hence the gate delay increases. Currently, more dividers are being fabricated at Rockwell Scientific with 120 nm collector thickness while employing a collector pedestal to further reduce the C_{cb}/I_c ratio of the HBT. With these considerations, the maximum simulated toggle frequency is 164 GHz, while consuming $\sim$ 210 mW. This would be approximately one-third of the power consumed by the 150 GHz ECL divider result reported.

6.2.2 Ultra low power CML static dividers

Additional CML designs were pursued with the intent of reducing to a minimum the required supply voltage and operating currents within the circuit, and investigating the maximum divider toggle rate associated with this bias. The circuit diagram of the ultra-low power CML divider is similar to the previously discussed CML designs, shown in Fig. 6.2. ΔV_{logic} is 250 mV and the effective loading resistance is 100 Ω (200 Ω $\parallel$ 200 Ω) – I_{data} = 2.5 mA. In order for the divider to simulate accurately, the emitter follower devices (Q3) required a minimum $I_{ef,clk}$ = 1.2 mA. The HBTs within the circuit are sized to the smallest yieldable device dimensions, yet J_e

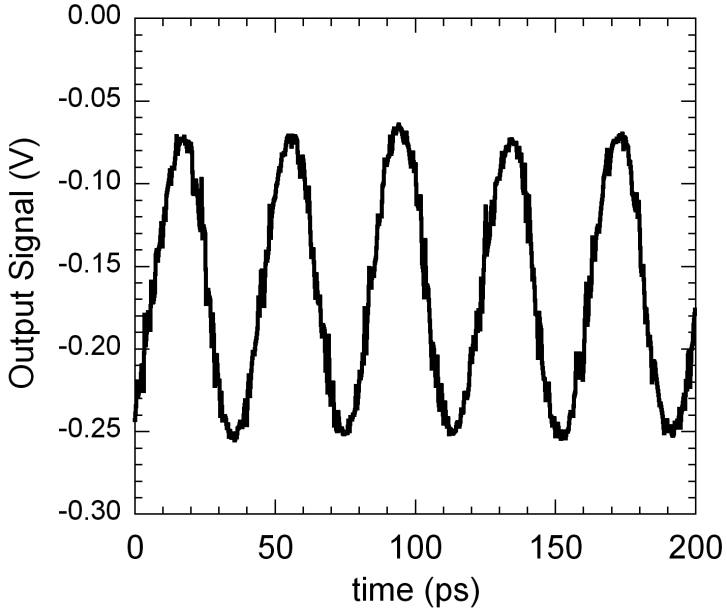

Figure 6.4: Ultra low power CML divide-by-2 output waveform – $f_{clk,max}$ = 51 GHz, f_{out} = 25.5 GHz

for these devices is still much less than J_{Kirk}.

Initial circuit results have been demonstrated. The dividers were fabricated at Rockwell Scientific utilizing their dielectric sidewall process. Divide-by-2 circuits were toggled from f_{clk} = 12 GHz to an $f_{clk,max}$ = 51 GHz (Fig. 6.4). Excluding the output buffers, the circuit consumed 23.6 mW at f_{clk} = 48 GHz, and 29.2 mW at $f_{clk,max}$. At higher frequencies the divider failed. The source-free self-oscillation frequency (no signal applied) was $\sim$ 34 GHz. The latch power-delay product (figure-of-merit of digital circuits) is 123 fJ and 143 fJ at 48 GHz and 51 GHz, respectively. This is a factor of 2 reduction in power-delay product for digital circuits in an InP

HBT material system [5]. These divider circuits will continue to improve in bandwidth. Because the emitter junction area is small compared to the collector area, the gate delay is dominated by the extrinsic C_{cb} of the device footprint. By utilizing a collector pedestal within the HBTs, the maximum toggle rate is projected to double to 100 GHz while consuming only $\sim$ 30 mW. If such a circuit could be realized, it would demonstrate how advanced InP HBT technologies could be used for both ultra high bandwidth circuits beyond 300 GHz (neglecting power budget) *and* 100 GHz applications consuming very little power – two domains where SiGe technologies would have difficulty competing.

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A

Metal-semiconductor contact resistance

THIS section reviews the basic theory of metal-semiconductor contacts having depletion type contacts ($\Phi_m > \Phi_s$, n-type and $\Phi_m < \Phi_s$, p-type), where Φ_s is the energy difference between the vacuum level and Fermi potential. A general expression for the three dominant carrier transport mechanisms across the Schottky barrier are thermionic emission over the potential barrier Φ_b, tunneling through the potential barrier (field emission) depletion region, or a combination of the two (thermionic-field emission). The specific contact resistance ρ_c is defined and determined from this expression. Accumulation type contacts are not discussed.

Fig. A.1 and Fig. A.2 show the band-lineup for a metal/p-type and metal/n-type semiconductor system before and after being brought together. In contact and under thermal equilibrium the metal and semiconductor Fermi levels align. Within the bulk semiconductor, $E_c - E_f$ (n-type) and $E_f - E_v$ (p-type) are unchanged before and after contact. However, at the interface a potential barrier Φ_b remains, that in turn creates a depletion region W in the semiconductor at the junction. It is a

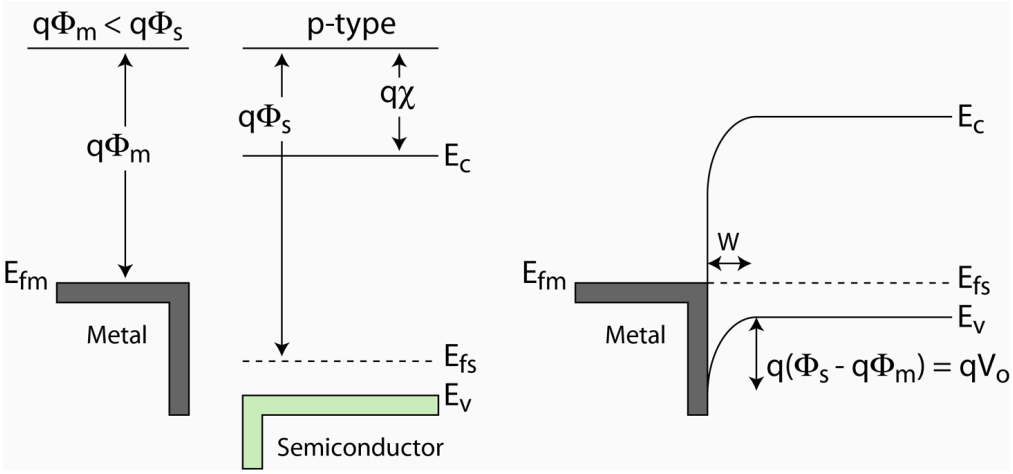

Figure A.1: Band line-up of p-type ohmic contact

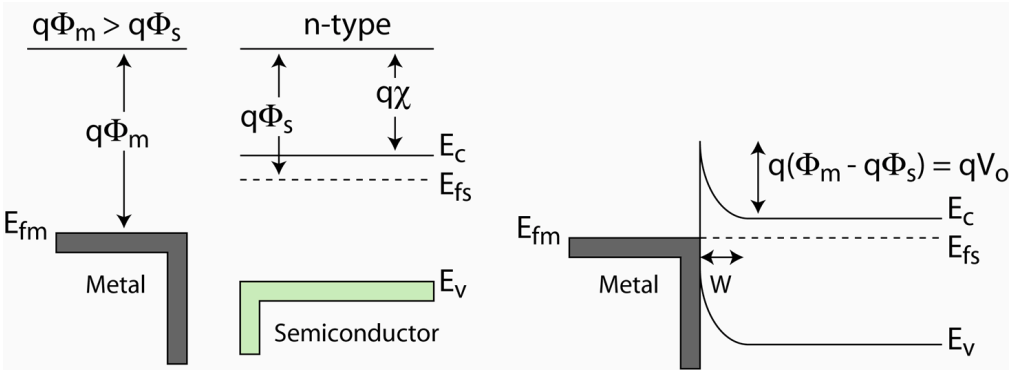

Figure A.2: Band line-up of n-type ohmic contact

consequence of the work function difference between the metal and semiconductor, the semiconductor doping, and can influenced by the history of the semiconductor surface before metal deposition.

If a parabolic barrier shape is assumed to describe the band bending over the depletion region and image force barrier lowing is ignored, the current density across the junction is [1]:

$$J = J_s \cdot \exp(qV/E_{00}) \tag{A.0.1}$$

where the saturation current is

$$J_s = \frac{A\pi^{1/2}E_{00}^{1/2}(\Phi_b - qV + \xi)^{1/2}}{kT\cosh(E_{00}/kT)} \exp\left[\frac{\xi}{kT} - \frac{\Phi_B + \xi}{E_{00}}\right] \tag{A.0.2}$$

Φ_B is the potential energy barrier at the metal-semiconductor interface, V is the applied bias at across the junction, ξ is the energy difference between the conduction band for electrons (valence band for holes) and Fermi level in the bulk semiconductor, k is Boltzmann's constant, T (K) is the temperature, and $A = 4\pi qk^2m^*/h^3$ is the Richardson constant. E_{00} is the *characteristic energy*,

$$E_{00} = \frac{qh}{2\pi}\sqrt{\frac{N}{m^* \cdot \varepsilon_o\varepsilon_r}} \tag{A.0.3}$$

where N is the doping concentration at the metal-semiconductor interface, m^* is the effective mass of the tunneling electrons, and $\varepsilon_o\varepsilon_r$ is the relative permeability of the semiconductor. If field-emission is the carrier transport mechanism, the applied potential V across the junction required to tunnel electrons across the barrier will be much smaller than the barrier energy Φ_B. The semiconductor doping will be high $\sim 10^{19}$ cm^{-3}, ξ will small in comparison to Φ_B, and the voltage dependence on the

saturation current is negligible. Under these assumptions, Equ. A.0.1 and A.0.2 can be written:

$$J = J_{so} \cdot \exp(qV/E_{00}) \tag{A.0.4}$$

$$J_{so} \cong \frac{A\pi^{1/2}E_{00}^{1/2}(\Phi_B + \xi)^{1/2}}{kT\cosh(E_{00}/kT)} \exp\left[-\frac{\Phi_B}{E_{00}}\right] = C_1 \cdot \exp\left[-\frac{\Phi_B}{E_{00}}\right] \tag{A.0.5}$$

The specific contact resistance R_c is defined as:

$$R_c \equiv \left(\frac{\partial J}{\partial V}\right)_{V=0}^{-1} = \frac{E_{00}}{q \cdot J_{so}} \tag{A.0.6}$$

$$R_c = \frac{E_{00}}{q \cdot C_1} \exp\left[\Phi_B \frac{2\pi}{qh}\sqrt{\frac{m^* \cdot \varepsilon_o \varepsilon_r}{N}}\right] \propto \exp\left[\Phi_B^{1/2} \cdot W_{barrier}\right] \tag{A.0.7}$$

A metal-semiconductor is utilized to electrically link the emitter, base, and collector semiconductor to their respective interconnects. The contact has associated with it a specific contact resistance due to an energy barrier Φ_b and depletion region at the junction interface. This barrier and depletion can be minimized through the combined use of a narrow bandgap semiconductor that is highly doped, proper surface preparation before metal deposition to reduce surface states, and choice of interfacial metal having an appropriate work function Φ_m.

References

[1] M. Jang and J. Lee, "Analysis of Schottky Barrier Height in Small Contacts Using a Thermionic-Field Emission Model", *Electronics and Telecommunications Research (ETRI) Journal*, vol. 24, no. 6, pp. 455-461, Dec. 2002

B

InP mesa HBT / Circuit Process Flow

THIS appendix describes the process flow for fabricating InP DHBTs and circuits.

- The process tolerances are sensitive to the quality of the photoresist
  - If uncertain of the age and/or quality of the PR, pour a new bottle
  - This is especially important for SPR-955, CEM, and nLOF 2020
- When spinning PR, use a slow acceration
  - i.e. It should take 2 $\rightarrow$ 2.5 seconds to reach maximum spin speed
- For the following steps, a focus array is required for accurate features:
  1. Emitter contact lithography
  2. Base contact lithography
  3. Base post lithography
  - Otherwise, the focus offset on subsequent steps is = 0
  - Always inspect the focus checkers thoroughly after development

1. **Wafer cleaving and preparation**
   - There are two type of wafers
     (a) European / Japan flat option wafer where the minor flat is to the left of the major flat
     (b) US flat option wafer where the minor flat is to the right of the major flat

- To ensure proper semiconductor mesa etch undercut, the long-axis of the emitter should be oriented...
  - Perpendicular to the major flat for European / Japan flat option wafers
  - Parallel to the major flat for US flat option wafers
- For the local-alignment DFAS (Dark-Field-Alignment-System) system to work on the i-line GCA stepper, the minimum size of the sample to be processed should be greater than 1 x 1 $inch^2$.

2. **Emitter contact lithography**

- Solvent clean – 3 min acetone, 3 min 2-propanol, 3 min DI water rinse
- Dehydration bake – 120°C, 10 min
- Cool wafer, 5 min
- Photoresist spin – SPR-955, 2.5 kRPM, 30 sec
- Pre-exposure PR bake – 92°C, 60 sec
- CEM coat and spin
  - Coat wafer w/ CEM and let sit for 60 sec
  - Then spin 4 kRPM, 30 sec
- Shoot 'emitter' pattern in stepper, 2.055 sec
- Post-exposure PR bake – 110°C, 60 sec
- Development
  (a) Rinse CEM from wafer surface using DI water, 30 sec
  (b) Immediately transfer wafer to MF-701 developer
    - Develope 2 min 20 sec
- Rinse wafer – DI water for 2 min, N_2 dry
- Inspect wafer using optical microscope

3. **Emitter contact deposition**

- Prepare ozone reactor – run empty, 20 min
- Surface preparation – oxidize wafer surface in ozone reactor, 10 min
- Vent E-beam 4, load private sources – Ti, Pd, and Au
- Surface preparation – HCl:H_2O 1:10 dip 10 sec, H_2O rinse 10 sec, N_2 dry

- Load sample in E-beam 4 – orient long-axis of emitter in the same direction as the sample rotation inside E-beam 4
- Allow system to pump-down for 90 min to $< 10^{-6}$ torr
- Deposit emitter contact
  - Ti 200 A (1 A/sec)
  - Pd 400 A (1 A/sec)
  - Au 7500 A
    - 1 A/sec for 1-300 A
    - 2 A/sec for 301-500 A
    - 3 A/sec for 501-1000 A
    - 4-5 A/sec 1001-7500 A
- Metal liftoff – 1165 stripper, 80°C, 2 hr
- Remove metal and place sample in fresh 1165 stripper, 80°C, 20 min
  - Gently agitate sample surface with small pipet
  - Rinse sample in 2-propanol before transferring to H_2O or Solvent clean
- Solvent clean – 3 min acetone, 3 min 2-propanol, 3 min DI water rinse
- Anneal emitter contact, 300°C, N_2 purge, 60 sec

4. **Emitter mesa etch**

- Prepare three beakers with...
  (a) NH_4OH:H_2O, 1:10
  (b) H_3PO_4:H_2O_2:H_2O, 1:1:25 – use stirrer at 200 RPM
  (c) H_3PO_4:HCl, 4:1 – use stirrer at 200 RPM
- Dip sample – NH_4OH:H_2O solution 10 sec, H_2O rinse 10 sec, N_2 dry
- Etch InGaAs emitter cap in H_3PO_4:H_2O_2:$H_2O \approx$ 21 sec
  - Overetch should only be 3 sec from the time the color change is complete
  - Inspect under microscope to ensure all InGaAs is etched
- Etch InP emitter in H_3PO_4:HCl $\approx$ 35 sec
  - Overetch should only be 5 sec from the time the color change is complete
  - Inspect under microscope to ensure all InP is etched

5. **Base contact lithography**

   - No solvent cleaned needed after emitter mesa etch
   - Dehydration bake – 120°C, 10 min
   - Photoresist spin – nLOF 2020, 4 kRPM, 30 sec
   - Pre-exposure PR bake – 111°C, 60 sec
   - Shoot 'base contact' pattern in stepper – 0.46 sec
   - Post-exposure PR bake – 114°C, 60 sec
   - Development – MF-701 developer, 2 min
   - Rinse wafer – DI water for 2 min, N_2 dry
   - Inspect wafer using optical microscope

6. **Base contact deposition**

   - Prepare ozone reactor – let run empty for 20 min
   - Surface preparation – oxidize wafer surface in ozone reactor, 10 min
   - Vent E-beam 4, load private sources – Ti, Pd, and Au
   - Surface preparation – NH_4OH:H_2O 1:10 dip 10 sec, N_2 dry, ***NO WATER RINSE***
   - Load sample in E-beam 4 – orient long-axis of emitter in the same direction as the sample rotation inside E-beam 4
   - Allow system to pump-down for 90 min to $< 10^{-6}$ torr
   - Deposit base contact
     - Pd 25 A, Ti 170 A, Pd 170 A, Au 650 A
       - 1 A/sec for all metal depositions
       - Higher deposition rates onto nLOF 2020 will leave more PR scum
   - Metal liftoff – 1165 stripper, 80°C, 1 hr
   - Remove metal and place sample in fresh AZ 300T stripper, 80°C, 10 min
     - Gently agitate sample surface with small pipet
     - Rinse sample in 2-propanol before transferring to H_2O or Solvent clean
     - The sample can proceed to 'base-post' lithography if there is no scum on post-end of the base contact

∗ Otherwise, repeat the AZ 300T step until that is the case

7. **Base post lithography**

   - Solvent clean – 3 min acetone, 3 min 2-propanol, 3 min DI water rinse
   - Dehydration bake – 120°C, 10 min
   - Cool wafer, 5 min
   - Photoresist spin – SPR-955, 2.5 kRPM, 30 sec
   - Pre-exposure PR bake – 92°C, 60 sec
   - CEM coat and spin
     - Coat wafer w/ CEM and let sit for 60 sec
     - Then spin 4 kRPM, 30 sec
   - Shoot 'base post' pattern in stepper, 2.055 sec
   - Post-exposure PR bake – 110°C, 60 sec
   - Development
     (a) Rinse CEM from wafer surface using DI water, 30 sec
     (b) Immediately transfer wafer to MF-701 developer, develope 2 min 20 sec
   - Rinse wafer – DI water for 2 min, N_2 dry
   - Inspect wafer using optical microscope

8. **Base post deposition**

   - Prepare ozone reactor – run empty, 20 min
   - Surface preparation – oxidize wafer surface in ozone reactor, 10 min
   - Vent E-beam 4, load private sources – Ti, Pd, and Au
   - Surface preparation – HCl:H_2O 1:10 dip 10 sec, H_2O rinse 10 sec, N_2 dry
   - Load sample in E-beam 4 – orient long-axis of emitter in the same direction as the sample rotation inside E-beam 4
   - Allow system to pump-down for 90 min to $< 10^{-6}$ torr
   - Deposit base post
     - Pd 25 A (1 A/sec)
     - Ti 170 A (1 A/sec)

  - Pd 170 A (1 A/sec)
  - Au 9300 A
    - 1 A/sec for 1-300 A
    - 2 A/sec for 301-500 A
    - 3 A/sec for 501-1000 A
    - 4-5 A/sec 1001-9300 A
- Metal liftoff – 1165 stripper, 80°C, 2 hr
- Remove metal and place sample in fresh 1165 stripper, 80°C, 20 min
  - Gently agitate sample surface with small pipet
  - Rinse sample in 2-propanol before transferring to H_2O or Solvent clean

9. **Base mesa lithography**

- Solvent clean – 3 min acetone, 3 min 2-propanol, 3 min DI water rinse
- Dehydration bake – 120°C, 10 min
- Cool wafer, 5 min
- Photoresist spin – SPR-510, 4 kRPM, 30 sec
- Pre-exposure PR bake – 90°C, 60 sec
- Shoot 'base mesa' pattern in stepper, 1.0 sec
- Post-exposure PR bake – 110°C, 60 sec
- Development – MF-701 developer, 90 sec
- Rinse wafer – DI water for 2 min, N_2 dry
- Inspect wafer using optical microscope

10. **Base mesa etch**

- Prepare three beakers with...
  (a) NH_4OH:H_2O, 1:10
  (b) H_3PO_4:H_2O_2:H_2O, 1:1:25 – use stirrer at 200 RPM
  (c) H_3PO_4:HCl, 4:1 – use stirrer at 200 RPM
- Dip sample – NH_4OH:H_2O solution 10 sec, H_2O rinse 10 sec, N_2 dry
- Etch InGaAs base, InGaAs collector setback, and ternary grade in H_3PO_4:H_2O_2:H_2O $\approx$ 35 sec

  - Overetch should only be 5 sec from the time the color change is complete
  - Inspect under microscope to ensure all InGaAs is etched
- Etch InP collector in H_3PO_4:HCl $\approx$ 35 sec
  - Overetch should only be 10 sec from the time the color change is complete
  - This extended overetch is for increased collector semiconductor undercut
  - Inspect under microscope to ensure all InP is etched
- Strip PR mask – 1165 stripper, 80°C, 20 min
  - Gently agitate sample surface with small pipet
  - Rinse sample in 2-propanol before transferring to H_2O or Solvent clean

11. **Device isolation lithography**

- Solvent clean – 3 min acetone, 3 min 2-propanol, 3 min DI water rinse
- Dehydration bake – 120°C, 10 min
- Cool wafer, 5 min
- Photoresist spin – SPR-510, 4 kRPM, 30 sec
- Pre-exposure PR bake – 90°C, 60 sec
- Shoot 'dev isolation' pattern in stepper, 1.0 sec
- Post-exposure PR bake – 110°C, 60 sec
- Development – MF-701 developer, 90 sec
- Rinse wafer – DI water for 2 min, N_2 dry
- Inspect wafer using optical microscope

12. **Device isolation etch**

- Prepare three beakers with...
  (a) NH_4OH:H_2O, 1:10
  (b) H_3PO_4:H_2O_2:H_2O, 1:1:25 – use stirrer at 200 RPM
  (c) H_3PO_4:HCl, 4:1 – use stirrer at 200 RPM
- Dip sample – NH_4OH:H_2O solution 10 sec, H_2O rinse 10 sec, N_2 dry
- Etch InGaAs sub-collector in H_3PO_4:H_2O_2:H_2O $\approx$ 15 sec

  - The color change is not visible to the 'naked eye'
    - The InGaAs layer is too thin
  - Inspect under microscope to ensure all InGaAs is etched
- Etch InP sub-collector and semi-insulating InP in H_3PO_4:HCl – 45 sec
  - There is no etch stop layer – etching of sub-collector continues into the semi-insulating InP (SI-InP)
  - For proper device isolation and dielectric planarization, only 100 nm of SI-InP should be etched
  - Dektak the etch depth and repeat InP etching in 7 sec increments as necessary
- Strip PR mask – 1165 stripper, 80°C, 20 min
  - Gently agitate sample surface with small pipet
  - Rinse sample in 2-propanol before transferring to H_2O or Solvent clean

13. **NiCr Resistor lithography**

- Solvent clean – 3 min acetone, 3 min 2-propanol, 3 min DI water rinse
- Dehydration bake – 120°C, 10 min
- Cool wafer, 5 min
- Photoresist spin – SPR-510, 4 kRPM, 30 sec
- Pre-exposure PR bake – 90°C, 60 sec
- CEM coat and spin
  - Coat wafer w/ CEM and let sit for 60 sec
  - Then spin 4 kRPM, 30 sec
- Shoot 'Resistor' pattern in stepper, 2.2 sec
- Post-exposure PR bake – 110°C, 60 sec
- Development
  (a) Rinse CEM from wafer surface using DI water, 30 sec
  (b) Immediately thereafter transfer wafer to MF-701 developer, develope 2 min 30 sec
- Rinse wafer – DI water for 2 min, N_2 dry
- Inspect wafer using optical microscope

14. **NiCr Resistor deposition**

- Prepare ozone reactor – run empty, 20 min
- Surface preparation – oxidize wafer surface in ozone reactor, 90 sec
- Vent E-beam 1, load private sources – Ti, SiO_2, NiCr
- Surface preparation – NH_4OH:H_2O 1:10 dip 10 sec, N_2 dry, ***NO WATER RINSE***
- Load sample in E-beam 1
- Allow system to pump-down for 60 min to $< 2{\cdot}10^{-6}$ torr
- Deposit NiCr resistors
  - Ti 50 A (1 A/sec)
  - SiO_2 200 A (1 A/sec)
  - NiCr xxx A (1 A/sec)
    - For NiCr, Cr out-diffuses more quickly than than Ni
    - Thus, the source resistivity goes down after each deposition
    - Refer to the NiCr worksheet for accurate determination of NiCr deposition thickness for 50 Ω/□
- Metal liftoff – 1165 stripper, 80°C, 2 hr
- Remove metal and place sample in fresh 1165 stripper, 80°C, 20 min
  - Gently agitate sample surface with small pipet
  - Rinse sample in 2-propanol before transferring to H_2O or Solvent clean

15. **Collector contact lithography**

- Solvent clean – 3 min acetone, 3 min 2-propanol, 3 min DI water rinse
- Dehydration bake – 120°C, 10 min
- Photoresist spin – nLOF 2020, 3.5 kRPM, 30 sec
- Pre-exposure PR bake – 111°C, 60 sec
- Shoot ‘collector contact’ pattern in stepper – 0.46 sec
- Post-exposure PR bake – 114°C, 60 sec
- Development – MF-701 developer, 2 min
- Rinse wafer – DI water for 2 min, N_2 dry
- Inspect wafer using optical microscope

16. **Collector contact deposition**

- Prepare ozone reactor – run empty, 20 min
- Surface preparation – oxidize wafer surface in ozone reactor, 90 sec
  - Do not run sample any longer in the ozone reactor
  - Longer ashing will remove PR from above the emitter contact *and* oxidize too much of the InGaAs sub-collector contact layer
- Vent E-beam 4, load private sources – Ti, Pd, and Au
- Surface preparation – NH_4OH:H_2O 1:10 dip 10 sec, N_2 dry, ***NO WATER RINSE***
- Load sample in E-beam 4 – orient long-axis of emitter in the same direction as the sample rotation inside E-beam 4
- Allow system to pump-down for 90 min to $< 10^{-6}$ torr
- Deposit collector contact
  - Ti 200 A (1 A/sec)
  - Pd 400 A (1 A/sec)
  - Au 4500 A
    - 1 A/sec for 1-300 A
    - 2 A/sec for 301-500 A
    - 3 A/sec for 501-1000 A
    - 4 A/sec 1001-4500 A
- Metal liftoff – 1165 stripper, 80°C, 2 hr
- Remove metal and place sample in fresh AZ 300T stripper, 80°C, 10 min
  - Gently agitate sample surface with small pipet
  - Rinse sample in 2-propanol before transferring to H_2O or Solvent clean

17. **Collector post lithography**

- Solvent clean – 3 min acetone, 3 min 2-propanol, 3 min DI water rinse
- Dehydration bake 120°C, 10 min
- Cool wafer, 5 min
- Photoresist spin – SPR-518, 3.0 kRPM, 30 sec
- Pre-exposure PR bake – 90°C, 60 sec

- CEM coat and spin – coat wafer w/ CEM and let sit for 60 sec, then spin 4 kRPM, 30 sec
- Shoot 'collector post' pattern in stepper, 2.6 sec
- Post-exposure PR bake – 110°C, 60 sec
- Development
  (a) Rinse CEM from wafer surface using DI water, 30 sec
  (b) Immediately transfer wafer to MF-701 developer, develope 2 min 30 sec
- Rinse wafer – DI water for 2 min, N_2 dry
- Inspect wafer using optical microscope

18. **Collector post deposition**

- Prepare ozone reactor – run empty, 20 min
- Surface preparation – oxidize wafer surface in ozone reactor, 5 min
- Vent E-beam 4, load private sources – Ti and Au
- Surface preparation – HCl:H_2O 1:10 dip 10 sec, H_2O rinse 10 sec, N_2 dry
- Load sample in E-beam 4 – orient long-axis of emitter perpendicular to the direction of sample rotation inside E-beam 4
- Allow system to pump-down for 90 min to $< 10^{-6}$ torr
- Deposit collector post
  - Ti 100 A (1 A/sec)
  - Au xxxx A (see list below for deposition rate)
    * The collector post needs to be level with the top of the emitter contact
    * Dektak to determine Au deposition thickness
    * 1 A/sec for 1-300 A
    * 2 A/sec for 301-500 A
    * 3 A/sec for 501-1000 A
    * 4-5 A/sec 1001-xxxx A
  - Ti 100 A (1 A/sec)
- Metal liftoff – 1165 stripper, 80°C, 2 hr
- Remove metal and place sample in fresh 1165 stripper, 80°C, 20 min

  - Gently agitate sample surface with small pipet
  - Rinse sample in 2-propanol before transferring to H_2O or Solvent clean

19. **Resistor post lithography**

  - Solvent clean – 3 min acetone, 3 min 2-propanol, 3 min DI water rinse
  - Dehydration bake 120°C, 10 min
  - Cool wafer, 5 min
  - Photoresist spin – SPR-518, 3.0 kRPM, 30 sec
  - Pre-exposure PR bake – 90°C, 60 sec
  - CEM coat and spin – coat wafer w/ CEM and let sit for 60 sec, then spin 4 kRPM, 30 sec
  - Shoot 'resistor post' pattern in stepper, 2.6 sec
  - Post-exposure PR bake – 110°C, 60 sec
  - Development
    (a) Rinse CEM from wafer surface using DI water, 30 sec
    (b) Immediately transfer wafer to MF-701 developer, develope 2 min 30 sec
  - Rinse wafer – DI water for 2 min, N_2 dry
  - Inspect wafer using optical microscope

20. **Resistor post deposition**

  - Prepare ozone reactor – run empty, 20 min
  - Surface preparation – oxidize wafer surface in ozone reactor, 5 min
  - Vent E-beam 4, load private sources – Ti and Au
  - Surface preparation – HCl:H_2O 1:10 dip 10 sec, H_2O rinse 10 sec, N_2 dry
  - Load sample in E-beam 4 – orient long-axis of emitter perpendicular to the direction of sample rotation inside E-beam 4
  - Allow system to pump-down for 90 min to $< 10^{-6}$ torr
  - Deposit resistor post contact
    - Ti 100 A (1 A/sec)
    - Au xxxx A (see list below for deposition rate)

        - The resistor post needs to level with the top of the emitter contact
        - Dektak to determine Au deposition thickness
        - 1 A/sec for 1-300 A
        - 2 A/sec for 301-500 A
        - 3 A/sec for 501-1000 A
        - 4-5 A/sec 1001-xxxx A
      - Ti 100 A (1 A/sec)
  - Metal liftoff – 1165 stripper, 80°C, 2 hr
  - Remove metal and place sample in fresh 1165 stripper, 80°C, 20 min
      - Gently agitate sample surface with small pipet
      - Rinse sample in 2-propanol before transferring to H_2O or Solvent clean

21. **BCB passivation**

  - The 'Blue Oven' must be at room temperature 25°C or less before beginning
      - Otherwise, BCB will bubble during the cure and the sample will be ruined
  - NOTE: there must not be any stops in the steps from sample surface preparation to loading the spun sample w/ BCB into the Blue oven
      - Any delays will allow increased surface oxide to regenerate on the semiconductor, increasing leakage currents
      - Oxygen contaminates BCB and prolonged exposure will compromise the cure and ruin the sample
  - Prepare the 'Blue Oven' – run N_2 through chamber at 100%
  - Prepare ozone reactor – run empty, 20 min
  - Solvent clean – 3 min acetone, 3 min 2-propanol, 3 min DI water rinse
  - Dehydration bake – 120°C, 10 min
  - Cool wafer, 5 min
  - Surface preparation – oxidize wafer surface in ozone reactor, 10 min
  - Surface preparation – NH_4OH:H_2O 1:10 dip 10 sec, N_2 dry, ***NO WATER RINSE***
  - Coat wafer with BCB 3022-35 – let sit on surface for 30 sec

- Spin BCB 1.5 kRPM, 30 sec – BCB thickness $\approx 1.88\ \mu$m
- Place sample into Al cup holder
  - The holder should be deformed such that the sample is completely level, yet has minimal contact with the bottom holder surface
  - Otherwise, cured BCB that has crept onto the bottom surface may prevent the sample from being removed from the holder
- Place sample (in holder) into the 'Blue Oven'
- Reduce N_2 flow to 60% after 3 min
- Load and run Program 5 (confirm in case it has been altered)
- Program sequence:
  (a) 5 min ramp to 50°C, 5 min soak
  (b) 15 min ramp to 100°C, 15 min soak
  (c) 15 min ramp to 150°C, 15 min soak
  (d) 60 min ramp to 250°C, 60 min soak
  (e) Natural cool down
  (f) Oven off
- Remove sample and inspect under the microscope
- Turn off the 'Blue Oven'

22. **Wafer planarization and interconnect surface preparation**

- Clean carrier wafer in Panasonic ICP – CF_4/O_2 50:200 sccm, 7 min
  (a) Load sample on carrier wafer, BCB ICP etch CF_4/O_2 50:200 sccm, 2 min
  (b) Inspect sample in FEI SEM to see if the device contacts and interconnect posts are exposed
- Repeat the above etch (1 min increments) and inspection until all contact and posts are exposed
  - Be sure to run the wafer clean program in between each etch cycle
- Repeat the BCB passivation step for further sample planarization
- Clean carrier wafer in Panasonic ICP – CF_4/O_2 50:200 sccm, 7 min
  (a) Load sample on carrier wafer, BCB ICP etch CF_4/O_2 50:200 sccm, 3 min 30 sec
  (b) Inspect sample in FEI SEM to see if the device contacts and interconnect post are exposed

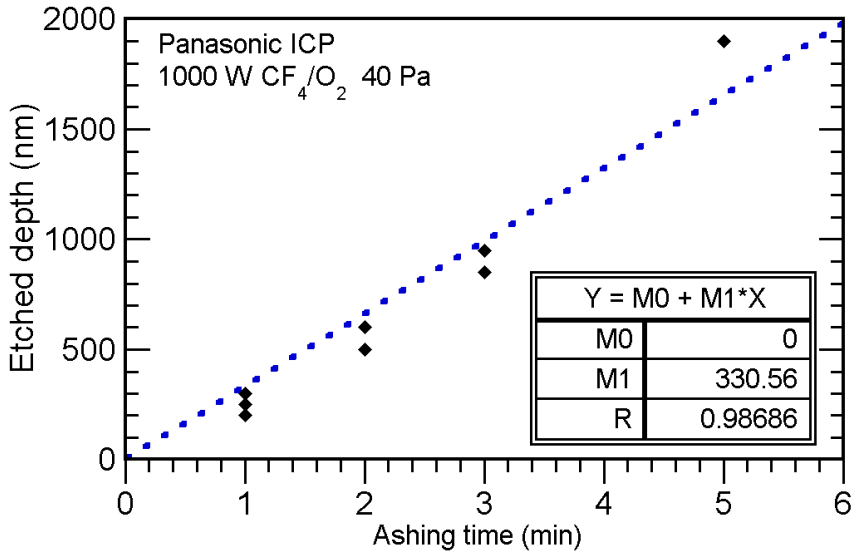

Figure B.1: BCB etch rate for the given $CF_4/0_2$ recipe

- Repeat the above etch (1 min increments) and inspection until all contact and posts are exposed
  - Be sure to run the wafer clean program in between each etch cycle
- Solvent clean – 3 min acetone, 3 min 2-propanol, 3 min DI water rinse
- Dehydration bake 120°C, 10 min
- Cool wafer, 5 min
- Prepare ozone reactor – run empty, 20 min
- Surface preparation – oxidize wafer surface in ozone reactor, 10 min
- Surface preparation – NH_4OH:H_2O 1:10 dip 10 sec, N_2 dry, ***NO WATER RINSE***
- Deposit 100 nm SiN_x on the BCB surface by PECVD
- Photoresist spin – SPR-510, 4 kRPM, 30 sec
- Pre-exposure PR bake – 90°C, 60 sec
- Shoot 'contact via' pattern in stepper, 2.0 sec
- Post-exposure PR bake – 110°C, 60 sec
- Development – MF-701 developer, 90 sec

- Rinse wafer – DI water for 2 min, N_2 dry
- Inspect wafer using optical microscope
- Clean carrier wafer in Panasonic ICP – CF_4/O_2 50:200 sccm, 7 min
- Load sample on carrier wafer for ICP etching
  (a) SiN_x ICP etch CF_4 125 sccm, 90 sec
  (b) Short BCB ashing CF_4/O_2 50:200 sccm, 10 sec
- Inspect sample in FEI SEM to see if the device contacts and interconnect posts are exposed
- Strip photoresist mask
  (a) Flood expose sample, 15 sec
  (b) Develope exposed PR – MF-701, 2 min
  (c) Strip remaining PR in acetone – 3 min
  (d) Inspect – if PR remaining, use 1165 stripper, 80°C, 3 min
  (e) Gently agitate sample surface with small pipet
- Rinse sample in 2-propanol before transferring to H_2O or Solvent clean

23. **Metal-1 interconnect lithography**

- Solvent clean – 3 min acetone, 3 min 2-propanol, 3 min DI water rinse
- Dehydration bake – 120°C, 10 min
- Photoresist spin – nLOF 2020, 4 kRPM, 30 sec
- Pre-exposure PR bake – 111°C, 60 sec
- Shoot ‘Metal 1’ pattern in stepper – 0.46 sec
- Post-exposure PR bake – 114°C, 60 sec
- Development – MF-701 developer, 2 min
- Rinse wafer – DI water for 2 min, N_2 dry
- Inspect wafer using optical microscope

24. **Metal-1 interconnect deposition**

- Prepare ozone reactor – run empty, 20 min
- Surface preparation – clean wafer surface in ozone reactor, 5 min
- Vent E-beam 4, load private sources – Ti and Au

- Surface preparation – NH_4OH:H_2O 1:10 dip 10 sec, N_2 dry, ***NO WATER RINSE***
- Load sample in E-beam 4 – orient long-axis of emitter perpendicular to the direction of sample rotation inside E-beam 4
- Allow system to pump-down for 90 min to $< 10^{-6}$ torr
- Deposit Metal-1 interconnect
  - Ti 100 A (1 A/sec)
  - Au 10 kA
    - 2 A/sec for 1-300 A
    - 3 A/sec for 301-500 A
    - 4 A/sec for 501-1000 A
    - 5-6 A/sec 1001-10000 A
  - Ti 100 A (1 A/sec)
- Metal liftoff – AZ 300T stripper, 80°C, 20 min
- Remove metal and place sample in fresh AZ 300T stripper, 80°C, 20 min
  - Gently agitate sample surface with small pipet
  - Rinse sample in 2-propanol before transferring to H_2O or Solvent clean

25. **Measure devices and TLMs**

- If device performance and TLMs are well behaved, continue

26. **SiN MIM capacitor formation**

- Solvent clean – 3 min acetone, 3 min 2-propanol, 3 min DI water rinse
- Dehydration bake 120°C, 10 min
- Cool wafer, 5 min
- Prepare ozone reactor – run empty, 20 min
- Surface preparation – oxidize wafer surface in ozone reactor, 10 min
- Surface preparation – NH_4OH:H_2O 1:10 dip 10 sec, N_2 dry, ***NO WATER RINSE***
- Deposit 400 nm SiN_x onto the sample by PECVD
- Photoresist spin – SPR-510, 4 kRPM, 30 sec
- Pre-exposure PR bake – 90°C, 60 sec

- Shoot 'SiN cap' pattern in stepper, 2.0 sec
- Post-exposure PR bake – 110°C, 60 sec
- Development – MF-701 developer, 90 sec
- Rinse wafer – DI water for 2 min, N_2 dry
- Inspect wafer using optical microscope
- Clean carrier wafer in Panasonic ICP – CF_4/O_2 200:40 sccm, 7 min
- Load sample on carrier wafer for ICP etching
  (a) SiN_x ICP etch CF_4 125 sccm, 3 min
  (b) Short ashing CF_4/O_2 50:200 sccm, 15 sec
- Strip photoresist mask
  (a) Flood expose sample, 15 sec
  (b) Develope exposed PR – MF-701, 2 min
  (c) Strip remaining PR in acetone – 3 min
  (d) Inspect – if PR remaining, use 1165 stripper, 80°C, 3 min
  (e) Gently agitate sample surface with small pipet
- Rinse sample in 2-propanol before transferring to H_2O or Solvent clean

27. **Metal-2 interconnect lithography**

- Solvent clean – 3 min acetone, 3 min 2-propanol, 3 min DI water rinse
- Dehydration bake – 120°C, 10 min
- Photoresist spin – nLOF 2020, 3 kRPM, 30 sec
- Pre-exposure PR bake – 111°C, 60 sec
- Shoot 'Metal 2' pattern in stepper – 0.46 sec
- Post-exposure PR bake – 114°C, 60 sec
- Development – MF-701 developer, 2 min
- Rinse wafer – DI water for 2 min, N_2 dry
- Inspect wafer using optical microscope

28. **Metal-2 interconnect deposition**

- Prepare ozone reactor – run empty, 20 min
- Surface preparation – clean wafer surface in ozone reactor, 5 min
- Vent E-beam 4, load private sources – Ti and Au

- Surface preparation – NH_4OH:H_2O 1:10 dip 10 sec, N_2 dry, ***NO WATER RINSE***
- Load sample in E-beam 4 – orient long-axis of emitter perpendicular to the direction of sample rotation inside E-beam 4
- Allow system to pump-down for 90 min to $< 10^{-6}$ torr
- Deposit Metal-2 interconnect
  - Ti 100 A (1 A/sec)
  - Au 10 kA
    - 2 A/sec for 1-300 A
    - 3 A/sec for 301-500 A
    - 4 A/sec for 501-1000 A
    - 5-6 A/sec 1001-10000 A
  - Ti 100 A (1 A/sec)
- Metal liftoff – 1165 stripper, 80°C, 2 hr
- Remove metal and place sample in fresh 1165 stripper, 80°C, 20 min
  - Gently agitate sample surface with small pipet
  - Rinse sample in 2-propanol before transferring to H_2O or Solvent clean

29. **Metal-2 to Metal-3 interconnect post lithography – 1**

- Solvent clean – 3 min acetone, 3 min 2-propanol, 3 min DI water rinse
- Dehydration bake – 120°C, 10 min
- Photoresist spin – SPR 518, 3 kRPM, 30 sec
- Pre-exposure PR bake – 90°C, 60 sec
- CEM coat and spin
  - Coat wafer w/ CEM and let sit for 60 sec
  - Then spin 4 kRPM, 30 sec
- Shoot ‘M2 - M3 post’ pattern in stepper – 2.8 sec
- Post-exposure PR bake – 110°C, 60 sec
- Development – MF-701 developer, 2 min 30 sec
- Rinse wafer – DI water for 2 min, N_2 dry
- Inspect wafer using optical microscope

30. **Metal-2 to Metal-3 interconnect post deposition – 1**

- Prepare ozone reactor – run empty, 20 min
- Surface preparation – clean wafer surface in ozone reactor, 5 min
- Vent E-beam 4, load private sources – Ti and Au
- Surface preparation – NH_4OH:H_2O 1:10 dip 10 sec, N_2 dry, ***NO WATER RINSE***
- Load sample in E-beam 4 – orient long-axis of emitter perpendicular to the direction of sample rotation inside E-beam 4
- Allow system to pump-down for 90 min to $< 10^{-6}$ torr
- Deposit M2-M3 post contact
  - Ti 100 A (1 A/sec)
  - Au 13 kA
    - 2 A/sec for 1-300 A
    - 3 A/sec for 301-500 A
    - 4 A/sec for 501-1000 A
    - 5-6 A/sec 1001-13000 A
  - Ti 100 A (1 A/sec)
- Metal liftoff – 1165 stripper, 80°C, 30 min
- Remove metal and place sample in fresh 1165 stripper, 80°C, 10 min
  - Gently agitate sample surface with small pipet
  - Rinse sample in 2-propanol before transferring to H_2O or Solvent clean

31. **Thin-film BCB microstrip wiring envirnment – layer 1**

- The 'Blue Oven' must be at room temperature 25°C or less before beginning
  - Otherwise, BCB will bubble during the cure and the sample will be ruined
- NOTE: there must not be any stops in the steps from sample surface preparation to loading the spun sample w/ BCB into the Blue oven
  - Any delays will allow increased surface oxide to regenerate on the surface, increasing leakage currents
  - Oxygen contaminates BCB and prolonged exposure will compromise the cure and ruin the sample

- Prepare the 'Blue Oven' – run N_2 through chamber at 100%
- Prepare ozone reactor – run empty, 20 min
- Solvent clean – 3 min acetone, 3 min 2-propanol, 3 min DI water rinse
- Dehydration bake – 120°C, 10 min
- Cool wafer, 5 min
- Surface preparation – clean wafer surface in ozone reactor, 10 min
- Surface preparation – NH_4OH:H_2O 1:10 dip 10 sec, N_2 dry, ***NO WATER RINSE***
- Coat wafer with BCB 3022-35 – let sit on surface for 30 sec
- Spin BCB 1.5 kRPM, 30 sec – BCB thickness $\approx$ 1.88 μm
- Place sample into Al cup holder
  - The holder should be deformed such that the sample is completely level, yet has minimal contact with the bottom holder surface
  - Otherwise, cured BCB that has crept onto the bottom surface may prevent the sample from being removed from the holder
- Place sample (in holder) into the 'Blue Oven'
- Reduce N_2 flow to 60% after 3 min
- Load and run Program 5 (see passivation step)
- Remove sample and inspect under the microscope
- Turn off the 'Blue Oven'
- Clean carrier wafer in Panasonic ICP – CF_4/O_2 50:200 sccm, 7 min
  (a) Load sample on carrier wafer, BCB ICP etch CF_4/O_2 50:200 sccm, 90 sec
  (b) Inspect sample in FEI SEM to see if the interconnect posts are exposed
- Repeat the above etch (45 sec increments) and inspection until all contact and posts are exposed
  - Be sure to run the wafer clean program in between each etch cycle

32. **Metal-2 to Metal-3 interconnect post lithography – 2**

- Repeat this step

33. **Metal-2 to Metal-3 interconnect post deposition – 2**

- Repeat this step

34. **Thin-film BCB microstrip wiring envirnment – layer 2**

    - Repeat this step

35. **Metal-3 adhession layer**

    - Solvent clean – 3 min acetone, 3 min 2-propanol, 3 min DI water rinse
    - Dehydration bake 120°C, 10 min
    - Cool wafer, 5 min
    - Prepare ozone reactor – run empty, 20 min
    - Surface preparation – clean wafer surface in ozone reactor, 10 min
    - Surface preparation – NH_4OH:H_2O 1:10 dip 10 sec, N_2 dry, ***NO WATER RINSE***
    - Deposit 100 nm SiN_x on the BCB surface by PECVD
    - Photoresist spin – SPR-510, 4 kRPM, 30 sec
    - Pre-exposure PR bake – 90°C, 60 sec
    - Shoot 'Metal-3 via' pattern in stepper, 2.0 sec
    - Post-exposure PR bake – 110°C, 60 sec
    - Development – MF-701 developer, 90 sec
    - Rinse wafer – DI water for 2 min, N_2 dry
    - Inspect wafer using optical microscope
    - Clean carrier wafer in Panasonic ICP – CF_4/O_2 50:200 sccm, 7 min
    - Load sample on carrier wafer for ICP etching
        (a) SiN_x ICP etch CF_4 125 sccm, 90 sec
        (b) Short BCB ashing CF_4/O_2 50:200 sccm, 10 sec
    - Inspect sample in FEI SEM to see if the interconnect posts are exposed
    - Strip photoresist mask
        (a) Flood expose sample, 15 sec
        (b) Develope exposed PR – MF-701, 2 min
        (c) Strip remaining PR in acetone – 3 min
        (d) Inspect – if PR remaining, use 1165 stripper, 80°C, 3 min
        (e) Gently agitate sample surface with small pipet

- Rinse sample in 2-propanol before transferring to H_2O or Solvent clean

36. **Metal-3 interconnect and ground plane lithography**

    - Solvent clean – 3 min acetone, 3 min 2-propanol, 3 min DI water rinse
    - Dehydration bake – 120°C, 10 min
    - Photoresist spin – nLOF 2020, 3 kRPM, 30 sec
    - Pre-exposure PR bake – 111°C, 60 sec
    - Shoot 'Metal 3' pattern in stepper – 0.47 sec
    - Post-exposure PR bake – 114°C, 60 sec
    - Development – MF-701 developer, 2 min
    - Rinse wafer – DI water for 2 min, N_2 dry
    - Inspect wafer using optical microscope

37. **Metal-3 interconnect and ground plane deposition**

    - Prepare ozone reactor – run empty, 20 min
    - Surface preparation – clean wafer surface in ozone reactor, 5 min
    - Vent E-beam 4, load private sources – Ti and Au
    - Surface preparation – NH_4OH:H_2O 1:10 dip 10 sec, N_2 dry, ***NO WATER RINSE***
    - Load sample in E-beam 4 – orient long-axis of emitter perpendicular to the direction of sample rotation inside E-beam 4
    - Allow system to pump-down for 90 min to $< 10^{-6}$ torr
    - Deposit Metal-3 (ground plane)
        - Ti 100 A (1 A/sec)
        - Au 15 kA
            - 2 A/sec for 1-300 A
            - 3 A/sec for 301-500 A
            - 4 A/sec for 501-1000 A
            - 5-6 A/sec 1001-15000 A
        - Ti 100 A (1 A/sec)
    - Metal liftoff – 1165 stripper, 80°C, 2 hr
    - Remove metal and place sample in fresh 1165 stripper, 80°C, 20 min
        - Gently agitate sample surface with small pipet
        - Rinse sample in 2-propanol before transferring to H_2O or Solvent clean