中文题名：高灵敏度硅基光电探测器的研究

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摘 要

本论文主要研究光电探测器的灵敏度，由灵敏度的定义和计算公式得到提高灵敏度的三个主要方法是：提高光响应，放大光电流以及降低暗电流。针对三种不同结构不同材料和不同应用领域的硅基光电探测器，分析它们的应用需求和结构特点，结合它们现今的发展现状，指出这三种器件要获得高灵敏度的器件性能需要解决的问题分别是：微波光学应用的高饱和 Ge/Si UTC 结构器件要解决响应度过低的问题，光通信应用的波导 Ge/Si SAM 结构雪崩器件要解决波导耦合效率和倍增效率之间的矛盾，可见光探测的 Si-PIN 结构探测器则要解决暗电流过高的问题。

1. 分析硅基锗单行载流子探测器的结构优化和设计，获得高频率响应和高光吸收性能的器件性能，通过高低温两步法生长 Si 基 Ge 薄膜，微纳加工制备双台面结构，测试分析器件的暗电流、光响应、频率响应以及饱和度特性，研制出高响应的 Ge/Si 垂直入射型 UTC 器件，在 1550nm 入射下光响应 R 为 0.18A/W，量子效率为 14.4%。在-1V 偏压下的暗电流密度最小为 61.9 mA/cm^2，3-dB 带宽最大为 9.73GHz @直径 15μm；直径 40μm 器件，带宽 2.55GHz，在 1GHz 的调制频率下，饱和输出射频为 4.6 dBmW，对应的饱和电流为 16.24mA；直径 18μm 器件，带宽 7.23GHz，在 3GHz 的调制频率下，饱和输出射频为 3.7 dBmW，对应的饱和电流为 16.22mA。

2. 分析现今波导 Si/Ge APD 的结构和优劣，设计新型的纳米结构：将倍增层横向放置到 Si 波导层，获得高耦合效率和高倍增因子。设计分析光纤与芯片上的单模波导的耦合结构，单模波导结构，波导与吸收层耦合结构以及 APD 器件的吸收层结构，获得最大耦合和吸收效率的器件光学结构，Ge 材料的长度达到 10μm，厚度为>0.4μm，倏逝波耦合效率达到 93%以上。并通过优化欧姆接触层，电荷层，倍增层的结构，使器件获得大倍增系数（>10^3）和低的过剩噪声。设计器件的制备流程对 SiO_2 掩膜层刻蚀的时间和条件进行了实验，得到刻蚀槽的宽度低于 0.9μm 以后，刻蚀速率随着刻蚀空线宽的减小而降低，器件外延层宽度为 0.5μm，刻蚀速率为~100 nm/min。

3. 分析限制 Si-PIN 探测灵敏度的关键因素暗电流的主要组成，分析保护环的设计，光敏面的离子注入能量对器件暗电流和响应度的影响。通过分析不同器件尺寸，不同的工作温度，以及工作偏压跟暗电流的关系，得到工作温度<50K，缺陷态辅助隧穿是器件暗电流的主要来源；工作温度>150K，产生-复合机制产生的暗电流占主导。通过正向偏置的偏压、温度以及暗电流的关系推测，器件的缺陷辅助电流是正向工作时的主要暗电流来源。

关键词： Si 基 Ge 薄膜，光电探测器，红外光互联，波导探测器

Abstract

This manuscript makes researches on the sensitivity of the photodetector. According to the definition and calculation formula of the sensitivity, there are three main methods to improve the sensitivity: the response of the light, amplified photocurrent and lower dark current. For three different silicon-based optoelectronic detectors with different materials, structures and applications, their application requirements and structural features were analyzed. According to their present development, three components problems need to be solved to increase the sensitivity of the device performance. High saturation Ge/Si UTC structure device in microwave optics application needs to solve the low responivitye problem, waveguide Ge/Si SAM avalanche device in the optical communication application needs to solve the contradiction between the waveguide coupling efficiency and multiplication, and Si - PIN detector in visible light detection needs to solve the too high dark current problem.

1. The structure of silicon germanium uni-traveling-carrier detector was optimized and designed for high frequency response and high absorption performance. After the two-step growth methord of Ge film on silicon, and micro-nano processing and preparation of double mesa structure, the measurements and analysis of dark current, light responsivity, frequency response and saturation were carried on. The optimized vertical incidence Ge/Si UTC device with high response has responsivity (R) of 0.18 A/W under the 1550 nm incident light, quantum efficiency of 14.4%. The minimum dark current density is 61.9 mA/cm^2 at -1V. The maximum 3 dB bandwidth is 9.73 GHz with a 15 μm-diameter. For the 40 μm-diameter devices, the bandwidth is 2.55 GHz, and the saturated RF output is 4.6 dBmW, corresponding to the saturation current of 16.24 mA, under a 1 GHz frequency modulation. For the 18 μm-diameter devices, the bandwidth is 7.23 GHz, and saturated RF output is 3.7 dBmW, corresponding to the saturation current of 16.22 mA, under the modulation frequency of 3 GHz.

2. Based on the analyzing of the structure, advantages and disadvantages of present Si/Ge APD waveguide, a new types of nanostructures was designed: multiplication layer was horizontally placed in Si waveguide, and the new device obtain high coupling efficiency and multiplication factor. The coupling structure between optical fiber and single mode waveguide on a chip, single mode waveguide structure, the coupling structure between waveguide and absorption layer and absorbing layer structure of APD device were analyzed and designed to maximize the coupling and the absorption efficiency of the device. It turns out that the length of

the Ge materials up to 10 μm and thickness > 0.4 μm, evanescent wave coupling efficiency is 93% or more. And by optimizing the ohmic contact layer, charge layer, multiplication layer, the device got a large multiplication factor (> 10^3) and low excess noise. The SiO_2 layer as Ge selective epitaxial mask was text for the etching speed on the preparation process and conditions. When etching groove width is less than 0.9 μm, etching rate would decrease with the width of the etching empty line. Our device epitaxial layer is 0.5 microns wide, and the etching rate is ~ 100 nm/min.

3. The key limitation of Si - PIN detection sensitivity is the dark current. The main composition of dark current was analyzed. The design of the protection ring and the ion implantation energy on the photosensitive surface has great influence on the dark current and responsivity of the device. Based on the analysis the dark current with different device size, different working temperature, different operation bias, the main sources of dark current were figured out. When working temperature is < 50 K, the defect assisted tunneling is the main source of dark current. The generation-recombination current is dominanted with a working temperature > 150K. At the forward biased bias, the relationship between temperature and dark current was speculated, and defect assisted current is a key source of dark current.

KEY WORDS: Si-based Ge film, photodetectors, IR optical communication, waveguide detectors.

目 录

第一章 绪论

半导体光电探测器是能够接收从红外到紫外各个波段光信号，并将它转化为电信号输出的一种半导体光电器件。根据接收的光波段不同，光电探测器在军事、国民经济中的各个领域都有着重要的作用，如可见光或近红外波段的光接收主要用于射线测量和探测、工业自动控制、光度计量、光互连，光纤通讯，微波光子系统，天线，红外遥控，环境光强度检测，激光功率检测，测距，矿藏勘探，工业自动控制等；在红外波段主要用于导弹制导、红外热成像、红外遥感等方面。此外，半导体光电探测器与闪烁体集成模块还是核辐射检测，CT 扫描，安检等系统的核心关键部件。

灵敏度是衡量光电探测综合性能的一个重要参数，它跟暗电流、噪声、响应度和带宽几个探测器性能的关键参数都有关系，表征光电探测器可检测到的最小光信号。灵敏度越高，说明探测器能检测的光信号越弱，说明光度计量范围能更广，遥控距离能更远，对环境光变化能更灵敏，可探测的距离更远，红外成像质量更精细，可以说，灵敏度是光电探测器在实际应用中最核心性能指标。

1.1 光电探测的灵敏度

光电探测器的灵敏度定义：在一定的传输带宽和传输速度下，探测器能够接收并区分的光的最小信号能量（S_{min}）。它是光电探测器光电转换特性、光电转换光谱以及频率的度量，常用单位为 dBmW。一个器件的灵敏度可表示为：

$$S_{\min} = (S/N)_{\min} k_0 T_0 B(NF) \tag{1-1}$$

一个探测系统的最小操作灵敏度（minimum operational sensitivity, MOS）可表示为：

$$MOS = (S/N)_{\min} k_0 T_0 B(NF)/G \tag{1-2}$$

其中，$(S/N)_{\min}$ 为可探测信号的最小的信噪比；NF 为噪声因子或指数；k_0 为 Boltzmann's 常数，单位：*J/K*；T_0 探测器的工作温度，单位：K；*B* 为探测器的带宽，单位：Hz；*G* 为探测系统的增益。

由上面的公式可知，若获得较高的灵敏度，器件可探测的最小信号功率要尽可能小，要求器件的最小信噪比，噪声因子，带宽以及温度都要降低，或者增大系统增益。

因此，提高探测器的灵敏度的方法主要是三种： 1、提高光响应；2、利用雪崩倍增效应将信号放大；3、降低噪声和暗电流。

1.1.1 光响应

衡量一个半导体光电探测器的光响应能力的参数有两个：量子效率（η）和响应度（R）。他们之间可以通过一个常数（$h\nu/e$）进行相互转换。

1. **量子效率**

光子能量大于禁带宽度的光照射到雪崩光电二极管上时将被半导体吸收，每一个被吸收的光子产生一个电子-空穴对。在耗尽区内光激发产生的载流子被电场分开并被收集，从而在外电路负载中产生电流。用量子效率来表征半导体内部一个入射光子产生电子-空穴对的概率，其定义为[1]：

$$\eta=\frac{\text{所产生的电子-空穴对数}}{\text{入射的光子数}}=\frac{I_P/e}{P_0/h\nu}=\frac{I_P h\nu}{eP_0} \tag{1-3}$$

式中，I_P 为光电流，P_0 为入射光在半导体表面处的光功率，$h\nu$ 为入射光子的能量。若所有的光子都在耗尽区内被吸收，且所有光激发的载流子都被吸收，则量子效率等于 1。对一个实际的光电二极管来说，入射光功率 P_0 中的一部分光 $R_f P_0$ 在空气与光电二极管的界面上被反射而消耗掉。同时，在耗尽区内被吸收的光子数与耗尽区的宽度以及随波长变化的光吸收系数 $\alpha_0(\lambda)$ 有关。因此，假如忽略光在表面 P 区的吸收，则量子效率 η 为：

$$\eta=(1-R_f)(1-e^{-\alpha_0 W}) \tag{1-4}$$

可见，为了提高 η，耗尽区必须足够宽以保证 $\alpha_0 \mathrm{W}>>1$。此外，为了获得高的量子效率，尽可能减小入射光子在半导体表面的反射（R_f）是很重要的。在半导体表面涂覆上一层合适的抗反射膜，可以大大增加空气与半导体界面的透过率。

2. **响应度**

实际的 PIN 结构光电二极管中，常用响应度 R 来表征单位入射光功率所产生的光电流，它等于入射光所产生的光电流除以入射光的光功率：

$$R=I_P/P_0=e\eta/h\nu=e\eta\lambda/hc \tag{1-5}$$

其中 h 为普朗克常数，ν 是光子频率。当波长 λ 以微米为单位时，$h\nu=1.24/\lambda(\mathrm{eV})$。因此，响应度的一个方便的表达式是：

$$R=\eta\frac{\lambda}{1.24} \tag{1-6}$$

量子效率和响应度 R 是衡量光电转化效率重要的参数，当入射光信号恒定时，量子效率越高，器件的响应度越高，获得的电信号强度越大，器件的灵敏度就越高。

1.1.2 光电流倍增

光信号电流的倍增是提高器件灵敏的又一方法，最常用的是利用雪崩倍增效应将光电流放大：当光电探测器的工作偏压增大到一定值是，会使器件内部的某一区域的电场高于雪崩阈值电场，载流子在此区域发生雪崩碰撞电离，光生载流子的数目在器件内部成倍的增加，入射的信号被放大，信噪比增加，有利于获得高的灵敏度特性。

1. **雪崩倍增效应**

雪崩倍增效应，是半导体材料最重要的可逆击穿机制，是三种基本击穿机制之一。当 pn 结两端的反向偏压很大时，势垒区中的电场很强，势垒区内的载流子由于受到强电场的漂移作用，具有很大的动能，部分载流子可以获得足够高的能量，这些载流子有可能通过碰撞把能量传递给价带上的电子，使之发生电离，从而产生电子-空穴对,这种过程称为碰撞电离。因此高能载流子的能量要大于半导体的禁带宽度，才有可能将价带电子激发到导带。而碰撞电离出的自由电子-空穴对，在电场的作用下分别向相反方向运动，并被电场加速，再次碰撞产生新的电子空穴对。依此方式可以使载流子大量增殖。如图 2-4 所示，这种现象称为雪崩倍增效应。早在 1964 年，K.M.Johnson 便设想出了光电二极管的雪崩击穿工作模式，用来探测弱光信号，提高探测灵敏度[2]。

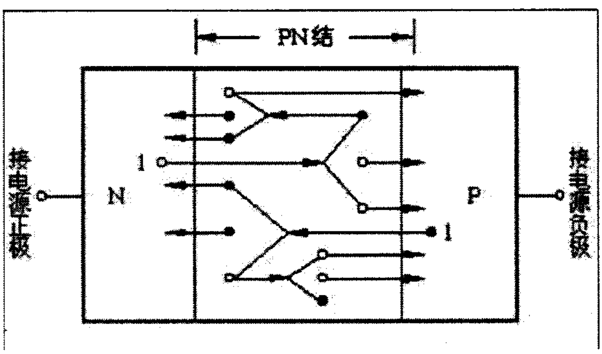

图 1-1 PN 结的雪崩倍增示意图

雪崩倍增效应 (avalanche multiplication effect in semiconductors)在半导体内部发生光生载流子的倍增，从而增大器件的内量子效率，提高响应度。对于雪崩光电二极管而言，由于雪崩倍增效应的作用，获得了 M 倍的放大，因此雪崩光电二极管的响应度为：

$$R_{APD} = M \cdot \frac{e\eta}{h\nu} = MR \tag{1-7}$$

2. **过剩噪声**

半导体内部的雪崩倍增现象是一个涉及载流子反馈（feedback）的复杂过程，其强弱由半导体的电离系数比决定，当电子和空穴的碰撞电离系数相近时，反馈效果明显。图 2-6 为相同的倍增系数下不同电离系数比（电子和空穴的碰撞电离系数之比值）的半导体的电离情况，(a) 电离系数比<<1；(b) k~1。可看到当 k~1 时，光子散射和局域电场等因素的影响，载流子反馈路径不能被预测，造成器件的倍增因子 M 是一个统计平均值，电离系数比越大，或者 k 值越接近 1，器件的倍增系数浮动越大，这部分浮动被称为雪崩器件的过剩噪声，会极大的限制器件灵敏度的提高。

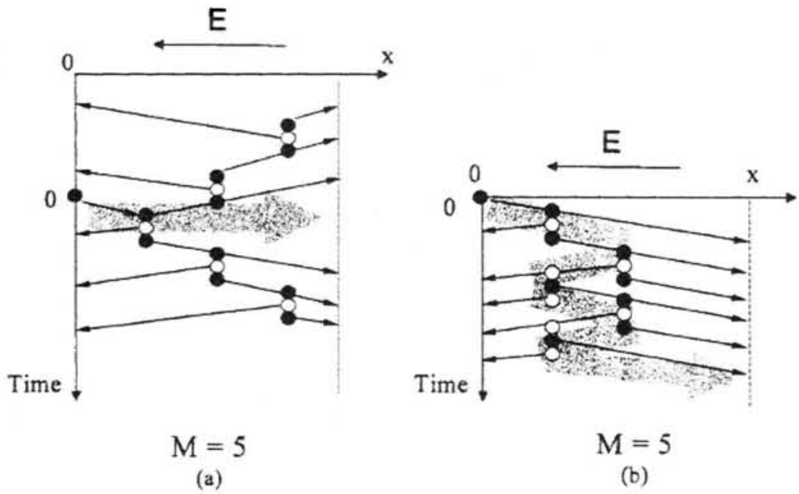

图 1-2 一个电子在不同电离系数比的半导体中的碰撞电离情况。(a) 电子的电离系数远大于空穴；(b)电子和空穴电离系数相当。

因此，低 k 值的材料有利于降低器件噪声，提高频率响应。而且对于雪崩探测器而言，当 k 在 0.01~0.1 器件增益能达到 100~1000 倍；当 k 在 0.3~1 之间器件增益只能达到 15 倍，因此为了获得更大的增益系数，APD 的倍增区材料的离化率也比要远小于 1。研究表明 Si 的 k 值随外加电场在 0.01-0.1 之间变动[3]，其值远小于 Ge 和 InP 材料，因而硅成为雪崩探测器理想的倍增材料。

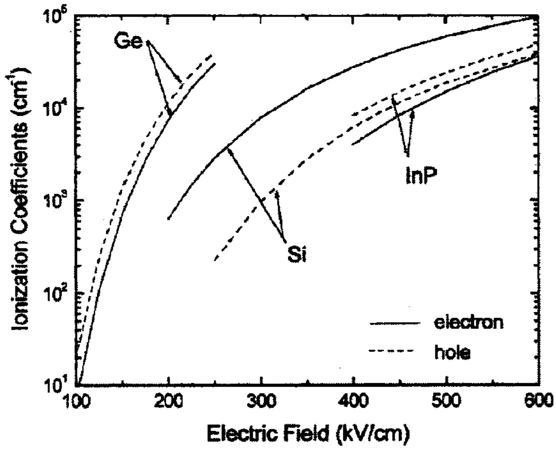

图 1-3 在 300K 下 Ge(100)[4]，Si[5]和 InP[6]电子和空穴的电离系数。

1.1.3 暗电流

暗电流的定义：光电二极管没有光照时，在半导体内部，由于热电子发射等原因也会产生自由载流子，即自由运动的电子和空穴，它们在电场的作用下也会产生电流，这种无光照时在电路上流动的电流称之为暗电流。对于光电探测器，一般工作在反偏或者零偏状态下，暗电流作为噪声（N），跟器件的灵敏度呈反比，不利于对光探测，应尽量减小。

光电二极管暗电流根据产生位置分：体漏电流（扩散电流 I_{diff}，产生复合电流 I_{ge}）和表面漏电流 I_s。

扩散电流：在无光照的情况下，半导体探测器在外加偏压下工作时，耗尽区内载流子浓度相对较高，但是由于电流保持很定，耗尽区内部准费米能级梯度要小，载流子的分布梯度小，而且耗尽区宽度通常小于扩散长度，耗尽区边沿外一定距离形成较大的浓度梯度和准费米能级梯度，多子由于扩散到达耗尽区，由一侧渡越到另一侧，形成扩散电流，但是此扩散电流的大小是由扩散到的少子区域决定的。

产生复合电流：在无光照的情况下，半导体探测器工作在反向偏压下，此时器件的载流子是被方反向抽取的，载流子的浓度 $np<<n_i^2$，此时耗尽区载流子的产生复合作用以产生作用为主。

表面漏电流：主要是由表面的缺陷态引起的缺陷态辅助电流，器件表面和侧壁上的缺陷态，会形成一个产生复合中心，在禁带宽度范围内形成缺陷态能级，由于缺陷态能级距离导带和价带的能级差小于禁带宽度，电子由价带顶跃迁到缺陷态能级以及空穴由导带底跃迁到缺陷态两个过程的发生几率，高于价带顶与导带底之间的跃迁，因此，增大了自由载流子的产生几率，增大了输运电流，即暗电流。

由于对于圆台型器件而言，表面漏电流不仅来自于光敏面漏电流，还来自于刻蚀侧壁

的缺陷、钝化等造成的漏电流。因此暗电流还可以根据器件的周长和面积分为体电流和侧壁漏电流两部分，前者是由光电二极管结区中热生成的电子和空穴引起的，后者则是由侧壁的表面缺陷、清洁度引起在偏置电压作用下形成局域漏电流。

1.2 高灵敏 Si 基 Ge 单行载流子探测器

1.2.1 大功率光接收探测器

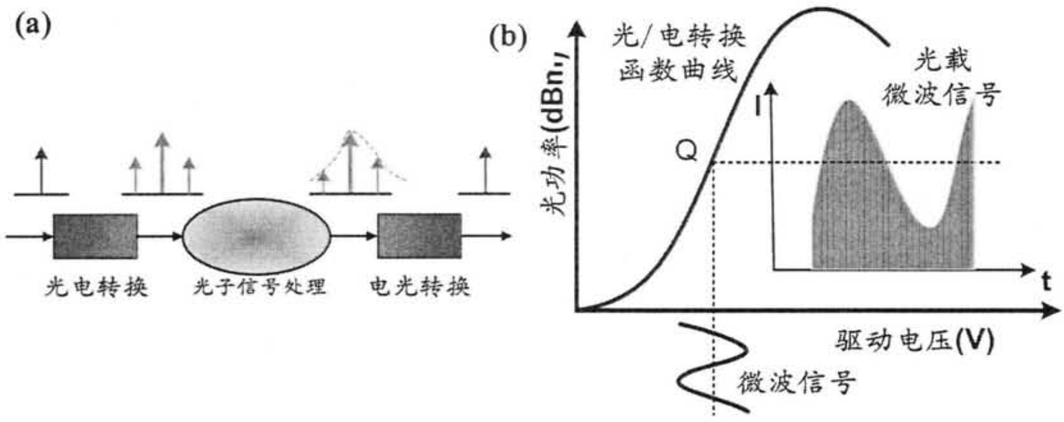

图 1-4 光载微波信号的载波原理示意图。

在现今的信息系统中，为了提高信号传输速率，降低多通道传输的相互串扰，降低信号传输中的能量损耗和热损耗，普遍采用光波作为电信号的载波，通过光纤进行信息的传输，在通过检波转化为微波信号传输到后续处理电路中，图 1-4(a)为光调制，光传输处理在到光探测整个过程的信号变换示意图。

信息领域中的一个大方向是微波系统，它传输和处理的为微波的连续信号，如正弦波信号，其对信噪比以及动态范围要求比数字系统高很多。以微波系统中最常用的功率调制载波法为例分析其光调制解调原理，如图 1-4(b)，Q 点为光波的静态功率点，光功率以 Q 点为平衡点正弦浮动。为了保证探测解调的微波信号与光功率调制信号的一一对应，调制的光信号的峰值和谷值要保证在探测器的线性区域内，得到完整的正弦微波信号。

因此，微波系统中要求光电探测器有更大的饱和输出电流，更高光电转化的线性度。这样，器件接收光的 Q 点的取值可以更多大，载波的峰值和谷值的差值更大，大大提高了微波系统信噪比，拓宽了系统的动态范围，而且载波光信号的功率（Q 值）的提高，其有利于降低外调制端口中的信号损耗和噪声指数，可简化高比特信号接收系统的结构，例如光操控相位阵列天线（optically-steered phased array antennas）增大输出的光电流就可以降

低振幅匹配电增益，从而简化振幅匹配电路。

1.2.2 单行载流子探测

传统的 PIN 结构器件，受到光生电子和空穴的空间电荷效应的限制，当入射光功率超过某一阈值后，输出的电信号（通常是电流信号）与入射的光功率不再呈线性关系，此时认为探测器达到饱和，这一阈值功率对应的输出电流，被称为饱和电流。限制传统 PIN 结构探测器的饱和输出电流值的一个重要因素就是空间电荷效应，大的光注入时，大量的光生载流子输运会形成电荷中心，光生的电子和空之间会形成与外加电场方向相反的内电场，造成能带的弯曲，如图 1-5(a)，阻碍载流子的输运和收集，当光生载流子足够多，将能带拉平时，输出的光电流最大值不再变化，即器件达到饱和。此外，器件的载流子输运时间取决于速度较慢的空穴，因此 PIN 器件带宽提高的空间有限。

因此，1997 年 Ishibashi T 等人提出了单行载流子（UTC）探测器结构 [7]，能带结构示意图如图 1-5 (a)，器件的吸收区域为 p 型掺杂区，空穴为多子，因此空穴的弛豫时间较短，探测器的信号输运主要靠电子，光生电子则在扩散和漂移的作用下移动到耗尽的空间电荷区，进入耗尽区后在外电场的作用下迅速漂移至收集区收集，大光强注入时 UTC 结构器件能带分布示意如图 1-5(a)，单电子的输运避免了空间电荷效应引发的能带弯曲而造成的电流饱和现象，同时器件内的有效载流子为电子，电子的漂移和扩散速率远大于空穴，有效缩短载流子的输运时间，因此器件具有高速光响应的优势，如图 1-6 所示。此外，III-V 族 UTC 探测器可利用III-V材料的速度过冲效应(Velocity overshoot effect)，使得电子漂移速度远大于饱和漂移速率[8, 9]，因此 UTC 探测器的渡越频率要远大于相似结构的 p-i-n 结构探测器，高饱和高速率的 UTC 器件成为了探测研究的又一热点方向。

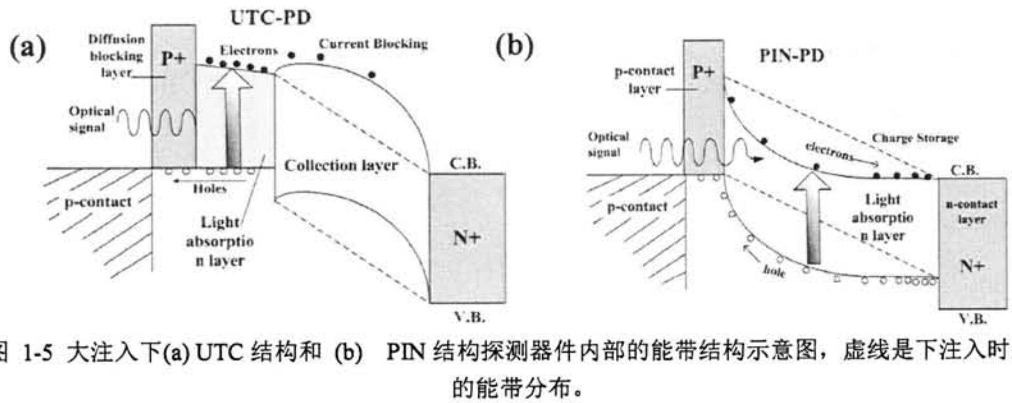

图 1-5 大注入下(a) UTC 结构和 (b) PIN 结构探测器件内部的能带结构示意图，虚线是下注入时正常的能带分布。

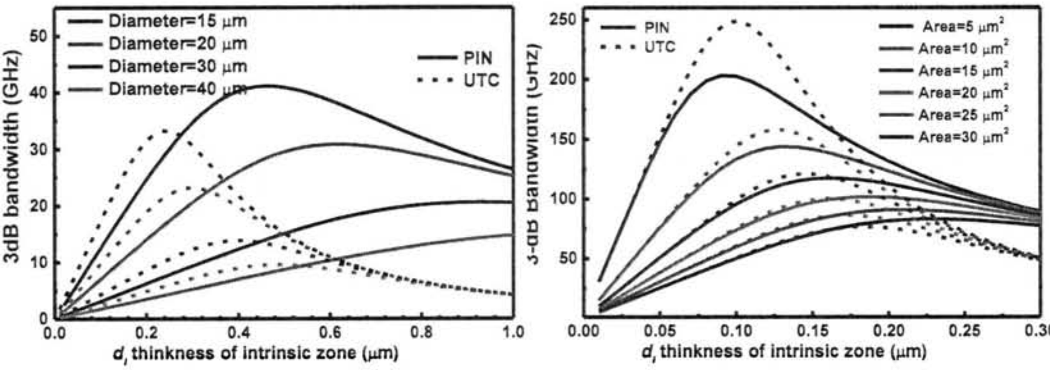

图 1-6 同一台面尺寸的 PIN 结构与 UTC 结构器件的 3-dB 带宽对比，此时 UTC 结构中的吸收层厚度 W_a 与本征收集层厚度相等 W_c (W_a=W_c)，可看到对于本征层薄的器件 UTC 结构比 PIN 结构在 3-dB 带宽特性方面更有优势。

1.2.3 高灵敏 Si/Ge 单行载流子探测发展

目前已报道的 3dB 带宽最高的面入射探测器是日本 NTT 公司 Ishibashi 等人研制的，他们通过减小 UTC 探测器面积提高带宽，2000 年他们报道了制作的尺寸为 5μm^2 的 InP/InGaAs 材料的 UTC 探测器其带宽达到了 310GHz，但是光响应仅为 0.07A/W[10]，2007 研制的 III-V 族波导 UTC 器件的带宽提高到 325GHz[11]，至此带宽已经达到现今工艺和理论的极限，因此，之后 NTT 公司转而致力于将 UTC 器件应用到微波光子和天线系统，通过与电容、电阻和天线等外电路的简单集成进一步提高系统接收带宽，系统已实现宽带宽 THz 的信息接收[12, ,13, 14]。国内对于 UTC 结构的研究主要集中在 InP/InGaAs 材料的单芯片，清华最新研制的双漂移层 UTC 的 3-dB 带宽为 106GHz，响应度 0.17A/W[15]。

但是，InP/InGaAs 材料体系价格昂贵，器件制备需要多层异质材料外延，不能与常规的 CMOS 工艺线兼容，与微电子电路集成困难，难以实现小型化，模块化以及单芯片的集成。而 IV 族的硅、锗材料体系可以完美的解决以上问题，而且限制器件的饱和性能的另一个重要因素是热效应，而 Ge 材料的热导率是 InGaAs 材料的 11 倍，Si 衬底的热导率大于 InP[16]，因此理论上 Ge/Si UTC 器件的饱和性能要优于 InP/InGaAs UTC 器件，由于 Si 基 Ge 异质材料外延以及原位掺杂工艺的技术限制，直到 2012 年 Molly Piels 在 OE 才报道处了初批 Ge/Si 垂直入射型 UTC 探测器的成果[17]，器件带宽为 20GHz，响应度为 0.12A/W @1550nm，之后同一课题组，利用了 Si 基探测器能够跟 Si 无源波导单片集成，同时提高器件带宽和响应度的优势，2014 年报到了其制备出的波导型 Ge/Si UTC 器件[18]，将器件的响应度和带宽进一步提高到 40GHz 和 0.5A/W。

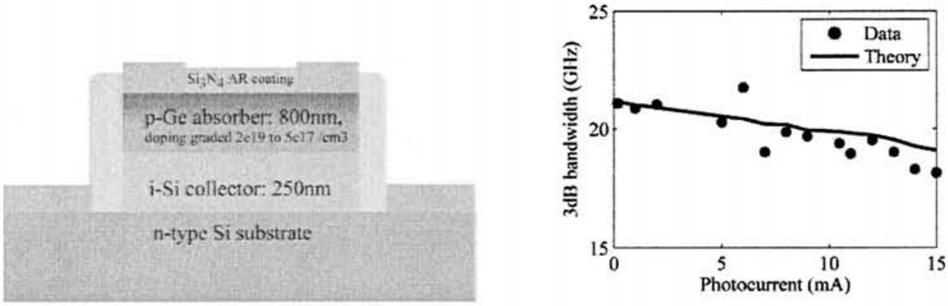

图 1-7 首批研制的垂直入射型 Ge/Si UTC 探测器结构和 3-dB 带宽性能

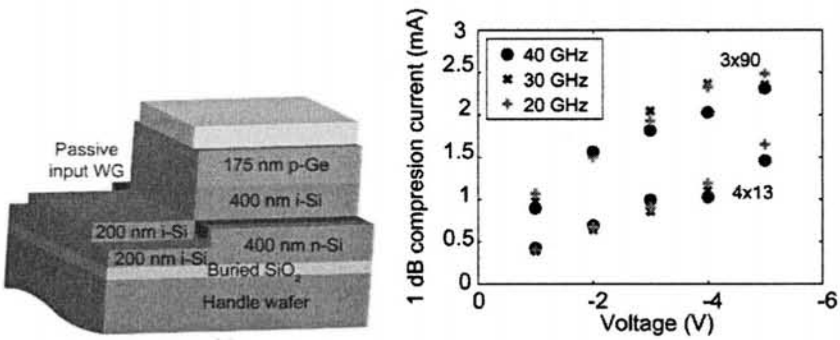

图 1-8 研制的波导耦合型 Ge/Si UTC 探测器结构和带宽与饱和度性能

垂直入射型探测器，由于器件封装的光耦合结构简单，器件制备的工艺容差大，对于片间或者板间的光通信非常有优势，但是垂直型结构的探测器的耗尽区与吸收区是同一区域，器件的响应度和带宽相互制约，因此在保证器件带宽和噪声的同时，提高器件光响应特性是提高 Si/Ge UTC 器件灵敏度最为关键也是最直接的途径。

我们利用 SOI 沉底的 BOX 与 Si 层界面的高折射率差，通过设计个膜层的厚度，使入射光在 BOX 于顶层 Si 界面处发生相干作用，提高该处的反射光强度，相当于加长了垂直入射的光吸收长度，从而提高器件的光响应度。

1.3 高灵敏硅基锗雪崩光电探测器

1.3.1 光通信 Si/Ge 探测器

早期光通信系统中，通信波长在 850nm 波长区域，此波段内的多模光纤(MMFs)传输的传播损耗在 2~3dB/km，标准光纤的带宽达到了 20THz，该波段的光被 Si 探测器和 Si ICs 单片集成构成的接收器芯片进行接收和转化。随着 1310nm 波长的激光器的研发，使得 1310nm 的通信窗口引入到了光纤通信系统中，其在单模波导（SMF）内的光损耗降到了

0.5dB/km。从 20 世纪 80 年代开始，单模光纤逐渐取代 850nm 的多模光纤成为通信主导。另外一个单模通信窗口为 1550nm，其最小的单模光损耗达到 0.22dB/km。因此在现今的光纤通信领域中，1310nm 和 1550nm 成为信息的主要载波波长。与硅材料同属元素周期表第 IV 族半导体且晶格结构同为金刚石结构的 Ge 晶体，其禁带宽度为 0.67eV，能够对 1310nm 和 1550nm 光传输低损耗窗口有较高的响应，由于 Ge 与 Si 材料的晶格结构类似，晶格常数相近，可以通过异质外延的方式，实现硅基 Ge 材料的大面积集成，这是 III-V 族探测器元件无法满足的，而且也避免了 Si 基键合型 InGaAs/Si 探测器在键合过程中引入的杂质，位错，工艺难以控制，不稳定，高成本，随机性太大和集成面积小等问题。随着硅基 Ge 低位错外延技术的不断提高，可以和硅基微电子芯片实现单片集成的 Si 基 Ge 探测器成为了光互连和光通信领域主流的研究方向。

总结 Ge/Si 探测器件的优点主要有以下几点：

A. 现有 Si 衬底外延 Ge 层技术已日渐成熟，异质结界面处位错密度可控制在器件性能允许的范围内，暗电流可被有效抑制；

B. 器件加工工艺与现有 CMOS 微电子加工兼容，降低了器件成本；

C. 器件为 Si 衬底器件，便于实现集成化，阵列化和模块化；

D. 器件吸收区为 Ge 材料，有效控制吸收区电场分布，可降低热激发率，使器件可工作在常温下，在 1550nm 和 1310nm 处均有较大响应；

E. Si 作为衬底，便于实现波导集成结构。

当然任何器件都会有自身缺陷，而 Si/Ge 器件最大的缺陷是 Si 材料和 Ge 材料之间 4.18% 的晶格失配形成异质结界面的位错及应力，它们会对器件暗电流及能带有一定的影响。通过外延技术的优化，Ge/Si 界面处的位错密度已经降到了~10^5，而且通过器件结构的优化，是可以弱化或消除位错对器件性能的影响。

1.3.2 Ge/Si 雪崩光电探测器结构

雪崩光电探测器(Avalance Photodetector, APD)是利用半导体的雪崩倍增效应，在半导体器件内进行光生载流子和内部电流的倍增，从而增大器件响应度和灵敏度的一种探测器类型。因此器件一般工作在高反向偏压下，也要求器件具有高增益和较高速度响应，但是高增益带来的是大噪声，因此，要综合考虑器件的噪声特性和增益特性。

APD 中有一种常用的结构为吸收倍增分离型（Separated Absorption Multiplication，缩写为 SAM）结构，如图 1-9 所示，此结构的探测器中光吸收过程和光生载流子的雪崩倍增过程分别在两个区域进行，有效降低因光子吸收位置不同，带来的载流子倍增系数的浮动，从而降低过剩噪声。同时，也增强了雪崩光电探测器结构设计的灵活度，可以选用低电离系数比的材料作为倍增区，进一步降低噪声。

硅基 Ge APD 通常也采用吸收倍增分离型结构，宽的低电场为器件的 Ge 吸收区，禁带宽度为 0.66eV 的 Ge 材料在近红外光通讯波段有着良好的吸收效率，具有高的迁移率与导热性，有利于器件降低载流子渡越时间，获得高的频率响应[19]；器件在雪崩状态工作时，器件内部的电场是由 n+层一直延伸到了 p+，整个器件都耗尽[20]，如图 1-10 所示，Ge 层生成的光生载流子可以以饱和速度进行漂移，穿过电荷区，到达窄的 Si 倍增高场区，由于 Si 材料的空穴与电子的电离率相差较大（k~0.01），与 InP、Ge 等材料相比，可有效的降低过剩噪声，并消除倍增材料中位错、缺陷等释放俘获的光生载流子而引起的后脉冲（after-pulsing）效应[21,22,23,24]，提高器件灵敏度，而且便于集成，与传统 CMOS 加工工艺兼容，成本低廉，吸收倍增分离型波导 Si/Ge 雪崩光电探测器具有良好的性能优势和广阔的应用前景。

当器件发生雪崩击穿时，有[25]：

$$\alpha_e(W_d-b)=\frac{\ln(k)}{k-1},\qquad k\equiv\frac{\alpha_h}{\alpha_e} \tag{1-8}$$

其中电离比 k 和电子的电离系数 α_e 跟外加电压相关，器件的耗尽区厚度为 W_d，是吸收区、电荷层以及倍增区厚度的总和；b 为高场区的厚度，是电荷层和倍增区的厚度总和；整倍增层的厚度 W_m 调节其最大电场强度 E_m。此时的器件的击穿电压为：

$$V_B=E_m b+(E_m-\frac{qQ}{\varepsilon_s})(W_d-b) \tag{1-9}$$

这种吸收和倍增分别在不同的材料中进行，使得光在窄带材料中吸收，宽带材料进行倍增。由于器件的击穿电压 V_b 与材料的 $Eg^{3/2}$ 成正比，因此在宽禁带的倍增区由隧穿和微等离子产生的暗电流大大减小，并有效防止 APD 结构中的边缘击穿。

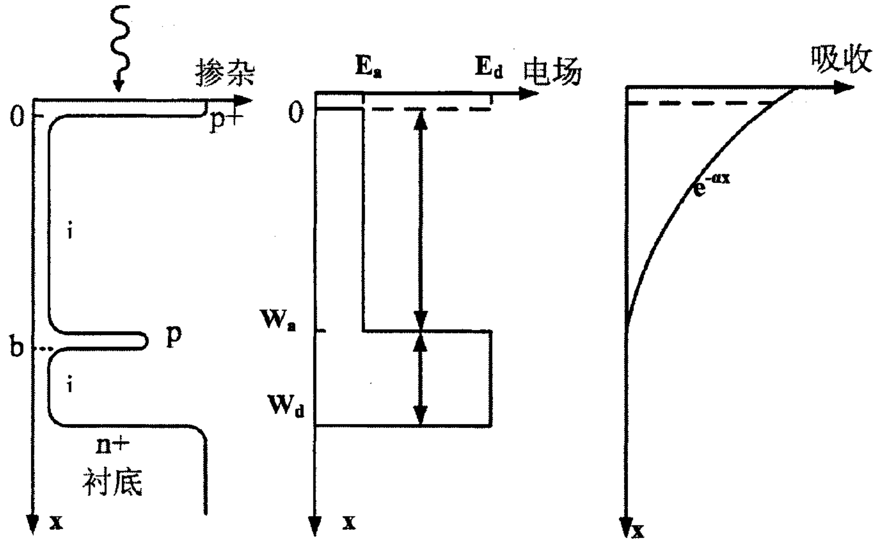

图 1-9 SACM 雪崩探测器的掺杂分布、电场分布以及光吸收分布

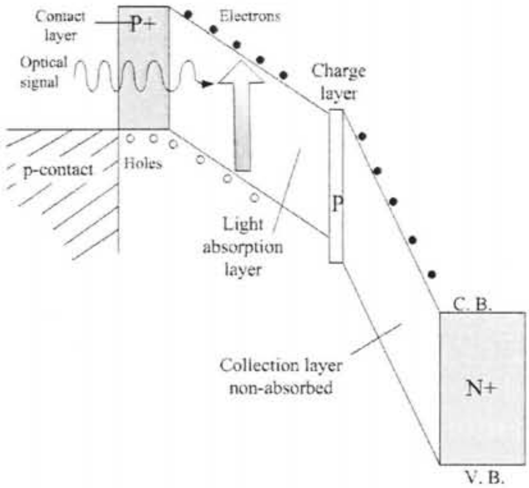

图 1-10 吸收倍增分离型雪崩探测器的能带图

1.3.3 高灵敏波导 Ge/Si SAM-APD 的发展概况

波导探测器突破了传统垂直入射结构探测器的光响应与频率响应之间的相互制约问题，且能天然的与光波导集成，具有高灵敏度、高频率响应和易与硅基芯片大规模集成等特性，是未来信息系统向高速大带宽发展必需的核心器件，是当前硅基光电子器件研究的热点之一。

传统 Si/Ge SAM-APD 中的倍增层为硅材料，为了保证足够高的雪崩增益，器件的硅材料层厚度一般>0.7μm，而光电集成芯片的光通道普遍为单模光波导，硅材料厚度仅为~0.22μm，光通道与雪崩探测器对硅材料厚度要求的不匹配增大了器件设计难度。早期的波导 Si/Ge SAM-APD 为保证高的雪崩增益，多采用多模 Si 波导与 Ge 吸收层的倏逝波耦合设计，但是多模波导内光强中心远离吸收层界面，单位长度的倏逝波耦合效率远低于单模波导，因此为提高光耦合效率，增加器件吸收长度是早期器件普遍采用的方法：2009 年 Joe C. Compal 研制了吸收长度为 70μm，灵敏度为-30.4dBm 的器件[26]，但是器件响应度仅为 R=0.6 A/W @1550nm。而申请人制备的相同吸收层截面尺寸的单模波导 Si/Ge 探测器件，吸收长度仅为 10μm，响应度可达 0.84A/W @1550nm[27]。因此，多模波导入射的 Si/Ge SAM-APD 器件由于单位长度耦合效率低，器件光响应度低，器件尺寸大。

因此，在保证一定倍增效率的前提下，提高波导器件单位长度耦合效率是波导 Si/Ge SAM-APD 器件研究的重点，目前国际上提出了三种优化结构设计：

第一种：基于多模干涉（MMI）原理的波导耦合结构，图 1(a)为该结构示意图。前端

多模硅波导长度为$L_{step}=N\cdot n_{Si}[H_{step}+(\lambda_0/\pi)(n_{Si}^2-n_{SiO2}^2)^{-(1/2)}]^2/\lambda_0$时，光发生对称型 MMI 现象，将波导截面的光强中心移至器件吸收层边缘，可以提高器件倏逝波耦合效率，实现了光子从单模波导到 APD 吸收层的传输。但是由于相干光场的强度中心随光传输长度增大而不断改变位置，无法一直处于吸收层边沿的高倏逝波耦合区域，因此时域有限差分法（FDTD）计算结果图 1(b)显示[28]，Ge 吸收长度为 10μm 器件的最大吸收效率仅为 72% @L_{step}=3μm，而光强中心始终位于吸收层边沿的单模波导的耦合效率达~ 92%。此外，该结构器件制备需要两次分别对 Si 和 Ge 材料的外延，工艺复杂。2013 年，新加坡 IME 制备了此类结构的 APD 器件[29]，1550nm 光入射，器件尺寸为 8μm×10μm，理论预测灵敏度-30.5dBm，器件响应度最高为 22A/W，3-dB 带宽最大到 20GHz，但是各参数对应的增益系数却未给出。

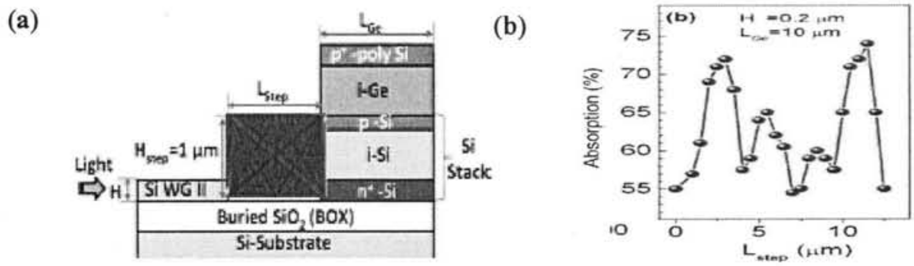

图 1-11 利用多模干涉的波导入射型器件(a)器件结构剖视图；(b)多模 Si 波导长度与吸收效率的关系。

第二种：利用边沿电场(fringing electric field)效应将 Ge 吸收层的光生载流子扫入位于脊形硅波导内的倍增区，载流子输运和电场分布如图 2(a)所示。这种方法的优势是器件尺寸可缩小到纳米量级，有利于提高集成度，更重要的是 Ge 吸收层位于 Si 单模波导之上，光强中心靠近吸收层边沿，有利于提高器件倏逝波耦合效率，但是载流子在边沿电场作用下先水平输运再进入 Si 倍增区进行同向的水平加速，因而载流子在倍增区的有效倍增长度被大大缩短，极大的制约了器件的光电流增益。同时由于扫入倍增区的光生载流子主要集中在倍增区与吸收层界面，而外延的 Ge/Si 界面处存在大量界面态，导致器件噪声大。2014 年发表的实验结果进一步验证了上述分析 [30]，器件剖视图如图 2(b)，最大倍增系数仅到 9，波长 1.3μm 入射，长 16μm 的器件响应度 0.9A/W，增益带宽积仅~60GHz，理论灵敏度为-30.5dBm。

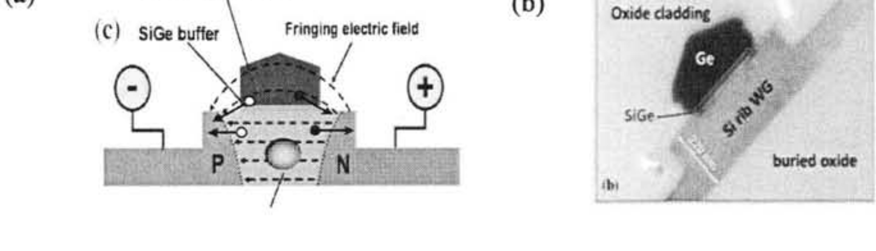

图 1-12 利用边沿电场效应的 Si/Ge 吸收倍增分离型 APD 器件：(a) 原理示意图 (b)剖视图。

第三种：新加坡 IME 提出了双侧横向倍增结构，在单模硅波导顶层直接一次外延 i-Ge 吸收层，单模波导光强中心仅靠吸收层，解决了波导与吸收层之间的倏逝波耦合效率问题；更是巧妙的利用了波导层硅基材料横向尺度大的优势，将电荷区和倍增区横置在硅波导层上，使器件具备了高光电流增益所要求的倍增长度。图 3(a) 显示了制备的器件结构示意图，Ge 吸收层的底部宽 4.4μm 长 80μm；图 3(b)显示了器件的吸收层附近的电场分布，图 3(c) 显示了器件横向的电场分布，可看出光生载流子主要靠纵向扩散到达电荷区，通过集中于 Si/Ge 异质结界面附近横向扩散到达倍增区，由于界面处存在大量缺陷态，大大缩短了电荷区少子寿命，且器件光电流由作为少子的电子决定，因此 M=1 时器件的响应度仅为 0.277A/W @1550nm[31]。此外长距离的横向扩散严重延长了载流子渡越时间，降低了器件响应频率。因此测得的器件的增益带宽积仅为 85.5GHz@-22V，暗电流高达~22μA。

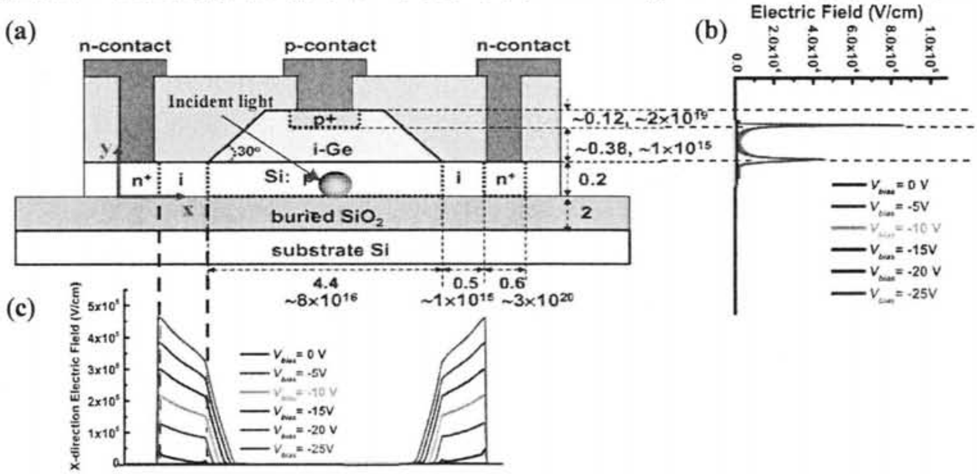

图 1-13 横向倍增纵向吸收波导 Ge-on-Si APD 结构剖视图以及不同偏压的电场分布。

通过上述分析可知，吸收倍增分离型波导雪崩器件的单位长度耦合效率与倍增效率是一对矛盾。相较于前两种解决方法，第三种方法理论上能够同时满足高效率耦合和高效率倍增，但是研究者忽略了横向和纵向电场的调控以及载流子输运对器件性能影响的复杂性，器件在响应度、增益带宽等性能方面仍然存在很大的提升空间。因此，如何在 Ge 吸收层与 Si 基光波导之间实现高效率耦合，以及如何同时在 Si 材料中实现高效率倍增，是高性能波导 Si/Ge SAM-APD 研究的关键问题。

1.4 高灵敏度硅 PIN 电探测器

1.4.1 300nm~1100nm 波段的 Si 探测器

硅材料是地球上分布最广的元素之一，地壳中的含量约 27.6%，仅次于氧元素，是地球上元素含量第二高、应用最广泛、对人类生活影响最大的元素，也是最关键的半导体材料。1962 年在 RCA 器件集成研究组工作的 Stanley，Heiman 和 Hofstein 等发现，可以通过扩散与热氧化在 Si 基板上形成的导电带、高阻沟道区以及氧化层绝缘层来构筑晶体管，即 MOS 管，硅材料成为了微电子芯片制备的最重要也是最核心的材料。硅晶体是禁带宽度为 1.12eV 的间接带隙半导体，决定了硅晶体的发光效率不高，却能够吸收截止波长为 1107nm 的光谱能量，并转化为电能传输，因此硅材料被广泛用于紫外，可见光和近红外区域的光接收和探测领域。

硅光电探测器是发展时间最长，工艺技术最成熟，应用范围最为广泛的一种探测器件。据了解，硅光电探测器主要在红外遥控接收，环境光强度检测，激光功率检测，测距，矿藏勘探，工业自动控制，电子黑板等方面，而军用方面，硅光电探测芯片是核辐射探测器的核心部件，而且被用于激光瞄准，制导跟踪及搜索装置中，在激光微定位、位移监控等精密测量系统中起着关键作用。

1.4.2 PIN 结构探测器结构

PIN 结构是最常用的光电二级管结构，具体结构如图 1-14，在器件 p 型区和 n 型区之间插入一定厚度的本征半导体区，由于内建电势差以及外部反偏电压的作用，本征区域耗尽，电阻率高，电压主要在此区域降低，形成较高电场以便有效收集光生电子-空穴对（electron-hole pairs, EHP），此类结构的器件的本征区厚度远大于高掺杂区，因此大部分的光生电子空穴对是在本征区产生，并在强电场的作用下分开，分别向 p+区和 n+区漂移，由于半导体载流子的漂移速度远大于扩散速度，因此大大的缩短了载流子的渡越时间。此外，耗尽层加宽明显减小了器件的结电容 C_j，减少探测器电路的时间常数，同时，宽的耗尽区有利于器件对光辐射的吸收，提高器件吸收长度和体积，利于提高器件的量子效率。因此，PIN 结构型器件的具有很好的高频特性，普遍用于高频接收型电路中。但是由于本征区的引入，耗尽区宽度的增大，会提高器件的暗电流，降低器件灵敏度。图 1-14 为垂直结构的 P-N 结和 PIN 结构探测器剖视图，以及各层对应的电场分布对比。

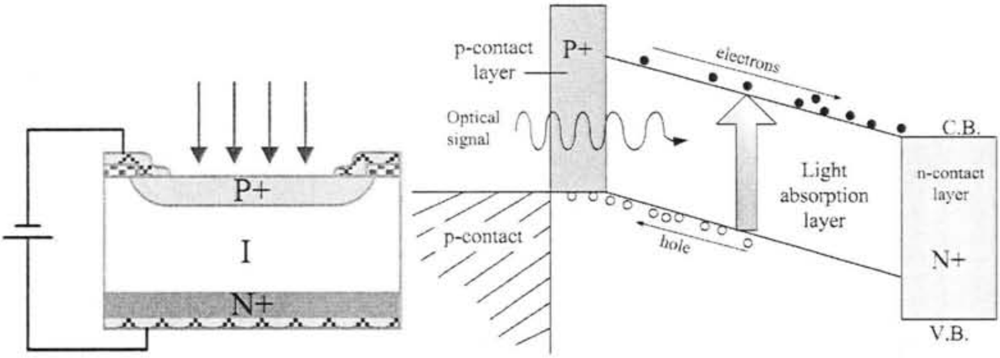

图 1-14 P-I-N 结构探测器的剖视图以及内部能带结构和工作过程。

1.4.3 高灵敏 Si-PIN 探测器发展

Si-PIN 已经产品化和产业化，国际上，Hamamatsu，Infineon，Vishay，Source Photonics Inc.，OSI Optoelectrionics，Everlight，EMCORE，menlosystems，SensL 等多家半导体芯片研发和生产公司都进行了 Si 光电探测器件的销售[32]，但是，中国大陆对于半导体光电产业的发展仍处于初始阶段，通过资本和人力吸引了台湾一些优秀的光电研发和生产公司在大陆建厂生产，但是器件研发和制备中最核心的关键技术仍掌握在境外公司手里，因此，我国的探测芯片仍然依赖进口，成本居高不下，在一些敏感应用领域的发展受到国外封锁，严重制约着我国在国家安全、核科学、遥感探测等领域的发展。

产品化的 Si-PIN 普遍采用垂直型结构，本征层足有上百微米厚（如图 1-15），其厚度可根据器件的量子效率、频率响应带宽以及暗电流密度的需求进行调整，一般在 200μm~400μm。器件在 350nm~1100nm 波段均有较高响应[33]。但是加宽的耗尽区也为暗电流噪声的产生和收集提高了便利，因此 PIN 光电探测器快速响应，相对较高的暗电流，其对小信号的识别，高质量成像，弱信号检测等方面的应用其到一定的限制作用，其较高的暗电流也是制约器件灵敏度提高的关键因素，因此提高 Si-PIN 器件的灵敏度需要对器件的暗电流进行分析，获得不同工作条件下，暗电流的主要产生机理，进而提出优化方案。

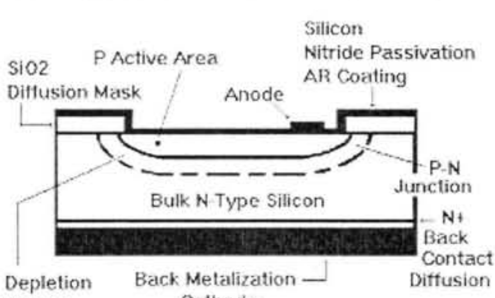

图 1-15 (a)商业型 Si-PIN 探测器的结构剖视图。

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第二章 高响应度的硅基锗单行载流子（UTC）探测器

微波光子学是现今研究的一大热点，利用微波技术与光传输技术相结合，进行高速大功率信号的处理，系统接收的光信号强度越强，系统的动态范围越广，在外调制端口中的信号损耗和噪声指数就越低，并可简化高比特信号接收系统的结构，在光操控相位阵列天线（optically-steered phased array antennas）增大输出的光电流有利于降低振幅匹配电增益，简化系统。空间电荷效应是限制传统 PIN 结构探测器的饱和输出电流值重要因素，因此 1997 年 Ishibashi T 等人提出了 UTC 探测器[1]，利用 P 型吸收层，将输运载流子变为仅电子，抑制了空间电荷效应的同时增大的光生载流子输运速率，因此高饱和高速率的 UTC 器件成为了探测研究的又一热点方向。

2.1 高响应度硅基锗 UTC 探测器的设计

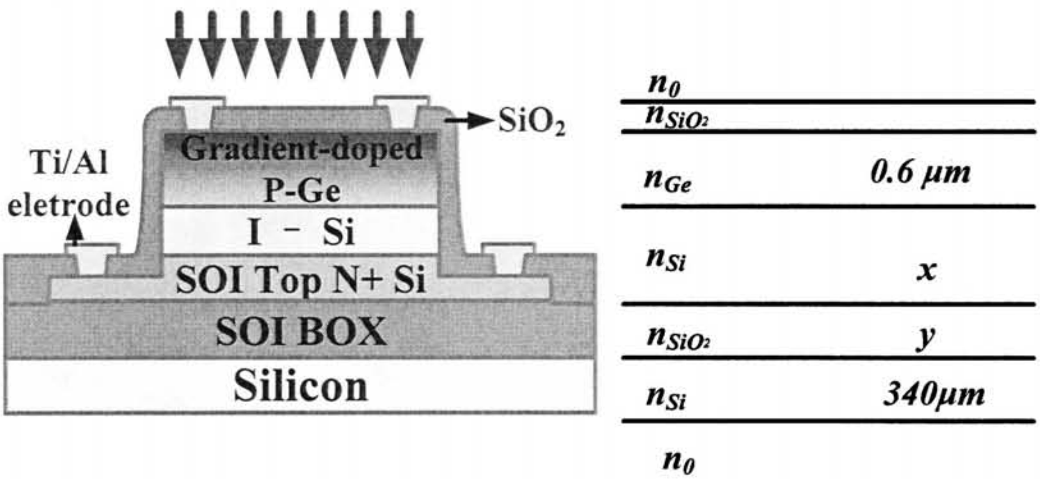

图 2-1 Ge/Si UTC 的结构示意图

图 2-1 为典型的 SOI 衬底的 Ge/Si UTC 器件的结构简图，由梯度掺杂是 p 型 Ge 吸收层，本征的 Si 载流子收集层，衬底顶层 Si 层通过磷杂质扩散形成 N+欧姆接触层；右侧的图为折射率分布简图。

2.1.1 高频率响应

1. 吸收层和收集层的厚度

UTC 结构的吸收层为 p 型掺杂层，光生载流子在该处是以扩散的方式进行输运的，扩散到本证收集层，再在电场的作用下漂移到欧姆接触层被收集，本证载流子收集层的禁带宽度大于吸收区材料，在价带形成势垒，防止空穴的反方向扩散，器件的渡越频率为：

$$f_t = 1/(2\pi\tau_a) = 1/(2\pi(W_a^2/3D_e + W_c/v_{th})) = 1/(2\pi(W_a^2/3D_e + W_c/\sqrt{2kT/\pi m_e^*})) \tag{2-1}$$

器件的 RC 响应频率可有下面公式计算：

$$f_{RC} = \frac{1}{2\pi(R_s + R_L)C} = \frac{1}{2\pi(R_s + R_L)\cdot\frac{\varepsilon\varepsilon_0\pi D^2}{4W_c}} \tag{2-2}$$

其中，W_c 为本征收集层的厚度，D_e 为电子在 p 型吸收层的扩散系数 W_a 为 p 型吸收层的厚度，垂直入射型器件的吸收层厚度一般等于吸收长度，因此为了保证器件的响应度在 0.1A/W 以上[2,3]，器件的吸收层的厚度设置为 0.6μm，器件的 3-dB 带宽计算公式：

$$f_{3dB} = \frac{1}{\sqrt{f_{RC}^2 + f_t^2}} \tag{2-3}$$

根据公式(2-1)、(2-2)和(2-3)得到不同尺寸的圆台器件的 3dB 带宽随着本征收集层的厚度变化的关系曲线，为了获得较高的 3dB 带宽，选取 W_c=0.3μm。

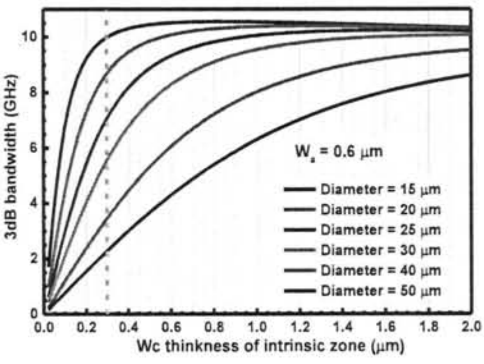

图 2-2 不同尺寸的 Ge/Si UTC 结构的圆台器件的 3dB 带宽随着本征收集层的厚度变化的关系曲线。

2. 吸收层内部电场设计

UTC 结构的吸收层是 p 型掺杂，载流子在其内部的渡越要通过扩散的方式进行，因此

大大拖慢了器件的渡越时间，因此设计了一种梯度掺杂的结构，在吸收区内部形成梯度电势，以增大载流子在此区域的渡越速率。分别讨论了缓变的掺杂浓度分布和突变的浓度梯度，其中突变梯度分布中将吸收区分别平均分成 2, 4, 6, 8, 10, 12 个区域，相邻两个区域的界面处是掺杂浓度的突变界面，通过 silvaco 半导体模拟软件的模拟计算得到，这几种结构器件的能带分布以及吸收区电势差，具体结果如图 2-3 所示，通过对比不同掺杂结构下，吸收区的两端的电势差，可获得载流子在渡越吸收区时获得总的动能，动能越大载流子的漂移速率越大，渡越时间越短，因此可以看到，将吸收区分成 4 等份每个等份的掺杂浓度相同，在相邻区域界面处突变掺杂浓度，最后载流子漂移获得的动能最大。

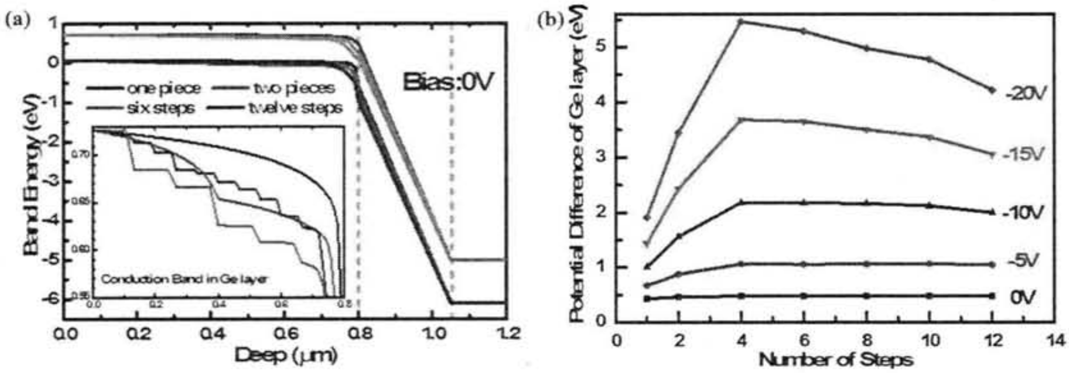

图 2-3 (a) 吸收区均匀梯度掺杂、等分成 2 分的均匀梯度，等分成 6 分，12 分突变掺杂变化的能带结构图；(b) 缓变的掺杂浓度分布突变梯度分布中将吸收区分别平均分成 2, 4, 6, 8, 10, 12 个区域的吸收区电势差，可看到将吸收区分成 4 等份的突变梯度在吸收区的电势差大，载流子可获得较大的动能渡越吸收区。

2.1.2 提高光吸收

器件的光吸收有响应度值反映的，响应度受到通光面的光透射率，吸收层材料的吸收系数，光吸收长度和光生载流子的收集效率决定。

(1) 通光面的光透射率可以通过增透膜的优化提高：以单层增透膜为例，空气、SiO_2 薄膜、Ge 吸收层的折射率分别为 n_1、n_0、n_2，薄膜 n_0 厚度为 d，得到空气与介质薄膜之间的反射率 r_{10} 以及介质薄膜与 Ge 吸收器件层的反射率 r_{02}。把入射光强度设为 1，可得到一次反射光线 1 的强度为 r10，经过两次透射一次反射的光线 3 的强度为 $r_{02}(1-r_{10})^2$，经过两次透射四次反射的光线 5 的强度为 $r_{02}^2 r_{10}^2(1-r_{10})^2$。事实上，反射光线 5 非常小(~$10^{-6}$) 可以忽略不计。返回空气中的光线主要是 1 和 3，因此只要光线 1 和 3 满足相位相反，振幅相同，才可发生电磁场的相干抵消。

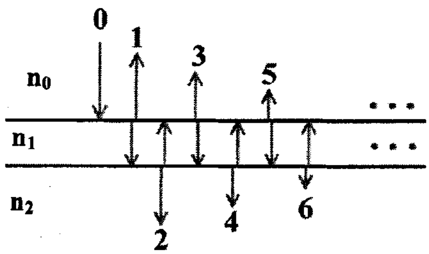

图 2-4 光在单层膜中的反射示意图

为使 1 和 3 的相位相差 π 的奇数倍，发生相消干涉。对薄膜的厚度有一定的设计要求。当光从光疏介质(折射率小，光传播速度速大)入射到光密介质(折射率大，光传播速度小)时，反射光有半波损失。由于本文设计的增透膜折射率关系式：$n_1<n_0<n_2$，所以光从 n_1 到 n_0 和 n_0 到 n_2 的反射有半波损失，因此光波 1 和 3 都经历了半波损失，互相抵消。继而得到单层增透膜的厚度 $d=(2k+1)\dfrac{\lambda}{4n_1}$，其中 k 为任一自然数，λ 为光在真空中的波长，本文中设置为 0.6μm。

⑵ 光生载流子的收集效率主要是受到器件电场分布和材料内部的复合中心的密度决定的，由于载流子的渡越时间一般小于载流子的复合寿命，因此载流子的收集效率一般认为是 1 [4,5]。

⑶ 吸收层材料的光吸收系数：本文的吸收材料为 Ge 材料，影响其吸收系数的主要是材料的应力，当 Ge 材料没有受到应力作用时，吸收系数为 840 /cm @1550nm，当受到 0.25% 的张应力时，材料的吸收系数提升到 4570 /cm @1550nm [6]。由于本器件采用 SOI 这种柔性衬底，可以有效降低外延层的应力[7,8,9]，本文的模拟中 Ge 材料在 1550nm 波段的吸收系数约为 1000/cm[10,11,12]。

⑷ 光吸收长度：本文利用 SOI 衬底的 BOX 与 Si 材料的之间的大折射率差，将透射到衬底未被吸收的光反射回到吸收层，提高光的吸收长度，从而提高响应度，图 2-5 是利用 FDTD solution 模拟的有 BOX 和无 BOX 的结构的 UTC 器件内部的光强度分布，可以看到 BOX 层插入可以将透射到 Si 层未被吸收的光反射到 Ge 吸收层被进一步吸收，同时还与入射的光发生相干作用，在各层中形成明暗交替的相干条纹，增强光反射和光吸收。光吸收效率由通常的 $P_{ab}=P_0\,(1-e^{-aD})$，进一步增大到 $P_{ab}=P_0\,(1-e^{-aD}) + P_0{\cdot}e^{-aD}{\cdot}R_{ref}{\cdot}(1-e^{-aD})$ 获得更高光吸收效率。

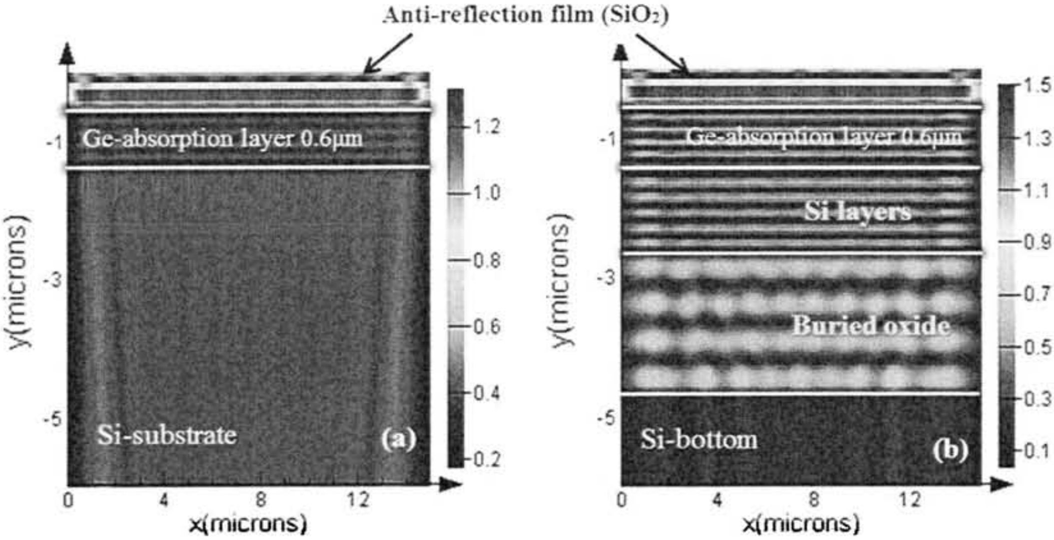

图 2-5 FDTD solution 模拟得到 SOI 衬底的 BOX 层反射的光与入射的光发生相干效应，形成明暗交替的波纹，同时看到 Si 底部漏光强度，SOI 衬底也远小于 Si 衬底。

定量的计算需要将传输矩阵法（SMM）将介质前后空间的电磁场联系起来，计算整个系统光透射率与 Si 材料层厚度 x 以及 BOX 层厚度 y 之间的关系，得到光吸收效率。

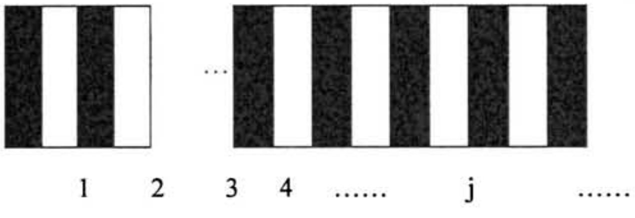

图 2-6 多层周期性交替排列介质

传输矩阵法多应用于多层周期性交替排列介质（如图 2-10 所示）， M(z)为传输矩阵，反映的介质前后空间电磁场之间的关系，而其实质是每层薄膜特征矩阵的乘积，若用 M_j 表示第 j 层的特征矩阵，则有[13]：

$$M(z)=\prod_{j=1}^{N}M_j=\begin{bmatrix} A & C \\ B & D \end{bmatrix} \tag{2-4}$$

$$M_j=\begin{bmatrix} \cos\delta_j & \dfrac{i}{\eta_j}\sin\delta_j \\ i\eta_j\sin\delta_j & \cos\delta_j \end{bmatrix} \tag{2-5}$$

其中 δ_j 为相位厚度，有 $\delta_j=\dfrac{2\pi}{\lambda}N_j d_j\cos\theta_j$ (2-6)

M_j 的表示为一个 2×2 的矩阵形式，其中每个矩阵元都没有任何实际物理意义，它只是一个计算结果。以薄膜光学理论，以及麦克斯韦方程组及边界条件得到，透射薄膜的特征矩阵中，N_j 为第 j 层介质的复折射率，d_j 为第 j 层介质的厚度，θ_j 为入射角，η_j 为修正导纳，对于垂直入射 η_j=N_j。可得一般情况下的反射、透射系数表达式：

$$r = \frac{\eta_0 - \eta_1}{\eta_0 + \eta_1} \quad t = \frac{2\eta_0}{\eta_0 + \eta_1} \tag{2-7}$$

对于垂直入射型 Ge/Si UTC 器件（如图 2-1），入射光波依次通过空气层、SiO_2 层、Ge 层（0.6μm）、Si 层（x μm）、BOX 层（y μm）、Si 层（340 μm）计算最小的透射率与反射率之和，入射光波长为 1550nm，锗在该波长的吸收系数为 1000/cm，可得到器件最大的吸收效率约为 0.176，此时的 Si 层厚度为 1.1μm，BOX 层厚度为 1.85 μm，相较于无 BOX 结构，吸收效率提高 1.5 倍。由于 SOI 衬底规格有一系列标准，选定的 BOX 厚度为 2μm，通过 SMM 计算得到 Si 层厚度与光吸收效率的关系如图 2-7（b），Si 材料的厚度对吸收效率的影响呈现周期性能，最高的吸收效率为 0.167，Si 材料厚度周期为 0.223μ。

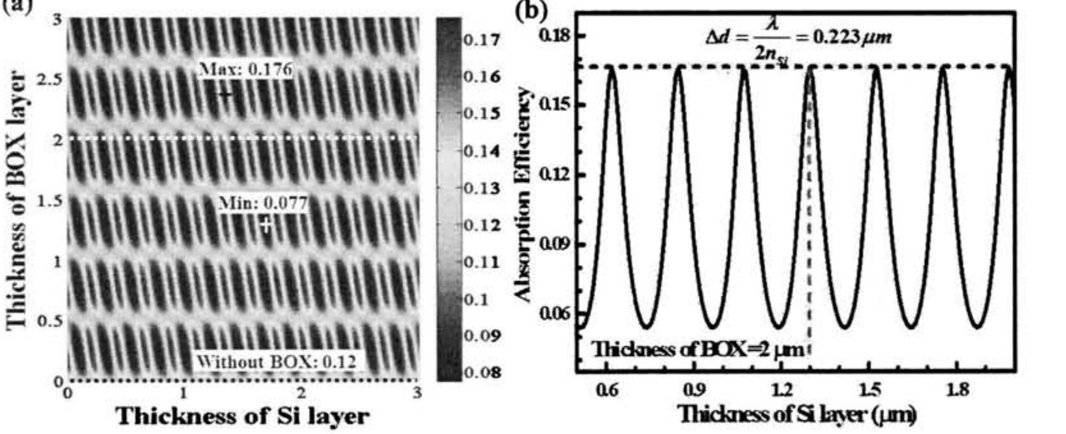

图 2-7 (a) 吸收效率与 BOX 层和 Si 材料层厚度之间的关系，(b) 将 BOX 层的厚度设置为 2μm，Si 层与吸收效率之间的关系曲线。

2.2 高响应度硅基锗 UTC 探测器的制备

2.2.1 低高温两步法生长 Si 基 Ge 薄膜

Ge、Si 的{100}、{110}晶向的表面能分别为 $\sigma_{Ge\{100\}}$=1835erg/cm^2、$\sigma_{Ge\{110\}}$=1300erg/cm^2、$\sigma_{Si\{100\}}$=2130erg/cm^2、$\sigma_{Si\{110\}}$=1510erg/cm^2（1erg=100nJ），因此 Ge 可以浸润 Si 表面[14]；另一方面 Ge/Si 之间的晶格失配为 4.18%，因此 Ge/Si 异质外延以 SK 模式进行。

Ge/Si 外延的 SK 转变发生之后，将主要形成两种位错，一种是在 Ge/Si 界面形成的失配位错（如图 2-8(a)），另一种是在 Ge 薄膜中形成的穿透位错（如图 2-8(b)）。失配位错是主要的释放应变能机制；穿透位错是形成失配位错的副产物[15]。位错只有在遇到表面、或者自身形成位错环时才能终结，而外延膜表面是最接近衬底的自由表面，因此穿透位错存在于整个 Ge 外延膜中、一般是从 Ge/Si 界面开始到 Ge 表面结束。

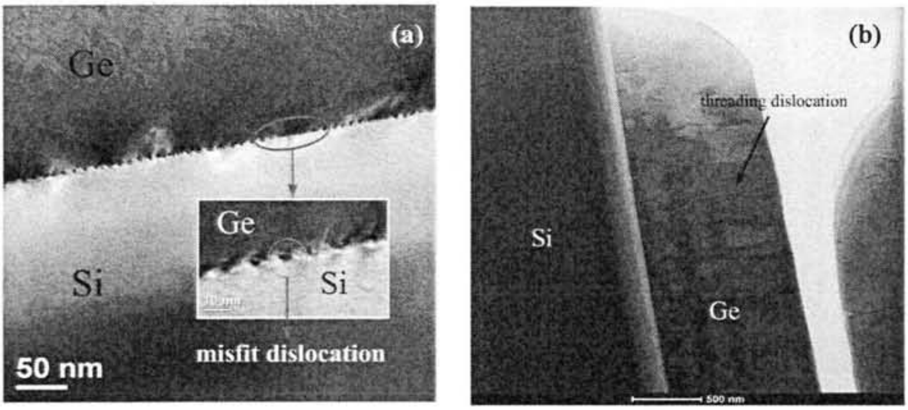

图 2-8 Ge/Si(001)外延膜的两种位错。(a) Ge/Si 界面的失配位错（misfit dislocation）；(b) Ge 薄膜中的穿透位错（threading dislocation）

由于 Si 和 Ge 室温下的晶格失配率约为 4.18%，并且会随温度的增加而继续增大[16]，使得在 Si 衬底上外延生长高质量的 Ge 材料，成为了一项重大的挑战。为了降低晶格失配，跟中科院半导体所合作采用高温 Ge 缓冲层[17]的外延生长方法。首先在 400℃以下的温度下生长出应力弛豫的 Ge Buffer 层，然后将衬底温度提高到 600℃左右，生长合适厚度的 Ge 层。生长后，为了提高材料质量，可以进行循环退火处理。最终获得的材料的位错密度在 107cm^2 量级的水平，表面的平整度也比较好。其中前两种工艺比较复杂，而且生长材料过渡层比较厚，不太适合集成器件的研制，而低温 Buffer 层技术工艺比较简单，过渡层薄，材料表面平整，成为目前 Si 衬底上 Ge 材料生长的主要方法。

本文所使用的样品便是采用低高温两步法生长的 Ge 外延膜。具体生长步骤如下：

1) 清洗 SOI(100)衬底；
2) SOI(100)衬底在分析室中除气，然后在生长室中脱氧；
3) 270°C 下使用高纯 GeH_4 生长 60nm 厚的 Ge 缓冲层；
4) 600°C 下使用高纯 GeH_4 生长 Ge 薄膜，同时通入 B_2H_6 气体进行原味掺杂.

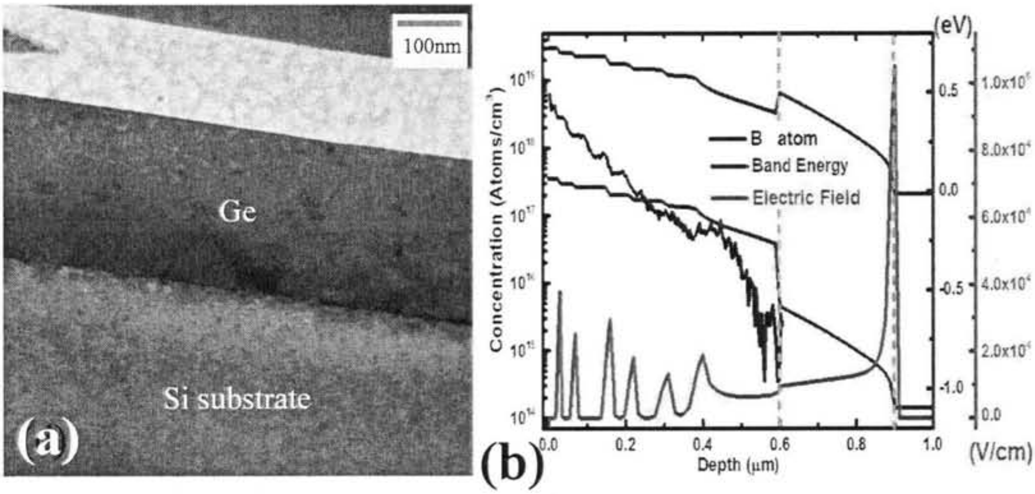

图 2-9 (a) Ge/Si 外延膜的 TEM 图样；(b) 利用 SIMS 测得 Ge 吸收层中 B 原子的分布，同时利用 silvaco 模拟此杂质分布下器件内部的能带结构和电场分布。

2.2.2 双台面器件结构加工

通过微纳加工将样品分成直径为 15/18/20/25/30/40/50/60/70/80/90/100/150/200μm 不同尺寸的圆台型垂直入射器件。具体工艺如下：

1) 离子注入 BF^{2+}，剂量(Dose)为 $4\times10^{15}cm^{-2}$，能量(Energy)为 30keV，在 Ge 表面形成高掺杂的 P+型接触层。

2) 退火激活离子注入。

3) 样品清洗。由于 Ge/Si 材料的特殊性，清洗时不可以用强酸、强碱以及强氧化性的化学试剂进行清洗，否则会将样品彻底损坏。所以，本论文中涉及到的所有 Ge/Si 样品，全部都是通过离子水→乙醇→丙酮→乙醇→去离子水，进行循环清洗。

4) 光刻 M1 版，形成各个尺寸的圆台。

5) 利用 Alcatel 601E 硅 ICP 刻蚀机，shallow2 程序设置参数，刻蚀深度 0.85-0.95μm 之间，到达 Si 重掺杂接触层。一般 ICP 刻蚀存在均匀性误差，样品中心和样品边缘刻蚀深度误差在 100nm 左右，随着刻蚀材料的均匀性不同，刻蚀参数设置的不同，这个误差值会增大或减小，但是无法消除。

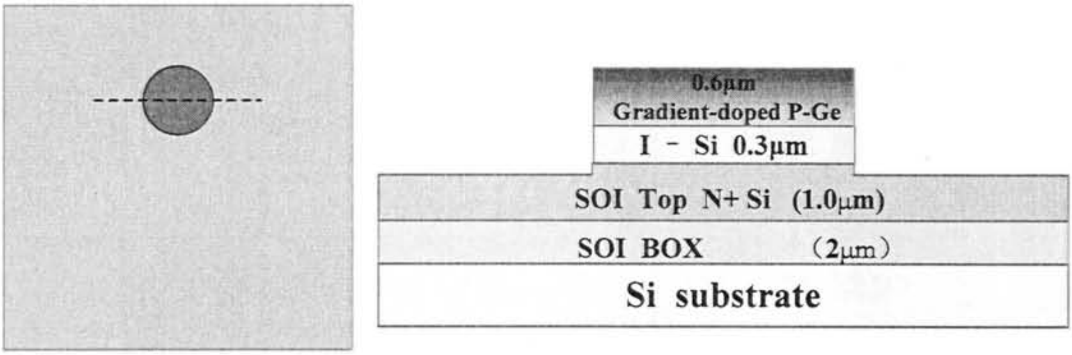

图 2-10 光刻版 M1，刻蚀上圆台

6) 套刻 M2 版，在上圆台外围形成下电极台面。

7) 利用 Alcatel 601E 硅 ICP 刻蚀机，shallow2 程序设置参数，刻蚀深度 1.0μm 左右，刻蚀到氧化绝缘层。

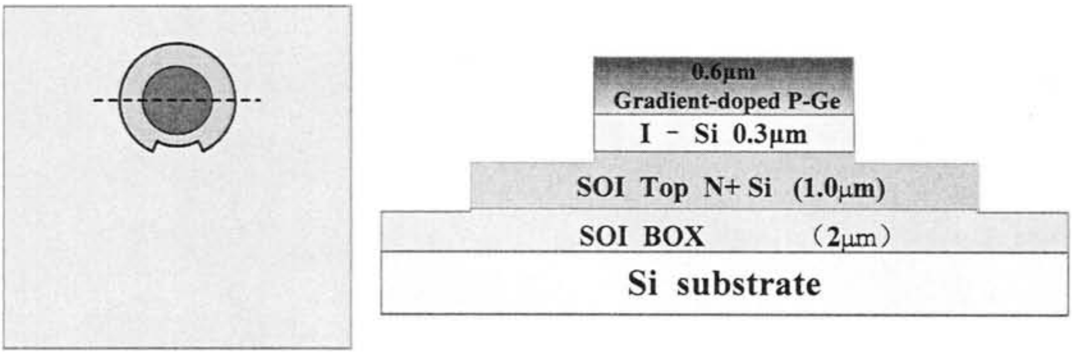

图 2-11 套刻版 M2，形成下电极台面

8) 套刻 M3 版，将下电极位置空出，其他位置涂胶。

9) 蒸发下电极金属 Ni/Al=100/250nm。

10) 带胶剥离下电极。

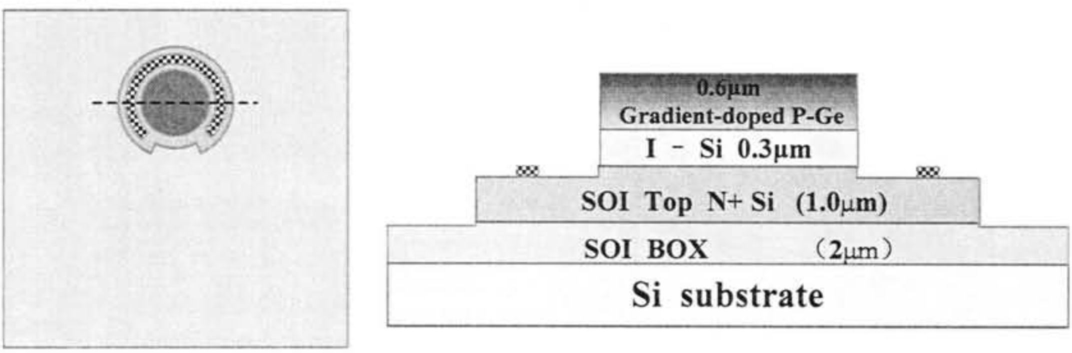

图 2-12 套刻版 M3，蒸发下电极

11) 退火合金。

12) 套刻 M5 版，将上电极位置空出，其他位置用胶覆盖。

13) 蒸发下电极金属 Ni/Al=50/350nm。

14) 带胶剥离下电极。

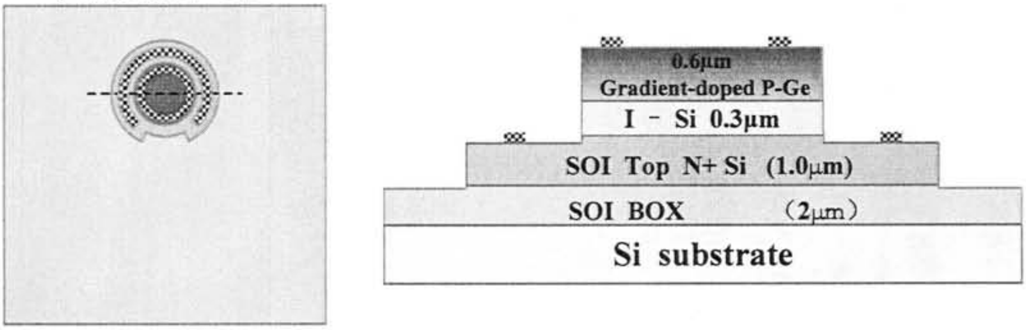

图 2-13 套刻版 M5，剥离形成上电极

15) 退火合金。

16) PECVD 沉淀 Si_3N_4 600nm 左右，钝化器件表面。

17) 套刻 M6 版，将上、下电极位置空出，其他位置用胶覆盖。

18) ICP 刻蚀 Si_3N_4 600nm，过刻蚀，将电极露出。

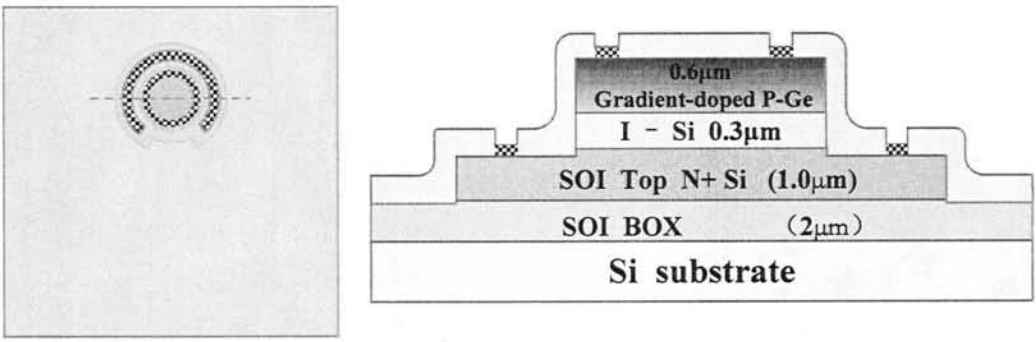

图 2-14 套刻版 M6，刻蚀钝化层，露出上下电极

19) 光刻 M7，将生长 pad 电极的区域暴露出来。

20) 沉积金属，剥离。

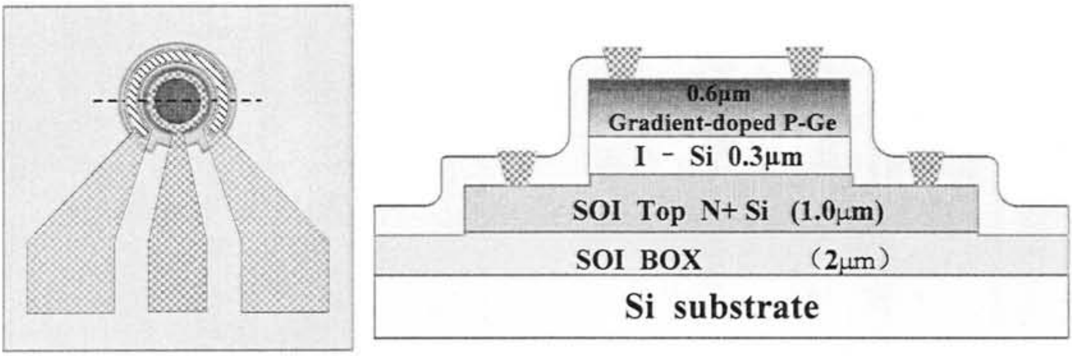

图 2-15 套刻版 M7，蒸发 pad 电极。

21) PECVD SiO_2，550nm。

22) M8 将电极测试点暴露出来。

23) 刻蚀 SiO_2，550nm，过刻蚀，到达电极层。

作用：将 Pad 电极用氧化层覆盖，防止金属电极与空气接触氧化，增大电极电阻。

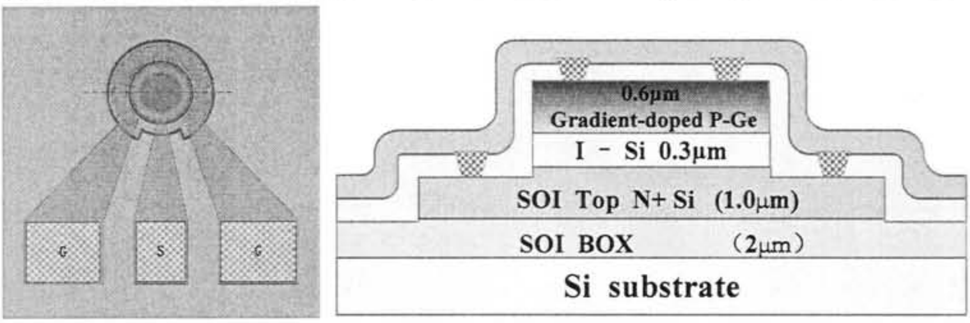

图 2-16 套刻版 M8，露出电极测试点。

2.2.3 器件工艺结果

通过以上的材料外延和 CMOS 工艺加工，得到垂直入射型 Ge/Si UTC 器件，直径为 15μm 的单元器件的俯视图如**错误!未找到引用源。**。可以看到，器件上电极采用开放式的半环，以提高小尺寸器件电极剥离成品率。

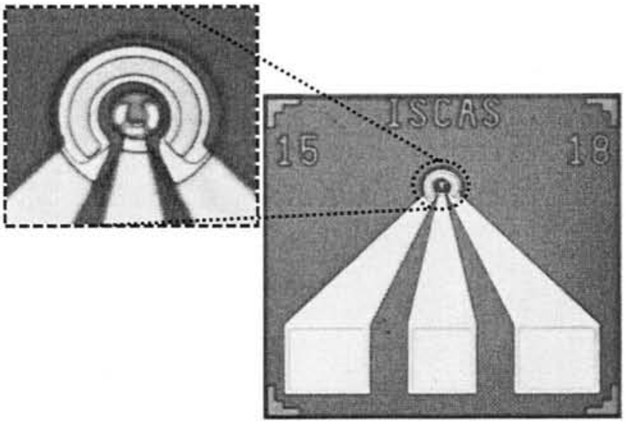

图 2-17 直径为 15μm 的器件的俯视图。

对于此批器件圆台直径低于 25μm 的器件，上电极圆环均采用开放式的马蹄铁形状。原因：光刻 M5 版（上电极图形）时，样品表面已经刻蚀上下台面，且上台面与样品底面存在 1.0μm 左右的台面高度差，造成光刻匀胶时上台面光刻胶厚度远小于样品底面，通常带胶剥离要求光刻胶的厚度至少是金属厚度三倍以上，才有可能全部剥离，特别是在封闭图形（如圆环）以及图形间距很小的情况下，光刻胶的厚度要求更高。举例说明：SUSS Delta80 匀胶机 3000 转 40s，在无图形光滑晶片上旋转涂附正胶 AZ6130，样品中心区域胶的厚度在 2.3μm 左右。如果晶片上已有圆台型图形，图形的上下台面有 1.5μm 高度差，则涂胶后晶片上台面中心处的胶厚降为 1.5μm 左右，胶的厚度会随着台面尺寸的减小而减薄，且圆台的中心区域最薄，此时对于上台面封闭圆环内部的金属根本无法剥离，因此选用了开放式马蹄铁形上电极，实验证明，改进的电极图形不仅未影响器件性能，还大大提高了小尺寸器件的成品率。

2.3 高响应度硅基锗 UTC 探测器的性能分析

完成了器件微纳加工工艺后，要对器件的电学以及光学性能进行表征，由本文第二章第一部分的分析可知，表征一个探测器性能好坏的参数有：暗电流 I-V 曲线，光电流 I-V 曲线，器件电容 C-V 曲线，以及器件带宽的输出功率-频率曲线。本实验室使用探针台进行 I-V 和 C-V 曲线电数据提取工作，使用 Agilent B1500A 进行数据的现实和分析。

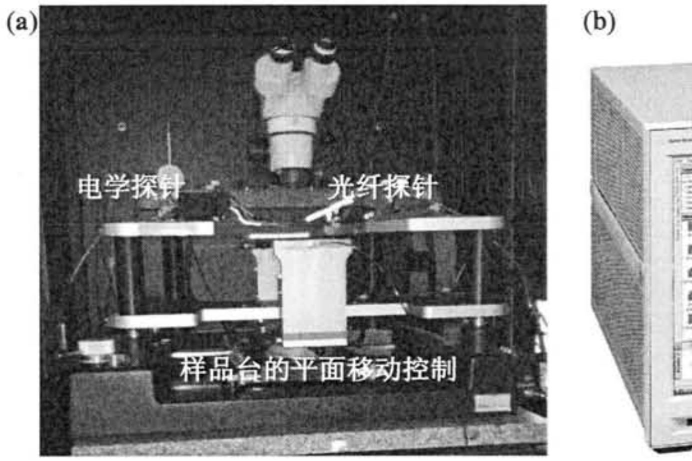

图 2-18 I-V 测试所用(a)探针台和(b)数据分析仪示意图

2.3.1 暗电流特性

通过测试得到各个尺寸器件的暗电流 I-V 曲线，如图 2-19 所示，器件表现出良好的二极管特性。器件圆台直径为 15μm，其在-1V 偏压下的暗电流为 58 nA，暗电流密度为 96.3 mA/cm^2；直径为 30μm 的器件的暗电流密度为 61.9 mA/cm^2。

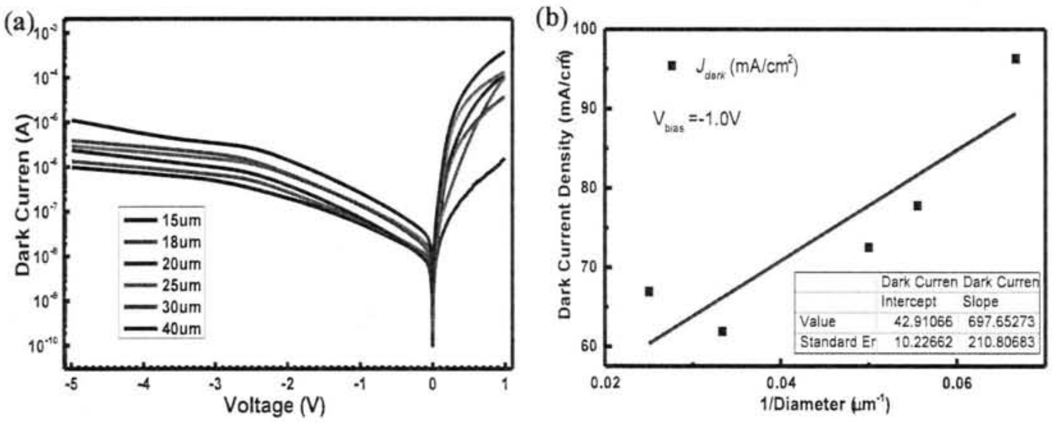

图 2-19 垂直入射型 Ge/Si UTC 各尺寸的暗电流的 I-V 特性； (b) 各尺寸器件暗电流密度与圆台直径的倒数 1/D 的关系。

由图可见，器件的暗电流密度随着器件尺寸增大而减小的，暗电流可写为[18]：

$$I_d = J_{bulk} \times \pi(\frac{D}{2})^2 + J_{surf} \times \pi D \tag{2-8}$$

$$J_d = J_{bulk} + J_{surf} \times \frac{4}{D} \tag{2-9}$$

理想情况下，器件的暗电流与 1/D（即器件直径的倒数）呈线性关系。**错误!未找到引用源。**标示出了不同尺寸器件（1/D）对应的暗电流密度，并得到以 1/D 为变量的一次方程的拟合曲线。直线的纵轴截距为器件的体暗电流密度，斜率为器件的侧壁漏电流线密度。得到 Ge/Si UTC 器件的体电流密度为 42.9 mA/cm^2，器件的线电流密度为 10.2 μA/cm。对于 Ge/Si 半导体器件而言，器件的体暗电流主要是源于晶格失配形成的线位错，其值正比于线位错密度 N_{TDD}。因此减小线位错密度，提高 Ge 外延层晶体质量是降低器件暗电流有效方法。

2.3.2 器件光响应特性

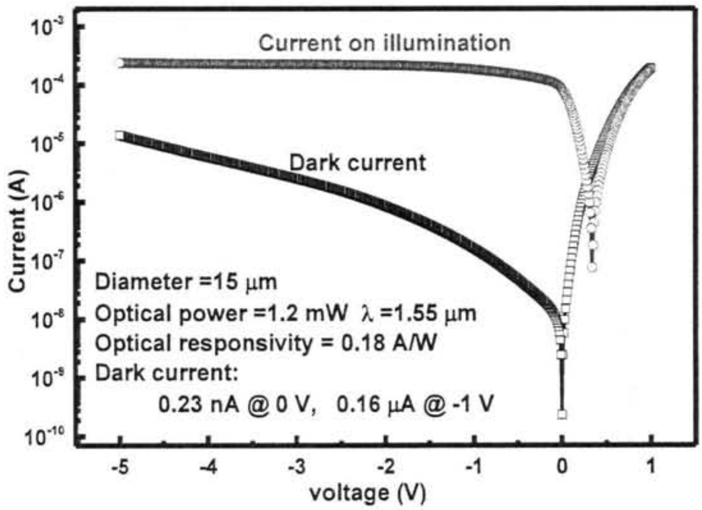

图 2-20 直径为 15μm 器件的光响应特性。

器件的光响应测试是利用 JWD1100 直流光源发射波长为 1550nm 的直流光信号，通过出射孔径为 9μm 的单模光纤探针导入到垂直型器件的通光孔上，并通过直流探针以及电学分析仪对输出信号进行检测。入射的光功率为 1.2mW，直径为 15μm 器件光/暗电流随偏压的变化曲线如图 2-20。器件在-1V 偏压下的光电流约为 0.216mA，对应的光响应 R 为 0.18A/W，量子效率为 14.4%。同时在图中可看到，在零偏压下的光电流与反偏电压下的相近，说明器件能在零偏压的条件下正常工作。

2.3.3 器件的频率特性

入射光的波长为 1550nm，光功率为 0.5mW，通过调制器调制入射光频率，将一定调制频率的光入射到光电探测器上，读取探测器的输出功率。对输出光功率进行归一化处理，得到调制频率与归一化输出功率的关系曲线（如**错误!未找到引用源。**）。当输出光响应功率

降为未调制（或低频调制）输出功率的一半（即-3dB）时，此时光调制频率为该探测器的截止频率。

UTC 结构探测器器件的 3-dB 带宽可以通过公式计算获得近似结果。假如取器件的负载电阻 R_L=50Ω，Ge 材料电子的饱和漂移速度 v_{th}=6×10^6 cm/s，Ge 的相对介电常数为 16.2，真空介电常数为 8.85418×10^{14} F/cm，由公式(2-1)、(2-2)和(2-3)可以得到理想状态下（即 R_s=0Ω，电容为结电容，不考虑其他寄生电容）不同尺寸的 UTC 结构器件耗尽层宽度与 3-dB 带宽的关系曲线（如图 2-21），同时图中也标出了器件的实际带宽。实际的器件内部存在欧姆接触电阻，结电阻，扩散电阻等内部电阻，器件侧壁及衬底等也存在着一定的寄生电容，以及测试误差等造成了实际器件的带宽要低于理论值。

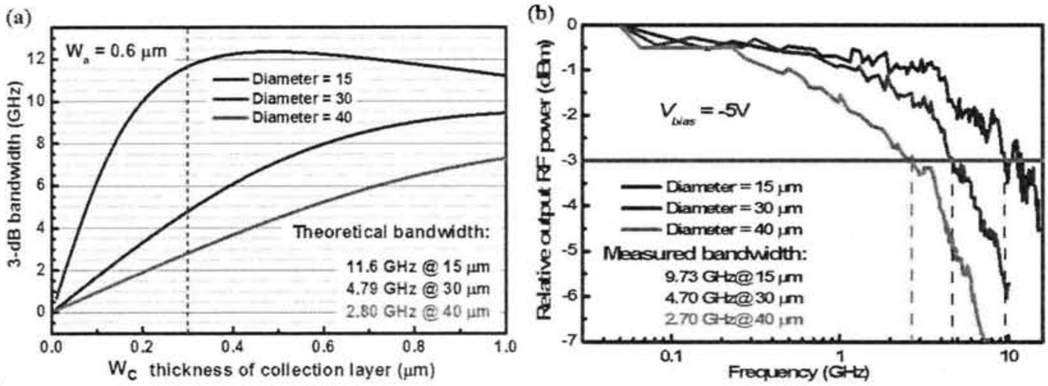

图 2-21 直径为 15μm，30μm 以及 40μm 器件在-5V 偏压下的 3-dB 带宽与理论计算的带宽对比。

2.3.4 饱和度特性

饱和度主要受到负载电阻的电压降低、收集区的空间电荷效应以及热效应的限制。探测器上的电压可写为：

$$V_{PD} = V_{bias} - I_{dc}R_s - I_{ac}\left(R_L + R_s\right)\Big/\sqrt{1+\left(2\pi fRC\right)^2} \tag{2-10}$$

其中，I_{ac} 为时变光电流，I_{dc} 为时间平均光电流，R_L 为负载电阻，R_S 为串联电阻。

空间电荷效应是未屏蔽负电荷的存在拉低了影响收集区电场，一旦电流密度达到足够高的量时，收集区的电场将会崩溃。通过解泊松方程可得到最大电流密度：

$$J_{\max} = \frac{2\varepsilon_{Si}v_n}{w_c^2}\left(V_{bi} + V_{PD} - E_{crit}w_c + \frac{qw_c^2}{2\varepsilon_{Si}}N_{DC}\right) \tag{2-11}$$

其中，ε_{Si} 为硅的介电常数，v_n 为电子的饱和漂移速率（~10^{7}cm/s），w_c 为收集区的宽

度，V_{bi}为内建电势，E_{cirt}为电子未饱和时的电场强度（35kV/cm @Si），N_{DC}为收集区的施主浓度。稍高于最大电流密度时，收集区电场趋近于 0，无电流被收集。

利用矢量网络分析设备分别测试直径为 40 μm 和 18 μm 在不同偏压和不同光入射功率下的 RF 功率，测试结果如图 2-22 所示，直径 40μm 器件，带宽 2.55GHz，在 1GHz 的调制频率下，饱和输出射频为 4.6 dBmW，对应的饱和电流为 16.24mA；直径 18μm 器件，带宽 7.23GHz，在 3GHz 的调制频率下，饱和输出射频为 3.7 dBmW，对应的饱和电流为 16.22mA。

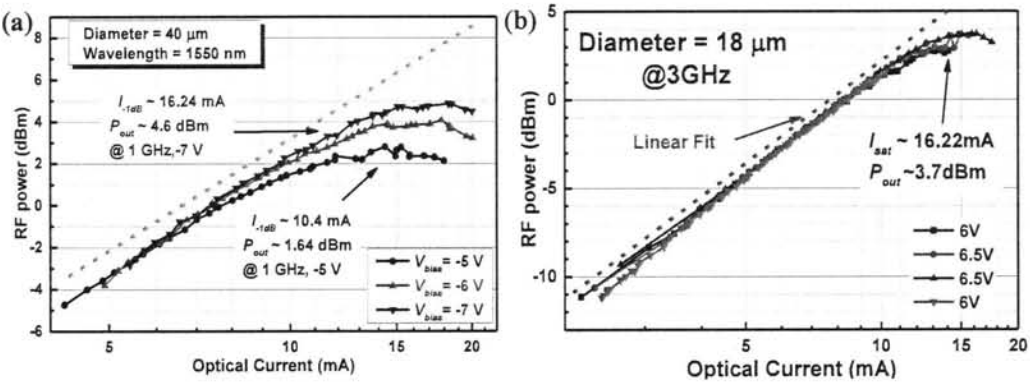

图 2-22 直径为 15μm 和 40μm 器件在不同偏压下的饱和性能。

2.4 本章小结

本章首先介绍了垂直入射型 Ge/Si UTC 探测器的发展现状，其次介绍器件的电学和光学设计，包括缩短载流子渡越时间以及增大光吸收效率，接着通过原位掺杂的高低温异质外延方法以及与 CMOS 兼容的半导体加工工艺，制备出不同尺寸的台面型垂直入射 Ge/Si UTC 探测器，最后对完成的器件进行性能表征，器件的暗电流密度(~61.9 mA/cm^2@-1V)，将器件的光响应提高到 0.18A/W，直径 15μm 器件带宽为 9.73GHz，同时器件具有良好的饱和度特性，直径 18μm 器件，在 3GHz 的调制频率下，饱和输出射频为 3.7 dBmW，对应的饱和电流为 16.22mA。

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第三章 高灵敏 Ge/Si 波导吸收倍增分离型雪崩光电探测器

随着信息科学和网络急速的迅速发展，人们对传输比特率，传输波长，长距离或长中继器(repeater)间距等提出了更高的要求[1]。中继器，又被叫做再生放大器，工作于 OSI 的物理层，是局域网上所有节点的中心，它的作用是将光信号转化为电信号，进行复制、调整和放大，以此补偿信号衰减延长网络间隔长度。由于信息传输存在损耗，在光纤中传输的信号功率会逐渐衰减，衰减到一定程度时将造成信号失真，因此会导致接收错误。中继器就是为解决这一问题而设计的。它完成物理线路的连接，对衰减的信号进行放大，保持与原数据相同。在网络传输中，减少中继器的数量可以扩展系统比特率容限，提高传输距离，增强可靠性，降低系统维护费，进而降低整个网络花费[2, 3, 4]。

网络中继器之间的间隔距离是由发送系统(transmitter)、光纤损耗、光纤连接器损耗以及接收器灵敏度共同决定的。图 3-1 给出了在光连接系统中各组成部分对光衰减的影响。其中接收器耦合损耗容差（Link loss budget）是由接收器前端输入的光功率减去接收器的灵敏度计算得到的，由系统各组成原件的质量，寿命、稳定性以及温度等因素决定的。

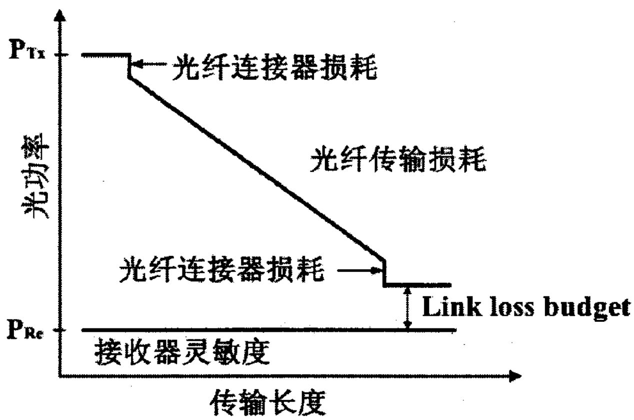


图 3-1 在光联接中损耗分布

随着信息科学和网络技术的发展，人们对于接收器的带宽要求越来越高，由 PIN 结构探测器分析可知，光信息的调制频率越高，长距离通信的损耗就越大，器件的可接收最小光功率就越越大，为了满足现今的长距离通信系统中高灵敏度要求，雪崩探测器(avalanche photodetectors, APDs)成为又一研究重点。

雪崩探测器内部部分电场要远高于普通的 PIN 器件，在该高场区的载流子发生雪崩倍增效应，形成光生载流子的内部增益，因而在相同光电流的输出情况下，雪崩探测器的入射光功率更小。统计结果显示，商用的雪崩二极管的灵敏度高于普通二极管 10dB 左右[5]，

在保证高比特率的同时中继器最大间隔增大了 50km，减少了光通信网络中中继器的使用，降低成本。但是，雪崩探测器倍增效应会增大器件的噪声，降低器件灵敏度。因此研究低噪声，高灵敏度的 APD 成为长波长红外通信系统重点研究方向。

3.1 新型 Ge/Si 波导雪崩光电探测器

3.1.1 新型纳米 Ge/Si WG SAM-APD 结构

基于高质量 Ge 单晶纳米条形结构的选择外延方法，结合纵向 Ge 吸收和横向 Si 倍增结构设计，我提出了一种新的纳米条形 Ge 纵向吸收、Si 波导层横向单侧倍增的波导 Si/Ge SAM-APD 结构，能够突破现有雪崩光电探测器由光学耦合吸收方向与雪崩倍增方向一致所导致的光学与电学性能相互制约问题，解决高效率光响应与高效率载流子倍增之间对器件结构要求的矛盾，具体结构如图 3-2 所示，具体优点和特点分析如下：

图 3-2 提出的纳米尺度波导 Si/Ge SAM-APD 器件结构示意图。

1. 采用Si 基单模波导到Ge吸收层的直接倏逝波耦合，消除传统波导器件前端的taper波导或多模波导等光耦合组件损耗，增大入射光强，并使光强中心集中于Ge吸收层边沿附近，增加单位长度下的倏逝波耦合效率，并且通过优化吸收区与电荷区电场设计，获得高的光生载流子收集效率和高的器件的光响应度。采用位于Si波导层的横向单侧倍增区，载流子倍增长度由现有的Si材料纵向厚度变为波导层的横向宽度，倍增层的厚度不再受到耦合效率的限制，增大器件电学结构设计的自由度，优化器件的倍增性能。因此本课题研究器件能够同时实现高的光响应和高效率倍增。

2. 将Ge吸收层的宽度缩小到纳米量级，能够在保证单位耦合效率的同时降低异质结截面积（$A\downarrow$），而且有利于将晶格失配造成的应变弛豫向材料边缘扩散并释放，晶格质量将远高于大尺寸选择外延材料，降低异质结界面处缺陷态引入的单位暗电流密度（$J_{dark}\downarrow$）和面积噪声，因此大大减小了器件的体暗电流（$I_{dark}= A\cdot J_{dark}$）。由于该部分暗电流会随雪崩效应发生倍增，因此减小Ge吸收层宽度，可以有效增大器件信噪比，优化灵敏度特性。

3. 将Ge吸收层的宽度缩小到纳米量级，有利于pn结界面的电场从倍增区向电荷区和

吸收层扩展，将电荷区和吸收层完全耗尽，载流子的输运方式由微米尺度结构的扩散运动转变为纳米尺度下的漂移运动，将大大减小载流子的渡越时间，从而提高了器件的频率响应。

4. 单侧Si材料倍增区，将载流子的输运和倍增通道确定并唯一，避免两侧相互独立且结构不严格相同的倍增区中，光生载流子随机选择不同的输运和倍增通道所引发的倍增系数（*M*）浮动现象，进一步提高器件性能。

5. 器件制备仅需一次的材料外延，有效简化制备工艺，与传统的CMOS工艺兼容，降低成本，工艺容差大，便于实现高性能。

因此，我们相信此新型的波导纳米级 Si/Ge SAM-APD 器件，不仅能够满足高耦合效率的光场设计要求，同时能够满足大倍增系数的电场设计要求，在实现高耦合效率高响应的同时具有低噪声和大带宽特性，能实现高灵敏度大带宽探测。

3.1.2 APD 探测器关键参数

1. 雪崩倍增因子 M

APD 的倍增因子 M 定义为

$$M=\frac{I_{ev}}{I_0} \tag{3-1}$$

其中 I_{ev} 是 APD 的输出平均信号电流，I_0 是平均一次信号电流。在 APD 中由于不可避免地伴随着噪声，倍增因子是在一个平均值上发生着随机起伏的量，上式的定义应理解为统计平均倍增因子。空穴电流增量等于在 dx 距离内每秒产生的电子-空穴对数目。我们可以通过以下的速率方程来求得 APD 的倍增系数。

$$dI_{APD}=\alpha I_n dx+\beta I_p dx \tag{3-2}$$

这里 I_n 和 I_p 分别为电子电流和空穴电流，α 和 β 为电子和空穴的碰撞离化系数。在 APD 的增益区内，稳态总电流 $I=I_n(x)+I_p(x)$ 应该保持不变，则式是(2-12)变

$$\frac{dI_{APD}}{dx}=(\alpha\text{-}\beta)I_n+\beta I \tag{3-3}$$

一般情况下，若增益区内的电场均匀，则 α 和 β 与 x 无关，如果再假设 α>β，考虑到雪崩过程是在厚度为 W_d 的增益区上 x=0 处开始，可以利用边界条件 $I_{APD}(W_d)=0$ 和 $I_{APD}(W_d)=I$。则由(2-13)式可以得到倍增因子的表示式

$$M=\frac{I_{APD}(W_d)}{I_0(0)}=\frac{1-\beta/\alpha}{\exp[-(\alpha-\beta)\mathrm{W}_d]-\beta/\alpha} \tag{3-4}$$

可见，APD 的倍增因子与碰撞电离系数的比值 β/α 有很大关系，当只有电子参加碰撞电离倍增过程时，$\beta=0$，这时 $M=exp(\alpha W_d)$，因此 APD 的倍增因子随 W_d 按指数增加。如果 $\alpha\approx\beta$，则用 $(1-(\alpha-\beta)W_d)$ 代替(2-14)式中的 $exp[-(\alpha-\beta)W_d]$，得到：

$$M=\frac{1}{1-\alpha W_d} \tag{3-5}$$

在 $\alpha W_d=1$ 时此公式失效，称为雪崩失效条件。尽管在 α 和 β 相近的情况下可以以很窄的增益区厚度获得较高的增益因子，但是在 α 和 β 较接近的情况下 APD 的响应带宽将大大减小，并且噪声很高，所以实际应用中采用电离系数比远小于 1 的（即 $\alpha>>\beta$ 或 $\beta>>\alpha$）材料，如本文中采用的 Si 材料。

2. **击穿电压（V_{BD}）**

雪崩击穿电压定义为当放大倍数趋近于无限大（∞）时对应的电压值。用电离积分表示的击穿条件为：

$$\int_0^{W_d}\alpha\exp[-\int_x^{W_d}(\alpha-\beta)dx']dx=1 \tag{3-6}$$

上式表示的是雪崩过程由电子引发的，若雪崩过程由空穴引发的表达式是等效的。因为击穿仅取决于耗尽区内发生了什么，与最初引发雪崩过程的载流子类型无关。

实验中，通常把 APD 器件的暗电流为 100μA 时的器件偏压看作是该器件的击穿电压 V_{BD}。

3. **过剩噪声**

对一个性能良好的光接收器而言，要求有尽可能高的接收灵敏度或尽可能低的最小可探测功率(即达到误码率为 10^{-9} 时所需的最小入射光功率)。对于 PIN 光探测器，影响其探测灵敏度的主要噪声源是来自于跟随其后的放大器的热噪声。而在具有内部增益的 APD 中，光接收器不再受外部放大器热噪声的限制，所以光生载流子的雪崩倍增作用成为了提高灵敏度的一个有效途径。由于单个粒子的碰撞电离行为不确定，所以整个雪崩过程的增益是不确定的，具有随机性。这种雪崩增益的随机性称为过剩噪声，以区别光电二极管固有的热噪声。过剩噪声可以引起接收器误码率的上升和灵敏度的下降。因雪崩增益有起伏，增益的均方根 $\langle M^2\rangle$ 大于其平均值的平方 $\langle M\rangle^2$。过剩噪声可用噪声因子表示为[6]:

$$F(M) \equiv \frac{\langle M^2 \rangle}{\langle M \rangle^2} = \frac{\langle M^2 \rangle}{M^2} \tag{3-7}$$

噪声因子是与理想无噪声倍增情况相比的散粒噪声增量的量度，依赖于电离系数比α/β及低频倍增因子M。若α和β数值相差较大，器件能获得较好的倍增因子，噪声因子也会较小。

对于本论文所设计的吸收和倍增分离型雪崩探测器，在倍增区仅有电子注入，噪声因子可写成[错误!未定义书签。]:

$$F = M[1\text{-}(1\text{-}k)(\frac{M\text{-}1}{M})^2] \approx kM + (2\text{-}\frac{1}{M})(1\text{-}k) \tag{3-8}$$

由于只有电子注入，则k=β/α，为是过剩载流子噪声降至最小，k值要小。而对于只有空穴注入的情况，k'=α/β,为获得小的过剩噪声，要降低k'值。而Si是所知的β/α较小的材料之一，因此Si/Ge分离型雪崩探测器倍增区为Si，可有效的降低散粒噪声，增大增益。

3.2 纳米 Ge/Si WG-SAM-APD 器件的光学结构设计

垂直入射型器件的响应度受到通过孔径和吸收区厚度的限制，而端面入射由于吸收长度等于器件长度，因此其相应的主要受到端面的透射吸收的限制。理论上相同的响应度的两种入射结构器件，端入射结构的器件尺寸要小于垂直入射器件，频率特性也更好。但是实际器件工艺中，侧入射器件的入射端面容易受到刻蚀，钝化以及划片等情况的污染，入射端面情况不易控制，成品率不高。波导耦合结构有效的避免了以上问题，同时吸收长度和载流子的渡越路径相互垂直，有利于获得高响应大带宽特性。倏逝波耦合型光电探测器完整的结构包括fiber-chip耦合端口，片上单模传输波导，波导-器件耦合端口，探测器四部分。其中fiber-chip耦合端口和波导-器件耦合端口一般利用taper波导以提高耦合效率，片上单模传输波导需要设计结构尺寸以降低传播损耗以及不必要的干扰。

3.2.1 fiber-chip 耦合设计

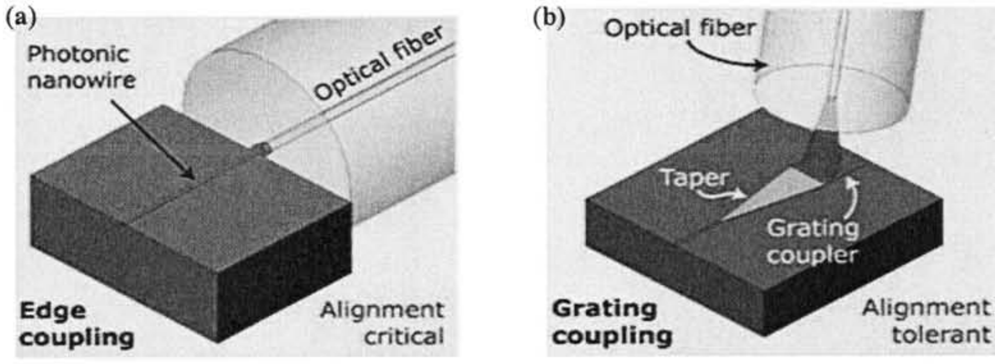


图 3-3 光纤与片上波导之间的耦合方式[7]：(a)端面耦合；(b)垂直耦合。

光纤与片上波导结构耦合的方式有两种：端面耦合(butt-coupling)和垂直耦合(Vertical-coupling)，如图 5-1 所示。端面耦合要求片上波导端面与光纤出射端口严格对准，样片端面要进行切割或抛光，且对偏振光波反应不灵敏，优点是大带宽，可耦合大调制频率的光信号。相反的，垂直耦合的对准要求不高，可直接进行片上测试，不需要切割或抛光，极化反应灵敏，但是带宽相对较小。

端面耦合实质上是一种模式转换器，一般利用锥形(taper)结构将光纤中的光模式转换到片上单模波导中。现最常用端面耦合分为三种结构[8]：横向锥体（Lateral taper)，如图 3-4；纵向锥体（Vertical taper)；横向和纵向结合型结构（Combined vertical & lateral taper)。

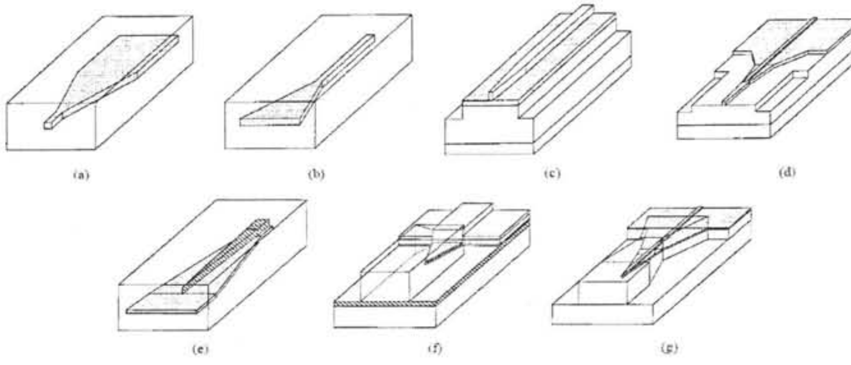


图 3-4 横向锥体设计：(a)横向倒锥掩埋波导[9]；(b)横向正锥掩埋波导[10]；(c)与耦合光纤通过横向单锥形波导与脊型波导进行模式匹配[11]；(d)通过多级锥体进行光纤波导与脊型波导的模式匹配[12]；(e) 双横向掩埋锥形波导重叠[13]；(f) 另一种双横向掩埋锥形波导重叠结构[14]；(g)通过嵌套式锥形波导将光纤波导与脊型波导模式匹配[15]。

硅基光波导常用单侧锥入射结构将脊型波导与光纤进行光场匹配[16, 17, 18]，通过 spot-size 转换器的光场匹配方式，解决了多模场尺寸不一的问题，并通过提高工艺质量降

低了由波导高折射率差造成的侧壁散射损耗。如图 3-5 为片上波导与光纤耦合端口，其中设计参数为高度 h，前端宽度 w_t，taper 长度 l_t，后端 channel 宽度 W_w 四个参数。为了实现单模传输波导（channel）的高度 h=220nm，宽度为 W_w=400nm。通过 R-soft 模拟可得到对于 TE/TM 模式 1550nm 光入射，端口耦合效率受到 w_t 的影响，当 w_t=200nm±20nm 光纤与片上波导的端耦合效率最高[16]，通过 2D FDTD solution 模拟和理论计算[19]，得到 l_t≥40μm，选用 l_t=150nm。

垂直耦合主要是光模式场匹配原理，将光耦合到多模波导中，再利用 taper 将耦合入射的光转化成单模。本文利用电磁场理论中模式展开法与等效折射率结合的方法计算与单模光纤出射光模式匹配的周期光栅结构，获得高的耦合效率。得到的耦合光栅的周期为 630nm，占空比 50%（光栅齿、光栅槽各宽 315nm），光栅槽刻蚀深度 70nm，耦合角度：8°（光纤偏离垂直方向的角度），结构剖视图如图 3-6 所示，耦合光栅长 12μm，共 20 个周期凹槽，此时的光耦合效率为 49%@1550nm。

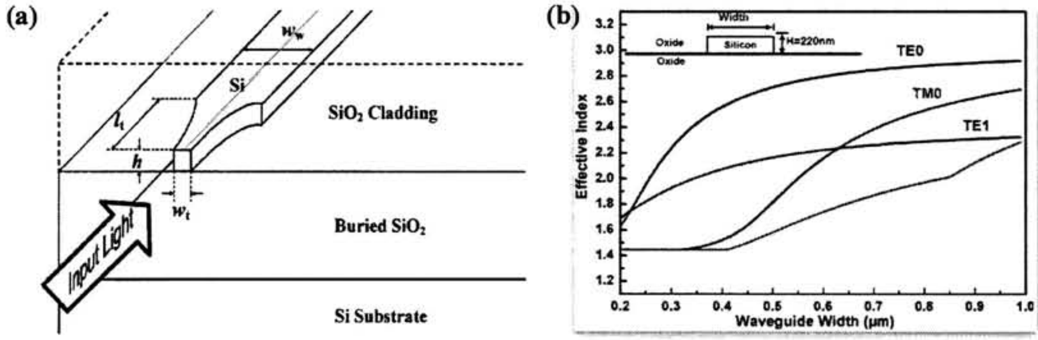


图 3-5(a)片上波导入射端口的 nanotaper 的空间视图；(b)单模光纤的尺寸选择。

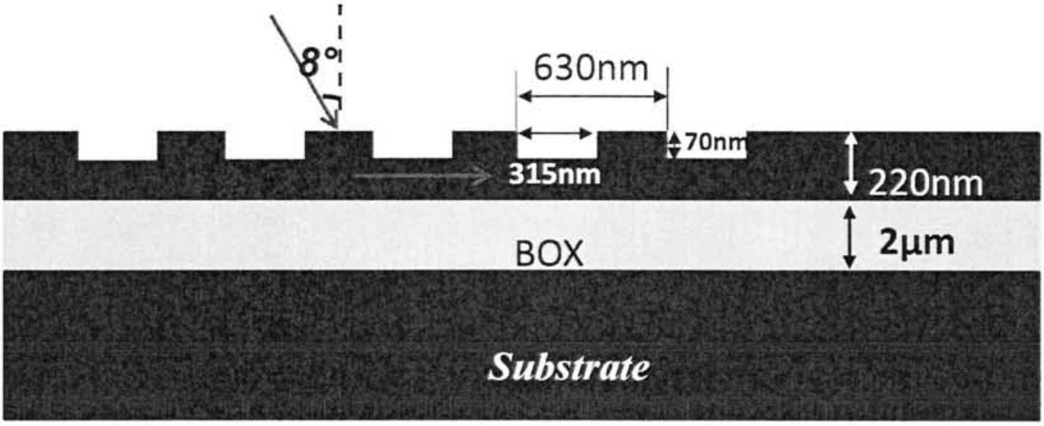


图 3-6 通过电磁场模式匹配计算得到优化的垂直耦合光栅结构。

3.2.2 单模传输波导

为了防止对准光纤中逸散光入射到探测器的侧面上，要将光纤耦合端与探测器放置到不同平面上（如图 5-6(a)所示）。为了减小波导的传输损耗，需要采用脊行弯曲波导进行光传输。因此，首先通过有效折射率方法(Effective Index Method)[20]计算大截面脊型光波导的单模条件，如图 5-6(b)。得到在中间区域仅有 m=0 的基模存在的条件是：

$$\frac{h}{H} > 0.5 - 0.5\sigma \tag{3-9}$$

$$\frac{w}{H} > (1+\sigma)\frac{(h+\sigma)/(H+\sigma)}{\sqrt{1-\left[(h+\sigma)/(H+\sigma)\right]^2}} \tag{3-10}$$

其中 $\sigma = \gamma_1 / \left[k(n_1^2 - n_2^2)\right]^{1/2} + \gamma_2 / \left[k(n_1^2 - n_3^2)\right]^{1/2}$，对于 TE 模式，$\gamma_1=\gamma_2=1$；对于 TM 模式，$\gamma_1=(n_2/n_1)^2$ 和 $\gamma_2=(n_3/n_1)^2$。同时，$k=2\pi/\lambda$。将 $n_2=n_3$ 为氧化硅的折射率 1.46，n_1 为 Si 的折射率 3.48，得到脊型波导的单模条件，图 5-7 所示。此次设计的脊型波导宽 W 为 400nm，刻蚀深度为 100nm。

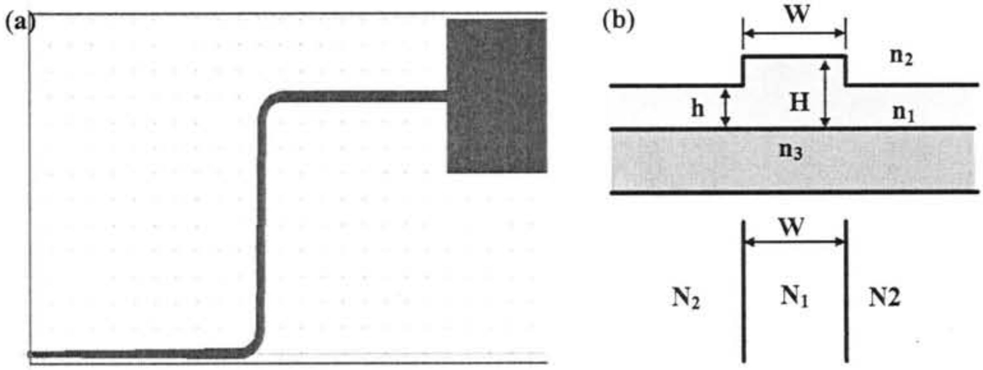


图 3-7(a)器件传输波导结构示意图；(b)有效折射率法计算单模脊型波导结构。

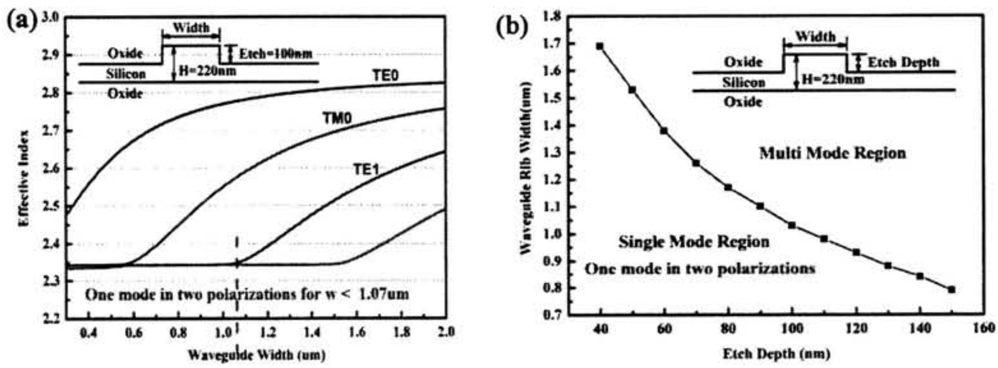


图 3-8 脊型波导的设计参数

其次，采用有效折射率方法（EIM）和速度补偿方法对曲线形 SOI 脊行弯曲波导的辐射损耗进行计算分析。对弯曲平板波导可采用速度补偿方法分析，为了保持光波波形的完整性，弯曲波导中的光波等相位面应该是以曲率中心为起点的一系列辐射状平面，因此波导中心轴外侧，随着中心轴距离的增加，导膜的相速度也越来越大，等效于波导的有效折射率越来越小。波导对光场的限制也越来越弱，当中心轴距离达到一定阈值时，波导的有效折射率等于覆盖层的折射率，此时的波导已对光场没有限制作用[21]，辐射损耗达到增大，根据有效折射率方法和速度补偿方法得到弯曲平面波导的场辐射衰减系数为：

$$\alpha = C_1 \exp(-C_2 R) \tag{3-11}$$

式中：
$$C_1 = \frac{\lambda_0 \cos^2(\frac{pw}{2}) e^{qw}}{qw^2\left[\frac{w}{2} + \frac{1}{2p}\sin(pw) + \frac{1}{q}\cos^2(\frac{pw}{2})\right]} \tag{3-12}$$

$$C_2 = \frac{2q(\beta - k_0 N_2)}{k_0 N_2} \tag{3-13}$$

其中，R 为曲率半径，H，h，w 和 d 等参数定义与图 5-6(b)相同，$k_0=2\pi/\lambda_0$，$\beta=k_0N$ 为直波导的传播常数由内外脊折射率和脊宽 w 决定；N 为等效光波导的有效折射率，$p=\sqrt{k_0^2N_1^2-\beta^2}$，$q=\sqrt{\beta^2-k_0^2N_2^2}$。上面的分析可知，$C_1$ 和 C_2 是与曲率半径 R 无关的常数，而振幅衰减系数 α 与曲率半径 R 呈指数关系，曲率半径越小，辐射损耗越严重。将振幅衰减吸收 α 为 1Np/m（1Np=8.686dB)的曲率半径定义为波导允许的最小曲率半径[22]，脊型波导结构和入射光等已知的条件，可得到此结构的最小曲率半径为 10μm。

3.2.3 波导与吸收层的耦合设计

根据耦合原理和方式不同又分为：a.倏逝波耦合 (evanescent coupling)和 b.对接耦合 (butt coupling)两种，分别如

图 3-9 所示。

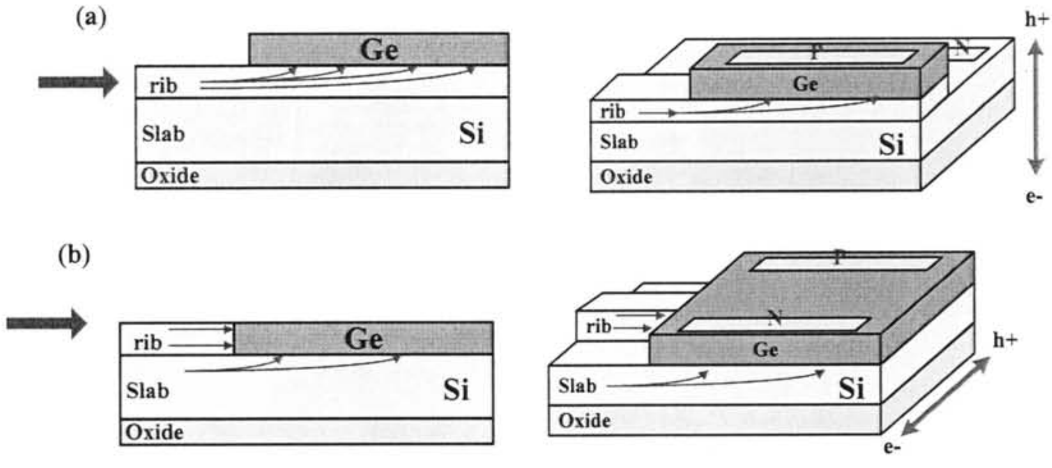


图 3-9 波导器件光耦合类型，(a)倏逝波耦合型；(b)对接耦合。

倏逝波耦合[23,24]的光传播方向和吸收方向垂直，利用电磁场的指数消逝理论将电磁波从一个介质传播到另一个介质中，根本上是两个电磁场的近场相互作用。从数学上讲，此过程类似于量子隧穿。对接耦合的光的传播方向和吸收方向平行，可以通过设计光入射到波导和吸收材料界面时的入射角以及增透膜的设计可以达到光波的 100%吸收，比倏逝波耦合效率高，通过 FDTD solution 模拟得到倏逝波耦合、对接耦合以及两种耦合模式共存时器件中心轴平面的光强分布，如图 3-10，通过光强的分布可看到倏逝波耦合和端面耦合在前 10μm 长度下已经将大部分的光吸收，但是由于对接耦合光入射角设计和增透膜设计大大增加了工艺难度，因此应用的反而较少。因此本论文论述的波导器件是倏逝波耦合入射结构。

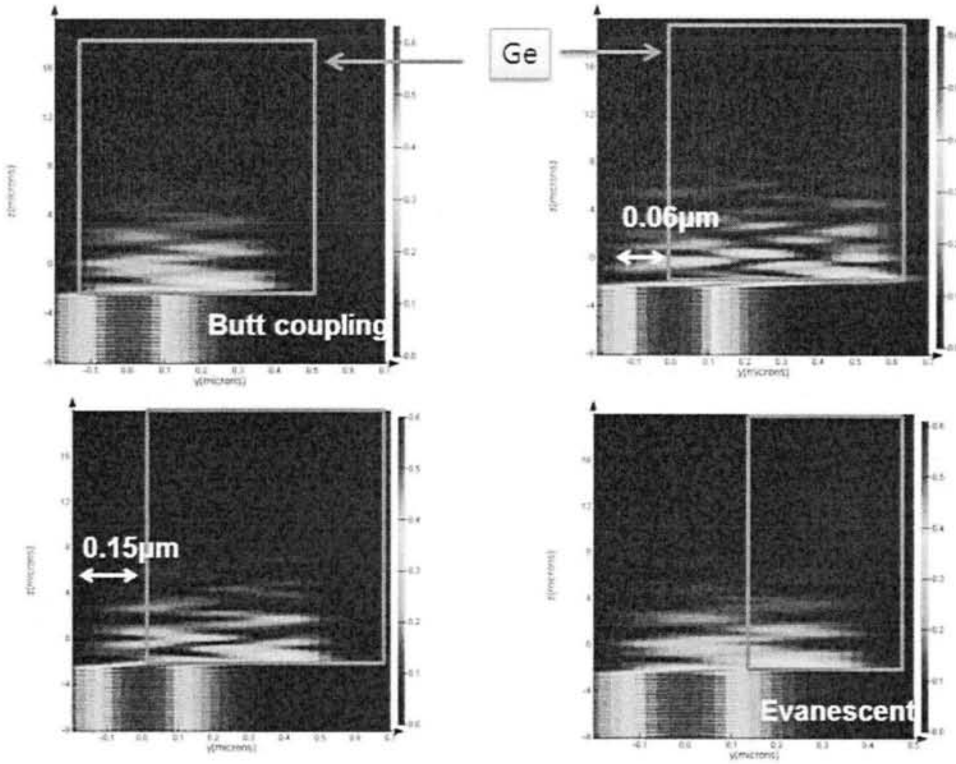


图 3-10 FDTD solution 模拟计算得到倏逝波耦合、对接耦合以及两种耦合模式共存时器件中心轴所在平面的光强度分布情况。

3.2.4 APD 吸收层厚度(W_a)设计

Ge 吸收层的长度：通过 FDTD solution 模拟得到倏逝波耦合、对接耦合以及两种耦合模式共存时 Ge 材料的吸收效率进行了计算，结果如图 3-11，当 Ge 材料的长度达到 10μm，厚度为 0.5μm，两种耦合模式均能使光吸收效率达到 93%以上。

Ge 吸收层的厚度：由于 Al 金属电极对 1550nm 近红外波段有较强的吸收，因此在讨论 Ge 吸收层厚度时，也要将金属电极的吸收考虑进去，模拟计算结果如图 3-12，当 Ge 厚度< 0.4μm 时，Al 金属吸收占主导；当 Ge 厚为 0.4μm 时，Al 金属和 Ge 材料形成了模式限制结构，有利于将光限制在 Ge 层，增强吸收；当 Ge 厚度> 0.4μm 时，Ge 层足够厚，能够到达 Ge 材料顶部的光很小，此时 Al 金属对光吸收影响较小。

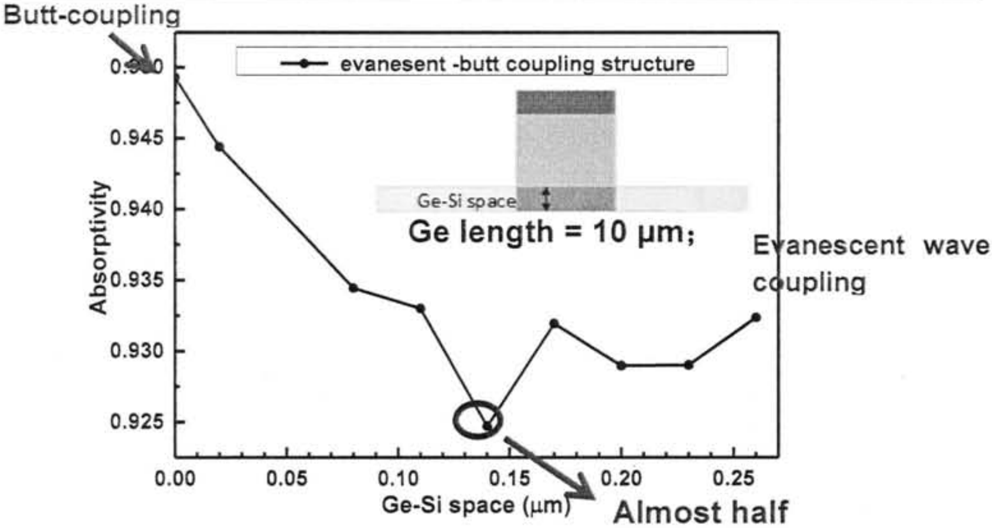


图 3-11 倏逝波耦合与对接耦合的耦合效率对比。

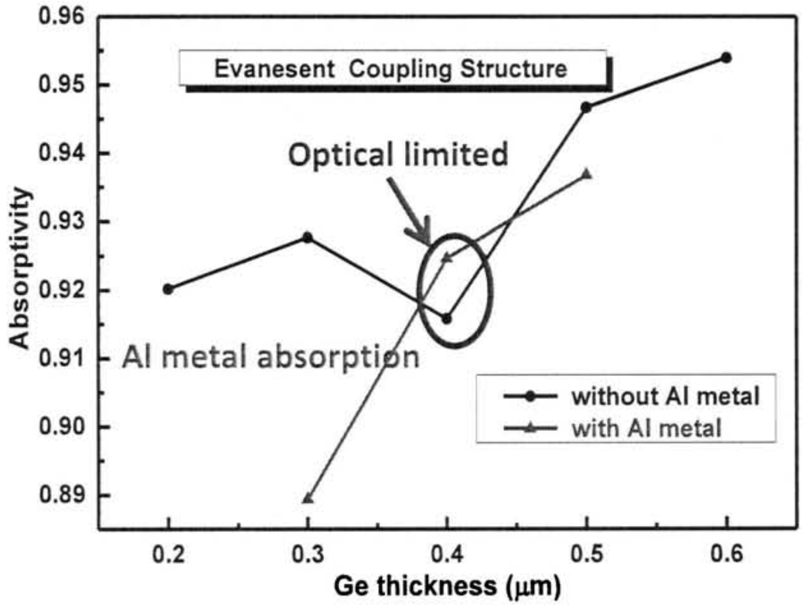


图 3-12 FDTD solution 模拟计算得到倏逝波耦合下不同 Ge 厚度时 Al 电极对吸收效率的影响。

3.3 纳米 Ge/Si WG-SAM-APD 的电学结构设计

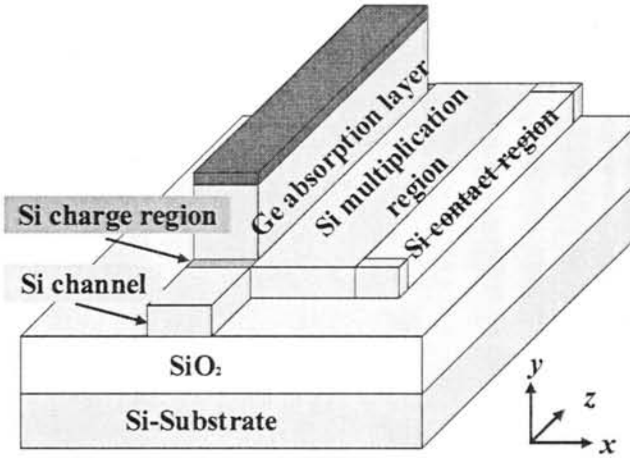


图 3-13 Ge/Si 吸收倍增垂直型波导雪崩探测器结构示意图

3.3.1 欧姆接触层的设计

欧姆接触的定义：指金属与半导体之间的接触，其接触面的电阻值远小于半导体本身的电阻，使得器件操作时，大部分的电压降在于有源区（Active region）而不在接触面，此时接触电阻可以忽略。理想的接触电阻对器件性能影响很小，接触面压降远不可与器件有源区压降相比。

定义欧姆接触的宏观参数：比接触电阻 R_c，定义为电流密度对界面上电压降的倒数[25]。

$$R_c \equiv \left(\frac{dJ}{dV}\right)_{V=0}^{-1} \tag{3-14}$$

结合热电子发射扩散理论[26]，形成好的欧姆接触有两个条件：A.金属与半导体间有低的电势差（Barrier Height）B.半导体有高浓度的杂质渗入（$N_D \geq 10^{18}$ cm^{-3}）。前者可使接触电流中热激发部分（Thermionic Emission）增加；后者则使接触面的耗尽区变窄，电子有更多的机会直接穿透（Tunneling），而接触阻值降低。一般对于 IV 族材料（Si，Ge）形成低阻抗的欧姆接触半导体的掺杂浓度要在 $10^{19}/cm^3$ 以上，由于载流子在该层采用扩散的方式达到金属电极，因此为了获得较大渡越频率，此层的厚度不应太厚，一般选用厚度为 0.1μm。下表列举了本文所用的硅和锗的半导体接触材料。

表 3-1 硅和锗材料的金属欧姆接触工艺[27]

半导体	金属	半导体	金属

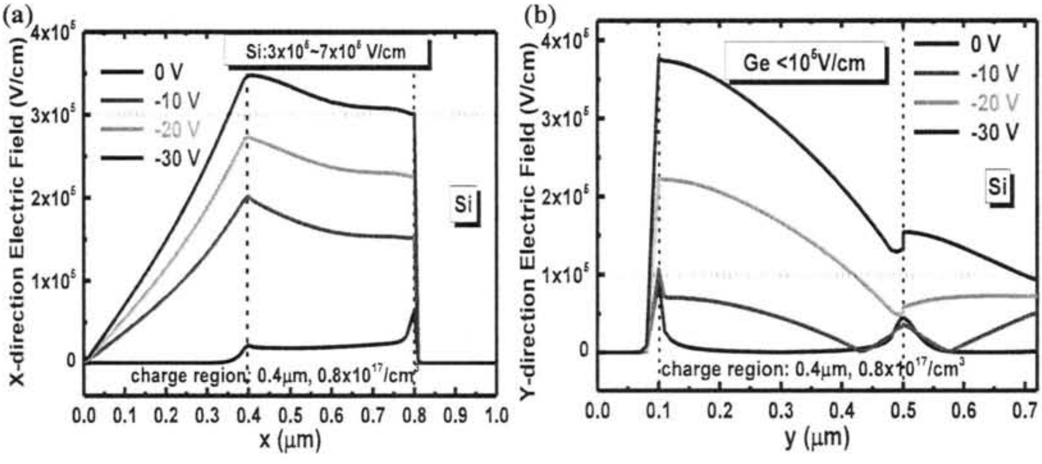
n-Ge	Ag-Al-Sb, Al, Al-Au-P, Au, Bi, Sb, Sn, Pb-Sn	p-Ge	Ag, **Al**, Au, Cu, Ga,Ga-In, In, Ai-Pb, **Ni**, Pt, Sn
n-Si	Ag, **Al**, Al-Au, Ni, Sn, In, Ge-Sn, Sb, Au-Sb, **Ti**,TiN	p-Si	Ag, Al, Al-Au, Au, Ni, Pt, Sn, In, Pb, Ga, Ge, Ti, TiN

当器件电极金属处的电流密度均匀，则器件的接触电阻 $R=R_c/A$，其中 A 为电极的接触面积。

3.3.2 电荷层的分析研究

雪崩探测器的电荷层为一层 P 型掺杂的 Si 薄层作用是在外加电场的作用下降吸收区和倍增区的电场分离与 N+掺杂的接触层 Si 本征区内形成雪崩高场，实现载流子的倍增，此时要求 Si 倍增层电场高于发生雪崩的阈值电场（Si：3×10^5 V/cm），低于隧穿阈值电场（Si：7×10^5 V/cm）；与 P+掺杂的接触层形成低场耗尽，使得载流子以饱和速度漂移输运，此时在 Ge 吸收区的电场要求低于雪崩阈值电场（Ge：1×10^5 V/cm），防止过高的过剩噪声，降低器件的灵敏度。而电荷层起到隔离吸收区和倍增区，并调节这两个区域的分压和电场分布的作用，由于新型纳米纳米 Ge/Si WG-SAM-APD 的电荷区为了有效调节吸收区电场，其宽度与 Ge 吸收区宽度匹配，而为了有效吸收单模波导耦合的光信号，Ge 吸收宽度与单模波导的宽度匹配，因此，Si 电荷区的宽度为 0.4μm。主要靠电荷区掺杂浓度条件电场分布：

A. 掺杂浓度过低：耗尽区过早到达吸收区，将吸收区和倍增区之间的电场强度差别拉低，当外加偏压使得倍增区的电场发生雪崩效应时，此时的吸收区的电场也会应为过高而发生击穿，如图 3-15(a)和(b)，此时的倍增区不仅有 Si 横向区域也包括 Ge 吸收区域，此时器件的倍增系数可以很高（$>10^5$），如图 3-15(c)，但是由于 Ge 材料的电离系数比接近 1，此时器件的过剩噪声也很高，器件的灵敏度较低。



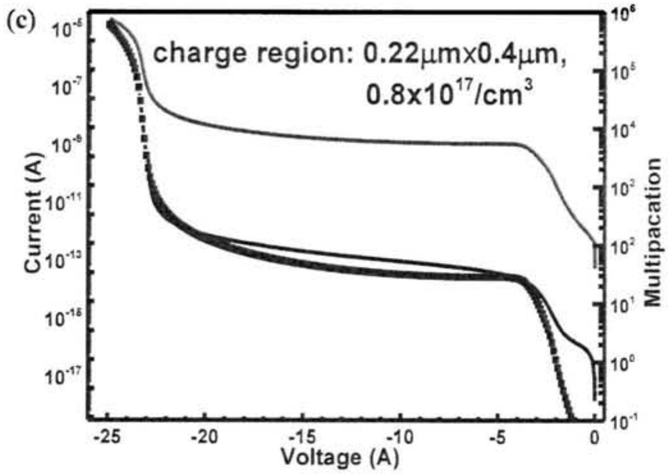
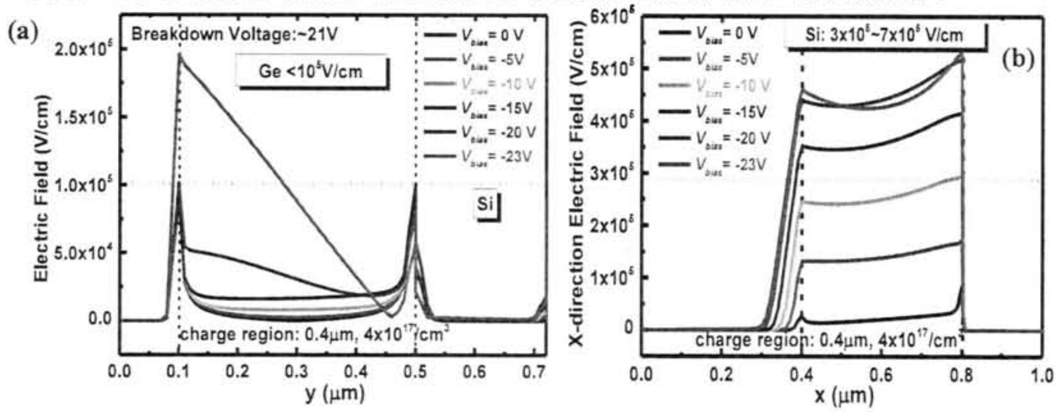


图 3-14 电荷层掺杂过低，Ge 吸收区电场过大以致发生倍增。

B. 掺杂浓度过高，将吸收区和倍增区完全阻隔，外加偏压主要降在倍增区两端，吸收区内部仅有因掺杂浓度不同形成的内建电场，如图 3-15(b)，虽然仍能完成载流子的收集工作，但是载流子的漂移速率收受到限制，影响低倍增系数下的响应频率；同时器件在雪崩倍增的大注入下，容易在 Ge 吸收层形成空间电荷效应而使器件发生饱和，从而限制倍增系数的提高。由于电荷区将吸收区和倍增区完全隔离，当偏压升高时，器件内部压降集中在倍增区两端，但是当偏压继续升高时，倍增区两端的压降不再变化，如@-20V 和@-23V 倍增区电场近似相同，多出的电势差则集中在 P 型欧姆接触层与 Ge 吸收层界面处，而不是由倍增区穿过电荷区扩展到吸收区（穿通型器件的电场扩展模式），这种电场分布不利于光生电子漂移穿过电荷区，进而进入倍增区发生雪崩倍增这一过程的进行。



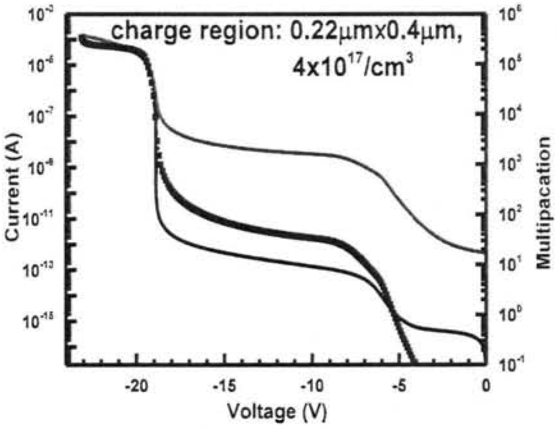


图 3-15 电荷层掺杂过高，吸收区的电场不随外场的变化而变化。

对于电荷掺杂浓度分别为 $0.8\times10^{17}/cm^3$，$1\times10^{17}/cm^3$，$1.5\times10^{17}/cm^3$，$2\times10^{17}/cm^3$，$3\times10^{17}/cm^3$，$4\times10^{17}/cm^3$ 时器件内部电场分布进行对比，如

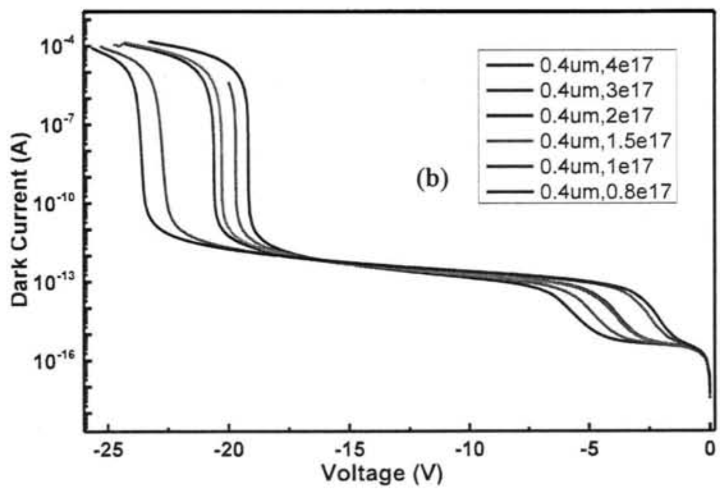


图 3-16 所示，可以看到满足吸收区和倍增区电场分布：电荷区宽度 0.4μm，掺杂浓度 $1\times10^{17}/cm^3\sim3\times10^{17}/cm^3$，由于点电荷区内部的电场强弱决定了光生载流子在吸收区的渡越时间快慢，因此，B 掺杂浓度选用 $1\times10^{17}/cm^3$ 有利于获得高响应频率和低噪声。

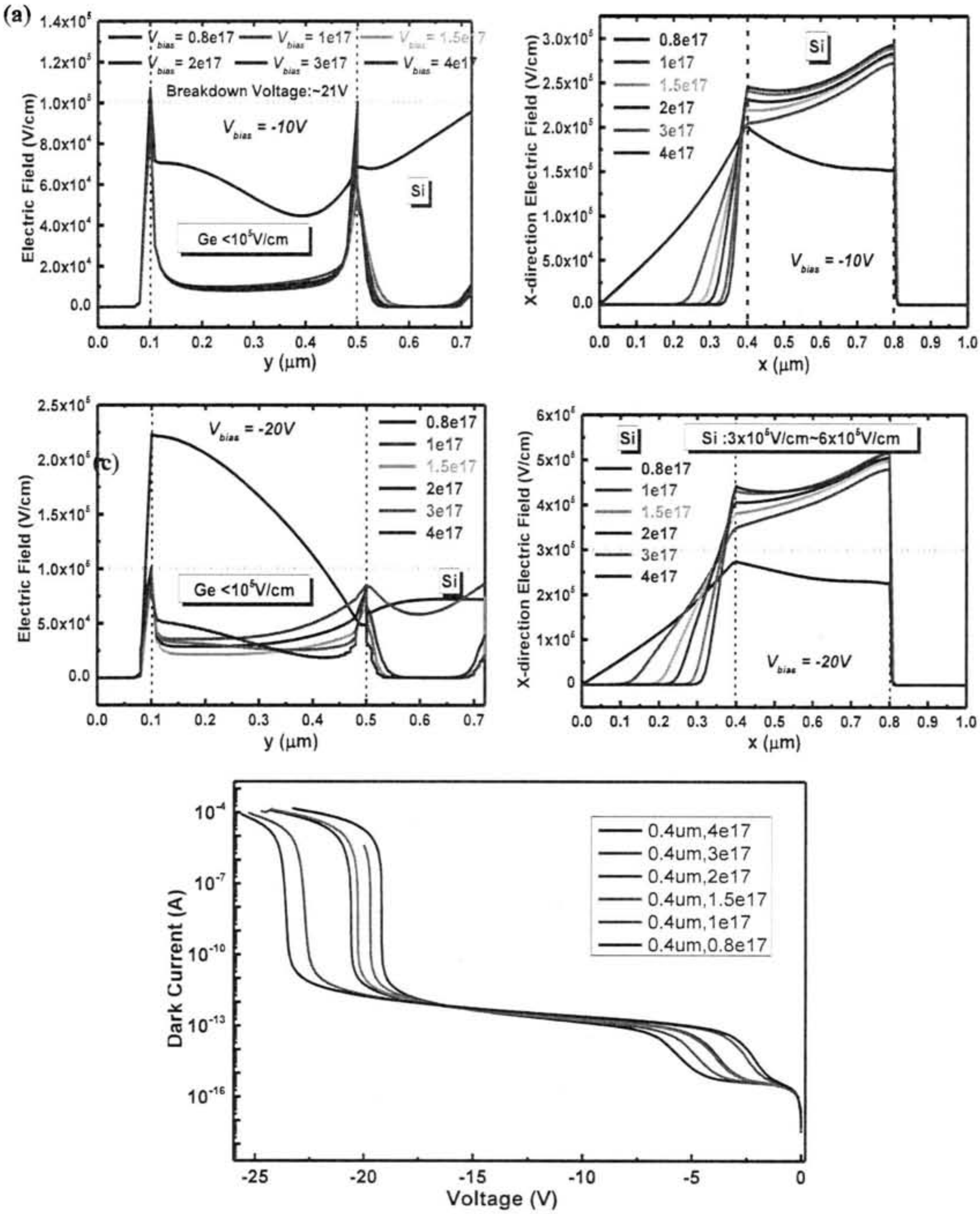


图 3-16 电荷掺杂浓度分别为 $0.8\times10^{17}/cm^3$，$1\times10^{17}/cm^3$，$1.5\times10^{17}/cm^3$，$2\times10^{17}/cm^3$，$3\times10^{17}/cm^3$，$4\times10^{17}/cm^3$ 时工作在(a) -10V 和(b) -20V 时器件内部电场分布和(c)暗电流以及击穿电压对比。

3.3.3 APD 倍增层设计

雪崩探测器的宽带雪崩倍增区是在 P+掺杂 Si 衬底上外延的一层本征硅单晶层。器件在较大的外加反偏下，该层形成高场耗尽，由吸收区漂移过来的光生电子在高场的作用下，加速并获得足够高的能量，通过碰撞晶体的束缚态的电子，将电子激发到导带底，产生电子-空穴对，新产生的电子空穴对又在外加强场的作用下分别向两个相反的方向运动并加速，当获得足够高的能量时又将碰撞电离，产生更多的电子-空穴对，自由载流子便于指数方式递增下去，直到到达电极被收集，形成信号电流。

因此较长的倍增区可以产生更多次的碰撞电离，更多的倍增过程和更大的增益，但是同时会产生更多的统计涨落，更大的过剩噪声。此外，由上面的分析可知，碰撞电离还需要一个最短距离，通常被称为“死域 (Dead Space)”，将载流子在该区的电场下聚集足够高的能量。“死域”的存在降低了倍增区的有效长度，因此在设计时还要尽量减小或消除倍增层内“死域”的厚度。由于载流子一定要经过“死域”的聚能，才能形成雪崩，因此，对于雪崩探测器而言“死域”是无法避免，但是为了不影响倍增层的厚度，可以将“死域”移出倍增区到电荷层或者吸收层。本文采取的方法是在吸收区形成相对高的电场，使得光生电子在吸收层和电荷层进行一定的加速，获得较高的能量。

由之前的 Si 材料参数可知，为了使倍增区的电场足够大发生雪崩效应，同时不会造成器件不可逆转的热击穿，雪崩倍增层的电场范围为： 3×10^5V/cm<E_d<7×10^5V/cm。Si 材料电子发生雪崩所需要的载流子能量值为 1.792eV，可计算在 Si 层的“死域”的厚度小于 60nm，为了获得较高的 M 值，倍增区一般选用 0.4 μm。

3.3.4 APD 结构模拟结果

由于半导体器件模拟软件是将半导体器件内部电场、载流子漂移以及复合等情况模式化、理想化。软件模拟对实际器件设计及性能仅提供参考，无法代表器件的实际性能。事实上，工艺完成的器件会受到材料外延，微纳加工过程的影响，而且实际测试系统也会造成部分误差，使得器件性能有一定的下降和改变，因此需要通过模拟结构和实际测试数据进行对比以完成器件的结构的修正和优化。

1. 器件模拟 I-V 特性

通过之前的分析和模拟，得到了理想的 Ge/Si WG-SAM-APD 的材料结构及掺杂分布，如表 3-2。通过 silvaco 模拟得到器件的剖视图（图 3-17(a)）以及器件在不考虑晶格位错等情况下的理想的暗电流和光响应电流的 I-V 特性曲线（图 3-17(b)）。通过器件 I-V 曲线可推测出器件的击穿电压在-28V 左右，穿通电压在-15V 以后。

表 3-2 器件最佳结构参数：

Name	Thickness (μm)	Width （μm）	Concentration (/cm3)	Doping profiles	Dopant type	Material
Contact layer	0.1	0.4	5e19	uniform	P+	Ge
Absorption layer	0.4	0.4	5e15（外延本征掺杂）	uniform	I	Ge
Charge layer	0.22	0.4	1e17	uniform	P	Si
Multiplication layer	0.22	0.4	1e13	uniform	I	Si
Substrate layer	0.22	>0.4	5e19	uniform	N+	Si

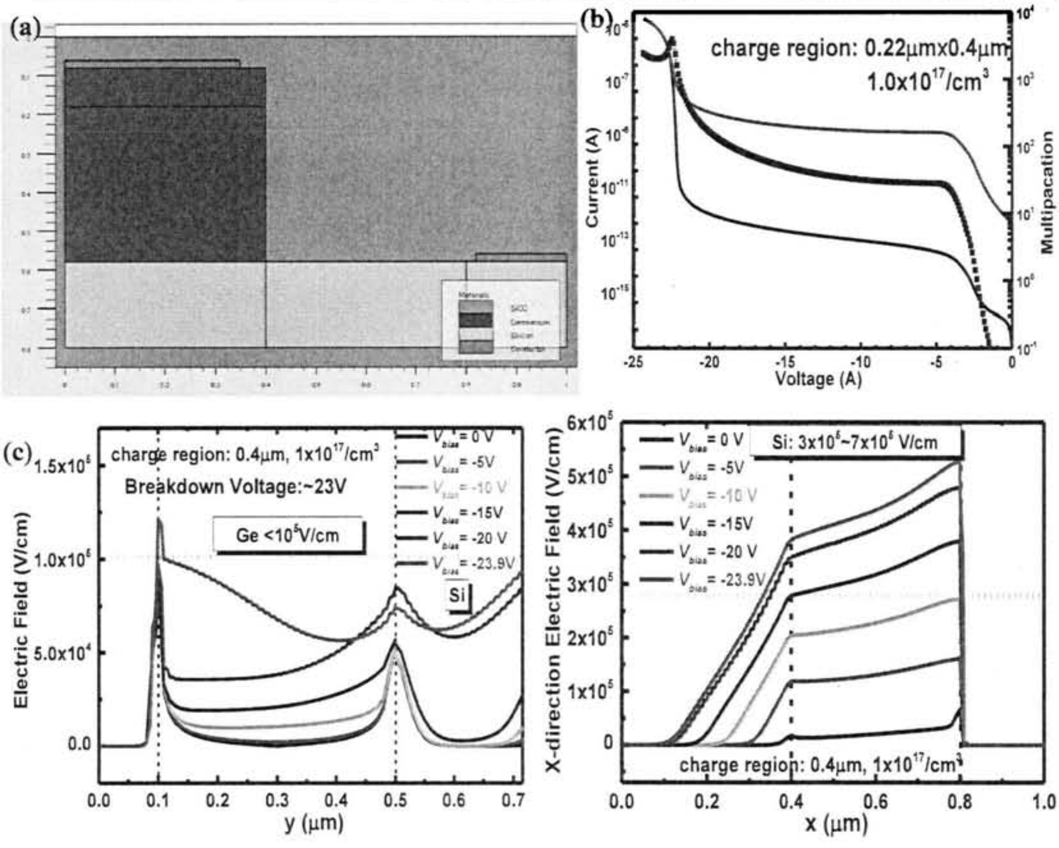


图 3-17 (a) 器件模拟结构；(b) 优化结构的 I-V 特性以及倍增系数曲线；(c) 优化结构在不同的工作偏压下横向吸收区电场和纵向倍增区电场分布

通过模拟可看到表 3-2 中参数设置完全满足器件的设计要求，有明显的倍增效应，电荷层的掺杂能够将吸收区和倍增有效隔离，并可控制各层的电场分布（如**错误!未找到引用源。**）。

3.4 Ge/Si SACM APD 器件的制备

3.4.1 Ge/Si 选择性外延

波导耦合型 Ge/Si 探测器的 Ge 材料层只能用 Si 基 Ge 材料的选择性外延的方法进行生长。选择外延的操作方法：首先在 Si 衬底上通过 PECVD 方式覆盖一层 SiO_2 掩膜层，接着利用光刻和刻蚀 SiO_2 的方法露出外延 Ge 薄膜的生长窗口，最后 Ge 薄膜露出 Si 生长窗口并在 SiO_2 表面合并，形成完整的 Ge 外延薄膜[28][29]。本实验采用的选择外延 Ge 材料的实验如图 3-18 所示[30]，SOI 表面法线为(100)晶向，波导沿(011)晶向分布。用低高温两步生长法在图形衬底上生长 Ge 薄膜，步骤如下：

1、图形衬底在分析室中除气；

2、图形衬底在生长室中脱氧；

3、280°C 下外延 60nm 厚的 Ge；

4、580°C 下外延要求厚度的 Ge。

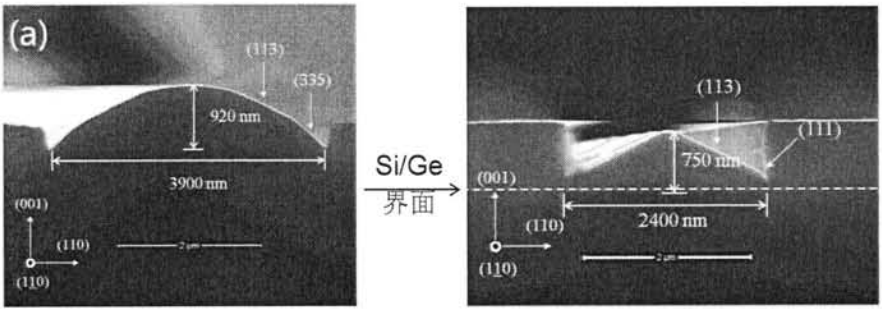


图 3-18 SiO_2 窗口中选择外延 Ge 薄膜的截面 SEM 图: (a)生长温度为 750℃，顶面形成鼓包；(b)600℃生长，SiO_2 窗口侧壁陡直，Ge 薄膜贴 SiO_2 侧壁生长

在 Si 衬底的顶层(100)面上淀积的 Ge 外延膜不是完全沿着 Si 方条方向生长的，而是类似一个空间梯形，与 Si(100)面有一个接触角 θ≈26°(有一些文献研究指出这个角度是 25°[31, 32, 33, 34]，部分差异应该源于测试系统误差)。假设梯形侧面晶面指数为($h\ k\ l$)，其晶面法线与晶格 x, y, z 轴的夹角分别为 α, β, γ，其中 $\alpha=\beta, \gamma=\theta=26°$，又有：

$$\cos^2\alpha+\cos^2\beta+\cos^2\gamma=1 \tag{3-15}$$

$$h: k: l=\cos\alpha: \cos\beta: \cos\gamma=1: 1: 3 \tag{3-16}$$

也就是说，Ge/Si(100)选择性外延出现了{311}晶面，即图 3-18 中的倾斜侧壁，还有些文献指出选择外延 Ge 也会形成其他晶面，如{111}晶面[31]。Ge/Si(100)选择性外延出现{311}晶面的具体物理机制目前并不明确，而{311}晶面的出现会影响选择性外延时 Ge 薄膜的形

貌却是确定无疑的。假设 Si 条的宽度为 L，在相同生长时间下按照(100)面的生长速度 Ge 厚度为 h，如图 3-18 所示：

(a)当 $L>2h\cot\theta$，Ge 薄膜是一个梯形形状，图 3-18 (a)就是这种情况；

(b)当 $L\leq 2h\cot\theta$，Ge 薄膜是一个三角形形状，如图 3-18 (b)所示。此时，外延的 Ge 三角形薄膜的厚度为 $h_0=L/(2\cot\theta)\leq h$，与设计的薄膜厚度 h 有一定的区别。$L\leq 2h\cot\theta$ 时{100}晶向的材料生长速度被新形成的{311}晶面较慢的生长速度限制了。

本文设计的波导型 Ge/Si WG-SAM-APD 要经过在 Si 衬底窗口中外延 Ge 本征层。通过实验可知，Si 上外延 Ge 薄膜类似，一样会出现{311}晶面，外延层呈现梯形结构，上电极位置设计时这部分要留有余量。

3.4.2 器件制备流程设计

由器件结构可知，完成 Ge/Si WG-SAM APD 的材料要经过一次选择性材料外延，对外延片的清洁度要求很高。具体的材料制备流程如下：

1) 选用顶层 Si 厚度为 0.22μm 的 SOI 衬底片，通过 PECVD 沉积 550nm 的 SiO_2 薄膜用于选择外延的掩膜。

2) 电子束曝光 M1 版，将外延窗口的胶去除，并利用 ICP 刻蚀，将外延窗口处的 SiO_2 薄膜刻蚀去除。

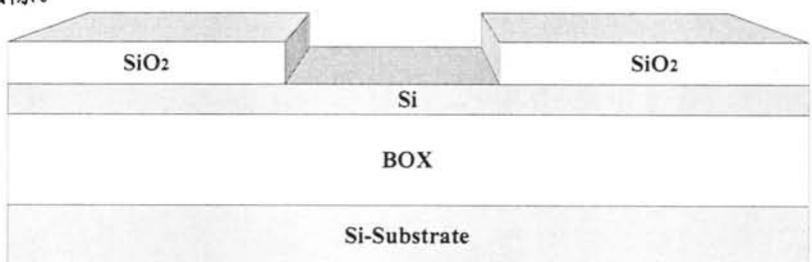


图 3-19 M1 刻蚀 p 型注入区域

3) 通过离子注入的方法将外延的窗口处注入 BF_2^+离子，注入的能量为 25keV，计量为 2e12 /cm^2，形成 Ge/Si WG-SAM-APD 器件的电荷层，电荷层掺杂浓度对器件性能起着关键影响。

4) 采用实验室改进的 RCA[35]方法清洗衬底片。

5) 900℃烘烤样品，去湿，脱氧。

6) 270°C 下使用高纯 GeH_4 生长 60nm 厚的 Ge 缓冲层。

作用：释放因 Ge/Si 的晶格失配（失配率为 4.18%；a_{Ge}=0.56579nm，a_{Si}=0.54310nm）所产生的应力，低温外延层由 9nm 生长到 60nm 厚时，压应力由 0.9%降至 0.2%。

7) 升温至 550℃，用高纯 GeH_4 生长需要 0.5μm 的本征 Ge 薄膜层。

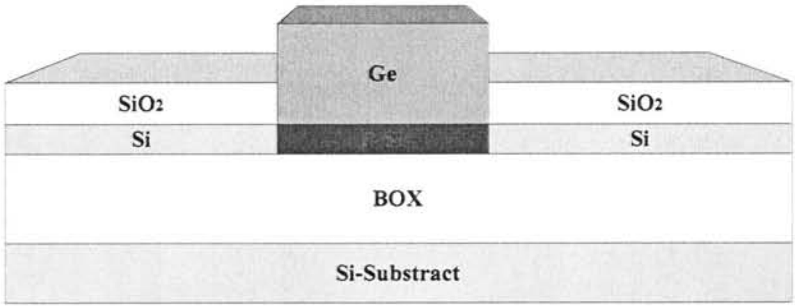


图 3-20 离子注入 p 型电荷区，选择性外延 Ge 吸收材料

8) 利用电子束曝光 M3，将 Ge 表面形成高掺杂的 P+型接触层的表面露出，离子注入 BF_2^+，剂量(Dose)为 $4\times10^{15}cm^{-2}$，能量(Energy)为 30keV。

9) 利用电子束曝光 M4 版，将 Si 表面形成高掺杂的 N+型接触层的表面露出，离子注入 P 离子，剂量(Dose)为 $3\times10^{15}cm^{-2}$，能量(Energy)为 30keV。

10) 退火激活离子注入。

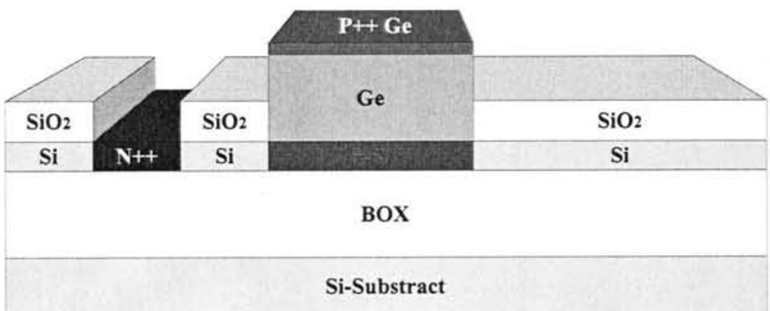


图 3-21 通过两次离子注入形成 P 型和 n 型的欧姆接触层。

11) 利用湿法腐蚀的方式将外延和离子注入后的衬底上面的掩膜 SiO_2 薄膜全部取出，重新利用 PECVD 沉积 500nm 的 SiO_2 薄膜。

12) 电子束曝光 M5 版，并利用 ICP 刻蚀，刻蚀欧姆上下了两个欧姆接触电极空。

13) 电子束曝光 M6 版，通过电子束蒸发和 lift-off 工艺，蒸镀上下了两个欧姆接触电极（Ni/Al=50/250nm），并通过 RTA 退火方式进行合金。

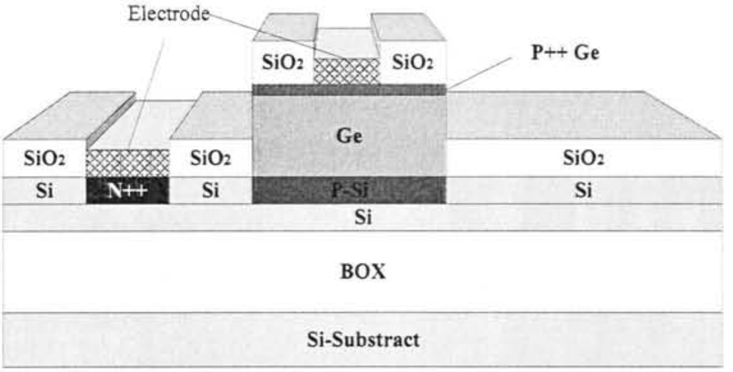


图 3-22 电子束蒸发和 left-off 制备器件欧姆接触电极

14) 电子束曝光 M7 版，通过 ICP 刻蚀 SiO_2 薄膜，并利用 SiO_2 薄膜做掩膜刻蚀出光纤与片上波导的耦合端口以及片上单模 Si 波导。

15) 光刻 M8 版，通过电子束蒸发和 lift-off 工艺，制备出 Pad 电极。

3.4.3 刻蚀工艺分析

对于小面积的钻孔刻蚀，ICP 刻蚀 SiO_2 薄膜速率受到刻蚀空的大小的限制，因此需要对 ICP 刻蚀速率与刻蚀尺寸进行前期实验摸索，确定刻蚀速率模型。

为了摸索刻蚀条件，本实验利用中科院半导体所集成中心的氧化硅 ICP 刻蚀机（Multiplex AOE）的 R:SiO-low1 程序，第一次刻蚀 4min，通过 SEM 测试不空线宽的槽的刻蚀深度（如图 3-23(a) SEM 测试刻蚀槽的深度图，其中电子束曝光版图的图形的尺寸(a) 2 μm，(b) 1 μm，(c) 0.9 μm，(d) 0.8 μm，(e) 0.7 μm，(f) 0.6 μm，(g) 0.5 μm，(h) 0.4 μm，(i) 0.3 μm，(j) 0.2 μm。），进而计算出相应的刻蚀速率，具体如表 3-3，由表可看出当刻蚀空的宽度低于 0.9μm 以后，刻蚀速率随着刻蚀空线宽的减小而降低，ICP 刻蚀是利用带电等离子体轰击样片表面，并与样品发生一定的化学反应，达到图形刻蚀的目的。等离子的轰击造成样品表面带电，由于电荷剧集原理，刻蚀图形边沿会剧集较多与刻蚀等离子体带同极性的电荷，形成排斥电场，抑制等离子体进入窄槽刻蚀，这种现象对窄线宽刻蚀尤为明显，如图 3-23 (d)-(j)。

表 3-3 不同的图形线宽 Multiplex AOE 设备（编号 R:SiO-low1 刻蚀参数）ICP 刻蚀 4min 后刻蚀深度和刻蚀速率

刻蚀线宽 (μm)	2	1	0.9	0.8	0.7	0.6	0.5	0.4	0.3	0.2
刻蚀深度	531.8	536.7	541.5	507.5	429.8	437.1	400.7	364.3	342.4	296.3

(nm)										
刻蚀速率 (nm/min)	132.95	134.175	135.375	126.875	107.45	109.275	100.175	91.075	85.6	74.075

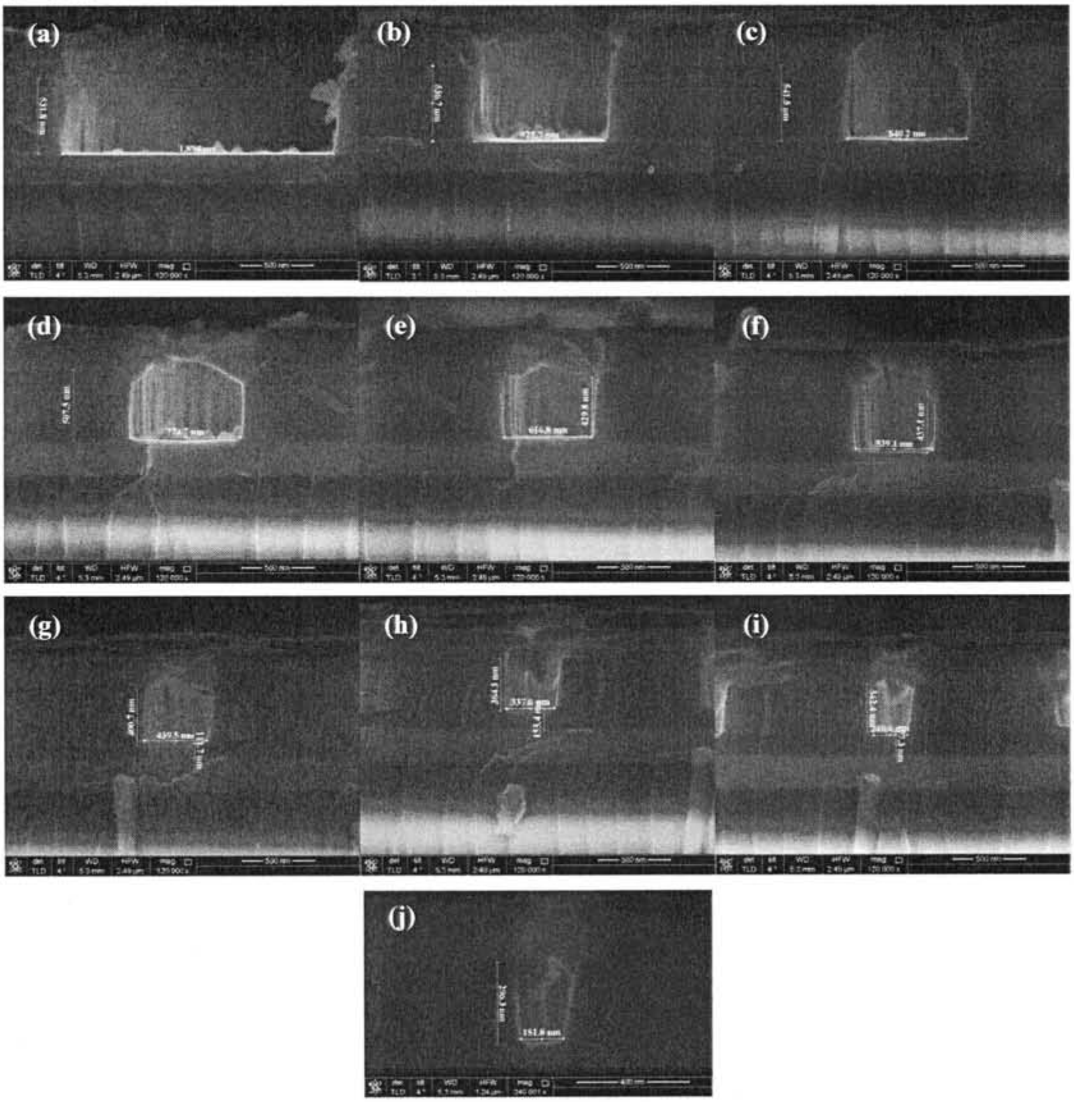


图 3-23(a) SEM 测试刻蚀槽的深度图，其中电子束曝光版图的图形的尺寸(a) 2 μm，(b) 1 μm，(c) 0.9 μm，(d) 0.8 μm，(e) 0.7 μm，(f) 0.6 μm，(g) 0.5 μm，(h) 0.4 μm，(i) 0.3 μm，(j) 0.2 μm。

对于这种窄槽刻蚀情况，在利用试验片监控刻蚀速率的同时，要在正式片刻蚀的同时增加实验片同时刻蚀，以实时监控刻蚀的情况，由于 Ge 无法在 SiO_2 薄膜上外延，所以在衬底片外延之前一定要保证外延窗口的洁净度且没有氧化层。

3.5 本章小结

本章首先介绍了 Ge/Si WG-SAM APD 器件的性能参数，发展概况以及本论文设计的新型纳米器件的大致结构，其次通过模拟和理论计算设计的波导 Ge/Si SAM APD 器件的光纤耦合结构、单模波导结构、倏逝波耦合结构以及器件的吸收层结构参数，之后借助半导体模拟软件对器件的电学结构和性能进行了分析和讨论，将雪崩倍增过程限制在低理论率比的 Si 材料中，获得较高的倍增系数（$\sim10^3$ 量级）的波导 Ge/Si SAM APD 器件结构参数，介绍了材料外延过程以及半导体微纳加工过程，分析讨论了 SiO_2 薄膜刻蚀线宽与刻蚀速率的关系，同时分析了产生这种现象的原因，以及工艺的优化方法。

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Wafer Cleaning Technology

第四章 低暗电流 Si-PIN 探测器

PIN 探测器以其工艺简单，集成度高，成本低廉，频率响应高，暗电流较小等优势，据统计 Hamamatsu，Infineon，Vishay，Source Photonics Inc.，OSI Optoelectrionics，Everlight，EMCORE，menlosystems 等半导体探测器研制和生产公司的产品[1]，PIN 结构是使用的最为普遍的探测器结构，硅基 PIN 探测器已经占领了射频，成像，雷达，近红外光互联等各类探测的市场。探测器的噪声或者暗电流决定了器件能够接收最小信号的功率，决定了成像质量，决定了对探测物的识别能力等，因此，低噪声低暗电流的探测器一直是研究的重点。

4.1 暗电流的组成

4.1.1 扩散电流

光电二极管的理想 I-V 特性分析是基于以下四个假设进行推导的：(1) 突变耗尽层近似，即有突变边界的偶极层承受内建电势和外加偏压，耗尽层边界以外，半导体呈中性；(2) 玻尔兹曼统计近似成立；(3)小注入假设，即注入的少子浓度小于多子浓度；(4) 耗尽区层内部不存在产生-复合电流，且在整个耗尽区内部，电子电流和空穴电流恒定。通过玻尔兹曼统计，连续性方程以及边界条件[2]，得到理想二级管定律，即肖克莱方程。由假设可知肖克莱方程得到的电流特性为仅考虑载流子扩散得到的电流密度，因此，时的电流密度为扩散电流密度就是暗电流最重要的组成之一，其表达式如下：

$$J_{diff}=(q\sqrt{\frac{D_n}{\tau_n}}\frac{n_i^2}{N_A}+q\sqrt{\frac{D_p}{\tau_p}}\frac{n_i^2}{N_D})\left[\exp(\frac{qV}{kT})-1\right]\approx -q\sqrt{\frac{D_n}{\tau_n}}\frac{n_i^2}{N_A}-q\sqrt{\frac{D_p}{\tau_p}}\frac{n_i^2}{N_D} \tag{4-1}$$

其中，D_n，D_p 分别为电子和空穴的扩散系数，τ_n 和 τ_p 分别为电子和空穴的寿命，N_A 为 p 型区的受主浓度，N_D 为 n 型区的施主浓度，n_i 为本征载流子浓度。

4.1.2 产生-复合电流

实际工作的光电探测器一般工作在反向偏压下，而且产生-复合过程是不可避免的，也是器件暗电流重要的组成之二。对于 Si 这种间接带隙半导体，主导的跃迁过程为体缺陷参与的间接复合或者产生过程，体缺陷密度为 N_t，其能级 E_t 位于带隙中，主要是电子俘获和空穴俘获，其净变化率（U）由肖特基-里德-霍尔（SRH）统计描述[3]。

假设：$E_t=E_i$，空穴和电子的俘获截面积相同为 σ，且偏压 $V>kT/q$，可得到器件暗电流重要组成之二的产生-复合电流的电流密度表达式为：

$$J_{ge}=\int_0^{W_D} q|U|dx \approx q|U|W_D \approx \frac{qn_iW_D}{\tau_g}\exp(\frac{qV}{2kT}) \tag{4-2}$$

其中，τ_g 为载流子的产生寿命，W_D 为二极管的耗尽区宽度。

4.1.3 隧穿电流和雪崩电流

隧穿和雪崩这两种暗电流机制，当光电探测器在较高的反偏电压下工作时较为显著。有文章总结当 pn 结的是重掺杂且击穿电压低于 6V 时，隧穿电流将成为光电探测器暗电流的主要来源[4]。平衡状态时，器件内部总的复合几率 R_{tot}，可以写为带间的跃迁（SRH）几率 R_{SRH}，带间隧穿（band-to-band tunneling）R_{bbt}，缺陷辅助隧穿（trap-assisted tunneling）R_{trap} 以及碰撞电离（impact ionization）R_{av} 之和，因此，得到在光电二极管内部，空穴一维的平衡状态的连续性方程：

$$\frac{dJ_P}{dx}=-qR_{tot}(x)=-q(R_{av}(x)+R_{trap}(x)+R_{SRH}(x)+R_{bbt}(x)) \tag{4-3}$$

其中，雪崩倍增的复合几率 R_{av}：$R_{av}(x)=-\frac{1}{q}\left\{\alpha_n(x)|J_n(x)|+\alpha_p(x)|J_p(x)|\right\}$ (4-4)

利用德尔塔函数（Dirac δ-function）产生率来表示带间隧穿几率 R_{bbt}：

$$R_{bbt}(x)=\frac{J_{bbt}}{q}\delta(x) \tag{4-5}$$

可得到，带间隧穿电流密度表达式：$J_{bbt}=C_{bbt}V_j(\frac{\xi_m}{\xi_0})^{3/2}\exp(-\frac{\xi_0}{\xi_m})$ (4-6)

其中，C_{bbt} 为与温度相关的常数，V_j 为结偏压，ξ_m 为最大电场值，ξ_0 为常数，与禁带宽度相关（$\xi_0 \sim E_g^{3/2}$），当室温下 ξ_0 为=1.9×10^7 V/cm。

缺陷辅助隧穿是半导体光电探测器暗电流的又一重要来源，特别是对于缺陷密度较大的半导体异质结器件影响尤为显著，缺陷辅助隧穿几率 $R_{trap}(x)=\Gamma(x)R_{SRH}(x)$ (4-7)

其中，$\Gamma(x)$为缺陷态俘获和释放的几率：

$$\Gamma(x)=2\sqrt{3\pi}\frac{|\xi(x)|}{\xi_\Gamma}\exp(\frac{\xi(x)}{\xi_\Gamma})^2,\quad \xi_\Gamma=\frac{\sqrt{24m^*(kT)^3}}{q\hbar} \tag{4-8}$$

R_{SRH}为带间跃迁的几率[4]：$$R_{SRH}=\frac{pn-n_{ie}^2}{\tau_p[n+n_{ie}\exp(-\frac{E_T-E_i}{kT})]+\tau_n(p+n_{ie}\exp(\frac{E_T-E_i}{kT}))} \tag{4-9}$$

通过简化和积分得到，缺陷辅助隧穿电流的表达式：

$$J_{tat}=-T^{3/2}\exp(\frac{(q\hbar\xi_m)^2}{24m^*k^3}T^{-3})\frac{\sqrt{72\pi m^*k^3}}{\hbar|\xi_m|}\frac{-n_{ie}W}{2\tau\cosh(\frac{E_T-E_i}{kT})}\left[1-\exp(-\frac{\sqrt{24m^*(kT)^3}}{q\hbar|\xi_m|}\frac{qV}{\Psi_{bi}+qV})\right] \tag{4-10}$$

4.2 Si-PIN 器件的结构和性能分析

随着高阻硅晶体制备和 CMOS 工艺的日益成熟和提高，拉动了国内硅光电二极管产业的产生和发展。但是光电器件的工艺需求与现有的微电集成芯片制备工艺之间存在着巨大的差异，首先光电器件对于衬底材料质量的要求远高于微电子器件，以本论文研究的垂直结构的器件为例，光入射产生的光生电子要从上表面通过漂移扩散到达下表面收集，信号载流子为少子，且渡越路径遍布整个衬底片，器件的暗电流、响应度以及电容等关键参数受到材料内部结构和上、下表面状态的限制，而微电子芯片的信号电子主要集中在表面膜层，一般为多子输运。其次光电器件的尺寸一般远高于微电子器件，光电子器件受到光吸收和传输的限制，器件尺寸在亚微米~毫米量级，而微电子器件对于集成度的追求导致了器件特征尺寸已经低于纳米量级。接着两种器件的制备对一些关键工艺要求亦是有着本质的区别，以 PECVD SiO_2 为例，微电子器件的 SiO_2 用于钝化绝缘时要求薄膜具有较高的致密性，用于平坦台面时则是要短时间沉积很厚的膜层，此时对膜层质量要求不高；而光电子器件对于 SiO_2 使用除了钝化作用外还有一个关键作用就是用于光学增透膜，因此对薄膜的折射率和厚度要求精确控制。

因此，需要仔细研究微电子的 CMOS 工艺线上制备的光电子硅基探测器的暗电流这一关键性能参数，反推影响此工艺条件下的光电器件性能的主要影响机制，进而提出器件结构、材料和制备工艺的改进方案。

4.2.1 Si-PIN器件的制备

本文研究的 Si PIN 光电探测器是在 ISO9001-2000 质量体系认证的五英寸 2μm 标准 CMOS 工艺加工线上进行加工制备的，器件的结构示意图如图 4-1(a)所示。根据**错误!未找到引用源。**中介绍的根据器件尺寸分析暗电流的方法，为了简化尺寸，本论文仅研究正方形结构的器件如图 4-1(b)所示，研究的器件的边长分别为 2.5mm，2mm，1.5mm，1.0mm，0.5mm，0.25mm。

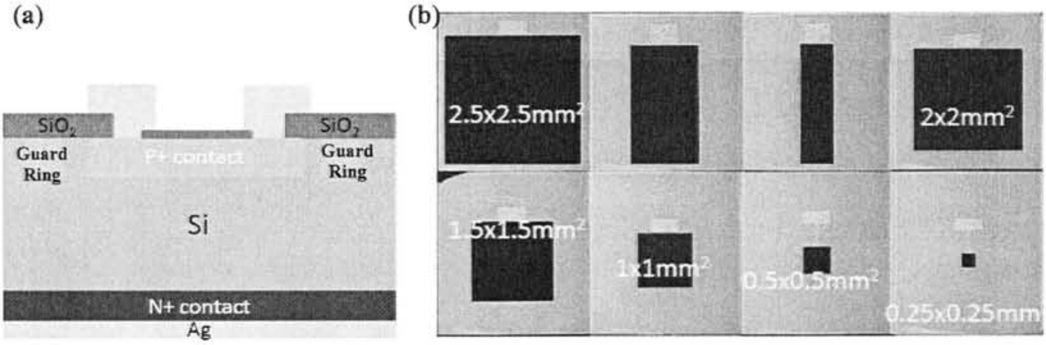


图 4-1 CMOS 工艺制备不同尺寸的 Si-PIN 探测器的结构剖视图和俯视图。

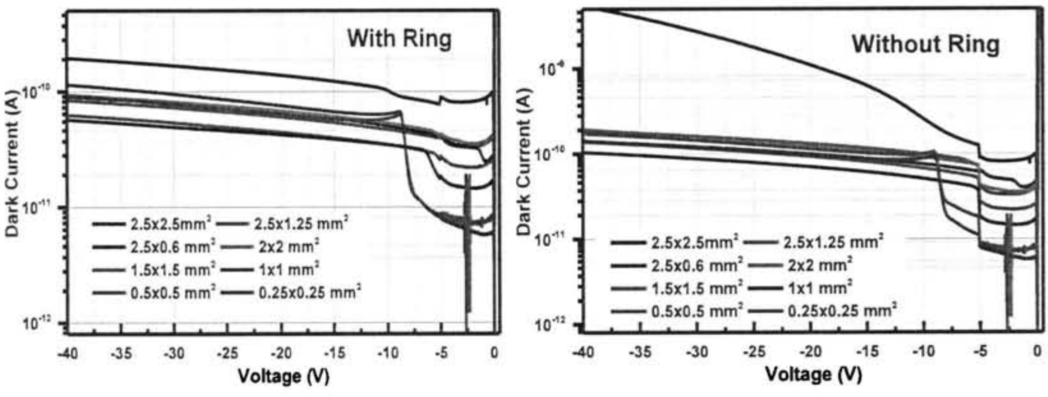
4.2.2 工艺参数对器件性能的影响

器件制备采用的衬底为 5 寸 N 型 Si 衬底，器件制备流程中通过改变衬底的阻抗系数，光敏面的离子注入能量，保护环（guard ring）确定获得最佳性能的器件制备参数。其中，通过对比衬底的阻抗系数以及软件模拟发现，响应度主要受到载流子的寿命有关，跟衬底的掺杂浓度关系不大，暂时未找到暗电流与衬底掺杂浓度之间的关系。

1. 保护环的作用

保护环是添加在上表面欧姆接触掺杂区域之外的一层环状掺杂区，其掺杂浓度与 P+ 掺杂区相同，主要是抑制圆环以外的杂散载流子通过扩散到达欧姆接触区被收集，从而增加器件的暗电流。图 4-2 为具有相同制备流程参数相同衬底片，仅有无保护环的区别的两系列的器件的暗电流和响应度特性，分析对比可看到：

（1）暗电流性能：各个器件尺寸下，有保护环的暗电流都低于无保护环的，由此说明，保护环的添加确实能够有效抑制暗电流，特别是在工作偏压较高时，能够明显降低暗电流，抑制器件的提前击穿。



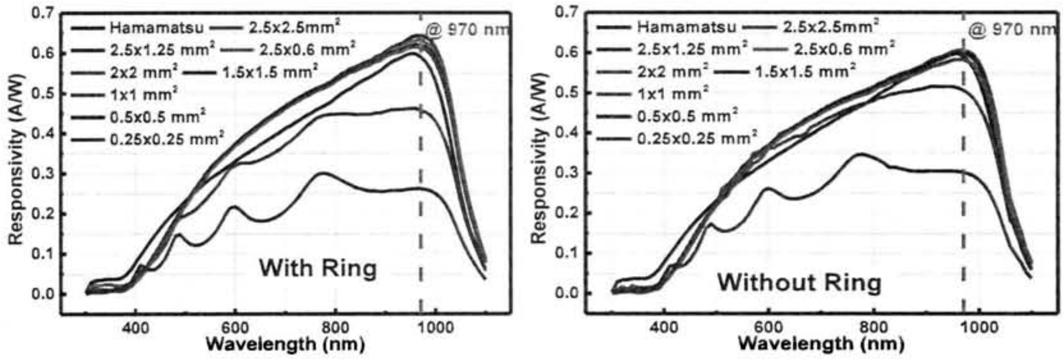


图 4-2 制备流程相同衬底片相同，仅有有无保护环的区别的两系列的器件的暗电流和响应度特性。

（2）响应度的性能：边长为 0.5μm 和 0.25μm 的器件，有保护环的响应度低于无保护环的，分析原因：两个器件的光敏面小于入射光斑的面积，光斑照射会到光敏面以外的区域，这部分仍能产生光生载流子，当没有保护环的阻挡时，会通过扩散被电极收集。这个现象再一次证明了保护环能够阻挡光敏面以外的扩散电流和产生复合电流，能够有效降低暗电流。

2. 光敏面离子注入能量

暗电流：根据暗电流与器件尺寸参数之间的关系，可将暗电流分成：(1) 与器件横截面积相关的面暗电流密度(J_a)；(2) 与器件的边沿周长相关的线暗电流密度(J_p)；(3) 与器件尺寸无关的暗电流 (I_c)。因此，本论文研究正方形器件的暗电流可以分解为：

$$I_{dark} = J_a \square b^2 + 4J_p b + I_c \tag{4-11}$$

其中，b 为器件的特征长度（一般为器件的边长）。将两种离子注入能量制备的器件的暗电流提取出来，在暗电流-特征尺寸坐标系中，得到两种工艺的暗电流与器件尺寸的关系拟合曲线：

$$\begin{aligned}
I_{dark} &= (1.15619\times10^{-11})b^2 + (1.91922\times10^{-11})b + (4.74626\times10^{-12}) \quad @-1V,45KeV \\
I_{dark} &= (1.3957\times10^{-11})b^2 + (1.71922\times10^{-11})b + (6.14985\times10^{-12}) \quad @-3V,45KeV \\
I_{dark} &= (1.60162\times10^{-11})b^2 + (1.80255\times10^{-11})b + (7.46611\times10^{-12}) \quad @-5V,45KeV \\
I_{dark} &= (1.16903\times10^{-11})b^2 + (4.97766\times10^{-12})b + (9.52502\times10^{-12}) \quad @-1V,25KeV \\
I_{dark} &= (1.43564\times10^{-11})b^2 + (3.2153\times10^{-12})b + (1.17015\times10^{-11}) \quad @-3V,25KeV \\
I_{dark} &= (2.2771\times10^{-11})b^2 + (1.85727\times10^{-12})b + (1.54538\times10^{-11}) \quad @-5V,25KeV
\end{aligned} \tag{4-12}$$

由上面的拟合曲线可知，45keV 注入能量的器件的面暗电流占的比例大于边沿暗电流，可能原因是，离子注入能量的增大，造成表面损伤增多，增大了表面缺陷态引发的缺陷辅助隧穿暗电流。

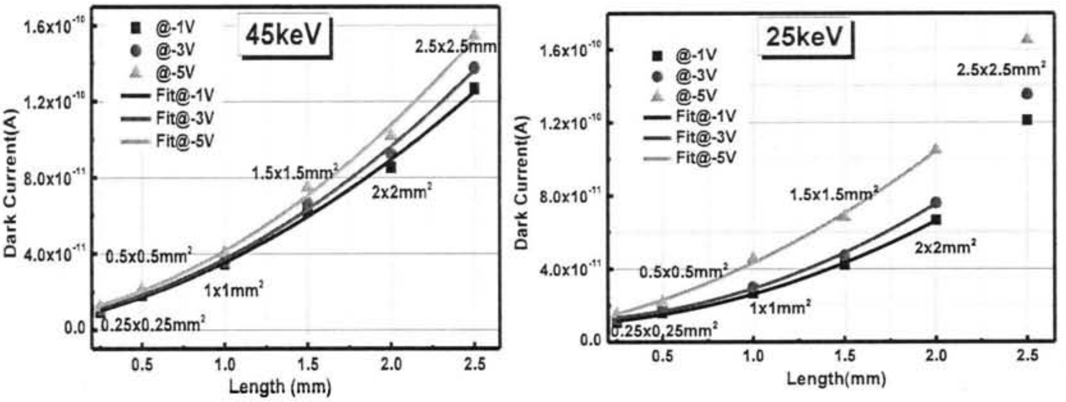


图 4-3 低偏压下两种离子注入能量的器件尺寸与暗电流之间关系的拟合曲线，其中 25keV 制备的边长 2.5mm 器件的暗电流造成拟合曲线系数为负数，判定此数值奇异点，不用于拟合。

响应度：上表面的离子注入能量能量决定了上表面欧姆接触区的厚度和 pn 结以及电场的深度，理论上，光在欧姆接触层内部被吸收产生的光生电子空穴对，由于没有电场的牵引，不容易分离形成有效的信号载流子，Si 在短波长吸收系数大，光吸收主要集中在靠近入射面的区域，因此，离子注入能量增大，会降低短波吸收效率，降低短波响应度，这一物理过程，被图 4-4 (a)的 silvaco 模拟 30keV 和 150keV 离子注入能量下器件的量子效率结果证实，但是，由于此批次器件的表面漏电较大，表面缺陷态较多，降低了表面短波吸收的光生载流子的收集效率，因此在实验中没有观测到明显的短波响应度增强的现象。此外，当入射的波长大于某一阈值时，由于 pn 结和电场的深度随着注入能量的增大而加深，有利于该波长吸收产生的光生载流子的分离和收集，因此此处的长波的吸收效率被增强，这一现象被制备的器件测试数据所证实如图 4-4 (b)。

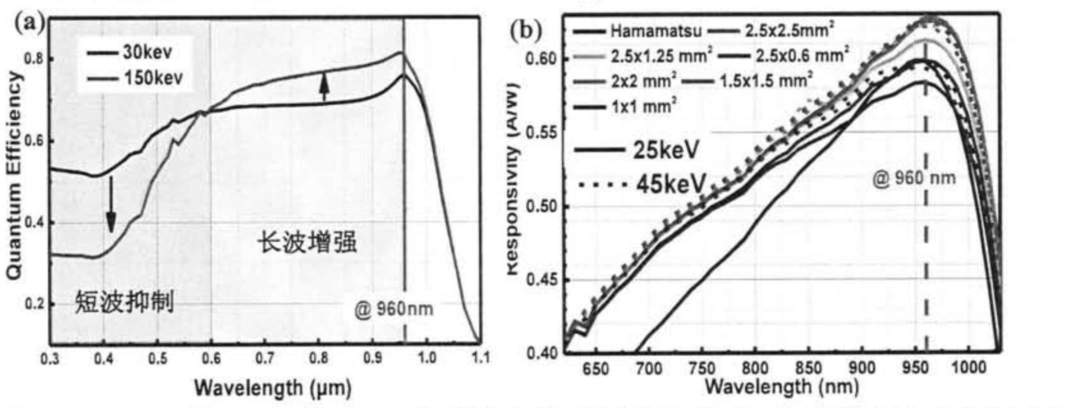


图 4-4 (a) silvaco 模拟 30keV 和 150keV 离子注入能量下器件的量子效率，(b) 制备的不同离子注入能量的器件长波响应度测试结果对比。

4.3 器件暗电流分析

通过以上对比研究可确定工艺参数对器件性能的影响，得到优化的器件制备参数。之后我们将选取其中有保护环的一组器件（主要工艺参数为：衬底：N 型 300μm 厚，阻抗范围在 1500~2500Ω；上表面离子注入：能量为 70keV，计量为 5e14 /cm^2；），基于器件尺寸，工作温度以及工作偏压与器件暗电流的关系曲线，分析器件的材料性能和光电性能，针对器件暗电流的主要影响机制优化器件结构。

4.3.1 基于器件尺寸的暗电流分析

根据暗电流与器件尺寸参数之间的关系，一般，对于 Si 基 Ge 异质结器件，外延层的线位错较多，体暗电流较大，器件的暗电流主要跟面积相关。对于晶格质量较高的台面器件，当台面刻蚀造成的侧壁缺陷态较多时，器件的暗电流主要跟周长相关。本论文研究的 Si-PIN 平面器件的暗电流较高，但是既不是异质结器件，又不是台面器件，影响暗电流的来源不清楚，因此设计了边长为 2.5mm，2mm，1.5mm，1.0mm，0.5mm，0.25mm 方形器件，测试得到暗电流如图 4-5(a)，其中边长为 2.5mm 器件的暗电流明显远大于其他器件，器件在-5V~-10V 之间存在突然上升的现象，推测是低偏压和高偏压下暗电流的主要影响机制不同造成的，当偏压高于-15V，暗电流趋于平坦缓变，因此暗电流的研究主要集中在-15V 以下。将 0V，-1V，-3V，-5V，-7V，-9V，-10V，-11V，-13V，-15V 处器件的暗电流提取出来，得到各个尺寸与暗电流关系点，如图 4-5(b)可以看出，0V 时，器件的暗电流近似，与器件尺寸关系不大；当工作偏压 0V<bias<-7V 时，暗电流随器件尺寸增大而增大，工作偏压高于-7V 后，暗电流与器件尺寸之间不再呈现单一关系。

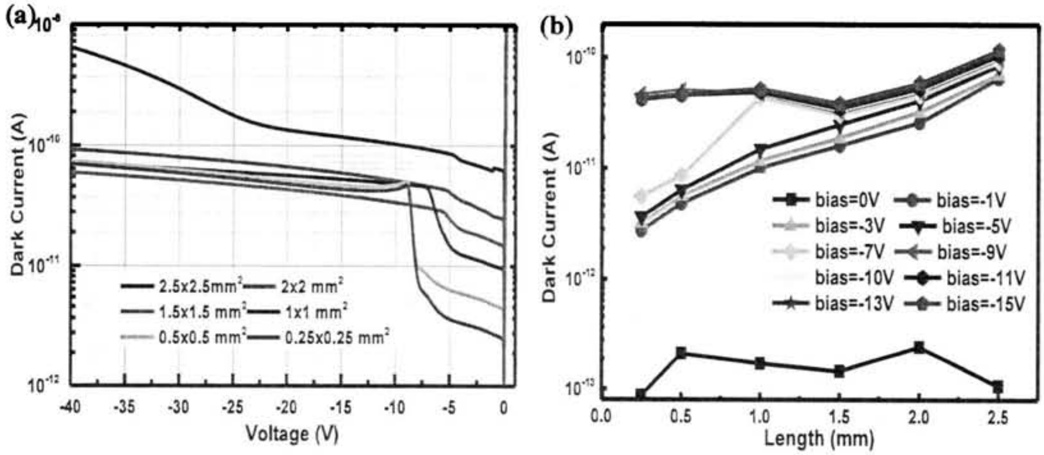


图 4-5 (a) 边长为 2.5mm，2mm，1.5mm，1.0mm，0.5mm，0.25mm 方形器件暗电流的 I-V 曲线。(b) 将 0V，-1V，-3V，-5V，-7V，-9V，-10V，-11V，-13V，-15V 处器件的暗电流提取出来，得到各个尺寸与暗电流关系点。

首先，我们研究低偏压的下暗电流和器件尺寸关系，拟合-1V，-3V 和-5V 时暗电流曲线，得到图 4-6，拟合系数不能为负，而边长 2.5mm 的暗电流过大，造成拟合系数为负值，因此判定边长 2.5mm 的暗电流为奇异点，因此在二次方曲线拟合是根据 0.25mm~2mm 测试结果得到的公式(4-13)，发现随着偏压的增大，与面积相关的暗电流比重在加大，分析此暗电流来源应该是：外加偏压的增大，拓宽了耗尽宽度，增大了产生-复合电流。

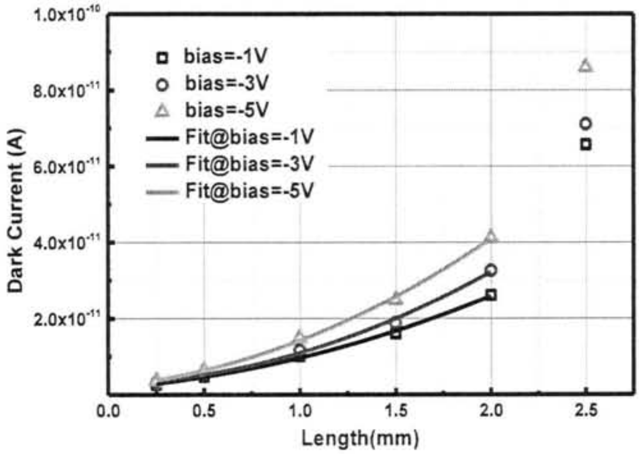


图 4-6 低偏压下器件尺寸与暗电流之间关系的拟合曲线。

$$
\begin{aligned}
I_{dark} &= (4.14449\times10^{-12})b^2+(3.79466\times10^{-12})b+(1.75412\times10^{-12}) \quad @-1V \\
I_{dark} &= (6.52758\times10^{-12})b^2+(1.66208\times10^{-12})b+(2.81697\times10^{-12}) \quad @-3V \\
I_{dark} &= (7.27132\times10^{-12})b^2+(4.79926\times10^{-12})b+(2.1852\times10^{-12}) \quad @-5V
\end{aligned}
\tag{4-13}
$$

其次，分析较高偏压下（≥ 9V）时，边长小于 1mm 的三个器件的暗电流呈现线性关系，即器件暗电流主要受到器件周长的影响，边沿漏电是小尺寸大偏压工作的器件主要暗电流来源。边长大于 1.5mm 的三个器件暗电流与边长，并不符合一次方拟合，此时器件的边沿和体内部对暗电流都有影响，但是需要更多的尺寸性能数据方可确定个因素的比例。

4.3.2 基于工作温度下的暗电流分析

由于暗电流的产生机理不同，其与器件的工作温度呈现不同关系曲线。

根据公式（4-1）得到，扩散电流与半导体材料的本征载流子浓度的平方成正比，由于

$$n_i=\sqrt{N_cN_v}\exp[-\frac{E_g}{2kT}]=A(\frac{T}{300})^{3/2}\exp(-\frac{E_g}{2kT}) \tag{4-14}$$

得到，扩散电流 J_{diff} ： $J_{diff}\sim n_i^2\sim T^3\exp(-\frac{E_g}{k}T^{-1})$ (4-15)

根据公式（4-2）得到，产生-复合电流与半导体材料的本征载流子浓度成正比，即：

产生-复合电流 J_g ： $J_g\sim n_i\sim T^{3/2}\exp(-\frac{E_g}{2k}T^{-1})$ (4-16)

缺陷态辅助隧穿电流 J_{tat}： $J_{tat}\sim T^{3/2}\exp(\frac{(q\hbar\xi_m)^2}{24m^*k^3}T^{-3})$ (4-17)

雪崩击穿机制形成的雪崩暗电流电流，是与温度无关的分量。

由图 4-5(b)可知，边长为 2.5mm，2mm，1.5mm 三个器件暗电流位置来源类似，边长为 0.25mm 和 0.5mm 两个小尺寸暗电流位置来源类似，因此研究暗电流与温度的关系时，仅选取边长为 2mm 和边长 0.5 mm 作为范例研究。

将 E_g=1.12eV=1.7944×10^{-19}J，k=1.38×10^{-23}J/K，ξ_m 为最大电场值，Si 材料的带间隧穿电场为 10^{6}V/cm[2]，计算时假设 ξ_m=10^{6}V/cm，带入数值得到扩散电流与温度：$J_{diff}\sim n_i^2\sim T^3\exp(-13003/T)$，产生复合电流与温度：$J_g\sim n_i\sim T^{3/2}\exp(-6501.6/T)$，缺陷态辅助隧穿电流与温度：$J_{tat}\sim T^{3/2}\exp(4673/T^3)$，因此，可根据以上算式得到理想条件下各个暗电流产生机制的电流密度与温度的关系曲线，如图 4-7。

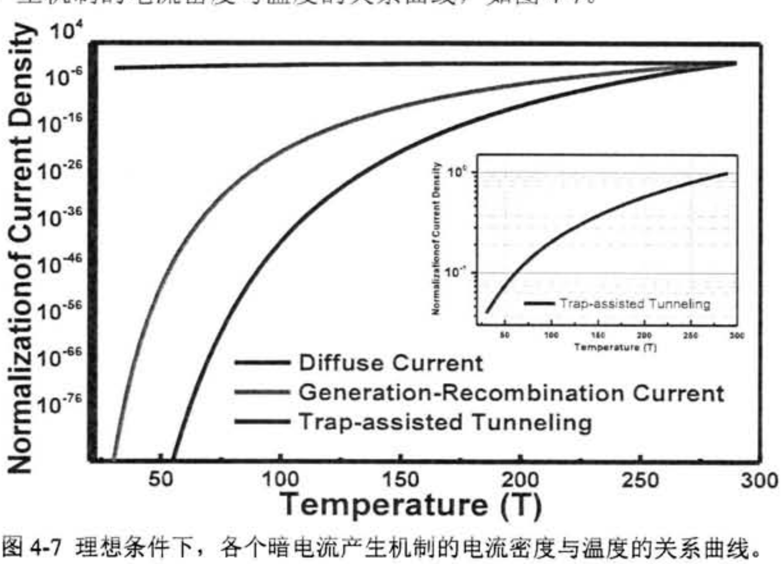


图 4-7 理想条件下，各个暗电流产生机制的电流密度与温度的关系曲线。

1. 边长 2mm 大尺寸器件温度与暗电流密度

利用 6K 闭循环制冷机将边长 2mm 和 0.5mm 的两个 Si-PIN 光电探测器的工作温度由室温 290K，逐渐下降到 30K，分别选取 290K，260K，230K，200K，180K，160K，140K，120K，100K，90K，80K，70K，60K，50K，40K，30K 温度下的器件，利用 4200-SCS 半导体特性分析系统测试分析器件反向偏压下的 I-V 特性曲线，如图 4-8 所示。可以看到同一尺寸不同工作温度下，当偏压增大到-15V 以后，器件的暗电流随着偏压遵循同一规律缓慢增大，因此，提取了 0V~-15V 之间几个关键偏压下器件暗电流随温度的变化趋势，如图 4-9 所示，0V 时器件的暗电流过小，达到了半导体测试设备的最小量程，因此暗电流浮动较大，没有规律；当工作偏压高于 0V 时，器件的 J-T 曲线又呈现出了低偏压和高偏压两种不同的规律，低偏压时，随着偏压的增大器件暗电流有明显提高，但是 J-K 曲线的变化趋势类似，当偏压大于某一阈值（-5V@2mm，-9V@0.5mm）后，器件暗电流随着偏压变化不大，J-K 曲线几乎重合。由此，我们研究具有代表性的两个点-3V 和-9V 两个点。

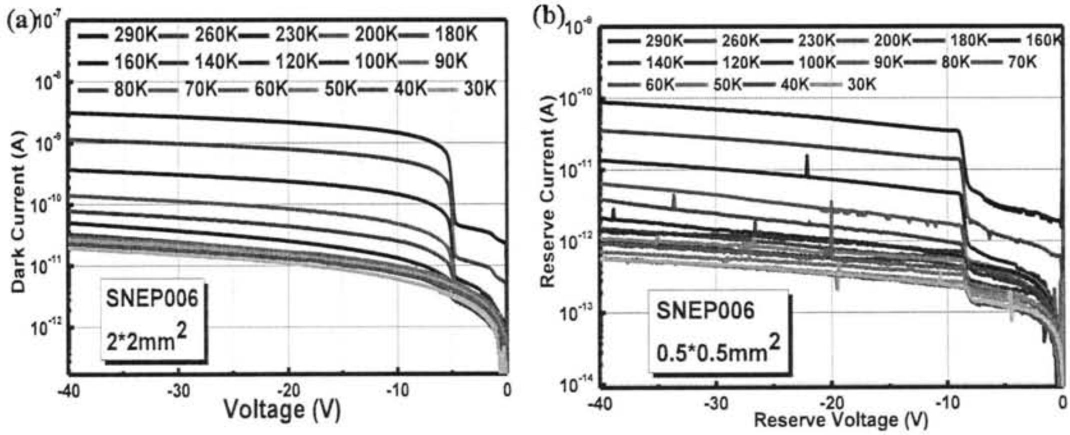


图 4-8 边长为(a) 2mm 和 (a) 0.5mm 方形器件在反偏，不同工作温度下的暗电流 I-V 特性曲线。

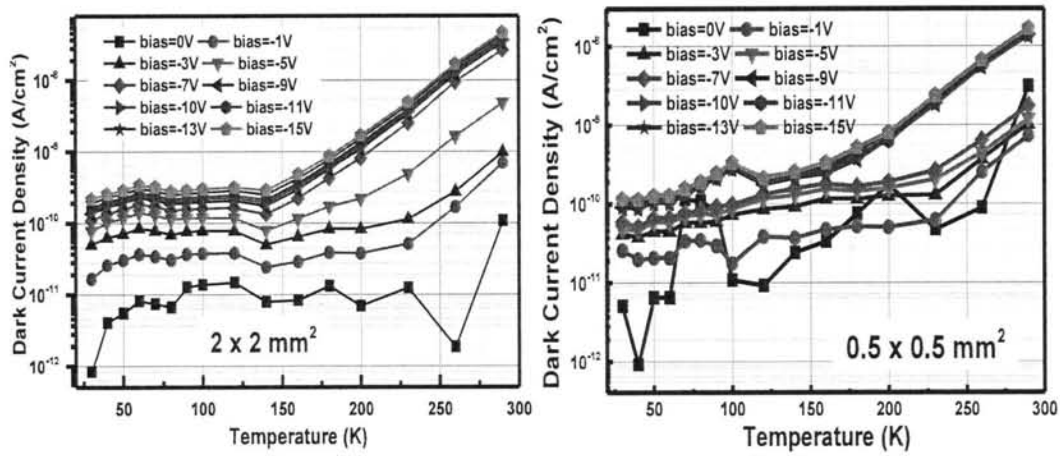


图 4-9 器件工作在 0V，-1V，-3V，-5V，-7V，-9V，-10V，-11V，-13V，-15V 时器件的暗电流随温度的变化趋势。

通过对这-3V 和-9V 偏压下的两种尺寸的 Si-PIN 光电探测器归一化的 J-K 曲线，并对比四种机制（扩散，产生-复合，缺陷态辅助隧穿，雪崩）作用下器件的归一化 J-K 曲线，如可推测：

(1) 在低工作温度（<50K），缺陷态辅助隧穿是器件暗电流的主要来源，对于大尺寸 2mm 器件这一现象尤为明显，实际测试结果几乎和缺陷态辅助隧穿电流趋势重合。

(2) 在高工作温度（>150K），产生-复合机制产生的暗电流占主导，而且大的工作电压增大载流子的收集效率，这种产生-复合暗电流趋势尤为明显。

(3) 工作温度在 50K~150K 之间时，器件暗电流与温度之间的变化关系不明显，比较接近雪崩击穿暗电流的 J-K 特性曲线趋势，推测是器件载流子分布不均，或者内部局域缺陷态造成局域电场过高达到雪崩电场，从而造成暗电流与温度关系不明显的现象，但是这一结论，需要进一步的测试才能确定。

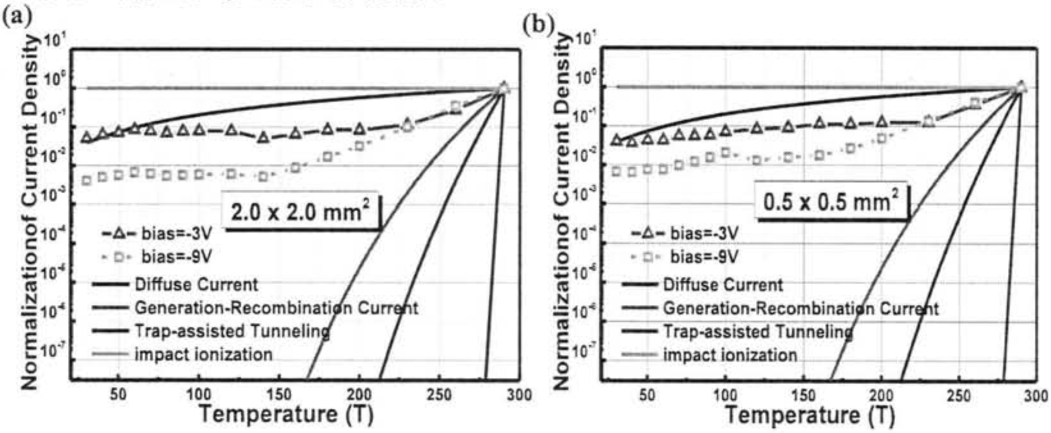


图 4-10 -3V 和-9V 偏压下的(a)边长 2mm 和(b) 边长 0.5mm 两个器件 J-K 的归一化曲线，与四种机制（扩散，产生-复合，缺陷态辅助隧穿，雪崩）作用下器件的归一化 J-K 曲线对比。

4.3.3 基于工作偏压的暗电流分析

暗电流的产生机理还造成不同的暗电流组成与器件的工作偏压呈现不同关系曲线。根据公式(4-1)得到，扩散电流与器件的工作偏压呈 e 指数关系，即：$J_{diff} \sim \exp(\frac{qV}{kT})-1$ (4-18)

根据公式(4-2)得到，产生-复合电流与 pn 结的耗尽宽度成正比，理想的 PIN 结构探测器的耗尽区宽度为 I 区厚度，与偏压无关，因此产生-复合电流 J_g ：$J_g \sim \exp(\frac{qV}{2kT})$ (4-19)

缺陷态辅助隧穿电流 J_{tat}：$J_{tat} \propto V_R\sqrt{\psi_{bi}+qV_R}\exp(-C_1(\psi_{bi}+qV_R)^{-1/2})$　　(4-20)

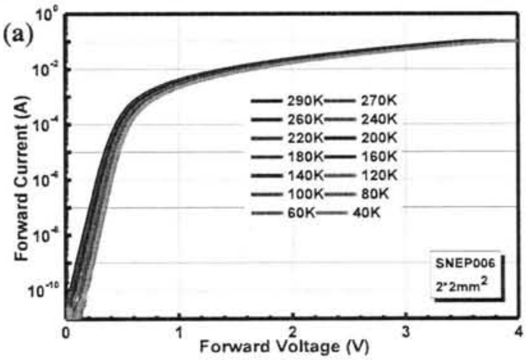
雪崩击穿机制形成的雪崩暗电流电流，主要与倍增系数和离化率比值相关，而倍增系数是有方向偏压值决定，离化率比值也受到工作偏压的影响，

当器件加反向偏压时，（qV/kT）为一负值，$exp(qV/kT)$是一个远小于 1 的小量，因此主要影响反向偏压的 J-V 特性的因素是缺陷态辅助隧穿电流，而当外加偏压继续增大，器件发生击穿，此时的电流瞬间增大，与电压没有特定的关系，因此通过 I-V 关系曲线研究暗电流的来源，意义不大。

研究 I-V 关系曲线来获得电流来源时，器件是通常工作在正向偏置状态下。此时为了研究正向电流与温度的关系，引入了理想因子(η)的定义：

$$\text{正向电流：} J_{forward} \sim \exp(\frac{qV}{\eta kT}) = \exp(11604 * \frac{V}{\eta T}) \tag{4-21}$$

由上面的公式可知，当外加偏压不变时，随着温度的增大，正向电流是减小的，因此温度和正向电流是负相关的，由图 4-13 的测试结果可知，150K~180K 之间器件呈现电流和工作温度成负相关，其他温度下都是正相关，这个正相关的关系能够说明在正向低偏压时，器件的缺陷态辅助隧穿是暗电流的主要来源。图 4-13 中不同正向偏压下的 J-K 曲线可近似看做温度的一次方函数，复合了缺陷态辅助隧穿与偏压的关系，当正向偏压高于 1.5V 时，正向电流很大，受到 T 影响很小，在正向偏压低于 1V 时，温度以 180K 为分界点，两边的拟合曲线不同，工作温度越高，拟合曲线的斜率越大，参与到缺陷态辅助隧穿过程的缺陷态密度越大。



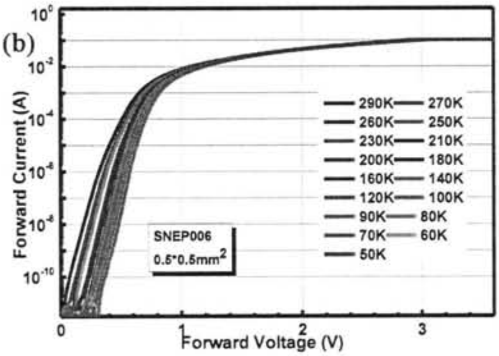


图 4-11 边长为(a) 2mm 和 (a) 0.5mm 方形器件在正向偏置，不同工作温度下的暗电流 I-V 特性曲线。

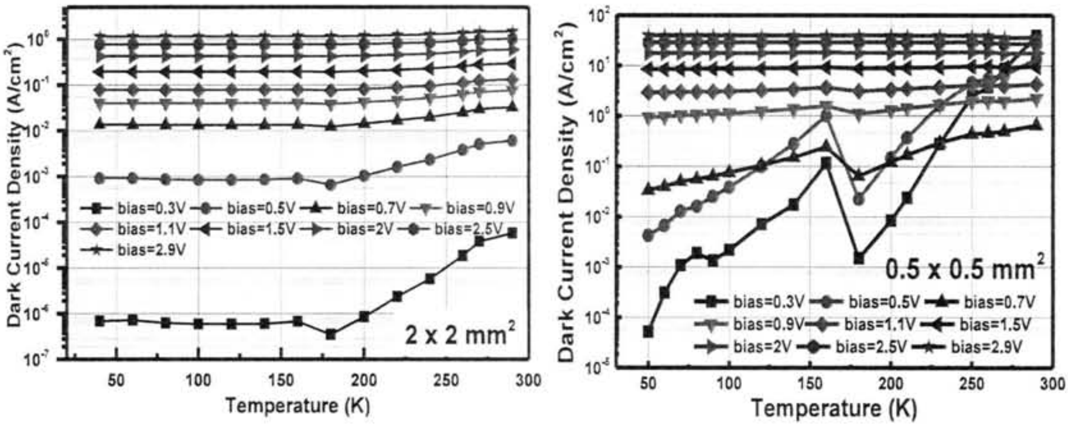


图 4-12 器件工作在 0.3V，0.5V，0.7V，0.9V，1.1V，1.5V，2V，2.5V，2.9V 时器件的暗电流随温度的变化趋势。

4.4 本章小结

本章首先介绍了 Si-PIN 结构探测器基本原理和应用，分析了器件暗电流的产生机理；其次介绍了在 ISO9001-2000 质量体系认证的五英寸 2μm 标准 CMOS 工艺加工线上制备的 Si-PIN 的结构和关键工艺，通过对比有无保护环以及光敏面不同注入能量下 Si-PIN 器件的暗电流和响应度，分析器件制备工艺参数对器件性能影响的物理机制；最后分别讨论了器尺寸、器件的工作温度、器件的工作偏压对器件的暗电流影响，确定了不同尺寸器件来源的机制以及位置，为进一步优化暗电流性能提供了基础。

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第五章 结论

本论文主要研究光电探测器的灵敏度，由灵敏度的定义和计算公式得到提高灵敏度的三个主要方法是：提高光响应，放大光电流以及降低暗电流。针对三种不同结构不同材料和不同应用领域的硅基光电探测器，分析它们的应用需求和结构特点，结合它们现今的发展现状，指出这三种器件要获得高灵敏度的器件性能需要各自解决的问题。这对这些问题，提出了研究和优化方案，得到的结论如下：

4. 低的响应度是限制 Ge/Si 垂直入射型 UTC 器件灵敏度的主要因素，利用 SOI 衬底 BOX 和 Si 层的高折射率差，设计 Si 层和 BOX 层厚度，得到入射光波长为 1550nm，锗在该波长的吸收系数为 1000/cm，Si 材料的厚度对吸收效率的影响呈现周期变化，最高的吸收效率为 0.167，Si 材料厚度周期为 0.223μm。通过原位掺杂外延梯度掺杂的 p 型吸收层，研制出高响应的 Ge/Si 垂直入射型 UTC 器件，在 1550nm 入射下光响应 R 为 0.18A/W，量子效率为 14.4%。在-1V 偏压下的暗电流密度最小为 61.9 mA/cm^2，3-dB 带宽最大为 9.73GHz @直径 15μm；直径 40μm 器件，带宽 2.55GHz，在 1GHz 的调制频率下，饱和输出射频为 4.6 dBmW，对应的饱和电流为 16.24mA；直径 18μm 器件，带宽 7.23GHz，在 3GHz 的调制频率下，饱和输出射频为 3.7 dBmW，对应的饱和电流为 16.22mA。

5. 耦合效率和倍增效率的相互制约是限制 Ge/Si WG SAM 结构雪崩器件灵敏度提高的主要因素。设计新型的纳米结构：将倍增层横向放置到 Si 波导层，获得高耦合效率和高倍增因子。计算耦合光栅的周期为 630nm，占空比 50%，光栅槽刻蚀深度 70nm，耦合角度：8°，光耦合效率为 49%@1550nm。Ge 材料的长度达到 10μm，厚度为>0.4μm，倏逝波耦合效率达到 93%以上。电荷层界面尺寸是 0.22μm×0.4μm，p 型掺杂浓度为 1×10^7/cm^3 时，器件能获得大倍增系数（>10^3）和低的过剩噪声，对 SiO_2 掩膜层刻蚀的时间和条件进行了实验，得到刻蚀槽的宽度低于 0.9μm 以后，刻蚀速率随着刻蚀空线宽的减小而降低，器件外延层宽度为 0.5μm，刻蚀速率为~100 nm/min。

6. 高的暗电流是限制 Si-PIN 探测灵敏度的关键因素，通过保护环的设计可以有效的降低器件的周围的扩散电流。对比光敏面的离子注入能量为 25keV 和 45keV 的器件，45keV 较高能注入造成表面缺陷态的增大，表面漏电增大，650nm~950nm 之间的响应度也较高。边长为 2.5mm，2mm，1.5mm，1.0mm，0.5mm，0.25mm 方形器件，当工作偏压 0V<bias<-7V 时，暗电流（I_{dark}）随器件的边长（b）在-1V 偏压下的关系式：$I_{dark}=(4.14449\times10^{-12})b^2+(3.79466\times10^{-12})b+(1.75412\times10^{-12})$，工作偏压高于-7V 后，边长<1mm 的器件暗电流与边长呈现 1 次方关系，说明此时边沿漏电远高于体漏电。工作温度

<50K，缺陷态辅助隧穿是器件暗电流的主要来源；工作温度>150K，产生-复合机制产生的暗电流占主导。通过正向偏置的偏压、温度以及暗电流的关系推测，器件的缺陷辅助电流是正向工作时的主要暗电流来源。

灵敏度一直是半导体光电探测器研究的重点，灵敏度的研究呈现多样性和复杂性：Ge/Si UTC 器件的响应度和灵敏度的再提高，则需要将其设计为波导耦合型光入射，提高响应度较小器件尺寸，提高器件带宽以及芯片集成度；Ge/Si WG SAM 结构雪崩器件的灵敏度的研究在解决了耦合与倍增问题后，要研究的就是降低噪声，通过研究离化率比和过剩噪声来降低暗电流和噪声。Si-PIN 探测灵已经知道了其暗电流的来源，下一步是优化器件结构，屏蔽或抑制暗电流来源。

致谢

本出站报告是在郭霞教授的悉心指导下完成，是我这两年在北京工业大学博士后流动站工作的总结，此次的总结系统的梳理了我这俩年来的所学所想，令我发现自己在工作和处事中还有很多不足和待改进的地方。因此我衷心的感谢合作老师郭霞教授在工作和科研上提供指导和帮助。

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李 冲

2016 年 7 月

博士期间发表的学术论文清单

1. **Chong Li**, Chunlai Xue, Zhi Liu, Buwen Cheng, Chuanbo Li and Qiming Wang, "High-Bandwidth and High-Responsivity Top-Illuminated Germanium Photodiodes for Optical Interconnection Electron Devices", IEEE Transaction on Electron Device,.60(3): 1183-1187, 2013.

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2. **国家“863”计划子课题**，2015AA017101，1310nm 波段 4×25Gb/s 激光器和探测器阵列芯片、2015/01-2017/12、73 万元、在研、子课题负责人

3. **北京市教委科技计划一般项目**，硅基锗波导雪崩光电探测器电场调控及工作模式研究、2016/01-2018/12、15 万元、在研、主持

4. **中国博后基金**，吸收倍增分离型 Si/Ge 波导雪崩探测器件研究，2015/10-2016/07、5 万元、在研、主持

5. **北京市博士后资助**，波导吸收倍增分离型 Si/Ge 雪崩探测器的研究，2015/05-2016/07、4 万元、在研、主持

High-responsivity vertical-illumination Si/Ge uni-traveling-carrier photodiodes based on silicon-on-insulator substrate

Chong Li, ChunLai Xue, Zhi Liu, Hui Cong, , Buwen Cheng, Xia Guo, and Wuming Liu

Si/Ge uni-traveling carrier photodiodes exhibit higher output current when space-charge effects are overcome and thermal effects are suppressed, which is highly beneficial for increasing the dynamic range of various microwave photonic systems and simplifying high-bit-rate digital receivers in different applications. From the point of view of packaging, detectors with vertical-illumination configuration can be easily handled by pick-and-place tools and are a popular choice for making photo-receiver modules. However, vertical-illumination Si/Ge uni-traveling carrier (UTC) devices suffer from inter-constraint between high speed and high responsivity. Here, we report a high responsivity vertical-illumination Si/Ge UTC photodiode based on a silicon-on-insulator substrate. The maximum absorption efficiency of the devices was 2.4 times greater than the silicon substrate owing to constructive interference. The Si/Ge UTC photodiode was successfully fabricated and had a dominant responsivity at 1550 nm of 0.18 A/W, a 50% improvement even with a 25% thinner Ge absorption layer.

Index Terms—**high-responsivity, silicon-on-insulator substrate, saturation, germanium, uni-traveling-carrier photodiode.**

Introduction

1High-current photodiodes, which receive communication signals in the near-infrared range, are highly beneficial in various photonic systems for increasing their dynamic range[1][2] and simplifying high-bit-rate digital receivers[3]. The output radio-frequency signal level from such photodiodes can be increased with the response photocurrent, and are thus a particularly important component for optically-steered phased array antennas, which can help the antenna to reduce its phase- and amplitude-matched electronic gain [4,5,6]. However, the conventional pin structure has a limitation in current density during high frequency operation, owing to the space-charge effect [7,8].

The uni-traveling carrier (UTC) structure was designed to overcome the space-charge effect and increase the transition frequency using a p-type doped absorption layer instead of a conventional intrinsic layer [9,10,11,12,13,14]. However, the output power of these devices was further limited by thermal effects [15,16]. Monoatomic crystals of materials such as Ge and Si material have higher thermal conductivity than that of InGaAs and InP alloy materials [17]. Additionally, Si/Ge devices have great advantages in their compatibility with complementary metal-oxide-semiconductor (CMOS) technology and large-scale monolithic integration circuits, low cost, and low power consumption [18,19,20,21,22]. Therefore, Si/Ge uni-traveling carrier photodiodes have dramatic practical potential for high-current output applications [23,24]. Besides, from the point of view of packaging, detectors having a vertical-illumination configuration can be easily handled by pick-and-place tools and are consequently a popular choice for making photo-receiver modules [25,26]. Therefore, the most commonly-used photodetectors are of the vertical-illumination type. To our knowledge, the best performance obtained for a vertical-illumination Si/Ge UTC device until now was reported by M. Piels, who demonstrated a low thermal impedance of 520 K/W and a 1 dB saturation photocurrent of 20 mA. However, the responsivity of this device at 1550 nm was as low as 0.12 A/W with a 0.8-μm-thick Ge absorption layer [24]. Such a low responsivity could seriously increase power dissipation and limit high-output applications. Although increasing the thickness of the Ge absorption layer could improve the responsivity of the device according to $R \propto (1-e^{-\alpha D})$ [27], the electron transit time also increases with Ge thickness, which decreases device response speed [28]. Therefore, it is a challenge to obtain both high responsivity and high speed at the same time in vertical-illumination Si/Ge UTC detectors.

Silicon-on-insulator (SOI) substrates have great advantages that can improve the responsivity and bandwidth performance of Si/Ge photodiodes. First, the large difference in refractive index between the buried oxide layer (BOX) and the Si is beneficial in recycling transmission light back to the absorption layer, which is equivalent to extending the absorption length. This allows the absorption efficiency of the photodiodes to be increased without sacrificing the response speed. Second, high quality Ge film with low threading dislocation density (TDD) can be obtained on the top silicon membrane of SOI by elastic deformation, and adapt to the lattice of a hetero-epitaxial file grown upon it [29,30]. The threading dislocations inside the Ge layer can decrease carrier lifetime and increase the non-radiative recombination rate [31,32], which can reduce the number of photon-generated carriers collected by the metal contacts. Therefore, the carrier collection efficiency of the device may be enhanced using a SOI substrate. Third, use of a SOI substrate could reduce the parasitic capacitance of the device, which would result in an improvement in frequency response performance[33,34] and a decrease in power loss [35].

Here, we report a high-speed, high responsivity vertical-illumination Si/Ge UTC-PD based on a silicon-on-insulator (SOI) substrate. The silicon-on-insulator substrate was used to reflect transmission light for high absorption efficiency, and to improve the lattice quality of the Ge epitaxial layer to increase the efficiency of photon-generated carrier collection. The absorption efficiency of the Ge-on-SOI UTC photodiode was found to vary periodically with the thicknesses of both the BOX and Si layers, owing to the interference between the incident light and the light reflected by the BOX layer of the SOI. Moreover, the maximum absorption efficiency of the devices on SOI was found to be 2.4 times greater than that of the silicon substrate and 4.9 times greater than the minimum absorption efficiency. Si/Ge UTC photodiodes on SOI substrate with a 0.6-μm-thick Ge absorption layer were fabricated and characterized. The responsivity of the photodiodes at 1550 nm was improved to 0.18 A/W.

The −1-dB compression current of the 15-μm-diameter device was 16.2 mA at 3 GHz, with a 3-dB bandwidth of 9.73 GHz.

Results:

Structure and electric field. Figure 1(a) shows a cross-sectional schematic view of a Si/Ge UTC photodiode based on a commercially available SOI substrate with 1.0-μm-thick n-doped Si and 2-μm-thick BOX layers. A step gradient doping profile was employed, which enabled the generation of several regions with high local electric field to further decrease the transit time of the photo-generated electrons, as the red curve shown in Fig. 1(b). A simulated band-gap diagram and electric field distribution at 0 V of such a device are illustrated in Fig. 1(b) by the blue and red curves, respectively, calculated after modifying the doping parameters according to the results of secondary ion mass spectrometry (SIMS) measurements. The built-in electric field was generated from the differences in the doping concentration. Each abrupt change in doping concentration corresponded to an electric field peak. The photon-generated electrons were accelerated in the Ge absorption layer and gained kinetic energy to pass through the Si/Ge heterojunction barrier under the action of the built-in electric field. A larger electric field and thus lower transit time can be obtained compared with those achievable with conventional linear gradient doping of the absorption layer [36,37,38]. A micrograph of a photodiode with a 15-μm-diameter top mesa is shown in the inset of Fig. 1(a).

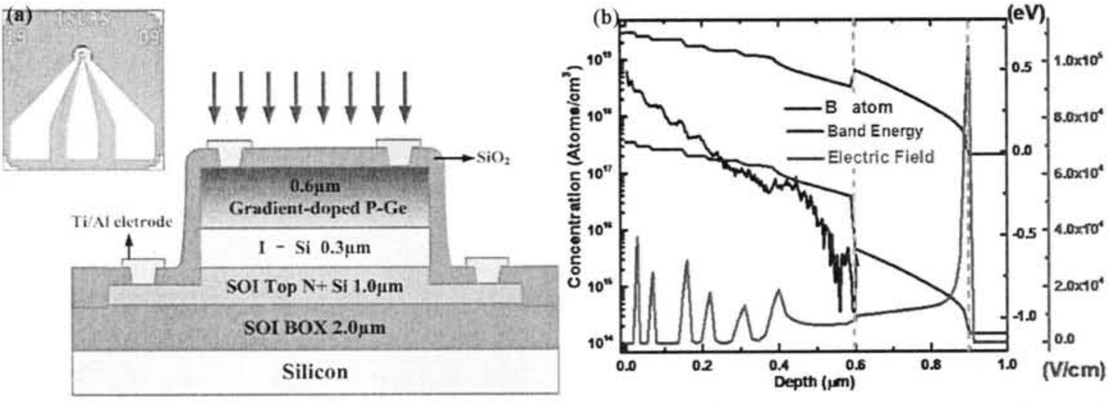

Fig. 1 (a) Cross-sectional schematic view of the reported Ge-on-SOI UTC photodetector and top view of a double-mesa structure of the Ge-on-SOI UTC photodetector. The substrate was SOI with a 1.0-μm-thick n-doped top Si film and a 2-μm-thick BOX layer, the collect layer was a 0.3-μm-thick intrinsic epitaxial silicon layer, and the absorption layer was a 0.6-μm-thick epitaxial germanium layer with step gradient doping of B atoms. (b). The left black coordinate and curve show that the doping concentration of B atoms in the Ge absorption layer step decreased from 5×10^{19} to $2 \times 10^{17}/cm^3$, as determined by SIMS. The etch step was nearly 0.05 μm wide, resulting in six high local electric fields to accelerate the photon-generated electrons and shorten the transmit time. The right red and blue coordinates show the electric field and band energy of our devices without bias, respectively. The peak value and width of the six local electric fields were determined by the doping concentration around the step interfaces. According to our simulation, six step gradients in the absorption layer enabled a maximum potential difference across the layer.

Responsivity characterization. The responsivity of a vertical-illumination photodiode is limited mainly by a combination of three factors: (1) the coupling efficiency determined by the top anti-reflection coating; (2) the absorption efficiency of the Ge layer; (3) the collection efficiency of the photon-generated carriers [39]. The former two factors can be optimized through the structural design of the devices. The last one is mainly determined by the quality of the epitaxial crystalline Ge and the electric field inside the devices. Generally, only the light coupled into the absorber (P_0) can be converted into electron-hole pairs. To maximize the coupled light, the thickness of the top anti-reflection coating should be N·(λ/4n), according to destructive coherence inside the coating, where N is a positive integer, and n is the refractive index of the coating [40]. The carrier collection efficiency of Si/Ge UTC photodiodes is mainly determined by the design of the electric field inside the devices and by the recombination caused by defects inside the Ge layer and at the hetero-interface [41,42].

Absorption efficiency is generally dependent on the absorption coefficient and thickness of the absorption layer. The absorption coefficient of Ge is relatively low at 1550 nm, which is near the band-gap edge. The power inside the absorption layer P_{ab} can be expressed by $P_{ab}=P_0(1-e^{-aD})$, where α is the absorption coefficient of the absorber and D is thickness of the absorber. The introduction of the SOI substrate was expected to cause recycling of the transmission light and improve the light absorption of the device. The new absorption power is:

$$P_{ab}=P_0(1-e^{-aD})+P_0\cdot e^{-aD}\cdot R_{ref}\cdot(1-e^{-aD}) \tag{1}$$

where R_{ref} is the reflection coefficient of the SOI substrate, and R_{ref} is the reflection coefficient of the top coating film and Ge film. The detailed optical power distributions in the Si/Ge UTC photodiodes on the Si and SOI substrates were compared by simulation with the commercial finite-difference-time-domain (FDTD) simulation package, as shown in Fig. 2. The scale bar illustrates the optical power. The optical power inside the Si bottom layer of the SOI substrate is obviously much lower than that in the silicon substrate, which indicates the unemployed or transit light power of the devices. Therefore, SOI substrate is more beneficial to higher light absorption by Ge through reflection of the BOX compared with the Si substrate.

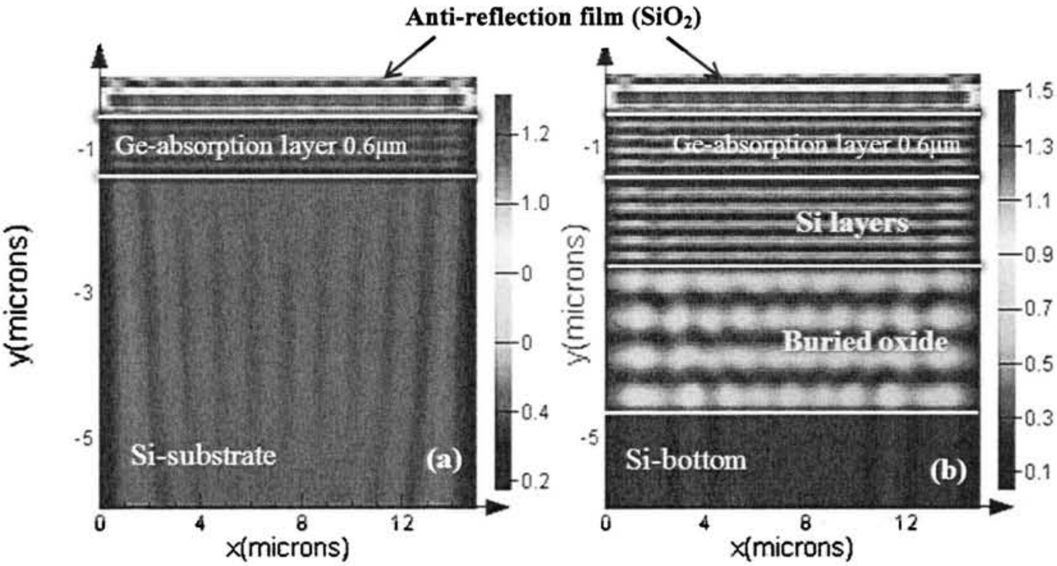

Fig. 2. Optical power distribution inside Si/Ge UTC devices grown on (a) Si substrate and (b) SOI substrate. The only difference between the two devices was the inserted 2-μm-thick BOX layer, and the thickness of the silicon collection and contact layers was 1.3 μm. The scale bar illustrates the optical power. Because of the coherence effect between the incident light and reflected light of the BOX layer, the optical power inside the Ge, Si, and BOX exhibited a periodic enhancement distribution. The period was determined by the refractive index and the wavelength of the incident light. The light inside the Si bottom layer of the SOI substrate and inside silicon substrate was the unemployed light of the devices. Obviously, that in the SOI was much lower than that in the silicon substrate. Thus, the SOI substrate was more beneficial for higher light absorption by Ge, compared with the Si substrate.

The relationship between the absorption efficiency and the thickness of the BOX and silicon layer was analysed and calculated according to the SMM using Matrix Laboratory (MATLAB). When the thickness of the anti-reflection coating was fixed, the absorption efficiency varied periodically with the thicknesses of both BOX and Si, shown in Fig. 2. The absorption efficiency of the device without BOX was 0.092 with a 0.6-μm-thick coating film, but the maximum obtained was 0.217 with a 1.1-μm-thick Si layer and a 1.85-μm-thick BOX, more than double. However, the general thickness of the BOX layer in commercial SOI substrates is 2 μm. Because of the constructive interference between the reflected and input waves, the thickness period (T) is $T = \lambda/2n$, where λ is the input wavelength and n *is* the refractive index of the transmission media. Here, the silicon thickness cycle was 0.223 μm with a Si thickness of 1.3 μm, i.e., the structural parameters of our device as shown in Fig. 1(a). Thus, theoretically, the maximal absorption efficiency is about 0.168, and the ideal responsivity is 0.208 A/W without photon-generated carrier recombination.

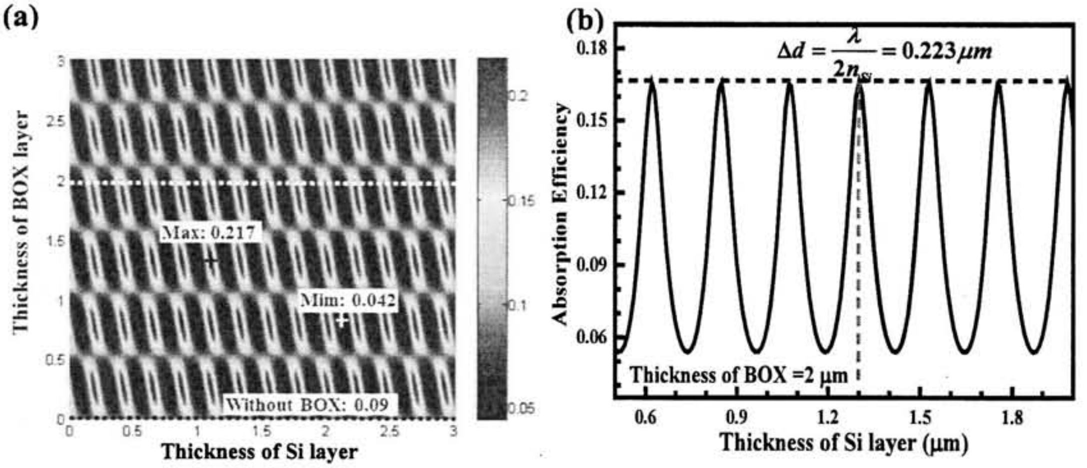

Fig. 3 The wavelength of the incident light was 1550 nm, and the absorption efficiency of the Ge material was 1000/cm. (a) Relationship between the absorption efficiency of Ge-on-SOI UTC photodiode and the thicknesses of the BOX and silicon layers. Using these thicknesses of the BOX and silicon as ordinate and abscissa, respectively, the absorption efficiency is mapped in colored points in a two-dimensional coordinate plane. The bottom black dashed line represents the absorption efficiency of the devices without BOX layer, which was 0.09. The other two special points are the maximum of 0.217 with a 1.1-μm-thick Si layer and a 1.85-μm-thick BOX, and the minimum of 0.044 with a 2.13-μm-thick Si layer and a 1.32-μm-thick BOX. (b) Relationship between the absorption efficiency and the thickness of the silicon layer, when the thickness of the BOX is the general commercial value of 2 μm. The absorption efficiency changes periodically with the thickness of Si layer because of constructive interference. The period is $T = \lambda/2n$, which is 0.223 μm for the silicon layer, and the maximum efficiency is 0.168 when the silicon thickness is 1.3 μm, which is the structural parameter of our device.

The experimentally determined device current for the 15-μm-diameter photodiodes, without illumination and with the normally incident light on the top surface, is shown in Fig. 4. The dark current was 58 nA under a reverse bias of 1 V, which corresponds to a current density of 96.3 mA/cm^2. The minimum dark current density was approximately 61.9 mA/cm^2 for the 40-μm-diameter device at −1 V. The dark current could be further reduced by appropriate thermal processing to decrease the threading dislocation density around the Si/Ge interface[11][12], by the passivation process, or by the application of a guard-ring around the sidewall.

At a reverse bias of 1 V, the optical responsivity was 0.18 A/W at 1550 nm with a 0.6-μm-thick Ge layer, 50% higher than that of the existing Si/Ge UTC devices, which is R=0.1 A/W with a 0.8-μm-thick Ge layer[7]. In Fig. 4, the mismatch between the dark and optical currents between 0.7 V and 0.3 V arose from the diffusion and collection of the photo-generated carriers because of the gradient doping of B and P atoms in the actual epitaxial layers. Because of the carrier recombination, this measurement responsivity is little lower than the former theoretical results.

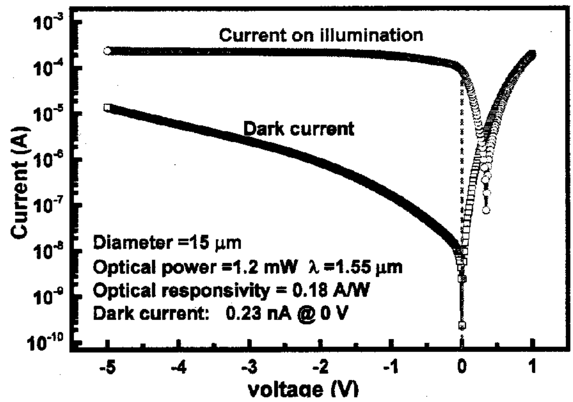

Fig. 4. Current-voltage characteristics of the 15-μm-diameter device without illumination and under laser irradiation with an input optical power of 1.2 mW at 1550 nm. The dark current without bias was 0.23 nA. When the reverse bias was increased to 1 V, the dark current rose to 58 nA, corresponding with a current density of 96.3 mA/cm. The optical responsivity was 0.18 A/W at 1550 nm. The dashed line indicates that there was a saturation of the optical responsivity values at 0 V bias, which indicates that this photodetector configuration allowed nearly complete photo-generated carrier collection without bias.

3-dB bandwidth characterization. The bandwidth of common photodiode is limited mainly by the resistor–capacitor (RC) bandwidth (f_{RC}) and the carrier transit-time-limited bandwidth (f_t) in the active region [43]. Particularly, for UTC devices, the most important limitation is the transfer time of electrons in the p-type absorption layer owing to their low diffusion velocity in it. Based on the principle of conservation of energy, the electrical potential difference across the absorption layer determines the change in kinetic energy of the carriers. A high kinetic energy in the absorber could shorten the transfer time of the electrons. Based on the direct relationship between the doping difference across the doped junction and the electrical potential difference, a step gradient-doping region was introduced in the absorption layer to increase the potential difference across the Ge layer. We can assume that the photo-generated electrons drifted with saturation velocity (v_s) in the p-type absorption layer of our devices owing to the high potential drop across the absorber, and then across the collection layer with thermionic emission velocity (v_{th}), because of the effect of the thermionic emission [6]. Then, the carrier transit frequency can be approximated by the following equation:

$$f_t = 1/(2\pi\tau_a) = 1/(W_a/v_s + W_c/v_{th}) = 1/(W_a/v_s + W_c/\sqrt{2kT/\pi m_e^*}), \tag{2}$$

where v_{th} is the thermionic emission velocity, v_s is the saturation velocity, and m_e* is the effective mass of the electrons. The capacitor in the absorption layer is ignored, so f_{RC} can be approximated using:

$$f_{RC} = \frac{1}{2\pi(R_s + R_L)C} = \frac{1}{2\pi(R_s + R_L)\cdot\frac{\varepsilon\varepsilon_0\pi D^2}{4W_c}}, \tag{1}$$

where W_c is the collection layer thickness, W_a is the absorption layer thickness, D is the mesa diameter, R_L is the load resistance (50 Ωin this case), R_S is the series resistance, and ε and ε_0 are the relative and vacuum permittivity, respectively. If the series resistance of the device is about 100 Ω, which was the measured resistance of our devices equal to the slope of I-V curve at the positive bias of nearly 0.26 V [44]. The theoretical values of f_{3dB} with various diameters are shown in Fig. 5(a). The results are almost consistent with the experimental results except for the 15-μm-diameter device, as shown in Fig. 5(b). Therefore, the step gradient-doping design was able to make the carriers drift in the absorber with a saturation velocity and efficiently increased the transit frequency of the UTC photodiodes. The different result observed for the 15-μm-diameter device may be from the higher series resistance of smaller size devices caused by the fabrication processes.

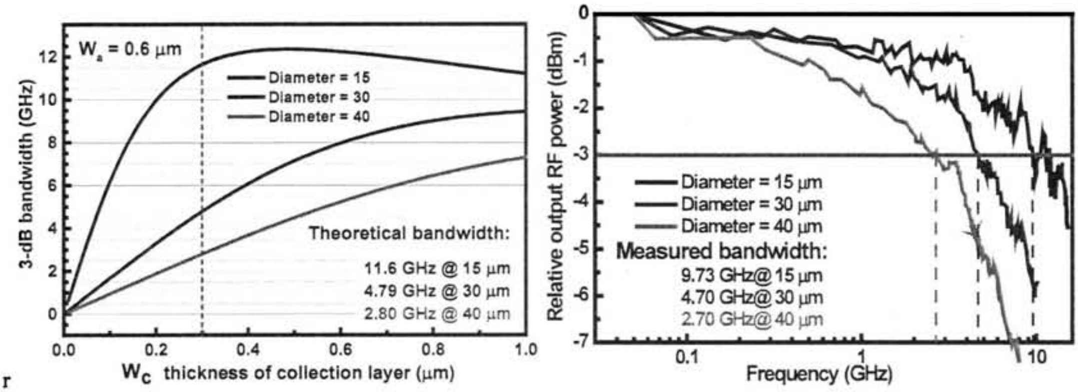

Fig. 5. Frequency responses for UTC photodiodes with diameters of 15, 30, and 40 μm under 1550 nm incident light: (a) theoretically predicted values for a series resistance of 100 Ω, which was measured using the slope of the I-V curve at the positive bias of ca. 0.26 V and on the assumption that the photo-generated electrons traveled across the p-type absorption layer by drifting with saturation velocity (v_s), and across the collect layer by drifting with thermionic emission velocity (v_{th}). (b) The 3-dB bandwidth was measured with a vector network analyser. The theoretical f_{3dB} values are almost consistent with the experimental results except for the 15-μm-diameter device, whose difference may have resulted from the higher series resistance of smaller size devices caused by the complicated fabrication processes.

Saturation characterization. The device saturation current was obtained using large signal measurements, as shown in Fig. 6. A 100% modulation depth tone was fixed at 3 GHz for measurement of the 15-μm-diameter device. The fabricated devices exhibited high saturation photocurrents. The 1-dB compression currents were measured to be 16.2 mA at reverse bias voltages of −6 V. For the 40-μm-diameter device with a 3 dB bandwidth of 2.7 GHz, the saturation current was 16.24 mA with a fixed modulation frequency of 1 GHz under −7 V bias, and the RF output power was 4.6 dBmW. The saturation of the Ge-on-SOI UTC photodiodes could be further improved by suppressing thermal effects [45,46] by substrate thinning and decreasing the thickness of the BOX layer.

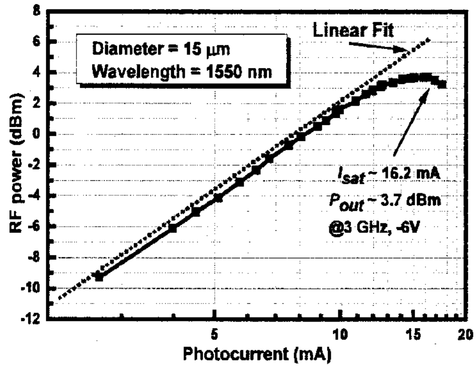

Fig. 6. Results of large signal −1-dB compression photocurrent measurement for the 15-μm-diameter Si/Ge UTC photodiodes. The incident light had a wavelength of 1550 nm, 100% modulation depth, and modulation frequency fixed at 3 GHz. The saturation current was 16.2 mA at a reverse bias of 6 V, and the output RF power was 3.7 dBmW. The saturation current and RF power were further increased with the reverse bias.

Discussion

The demonstrated on-chip performance of the present high-responsivity vertical-illumination Si/Ge uni-traveling-carrier photodiodes paves the way for all kinds of vertical-illumination Si/Ge photodetectors with high responsivity, and high-quality epitaxial germanium. It will also allow the realization of large-scale monolithic integrated microwave optoelectronic antenna systems with low cost and low power consumption. The use of silicon-on-insulator substrate for Si/Ge UTC photodiodes offers advantages in reflecting the transmission light to increase the absorption efficiency of the input optical signal, and improving the lattice quality of Ge epitaxial layer to increase the efficiency of photon generated carrier collection. Because of the constructive interference between the incident light and the light reflected by the buried oxide layer of the SOI, the maximum absorption efficiency of the devices on SOI substrate was 2.4 times greater than that obtained with silicon substrate and 4.9 times greater than the minimum absorption efficiency. The photodiodes showed a responsivity of 0.18 A/W at a wavelength of 1.55 μm, which is a 50% higher responsivity with a 25% thinner Ge absorber than that reported for previous Si/Ge UTC devices. Furthermore, use of a step gradient-doping absorber caused the carriers to drift with a saturation velocity in the absorber, which efficiently increased the transit frequency of the UTC photodiodes. As a result, the 3-dB bandwidth of the 15-μm-diameter device was improved to 9.72 GHz under a −5 V bias voltage. The 1-dB compression current of the device was 16.2 mA at 3 GHz.

Methods

Silicon and germanium film growth and characteristics. After the growth of the intrinsic Si layer at 750 °C by cold-wall ultra-high vacuum chemical vapour deposition on the SOI substrate using a source gas of pure Si_2H_6 (UHV-CVD), a brief interruption was introduced to decrease the growth temperature to 290 °C for the growth of the 60-nm-thick p-doped Ge buffer layer. A 600-nm-thick boron-doped Ge layer was then grown on the top as the absorption layer at 600 °C using pure GeH_4 and diluted B_2H_6 source gases. Six boron-doping concentration steps were made in the Ge absorption layer, decreasing from 5×10^{19} to $2 \times 10^{17}/cm^3$, which was confirmed by SIMS measurements, as shown by the black curve in Fig. 3(b).

Fabrication and characterization of photodiodes. Circular Ge layer mesas for normal incidence Si/Ge UTC photodiodes with diameters ranging from 15 to 40 μm were defined by standard photolithography and inductively coupled plasma (ICP) etching. The second mesa was etched to the 2-μm-thick buried oxide layer. The double mesa layout significantly reduced the parasitic capacitance. Top and bottom contacts were lithographically defined on evaporated Ti/Al and a rapid-thermal-annealing (RTA) process was carried out for impurity activation. A passivation/antireflection coating was deposited by plasma enhanced chemical vapour deposition (PE-CVD). Windows for the metal contacts were opened by C_4F_8 ICP etching. The metal pad was evaporated and lifted off. A micrograph of a photodiode with a 15-diameter top mesa is shown in Fig. 1(b). The current-voltage characteristics of our device was measured using an Agilent B1500A semiconductor parameter analyser on a probe station at room temperature. The photocurrent-voltage characteristics were obtained under laser irradiation at a wavelength of 1550 nm with power of 1.2 mW.

Saturation measurements. The device saturation current was obtained using large signal measurements. A heterodyne technique using two free-running lasers at 1550 nm was used and a modulation index was ultimately obtained. A 100% modulation depth tone was fixed at −3 GHz for measurement of the 15-μm-diameter device.

Acknowledgements

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Hybrid film of silver nanowires and carbon nanotubes as a transparent conductive layer in light-emitting diodes

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Hybrid film of silver nanowires and carbon nanotubes as a transparent conductive layer in light-emitting diodes

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A hybrid film of carbon nanotubes (CNTs) and silver nanowires (AgNWs) that could be regarded as a parallel circuit of CNTs and AgNWs was developed, which exhibited a low sheet resistance of 23 Ω/sq and transmittance at 550 nm of 93%. The relatively high, intertube contact resistance of CNTs was reduced by the metallic AgNWs, which acted as bridges to aid carrier transport between CNTs. A hybrid film of CNTs and AgNWs was used as a transparent conductive layer in an AlGaInP light-emitting diode (LED). Including the hybrid film in the LED increased the optical output power by about 1.6 times and decreased the red shift of emission wavelength from 13.11 to 9.7. © *2015 AIP Publishing LLC.* [http://dx.doi.org/10.1063/1.4906351]

Transparent conductive layers (TCLs) are important in light-emitting diodes (LEDs) to transport the injected current from the electrodes to the emitting area. This enhances the quantum efficiency of LEDs, and avoids current crowding under the electrode in the vertical direction, which causes heat generation and decreases reliability. Indium-doped tin oxide (ITO) is widely used as a TCL in LEDs, organic LEDs, and touch screens. However, ITO is expensive because indium is scarce, which is the main motivation to find an alternative material with good optical and electrical performance similar to or better than that of ITO.

Nanomaterials such as graphene,[1] carbon nanotubes (CNTs),[2] and silver nanowires (AgNWs) have attached considerable attention because of their unique electrical properties,[3] excellent chemical stability, and mechanical flexibility, which make them promising candidates to replace ITO in optoelectronic devices. Graphene has high mobility and optical transmittance.[1] However, there is a large difference in work function between graphene (~4.5 eV) and p-type substrates such as p-GaN (~7.5 eV).[4,5] This large difference of work function causes a high turn-on voltage and inefficient current spreading, resulting in light emission occurring only near the p-metal regions, especially on p-GaN because of its high sheet and contact resistance.[6]

AgNWs are a strong candidate to replace ITO because of their intrinsic high conductivity and favorable optical transparency. However, the easy oxidation under ambient conditions, poor adhesion to substrates, and self-aggregation of AgNWs made it difficult to fabricate uniform AgNW films on a large scale. CNTs have a typical sheet resistance (R_s) of 200–1000 Ω/sq and transmittance at 550 nm ($T_{550\,nm}$) of 80%–90%. They also have the most mature fabrication technology of alternatives to ITO, and have successfully replaced ITO in the touch panel of cellular phones.[7] However, the R_s of CNTs is still limited by their intertube contact resistance. A thin metal coating on CNTs can decrease R_s from 1000 to 100 Ω/sq, but this is still relatively high compared with that of ITO of 10–50 Ω/sq. Under the same conditions, there is an additional 10% transmittance loss using CNTs instead of ITO.[8]

Recent reports have revealed that using a combination of nanomaterials as a TCL can provide superior properties and fill new roles. A graphene-AgNW hybrid structure was used as a TCL in ultraviolet LEDs.[9] This caused the R_s of graphene to decrease from 500 to 30 Ω/sq, because the AgNWs bridged the grain boundaries of graphene and increased the conduction channels, which resulted in a marked enhancement of light output power. A hybrid of mesoscale Cu and nanoscale Au improved the $T_{550\,nm}$-R_s performance of optoelectronic devices, which decreased their power loss.[3] However, the scale of tens of micrometers used in the hybrid structure was not suitable for LEDs. The size of the LED chips is typically about 200 μm to 1 mm, while the diameter of an electrode pad is about 100 μm. Mesoscale Cu (1–5 μm) is too large to use on LED chips with a typical size of several hundred micrometers because it would cause considerable optical loss.[3]

Both CNTs and AgNWs have a one-dimensional structure with a nanometer-scale diameter. One of the largest challenges for one-dimensional network films is to obtain low R_s and high transmittance simultaneously.[10] Individual CNT possesses extremely high mobility and conductivity, and favor charge transport along the tubes. AgNWs possess lower contact resistance than CNTs, so the combination of CNTs and AgNWs could improve their $T_{550\,nm}$-R_s performance for use in nanoscale devices. In this paper, a hybrid film of CNTs and AgNWs was fabricated to reduce R_s of CNTs at a given transmittance. The hybrid film is used as a TCL in an AlGaInP LED to investigate its potential as a replacement for ITO.

The structure of the LED with hybrid film of CNTs and AgNWs as a TCL is illustrated in Fig. 1. The AgNWs can

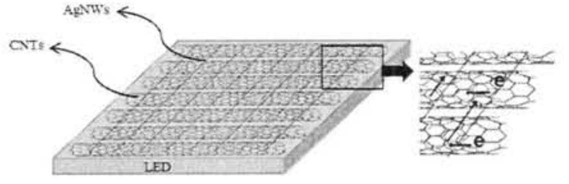

FIG. 1. Schematic diagram of the LED with CNT/AgNW hybrid film as a TCL. The AgNW network acts as a carrier bridge to increase carrier transport between the CNTs, resulting in a symmetric carrier distribution.

obtain carriers from the CNTs and then act as a current source to redistribute the carriers to other CNTs with lower intertube contact resistance than that between CNTs alone. The hybrid film takes advantage of the extremely high mobility and conductivity of individual CNTs and avoids the high intertube contact resistance of CNT networks by including AgNWs. The carriers are not only transported along the CNTs but also between CNTs through the AgNW bridges in a vertical direction, providing a symmetric carrier distribution. This could increase the distance of carrier transport, resulting in high conductivity and low power dissipation. The possible electron transport paths are illustrated in the inset of Fig. 1.

AlGaInP LEDs were fabricated on n-GaAs substrates by deposition of 15 pairs of $Al_{0.6}Ga_{0.4}As/AlAs$ distributed Bragg reflectors on a 100-nm-thick GaAs buffer layer. The active region was 800 nm thick and comprised 60-period $(Al_{0.5}Ga_{0.5})_{0.5}In_{0.5}P/(Al_{0.1}Ga_{0.9})_{0.5}In_{0.5}P$ multi-quantum wells, which were sandwiched between p- and n-$(Al_{0.7}Ga_{0.3})_{0.5}In_{0.5}P$ cladding layers for electron and hole confinement, respectively. To study the current-spreading effect of the hybrid film, a 500-nm-thick Mg-doped, p-GaP window layer with a doping density of $5 \times 10^{18}\,cm^{-3}$ was deposited on top of the LEDs.

As a p-type electrode, Au/BeAu/Au (50/150/200 nm) with a diameter of 100 μm was deposited on the LEDs and then patterned by wet etching. A super-aligned CNT (SACNT) film was drawn continuously from multi-walled CNT arrays and then adsorbed on the surface of each LED wafer through van der Waals interactions.[11] To keep the SACNTs in place, Ti/Au (150/300 nm) was deposited and patterned on each p-type electrode. The AuGeNi/Au n-electrode was deposited on the n-GaAs substrate by sputtering. For comparison, bare AlGaInP LEDs without a hybrid film were also fabricated. The chip size was $300 \times 300\,\mu$m.

The original SACNT film was relatively thick with $T_{550\,nm}$ of about 86%. To decrease both the density of nanotubes and optical loss, the SACNT film was etched with O_2 plasma with an O_2 flow rate of 40 sccm and power of 300 W. After etching for 30 s, $T_{550\,nm}$ of the SACNT film was about 96%, indicating that few CNTs remained on the surface. Fig. 2(a) shows the transmittance of the CNT film before and after O_2 plasma etching, which was reproducible. Solution-based AgNWs were spin coated on the surface of the SACNT film after O_2 plasma etching. The CNTs increased the surface roughness of the substrates, which benefited the adhesion of AgNWs. The hybrid film was annealed at 200 °C for 10 min to improve the contact between the CNTs, AgNWs, and LED surface. Fig. 2(b) depicts a scanning electron microscope (SEM) image of a hybrid film of AgNWs and SACNTs after O_2 plasma etching. Bunches of CNTs were vertically aligned, and there were still large uncovered areas that would allow light transmission without loss.

R_s of the hybrid films generally ranged from 500 to 1000 Ω/sq. The diameter of the AgNWs was about 40 nm and their concentration in the films was 0.5 mg/ml. Fig. 2(c) shows the dependence of $T_{550\,nm}$ on R_s of the hybrid films with the concentration of AgNWs ranging from 0.25 to 3 mg/ml, which demonstrated a typical percolation effect. For AgNW concentrations of 0.25 and 0.5 mg/ml, $T_{550\,nm}$ (R_s) of the hybrid films was 93% (88 Ω/sq) and 90% (23 Ω/sq), respectively. The decrease of transmittance of about 3%–6% was caused by the addition of AgNWs. However, R_s of the hybrid films was considerably lower compared with that of the original CNT film. $T_{550\,nm}$ (R_s) data for films with and without AgNWs prepared using the same conditions were 97.1% (265 Ω/sq) and 94.2% (31 Ω/sq), respectively. R_s decreased for the film with AgNWs, which indicated the percolation effect was relieved a little bit. R_s of the hybrid film decreased by about 25%–75% compared with that the film containing AgNWs only. The difference of $T_{550\,nm}$ between the hybrid and AgNW films was just 4%, which was caused by the absorption of the CNT film. The data obtained for the hybrid films are comparable with the reported data for AgNW films of $T_{550\,nm} = 80\%$, $R_s = 20$ Ω/sq,[12] $T_{550\,nm} = 90\%$, $R_s = 50$ Ω/sq,[13] $T_{550\,nm} = 88\%$, and $R_s = 12$ Ω/sq on cellulose nanopaper,[14] and $T_{550\,nm} = 97.9\%$ and $R_s = 91.3$ Ω/sq by adding exfoliated clays to the AgNW solution to reduce the self-aggregation of nanowires.[15] These values indicate that the $T_{550\,nm}$-R_s performance of the hybrid film is better than that of AgNWs and CNTs alone.

Transmission $T(\lambda)$ and R_s of a NW film can be expressed as

$$T(\lambda) = \left(1 + \frac{Z_0}{2R_s}\frac{\sigma_{op}}{\sigma_{dc}}\right)^{-2}, \qquad (1)$$

where Z_0 is the impedance of free space and is equal to 377 Ω (Ref. 16) and σ_{op} and σ_{dc} are the optical and DC conductivity of the film, respectively. The optical and electrical performance of the films can be evaluated by the ratio of σ_{dc}/σ_{op}. High transmittance and low sheet resistance give a large ratio of σ_{dc}/σ_{op}. The first criterion for a high-performance TCL is $\sigma_{dc}/\sigma_{op} \geq 35$ to achieve the target that the transmittance is greater than or equal to 90%, and the resistance is less than or equal to $100\,\Omega/\mathrm{sq}$.[17] σ_{dc}/σ_{op} of the film prepared by spin coating was 250, as shown in Fig. 2(c), which was much larger than that of CNTs alone.[17] The theoretical prediction fitted the experimental data well except for that for a low concentration of AgNWs.

Fig. 3 shows the current-voltage (I-V) characteristics of fabricated AlGaInP LEDs with and without hybrid films. The LEDs showed rectifying behavior with similar reverse leakage current. The forward voltage at an injection current of 20 mA was 2.0 and 2.1 V for the LED with and without a hybrid film, respectively. The decrease of forward voltage was caused by the change of current injection in the hybrid film in the AlGaInP LED. According to the simulation, the

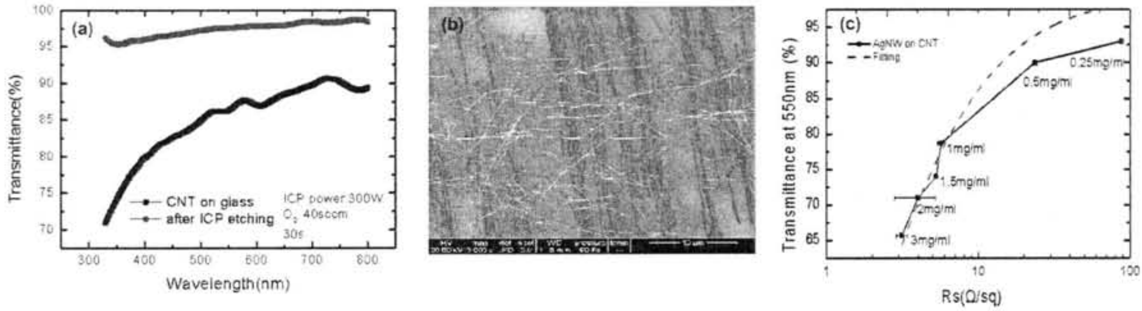

FIG. 2. (a) Transmittance of a CNT film on glass before and after O_2 etching. (b) SEM image of the AgNWs on SACNTs after O_2 etching with an AgNW concentration of 0.5 mg/ml. (c) Dependence of the transmittance at 550 nm on the sheet resistance of the AgNW/SACNT hybrid films on glass for different AgNW concentrations.

carriers injected into the semiconductor originated from the sparse network of hybrid film that was equipotential under the bias. The carrier distribution in the active region was uniform, which resulted in uniform emission in the active region. For a conventional LED structure with ITO or GaP as a TCL, the carrier spread depends on the mobility, thickness, and electrical field distribution of the top layer. Generally, the high carrier distribution under the electrode caused by the carrier-crowding effect results in high-intensity light emission in the active region, which decreases the reliability of the devices.[18,19] The electroluminescence (EL) spectra of the AlGaInP LEDs with and without a hybrid film as a TCL at an injection current of 20 mA are presented in Fig. 3(b). Although there was 10% optical loss caused by the absorption of the hybrid film, the EL intensity of the AlGaInP LEDs with a hybrid film was greatly enhanced because of the efficient carrier injection to GaP and then the active region and the effective current spreading by the hybrid film. The high surface roughness of the hybrid film further increased the light output of the LED. The inset of Fig. 3(b) shows EL images of the AlGaInP LED wafers before dicing with an image size of about $2.5 \times 2.5\,\mu m$ under an injection current of 5 mA. Emission with high intensity was localized around the electrode of the LED without a hybrid film because of the current-crowding effect. The integrated area of the EL spectrum for the LED with a hybrid

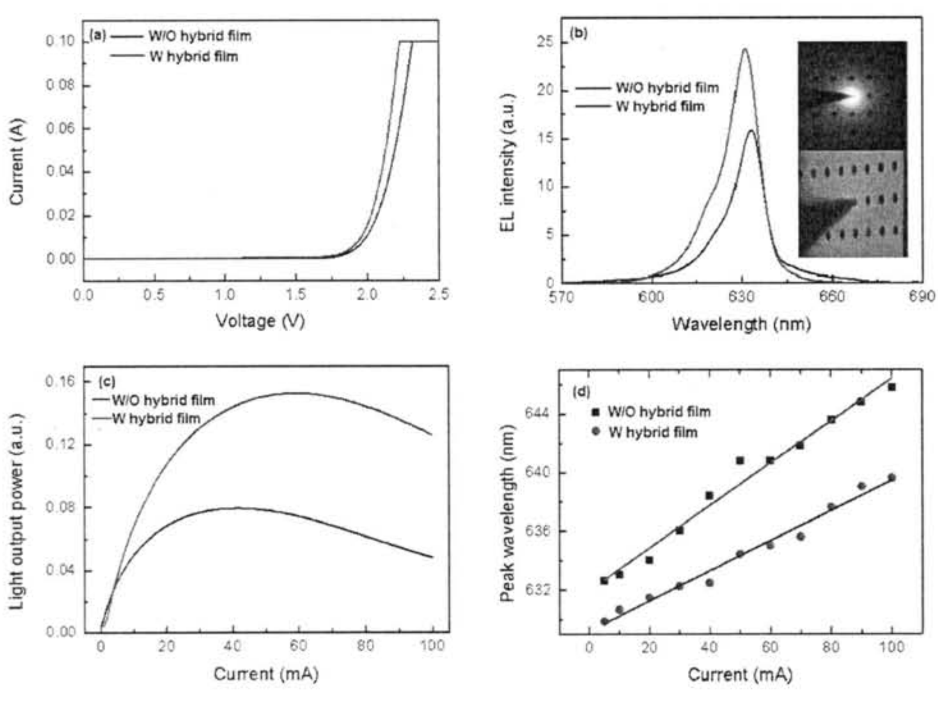

FIG. 3. (a) I-V performance, (b) electroluminescence (EL) spectra at 20 mA, and dependence of (c) light output, and (d) peak wavelength on the injection current of AlGaInP LEDs with and without an AgNW/CNT hybrid film, respectively. Points are experimental data and lines are fitting results. The inset of (b) shows EL images of AlGaInP LED wafers with dimensions of about $2.5 \times 2.5\,\mu m$ at an injection current of 5 mA.

film was 1.6 times greater than that of the LED without a hybrid film. The EL image of the LED wafer with a hybrid film reveals bright uniform emission over the whole wafer, providing strong evidence for effective current spreading by the hybrid film. Fig. 3(c) shows the dependence of light output power of the devices on injection current from 0 to 100 mA. The light output power and external quantum efficiency at 20 mA of the LED with a hybrid film were 1.6 times greater than that of the LED without a hybrid film, consistent with the integrated area ratio of the EL spectra. The extraction quantum efficiency of the LED with a hybrid film was also 1.6 times greater than that of the LED without a hybrid film because these LEDs were fabricated on the same wafer. The obvious enhancement of extraction quantum efficiency resulted from the effective carrier spreading by the hybrid film. The maximum optical power of the LED with a hybrid film was also 1.6 times greater than that of the LED without a hybrid film at injection currents of 60 and 42 mA, which was limited by heat generation inside the devices. Effective current spreading by the hybrid film decreased the degree that the temperature rose. The emission wavelength of the AlGaInP quantum well material was sensitive to temperature. Fig. 3(d) shows the relationship of the peak wavelength of LEDs with and without a hybrid film on injection current. The peak wavelength exhibited a red shift of 9.7 and 13.11 nm with increasing injection current for the LEDs with and without a hybrid film, respectively. The slopes of the lines fitted to these data were 0.1 and 0.15 nm/mA for the LEDs with and without a hybrid film, respectively, revealing that the hybrid film effectively decreased the red shift of emission wavelength with increasing injection current.

In conclusion, a hybrid film of AgNWs and CNTs with $T_{550\,nm}$ (R_s) of 94.2% (31 Ω/sq) was used as a current spreading layer in LEDs, obtaining a 100% enhancement of light optical power at 20 mA and a decrease of emission wavelength red shift from 0.15 to 0.1 nm/mA.

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Optimal oxide-aperture for improving the power conversion efficiency of VCSEL arrays

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Optimal oxide-aperture for improving the power conversion efficiency of VCSEL arrays*

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The maximum power conversion efficiencies of the top-emitting, oxide-confined, two-dimensional integrated 2×2 and 4×4 vertical-cavity surface-emitting laser (VCSEL) arrays with the oxide-apertures of 6 μm, 16 μm, 19 μm, 26 μm, 29 μm, 36 μm, 39 μm, and 46 μm are fabricated and characterized, respectively. The maximum power conversion efficiencies increase rapidly with the augment of oxide-aperture at the beginning and then decrease slowly. A maximum value of 27.91% at an oxide-aperture of 18.6 μm is achieved by simulation. The experimental data are well consistent with the simulation results, which are analyzed by utilizing an empirical model.

Keywords: vertical-cavity surface-emitting laser arrays, power conversion efficiency, oxide-aperture

PACS: 42.55.Px, 42.60.Da, 42.60.Lh **DOI:** 10.1088/1674-1056/24/2/024209

1. Introduction

Vertical-cavity surface-emitting lasers (VCSELs) have been widely used in optical interconnection, optical communications, high-speed data transmission, and many other applications,[1–3] due to their advantages in terms of low power dissipation, low threshold, high efficiency, high speed modulation, cost-effective, etc.[4,5] High-power VCSEL arrays are attractive for optically pumping solid-state and fiber lasers. Due to the low round-trip gain of VCSEL, increasing the aperture diameter of each element in the arrays, even to several hundreds of microns, is widely regarded as an effective way to achieve high optical output power. However, the carrier distribution, active gain, and refractive index become non-uniform with the increase of the aperture, which is mainly determined by the spatial hole-burning effect originating from lateral series resistance.[6–8] Hence, the power conversion efficiency decreases, which is a significant performance in the application of VCSEL arrays. A recent report has shown that the maximum power conversion efficiency of 4×4 VCSEL arrays with 200-μm aperture is only about 17.8%.[9] This is difficult to use in practical applications because the power supply must be very high due to the low power conversion efficiency. Seurin *et al.*[10] found that the maximum power conversion efficiency (MPCE) of the single VCSEL increases quickly with the augment of aperture, it reaches its maximum value at the beginning and then decreases slowly. The MPCE of 50% with an aperture of 10 μm is achieved for the individual VCSEL. As evidenced by their experimental results, Hofmann *et al.*[11] demonstrated that the MPCE followed a similar tendency and obtained a maximum value about 22% at a 10-μm aperture. However, the tendency of MPCE for VCSEL arrays has not yet been analyzed in theory or verified in experiment. Therefore, it is important to systematically understand the relationship between the power conversion efficiency and the aperture of VCSEL array.

In this paper, we investigate the relationship of the power conversion efficiency with the oxide aperture by the top-emitting 2×2-nm and 4×4 850-nm VCSEL arrays. Both theoretical analysis and experimental measurement indicate that there exists an optimal oxide aperture for VCSEL arrays to obtain maximum power conversion efficiency. Our study puts forward an insight into the optimization of the VCSEL array design for improving the power conversion efficiency.

2. Structure and fabrication of the device

The reported VCSEL arrays are fabricated from a metal organic vapor phase epitaxy grown AlGaAs structure on an n-type GaAs substrate. The bottom n-type mirror below the active region consists of 34.5 pairs of Si-doped $Al_{0.9}Ga_{0.1}As/Al_{0.12}Ga_{0.88}As$ distributed Bragg reflectors (DBRs) for high optical reflectivity. The un-doped active region contains three GaAs quantum wells that are centered on the anti-node of the optical standing wave within the one-wavelength cavity, with its photoluminescence peak at 835 nm. The top p-type mirror above the active region consists of 20.5 pairs of C-doped $Al_{0.12}Ga_{0.88}As/Al_{0.9}Ga_{0.1}As$ DBRs, each of which has an Al fraction similar to the bottom n-DBR. Graded interfaces and dopings are used on the top and bottom DBR layer to reduce the differential resistance and maintain low free carrier absorption loss. A single low-index quarter-

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wavelength $Al_{0.98}Ga_{0.02}As$ oxidization layer in the p-type mirror adjacent to the active region is employed to form an oxide aperture for current and later optical confinement. After that, a highly doped 25-nm GaAs Ohmic contact layer is formed on the top of the epitaxial wafer. The operation wavelength of this structure is designed to be 850 nm.

The top-emitting, oxide-confined 2×2 and 4×4 850-nm VCSEL arrays are fabricated through a series of processing steps, including mesa etching, wet oxidation, and contact formation, and its schematic cross section is presented in Fig. 1. The fabrication of the VCSEL arrays is described as follows. To form about 3-μm height cylindrical mesa for exposing the oxidation layer ($Al_{0.98}Ga_{0.02}As$), the sample was soaked for 9 min in a CH_3OH:H_3PO_4:H_2O_2 solution with 3:1:1 volume ratio in ice–water mixture, by using 200-nm SiO_2 as the etching mask. After that, the $Al_{0.98}Ga_{0.02}As$ oxide-confined layer was selectively wet-oxidized in a high humidity furnace at 400 °C with a 90-°C water bath and 1-L/min N_2 flow in order to form the current oxide-aperture and provide lateral current confinement. The oxide-apertures of VCSEL arrays are 6 μm, 16 μm, 19 μm, 26 μm, 29 μm, 36 μm, 39 μm, and 46 μm, respectively. Before evaporating the 15-nm/300-nm Ti/Au p-type annular contact, the surface is passivated by depositing 400-nm SiO_2 to electrically insulate all the mesa sidewalls from the p-contact. To minimize absorption losses and resistance series on substrate, the substrate was thinned to around 120 μm. Then, the evaporation of the 50 nm/300 nm AuGeNi/Au n-type bottom contact and a subsequent annealing process are carried out. Thus, the processing is completed.

The cleaved chips of arrays are attached to the copper subcarriers with indium coating for electrical supply and thermal dissipation. A schematic diagram of individual VCSEL in arrays is shown in Fig. 1. The spacing between the neighboring elements is 50 μm, which reduces the thermal crosstalk.

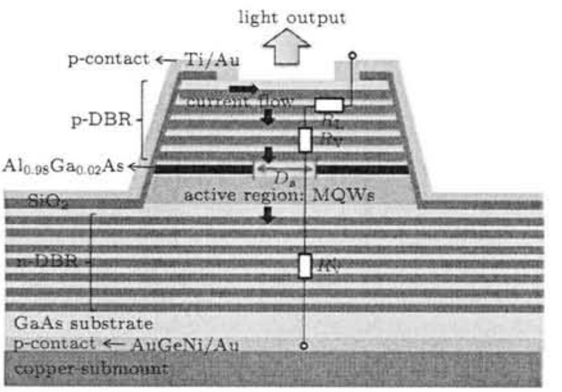

Fig. 1. (color online) Schematic cross-sectional view of the selectively oxidized-confined top-emitting VCSEL, where D_a is the oxide-aperture diameter, R_L the lateral resistance, R_V and R_V' are the vertical resistances of p-DBR and n-DBR, respectively, and the differential resistance of each element in VCSEL arrays is the sum of series-connected resistances R_L, R_V, and R_V'.[12,13]

3. Device measurements

The typical optical output powers and the current–voltage (I–V) performances of 4×4 VCSEL arrays with the apertures of 6 μm, 19 μm, 29 μm, and 39 μm are presented in Fig. 2(a), respectively, under the pulsed operation with a pulse width of 50 μs and a repetition rate of 100 Hz at room temperature. As the current injection increases, the optical output power increases to the thermal rollover point that is induced by carrier leakage and joule heat caused by series resistance.[14,15] The threshold currents of the arrays exhibit 0.91 mA, 15.09 mA, 50.93 mA, and 88.05 mA, respectively. Maximum optical output powers of 16.45 mW, 161.97 mW, 341.03 mW, and 464.23 mW are obtained. The slopes of I–V curves, which represent the differential resistances, decrease with the increase of oxide-aperture, owing to the reduced lateral resistance through the oxide-aperture to the active region.[16] The differential resistances are 6.54 Ω, 3.08 Ω, 2.73 Ω, and 2.18 Ω, respectively.

The power conversion efficiency of VCSEL arrays, which also is presented in Fig. 2(a), is calculated from

$$\eta_{\mathrm{PCE}} = \frac{P_{\mathrm{ex}}}{P_{\mathrm{in}}} = \frac{P_{\mathrm{ex}}}{IV} = \frac{h\nu}{qV_0} \cdot \left[\frac{\eta_{\mathrm{e}}(I-I_{\mathrm{th}})}{I(V_0+IR_{\mathrm{s}})}\right], \tag{1}$$

where P_{ex} is the optical output power, P_{in} is the electrical output power, I is the driven current, V is the applied voltage, $h\nu$ is the photon energy, q is the electronic charge, η_{e} is the external differential quantum efficiency, I_{th} is the threshold current, R_{s} is the differential resistance ($\mathrm{d}V/\mathrm{d}I$), V_0 the turn-on voltage (zero-current intercept), and the measured value is 1.68 V. The values of η_{e} of around 23.16%, 51.13%, 56.95%, and 52.30% are calculated from $\eta_{\mathrm{e}} = [(P_{\mathrm{ex}}-P_{\mathrm{t}})/h\nu]/[(I-I_{\mathrm{th}})/q]$,[4] where P_{t} is the optical output power at the threshold current. The values of MPCE are 12.33%, 27.30%, 22.12%, and 18.34%, respectively. The optical output power, the current–voltage (I–V) curve, and power conversion efficiency of 2×2 VCSEL arrays with the apertures of 6 μm, 19 μm, 29 μm, and 39 μm are shown in Fig. 2(b), respectively. Figures 2(a) and 2(b) show that, as the oxide-aperture increases, the values of the MPCE first increase due to the decrease of differential resistance, and then decrease for both 2×2 and 4×4 VCSEL arrays.

The single VCSEL emitter with a 29-μm oxide-aperture has an output power of 14.34 mW at 30-mA bias current from Fig. 2(b). This means that the theoretically expected output power of an array of 4 or 16 elements biased at 4 × 30 mA = 120 mA or 16 × 30 mA = 480 mA is 4 × 14.34 mW = 57.36 mW or 16 × 14.34 mW = 229.44 mW; the two values are close to the ideal values considering that there is no heat generation inside the VCSELs. This result emphasizes that there is very mild thermal crosstalk among elements and these VCSEL arrays have the potential to be scaled up to achieve higher powers, so the thermal problem in our study can be ignored.

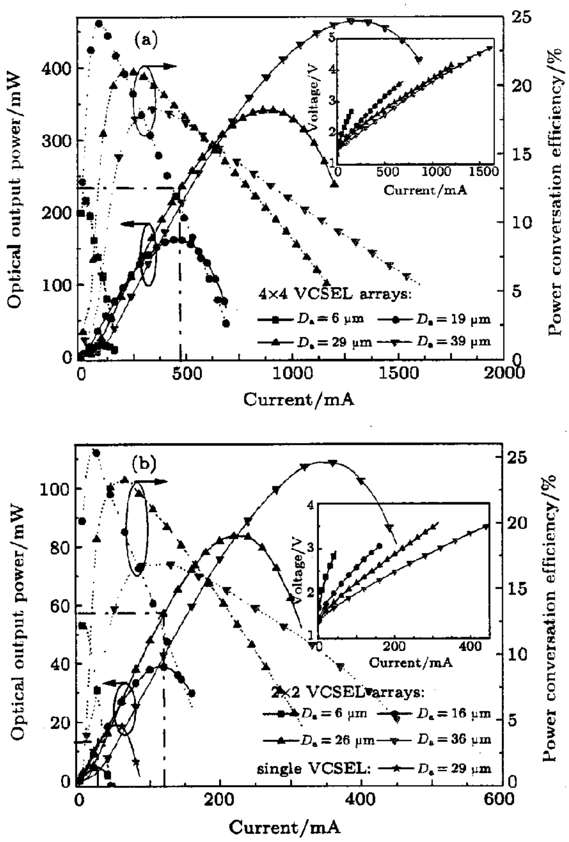

Fig. 2. (color online) Plots of optical output power, power conversion efficiency, and voltage in insets versus current with the values of oxide-aperture D_a of 6 μm, 19 μm, 29 μm, and 39 μm for (a) 4×4 VCSEL arrays and (b) 2×2 VCSEL arrays. The dash–dot lines represent the output powers of 14.34 mW, 57.30 mW, and 235.90 mW for the single VCSEL emitter, the 2×2 VCSEL and the 4×4 VCSEL arrays with 29-μm oxide-apertures, at 30 mA, 120 mA, and 480 mA, respectively.

4. Empirical model and discussion

The power conversion efficiency of VCSEL arrays can be improved by enhancing the external differential quantum efficiency, and reducing the threshold current and the differential resistance. But these three limiting factors also influence and restrict each other. As the oxide-aperture increases, the following expected trend can appear: a decrease in differential resistance, an increase in threshold current, and an increase in external differential quantum efficiency. Therefore, the MPCE is affected synthetically by differential resistance, threshold current, and external differential quantum efficiency. To better understand the various physical processes, it is significant to further analyze the interaction of the three factors.

The MPCE is a function of external differential quantum efficiency, threshold current, and differential resistance, and according to $\mathrm{d}\eta_{\mathrm{PCE}}/\mathrm{d}I = 0$,[4,10,17] the analytical expression can be expressed as

$$\eta_{\mathrm{MPCE}} = \frac{h\nu}{qV_0} \cdot \eta_{\mathrm{e}} \cdot \left[\frac{V_0/(I_{\mathrm{th}}R_{\mathrm{s}})}{\left(1+\sqrt{1+V_0/(I_{\mathrm{th}}R_{\mathrm{s}})}\right)^2} \right], \tag{2}$$

in which R_{s} is the sum of the series-connected lateral resistance R_{L} and the vertical resistance R_{V} of p-DBR, which is a function of aperture size D_{a}, because the R'_{V} is the sum of the vertical resistance of n-DBR and junction resistance which is small enough to be ignored when compared with R_{V}. The analytical expression of the R_{s} can be written as[4,13]

$$R_{\mathrm{s}} = \frac{(R_{\mathrm{L}}+R_{\mathrm{V}})}{n} = \frac{\left[\dfrac{\rho_{\mathrm{L}}}{\pi D_{\mathrm{a}}} + \dfrac{\rho_{\mathrm{V}}}{\pi (D_{\mathrm{a}}/2)^2}\right]}{n}, \tag{3}$$

where ρ_{L} and ρ_{V} are the lateral and vertical characteristic resistivity, respectively, n is the element number in the array. The lateral resistance $R_{\mathrm{L}} = \rho_{\mathrm{L}}/(\pi D_{\mathrm{a}})$ represents the lateral and contact resistance, which derives from the current or carrier spreading through contact, and it is inversely proportional to the oxide-aperture perimeter. The vertical resistance $R_{\mathrm{V}} = \rho_{\mathrm{V}}/[\pi(D_{\mathrm{a}}/2)^2]$ relates to uniform vertical current flow or carriers through the oxide-aperture, meanwhile the resistance is inversely proportional to the oxide-aperture area and its resistivity ρ_{V} essentially represents the vertical resistivity of the p-DBR.[4] The analytical expressions of the external differential quantum efficiency and the threshold current as a function of aperture size can be, respectively, represented as[4,13]

$$\eta_{\mathrm{e}} = \frac{\eta_{\infty}}{(1+D_0/D_{\mathrm{a}})}, \tag{4}$$

$$I_{\mathrm{th}} = \left[\pi J_{\infty}\left(\frac{D_{\mathrm{a}}}{2}\right)^2 + \frac{I_0}{2} + \frac{D_{\mathrm{a}}}{2}\sqrt{\pi I_0 J_{\infty}}\right] \cdot n, \tag{5}$$

where I_0 is the characteristic spreading current, D_0 the characteristic spreading distance, J_{∞} and η_{∞} are the threshold current density and the external differential quantum efficiency under a uniform current distribution, respectively, which depend only on the intrinsic structure of the device.

Figures 3(a)–3(c) show the experiment data extracted from Fig. 2 the differential resistance of each element in arrays, the external differential quantum efficiency, and the threshold current each as a function of D_{a}. The lines in Fig. 3 show the fitting results according to Eqs. (3)–(5), which demonstrate that the differential resistance decreases as D_{a} increases, the external differential quantum efficiency increases as D_{a} increases, and then reaches a saturation value. Meanwhile, the threshold current always increases quickly as D_{a} increases, due to the increase of the active volume. The characteristic parameters of ρ_{L}, ρ_{V}, J_{∞}, D_0, I_0, and η_{∞} are extracted and shown in Table 1, by the numerical fitting results according to Eqs. (3)–(5).

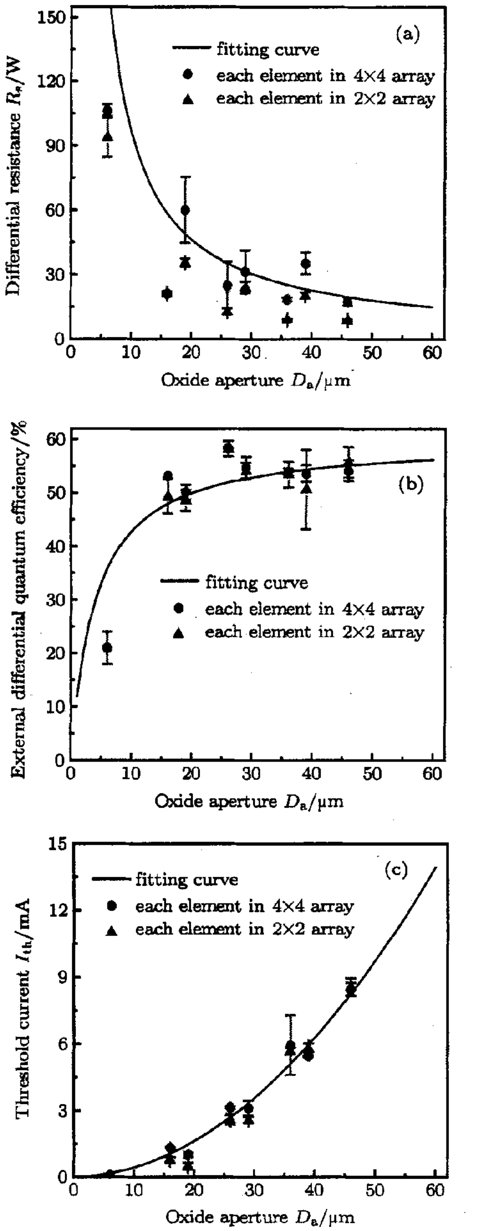

Fig. 3. (color online) Experimental data and the numerical fitting curves of (a) the differential resistance of each element in arrays, (b) the external differential quantum efficiency, and (c) the threshold current versus the oxide-aperture. The data are the measured data and the error bars represent the standard deviation of arrays.

Table 1. Calculated and extracted characteristic parameters of VCSEL arrays.

Symbol	Characteristic parameter	Fitting value
ρ_L	lateral characteristic resistivity	0.28 Ω·cm
ρ_V	vertical characteristic resistivity	6×10^{-8} Ω·cm^2
J_∞	the threshold current density	480 A/cm^2
D_0	characteristic spreading distance	4 μm
I_0	characteristic spreading current	0.01 mA
η_∞	differential quantum efficiency	60%

Figure 4 shows the calculated MPCE curve of VCSEL arrays as a function of aperture size, according to Eq. (2). All of the simulation data are based on the fitting results of Fig. 3. The MPCE increases rapidly as the aperture size increases, which is due to the decrease of the electrical dissipation,[18] and then decreases slowly after it has reached its maximum, which is attributed to the combined interaction of differential resistance, threshold current, and the external differential quantum efficiency. According to our device structure, the maximum MPCE is 27.91% at an 18.6-μm oxide-aperture. For an aperture size ranging from 15 μm to 25 μm, the MPCE could reach 99% of the maximum value. With the increase of the aperture size, the threshold current keeps increasing but the differential resistance and the external differential quantum efficiency have little change, which causes the value of MPCE to decrease gradually to zero[13] according to Eq. (2).

The experimental data, which are calculated according to the measurement results, are also shown in Fig. 4, and its behaviour is approximately consistent with the calculated MCPE curve. The measured maximum values of MPCE are 28.6% and 27.6% with an aperture size of 16-μm oxide-aperture for 2×2 and 4×4 VCSEL arrays, respectively, which are close to the calculated maximum value. The experimental data are slightly lower than the numerical calculation curve, especially for an aperture size above 25 μm. We believe that there still exists a slight thermal effect among the adjacent elements of arrays which need high current injection.[14,19]

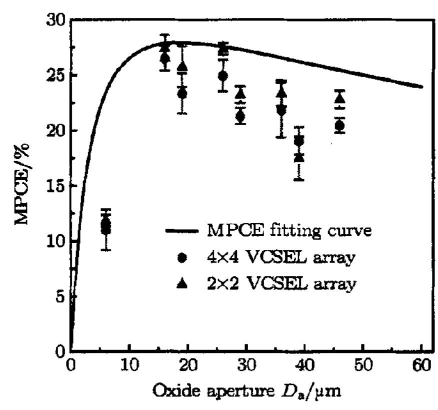

Fig. 4. (color online) The MPCE versus the oxide aperture of the experimental data and the numerical fitting curves of VCSEL arrays, where the data are the measured data and the error bars represent standard deviations of five arrays.

The deviation between the experimental data and the numerical fitting curve increases as the oxide-aperture augments. In the analysis above, figures 3(a)–3(c) show the fitting curves of the differential resistance, the external differential quantum efficiency, and the threshold current, each as a function of the oxide-aperture based on Eqs. (3)–(5), when the thermal crosstalk problem among elements is ignored. However, for an actual VCSEL array device, there still exist small errors in the numerical fitting processes of the differential resistance, the external differential quantum efficiency, and the threshold current derived from the crosstalk problem. The deviation accumulation between the experimental data and numerical fitting can ultimately lead to a relatively great influence on the values of MPCE. With the increase of the oxide-aperture, the deviation increases because the increasingly serious crosstalk and the larger oxide-aperture will lead to a non-uniform injection current for the annular electrode.[6,20]

5. Conclusions

The relationship between MPCE and the oxide-aperture of VCSEL arrays is analyzed by using an empirical model. The MPCE increases rapidly with the oxide-aperture increase and then decreases slowly after it has reached its maximum, which is attributed to the combined interaction of differential resistance, threshold current, and external differential quantum efficiency. The maximum value of MPCE is 27.91% at 18.6-μm optimal oxide-aperture and can reach 99% of the maximum value in an aperture size range from 15 μm to 25 μm. The experimental data match the theoretical analyses well. The analyses of the various oxide-apertures contributing to the MPCE saturation of the device can provide a guidance for improving the power conversion efficiency.

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Polarization-Stable 980 nm Vertical-Cavity Surface-Emitting Lasers with Diamond-Shaped Oxide Aperture *

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Polarization-stable 980 nm oxide-confined vertical-cavity surface-emitting lasers with 3 μm diamond-shaped aperture are fabricated by comprehensively utilizing the anisotropic properties of wet etching and wet nitrogen oxidation of III–V semiconductor materials. Polarization-stable operation along the major axis of the diamond-shaped oxide aperture with 11 dB orthogonal polarization suppression ratio is achieved in a temperature range of 15–55°C from the threshold to 4 mA.

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Vertical-cavity surface-emitting lasers (VCSELs) are widely used as light sources for short distance data communication due to their attractive properties, such as high speed, low power consumption, low-cost manufacturing, high-efficiency two-dimensional arrays.[1] Recently, modulation bandwidth of 29 GHz was reported by the photon-photon resonance for 980 nm oxide confined VCSELs.[2] In a conventional VCSEL, degenerated transverse polarization modes can cause mode-partition noise in an optical communication system due to polarization switching.[3] For a VCSEL grown on a (100)-oriented substrate, the output beam will polarize along the [011] or the [01$\bar{1}$] crystal axis due to the electro-optic effect.[4] The polarization for most VCSELs, changing with the current injection and temperature as a result of the changing relative position between gain peak and cavity mode, is inherently unstable due to the symmetric gain structure.[5] Many new applications, such as atomic clock, optical mouse, and optical sensing, require stable polarization of VCSELs to obtain low relative intensity noise.[6] For instance, a new generation polarization-stable optical mice solves the unwanted movement of the mouse cursor on the computer screen due to polarization switching.[7]

Recently, polarization-stable VCSELs have been demonstrated. By introducing anisotropic gain or cavity structure, the polarization-switching could be controlled. Ebeling's group demonstrated polarization-stable VCSELs with 3μm-diameter elliptic oxide aperture operation, which resulted from anisotropy current injection and scattering loss induced by a small elliptical oxide aperture.[8] The orthogonal polarization suppression ratio (OPSR) reaches 20 dB. By introducing the asymmetric distribution of photonic crystal structure on top DBR of the VCSELs, stable polarization could be obtained with OPSR of 20 dB. The threshold current increases to 5 mA due to the introduction of photonic crystal.[9] The surface grating on the surface of the VCSELs was proved to control the polarization effectively by the anisotropic mirror loss.[10] The combination of a surface grating and an annular surface relief in an extra topmost anti-phase layer results in a polarization-stable laser emission. The OPSRs of 20 dB for VCSELs with 5 μm active diameter were achieved.[11] The property of larger angular dependence of reflectivity of high contrast grating could discriminate polarization with the OPSR of 20 dB.[12] However, for the technique of surface microstructure to control the polarization, the threshold current more or less increases due to the extra mirror loss.

In this Letter, we present polarization-stable oxide-confined VCSELs with 3 μm diamond-shaped aperture, comprehensively utilizing the anisotropic properties of traditional wet etching and wet nitrogen oxidation processes, which are low-cost and feasible to fabricate. The emitted light is polarized along the major axis of the diamond-shaped aperture with OPSR of 11 dB from 15°C to 55°C due to the induction of the asymmetric gain.

The epitaxial structure was grown on a (100) GaAs substrate misoriented by 2° toward the (111) plane. The active region of three $GaAs_{0.92}P_{0.08}$ (6 nm)/$Ga_{0.83}In_{0.17}As$ (4 nm) quantum wells, with a photoluminescence peak at 971 nm, was sandwiched between a top p-doped and a bottom n-doped distributed Bragg reflector (DBRs), which consists of $Al_{0.9}Ga_{0.1}As/Al_{0.12}Ga_{0.88}As$ layers. A 30 nm

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$Al_{0.98}Ga_{0.02}As$ oxidation layer was positioned just under the top DBR, serving as current- and optical-confinement mechanism. A 5 nm p^+-GaAs ohmic contact layer was placed on the top of the epitaxial wafer.

The anisotropic wet etching can be illustrated by a diagram of the GaAs crystal structure, as shown in Fig. 1(a), demonstrating As and Ga (111) planes and their relationship with [011] and [01$\bar{1}$] crystallographic orientation. The (011) plane was just the cleavage face of the GaAs material, which could be easily distinguished during the device fabrication. The As (111) planes were more chemically reactive compared with Ga (111) planes, resulting in the wet etching rate behavior, such as As (111)>Ga (111).[13] Then, the etching rate along the [01$\bar{1}$] crystallographic orientation was faster than that along the [011] crystallographic orientation. The anisotropic elliptical mesa was obtained by using a symmetric circular mask with 64 μm in diameter after wet etching in the solution of CH_3OH:H_3PO_4:H_2O_2:H_2O=1:3:1:5 for 6 min at 0℃ with the etch depth of about 4 μm for exposure of the $Al_{0.98}Ga_{0.02}As$ oxidation layer. The major and minor axes of the elliptical mesa were 58 μm along [011] and 54 μm along [01$\bar{1}$] crystallographic orientation, respectively, as shown in Fig. 1(b). The size difference of 6–10 μm between the etched mesa and the mask was caused by the undercut of the wet etching.

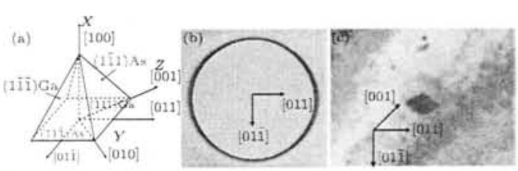

Fig. 1. (a) A diagram of the GaAs crystal structure. (b) Microscope photo of the etched mesa after wet etching, with the major and minor axes of 58 μm and 54 μm, respectively. (c) Microscope photo of the etched mesa after wet nitrogen oxidation, with the major and minor axes of the oxide apertures of 3 μm and 2 μm, respectively.

The wet nitrogen oxidation process is also dependent on the crystallographic orientation. For high Al-content layers (>0.94), a slight crystallographic oxidation dependence of wet nitrogen oxidation was observed from circular mesa.[14] The oxidation rate along the [001] crystallographic orientation was slightly faster than that along the [011] crystallographic orientation, which is consistent with the lower surface reactivity of {011} planes than that of {001} in GaAs. Furthermore, due to the fact that the substrate was misoriented by 2° toward the (111) plane, the oxidation rate of [011] crystallographic orientation was slightly larger than [01$\bar{1}$] crystallographic orientation,[15] which enhances the anisotropy of the wet nitrogen oxidation process.

A microscopic photo of the oxide aperture is shown in Fig. 1(c), which was obtained after 33 min wet nitrogen oxidation process with a furnace temperature of 400℃ and a vapor temperature of 85℃. The colorful region was formed by the oxidized $Al_{0.98}Ga_{0.02}As$ layer, which had a higher oxidation speed due to higher Al content. The center gray region was the unoxidized $Al_{0.98}Ga_{0.02}As$ material serving as the current injection aperture, with major and minor axes of 3 μm and 2 μm, respectively. The measured inner angles of the oxide aperture were 112° and 68°, respectively, and the four equal sides were calculated to be about 1.8 μm, which was a typical diamond shape. It has been reported that the circular mesa by isotropic dry etching can change to a square aperture after wet nitrogen oxidation.[14] However, in our experiment, the final aperture shape changes to a diamond shape, which is caused by the original elliptical mesa before the wet nitrogen oxidation. In this experiment, two sizes of VCSEL aperture were fabricated for comparison under the same process, with major and minor axis sizes of 4 μm and 3 μm, 3 μm and 2 μm, respectively, which are briefly called 4 μm and 3 μm aperture devices.

After the 450 nm SiO_2 passivation layer was deposited by PECVD, 15 nm/300 nm Ti/Au and 50 nm/300 nm AuGeNi/Au metal systems were sputtered as the top and bottom electrodes, respectively, with a rapid thermal annealing process for 35 s at 400℃. The on-chip optical and electrical characteristics were measured under continuous-wave conditions at room temperature.

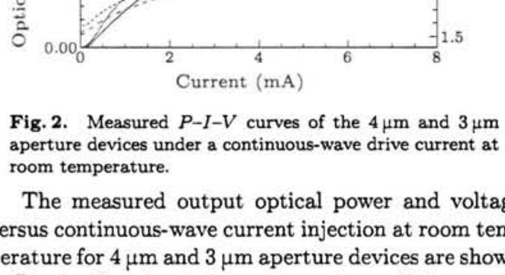

Fig. 2. Measured P–I–V curves of the 4 μm and 3 μm aperture devices under a continuous-wave drive current at room temperature.

The measured output optical power and voltage versus continuous-wave current injection at room temperature for 4 μm and 3 μm aperture devices are shown in Fig. 2. The threshold current, slope efficiency and maximum output optical power of the 4 μm aperture device are 0.2 mA, 0.15 mW/mA and 0.8 mW at about 7.1 mA, respectively. While for the 3 μm aperture device, the threshold current is 0.15 mA and the slope efficiency reduces to 0.13 mW/mA. The threshold current is lower than that of VCSEL with 3 μm circular aperture.[16,17] The maximum output optical power of 0.45 mW is obtained at 5 mA, which is limited by the heating.

Figure 3 shows the measured optical spectra of the 3 μm aperture device under a continuous-wave current injection from 1 mA to 5 mA. The corresponding peak wavelengths are 970.4 nm, 971.2 nm, 972.2 nm, 973.2 nm and 974.4 nm, respectively, which shift with current injection to the red direction with the average rate of 0.8 nm/mA. The full widths of half maximum (FWHM) of the spectra at 1 mA and 2 mA are 0.6 nm, while for the other three they are 0.8 nm, which are caused by the large current injection and heat generation in the cavity. The inset of Fig. 3 shows the optical spectra of 4 μm aperture device under the continuous-wave current injection from 2 mA to 6 mA. The corresponding peak wavelengths are 970.4 nm, 971.8 nm, and 974.0 nm, respectively. It is clearly seen that there are small peaks existing in the cavity.

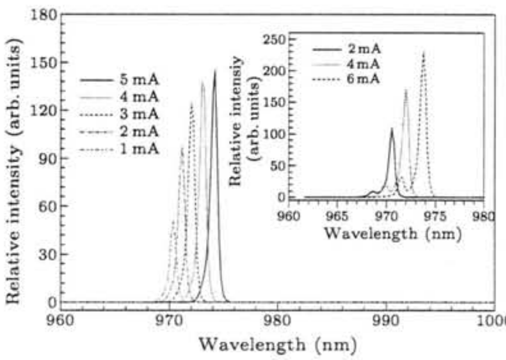

Fig. 3. The measured optical spectra of 3 μm aperture device at room temperature with current injection from 1 mA to 5 mA in steps of 1 mA. The inset shows the optical spectra of 4 μm aperture device, with the current injection from 2 mA to 6 mA in steps of 2 mA.

Polarization-resolved relative optical output power as a function of current injection for the 3 μm aperture device is shown in Fig. 4. It can be seen from Fig. 4 that the light emission polarized along the major axis, i.e., [011] crystallographic orientation, exhibits typical laser P–I–V performances. The threshold current is 0.15 mA at a temperature of 25℃, which is the same as the data measured without a splitter. However, the insertion loss caused by inserting the polarized beam splitter, which is used to resolve the polarized light, between the laser and the detector causes the output optical power to decrease to 0.27 mW at a temperature of 25℃. The output optical power declines with the environment temperature due to the increased carrier leakage and decreased gain. On the contrary, the optical output power along the short axis, i.e., [01$\bar{1}$] crystallographic orientation, is suppressed without typical lasing property demonstration. All of the OPSRs that are used to analyze the polarization control ability of device are over 11 dB from the threshold to 4 mA from 15℃ to 55℃. The decrease of OPSR when the current injection over 4 mA for the curves of 15℃ and 25℃ is attributed to the slight stimulation radiation for the polarization along [01$\bar{1}$] crystallographic orientation. Compared with the polarization control ability of a symmetric oxide aperture obtained by isotropic inductively coupled plasma etching which indicates symmetric gain, the two polarization states switch alternatively with the current injection, as shown in the inset of Fig. 4.

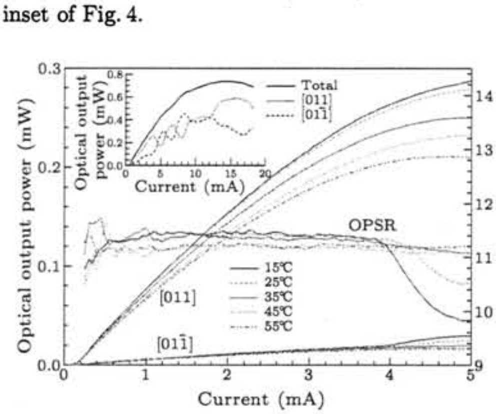

Fig. 4. Polarization-resolved P–I curves of the 3 μm aperture device at the temperature from 15℃ to 55℃ in steps of 10℃. The inset shows the polarization-resolved P–I curve of a VCSEL at room temperature with symmetric oxide aperture, which is obtained by inductively coupled plasma etching instead of wet etching. The two polarization modes switch with the current injection.

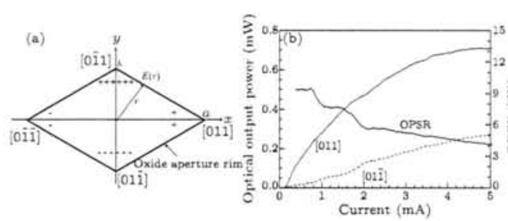

Fig. 5. (a) Schematic diagram of the diamond-shaped oxide aperture, unequal loss is induced by the oscillating electric dipoles on the inner vertical walls of oxide aperture. (b) Polarization-resolved P–I curves of the 4 μm diamond-shaped aperture device at room temperature.

The dominant reason that the polarization direction of the light emission is pinned by the asymmetric oxide aperture is interpreted by the unequal scattering loss between the two orthogonal polarizations of the same cavity eigenmodes.[18] The electric dipoles on the inner vertical walls of the oxide aperture consume the electromagnetic energy by a polarization process. The induced surface polarized charges generated by the electric field radiation normal to the aperture rim are illustrated as symbols + and −, as shown in Fig. 5. Due to the fact that the induced charge is proportional to the normal to the surface electric field. the magnitude of the induced oscillating dipole depends on the electric field. Since the quantity of induced charge is proportional to the normal surface electric field intensity, the magnitude of the induced oscillating dipole depends on the electric field intensity. The induced charges are weaker for the electric field oriented along the major axis than those along the minor axis due to the radial decay of the electric intensity $E(r)$, since the surface-normal field $E(r=a)$ is smaller than $E(r=b)$. Here, $E(r)$ decays exponentially as $\exp(-r^2/w^2)$ with w being the mode waist. Thus, the induced dipole moment for the polarization along the major axis is also smaller than that for the polarization along the minor axis. Due to the fact that scatting losses scales as the induced dipole moment squared dominate the total cavity losses for aperture sizes are comparable to the mode waist,[19,20] the difference in scattering losses is sufficient to select the mode. The lowest loss polarization is oriented along the major axis for the polarization discrimination. The OPSR can be further increased by extending the axis difference of the oxide aperture due to the further increase of the scattering loss polarized along the short axis. This can be achieved by forming the size difference in the major and minor axis directions when mesa etching. It should be pointed out that extending the axis difference of the oxide aperture may cause the output beam deviation from circular distribution. In the case of VCSELs coupling with single-mode fibers, the coupling efficiency will be decreased.

Figure 5(b) shows the polarization-resolved output optical power versus the current injection for the 4 μm aperture device at room temperature. Compared with the 3 μm aperture device, the emission of the 4 μm aperture device polarized along both the [011] and [01$\bar{1}$] crystallographic orientations exhibits stimulated radiation. The OPSR decreases quickly from 9.3 dB to 5.4 dB as the current injection increases from 1 mA to 5 mA due to the thermal rollover of the emission along [011] crystallographic orientation. The 3 μm aperture device with the major and minor axis ratio of 1.5 has a larger OPSR than that of the 4 μm aperture device with an axis ratio of 1.3, which agrees with the above theoretical prediction.

In summary, polarization-stable 980 nm oxide confined VCSELs with 3 μm diamond-shaped oxide aperture, which are obtained by comprehensively using the anisotropic properties of the traditional wet etching and wet nitrogen oxidation processes, are demonstrated with a threshold current of 0.15 mA and a maximum optical output power of 0.45 mW under continuous-wave current injection. The OPSR is over 11 dB in the temperature range from 15°C to 55°C. The relationship of OPSR with the major and minor axis ratio is discussed.

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Physics of Si based Avalanche Detectors With Built-In Self-Quenching and Self-Recovering Capabilities

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Abstract: A silicon based single photon avalanche detector with a transient carrier buffer layer was designed. The buffer layer as an energy barrier tentatively stops avalanche-generated carriers. The device demonstrates self-quenching and self-recovering capabilities.
OCIS codes: 040.1345, 040.5160.

Single photon avalanche detectors (SPADs) have attracted increasing attention because of their critical roles in many important applications such as quantum cryptography[1] , optical time-domain reflectometry [2], 3-D imaging, time-resolved spectroscopy, non-line-of-sight optical communication, space communication and light detection and ranging [3],[4]. Of all SPADs, silicon SPADs have demonstrated superior performance with high detection efficiency, low dark count rate and reduced after pulsing effect.

In this paper, a novel structure of silicon based with self-quenching and self-recovering was designed. The device with a small multiplication region and a bulk absorption region is proposed, shown in fig. 1. The photon-generated carriers were emerged in a large bulk absorption region underneath a small pillar, built on an p-type substrate. The pillar, located at the device's upper center, contains a p^+-type multiplication region and a n^+-type capping layer. Besides, an n-type layer was inserted between p^+-layer and p^-layer, forming a potential well to stop avanlance-generared carriers instead of the complicated feedback circuit, shown in fig. 2.

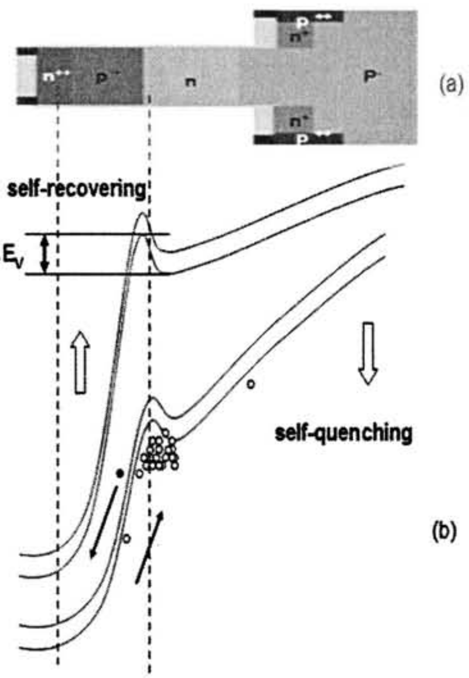

Figure 1 Schematic cross-sectional view of the reported Si-based APD.

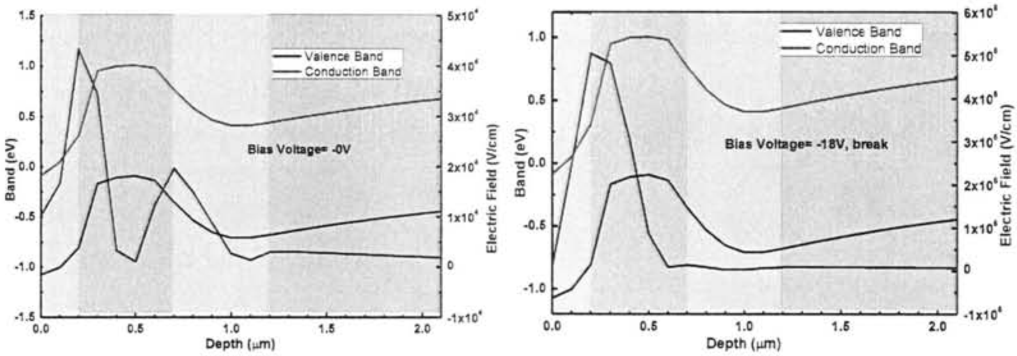

Figure 2 the energy band and electric field of the device at (a)0V and (b) -18V.

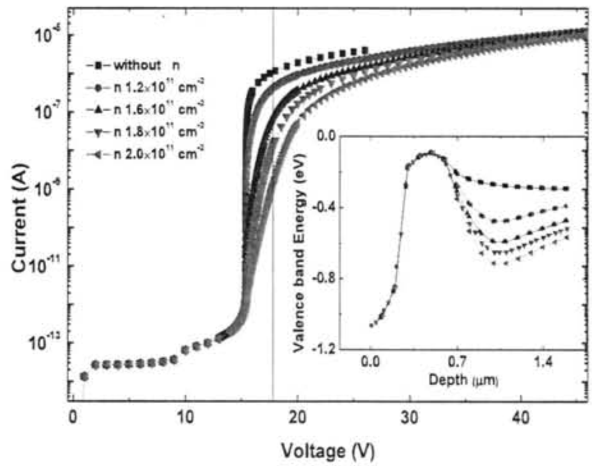

Figure 3 shows the I-V characteristic curves without illumination for different phosphorus implantation dose. The inserted figure is the relation between deep and valence band energy.

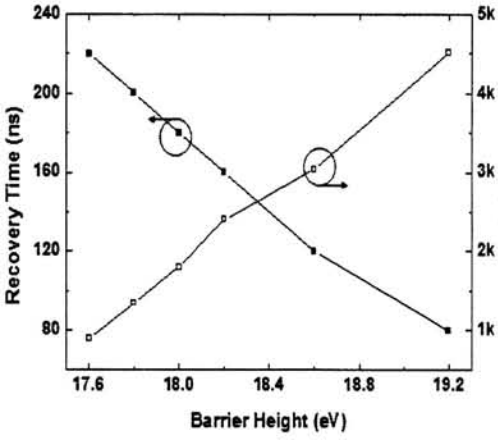

Figure 4 shows the change rules of the recoery time and gain with the barrirer height (ΔE_V) .

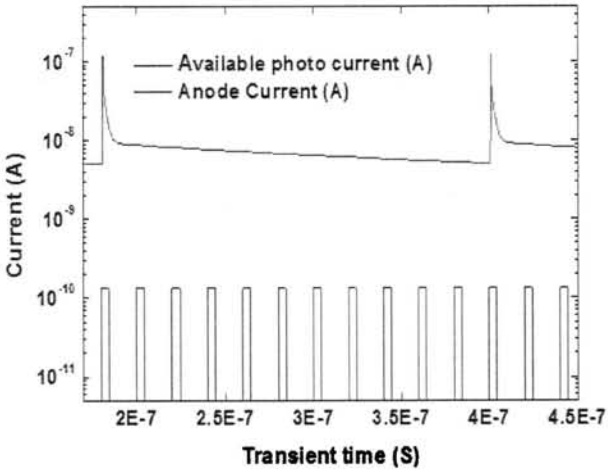

Figure 5 the simulation output by silvaco of the device with a light pulse input and the pulse period is 20ns.

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Research of high performance Ge/Si avalanche photodiodes for single-photon detection

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Abstract: A separate-absorption-charge-multiplication Ge/Si avalanche photodiode was designed. The devices have high dark current at low reverse bias, because of surface impurity and rough sidewall. A guard-ring structure and in-situ doping was introduced to decrease leakage-current.

OCIS codes: 040.1345, 040.5160.

1. Introduction

Single-photon avalanche diodes (SPADs) with high responsivity and low dark-current over the visible and near infrared range can be widely used in imaging, telecommunication, and medical detections. Applications for high detection efficiency SPADs in the near infrared range (1.0 – 1.6μm) include quantum key distribution, 3-D imaging, time-resolved spectroscopy, several imaging techniques based on near infrared sources, etc. Because of lattice mismatch between Si and III-V compounds, a fundamental incompatibility with standard CMOS process is common for all of these technologies, and thus they cannot be mentioned as low-cost photon counters and large photon-counting pixel arrays. Ge-based photo-detectors on Si or silicon-on-insulator (SOI) have attracted much attention, because of high absorption at 1.1~1.6μm for germanium [1].

2. Fabrication

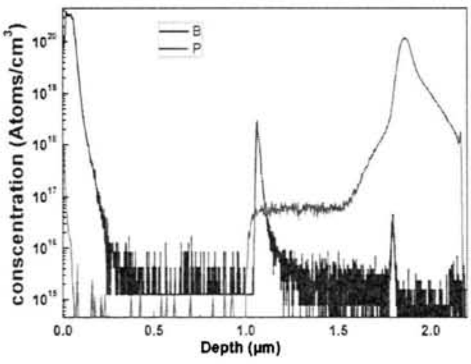

Figure 1 the doping concentration distribution measured by SIMS.

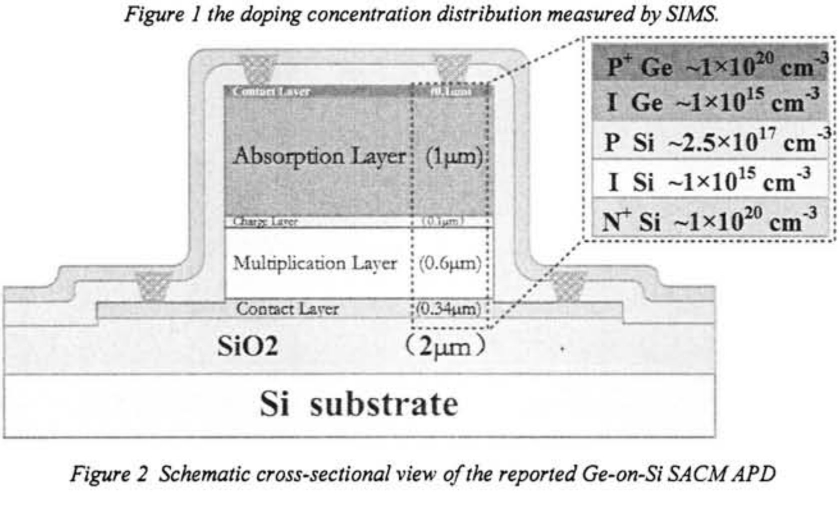

Figure 2 Schematic cross-sectional view of the reported Ge-on-Si SACM APD

In this paper, an SOI substrate with 2.0-μm-thick buried oxide and a highly phosphorus doped Si were chosen to reduce radio-frequency losses. Intrinsic silicon was deposited on the top n+-Si (001) layer of the SOI wafers using silicane (SiH_4) by cold wall ultrahigh vacuum chemical vapor deposition (UHV-CVD). Then, the wafer was implanted with BF^{2+} ions on the top of Si film to form the charge layer. In order to minimize the dislocation density of the heterogeneous region, the hetero-epitaxy of 50-nm-thick Ge on Si was initiated at 290 °C. After the low-temperature Ge buffer deposition, the substrate temperature was elevated to 600 °C and Ge was deposited on the buffer layer [2, 3]. The wafer was implanted with BF2+ ions on the top of Ge film and went through a rapid-thermal-annealing (RTA) process. The doping concentration distribution for the wafer was measured by SIMS, shown in Figure 1. Normal-incidence Ge/Si SACM-APDs are realized as a double-mesa structure, which are fabricated by dry etching [4]. Ti/Al for the pad contacts was deposited by e-beam evaporation and patterned by lift-off. The structure of the device is shown in Figure 2.

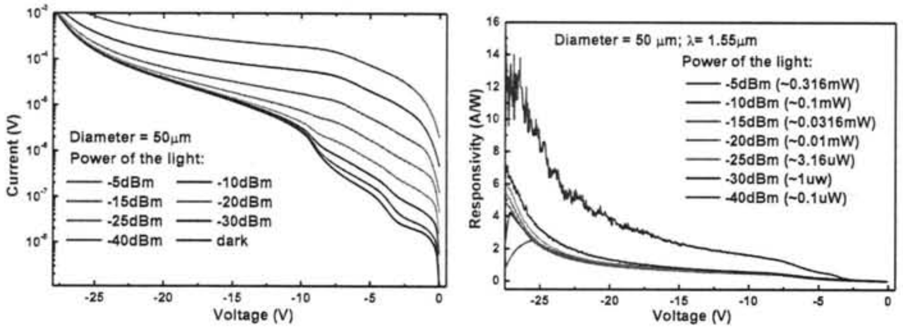

Figure 3 (a) Measured reverse current-voltage characteristics with several incident optical powers at 1550 nm for a 50μm-diameter detector and (b) the responsivity via reversed bias voltages, respectively.

Figure 3(a) shows reverse current-voltage characteristics of a typical 50μm-diameter device with different incident optical powers at 1550nm and the respective gains are shown in Figure 3(b). The huge noise of the device has a strong impact on the improvement of the gain characteristic of the APD.

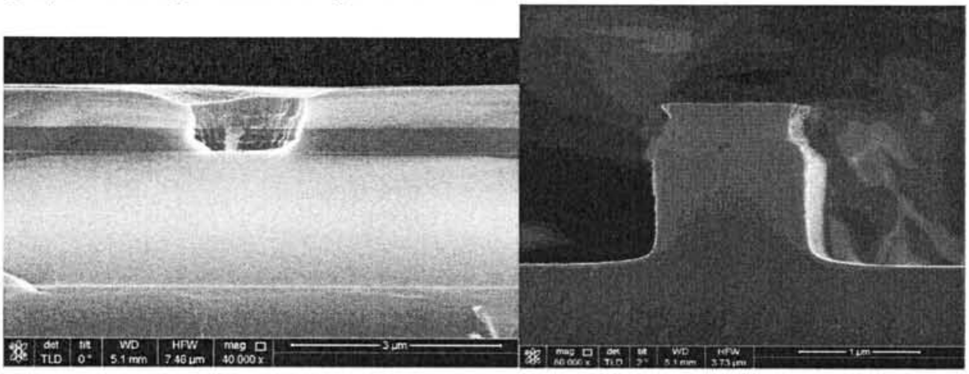

Figure 4 (a) A SEM image of the cross-section drawn of the square dot on the surface of the sample and (b) the SEM image of the sidewall after ion etching.

Figure 4(a) is a SEM image of the cross-section drawn of the square dot on the device surface. We concluded that, the square dots are inherent for silicon and germanium epitaxial layer because of the surface impurity. These square pits insert local electric field, limit the horizontal transport of the carriers, and increase the leakage current and odds of breakdown and failure for the devices. Therefore, in-situ doping will be used to form the charge layer, instead of ion implanting. The whole epitaxy process could finish in the vacuum growth cavity of UHV-CAD without second impurity pollution. The high roughness of Ge-layer sidewall also increase the leakage current, shown in fig 4(b). Therefore, the guard-ring structure will be used to decline the electric field around the sidewall and decrease the sidewall leakage current.

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High-responsivity and high-saturation-current Si/Ge uni-traveling-carrier photodetector

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ABSTRACT

A Ge-on-SOI uni-traveling carrier (UTC) photodetector was reported for high-power high-speed applications. The performances, in terms of dark-current, photocurrent responsivity and 3-dB bandwidth, were characterized for analog and coherent communications applications. The responsivity was 0.18 A/W at 1550 nm. The detector with a 40μm-diameter demonstrated an optical bandwidth of 2.72 GHz at -5V for 1550nm. The -1dB compression photocurrent at 1 GHz under -7V for 40μm-diameter device was about 16.24mA, the RF output power came to be 4.6 dBmw.

Keywords: Optical telecommunication, germanium, saturation, photodetector

1. INTRODUCTION

High-current photodiodes, receiving communication signal in near-infrared range, have great benefit to various photonic systems, because high-power output could increases the dynamic range, reduce the loss and noise figure in externally modulated links[1,2,3] and simplify the high-bit-rate digital receivers[4]. The output radio frequency signal level from the photodetector possibly increases with the output photocurrent, which is particularly important for the optically steered phased array antennas. Any increase in photodetector output signal level could reduce the necessary phase- and amplitude-matched electronic gain at each antenna element. Generally, photodetector output power is limited by the voltage drop and swing, space-charge effect and thermal effect. The uni-traveling-carrier (UTC) photodiode was designed to overcome the space-charge effect of p-i-n devices by using a graded p-type doping absorption layer instead of intrinsic layer [5]. The InGaAs/InP materials were dominant in the UTC photodetector field because of their excellent optoelectronic properties [6,7,8,9]. However, the silicon-based germanium devices have better thermal conduction than InGaAs/InP devices. This is because the thermal conductivity of germanium is 11 times higher than the InGaAs when used as the absorption material in infrared communication wavelengths, and the silicon substrate, has a higher thermal conductivity than InP [10]. Moreover, the silicon-based Ge devices have compatibility with Si complementary metal-oxide semiconductor (CMOS) and could integrate electronic circuits or systems on a chip at low cost. Therefore, the Si/Ge UTC photodetector should be an excellent candidate in high-power output receiver systems[11,12].

In this paper, the Si/Ge UTC photodetectors were designed, fabricated and measured. The direct current and radio frequency characteristics of this Si/Ge UTC device were systematically discussed. The responsivity was 0.18A/W at 1550nm, a little lower than the theoretical value 0.22A/W, which was calculated by Scattering Matrix Methods (SMM). The -1dB compression current was 16.24mA, at 1 GHz under -7V bias for 40μm-diameter device, which was similar with the predicted value by the voltage drop and swing, the space charge effect and thermal heating effect.

2. MATERIAL GROWTH AND DEVICE FABRICATION

The structure of the UTC Si/Ge photodetector is shown in Fig. 1(a). Si intrinsic film and p-doping Ge were successively grown by cold-wall ultra-high vacuum chemical vapor deposition (UHV-CVD) on n-type heavy doped silicon-on-insulator (SOI) substrate. The SOI substrate was first cleaned by an ex situ improved wet-chemical cleaning recipe, loaded into a pretreatment chamber, and then degassed at 300 °C. Afterwards, the substrate was heated up to 920 °C for 5 min in the growth chamber under a background pressure lower than 5×10^{-8} Pa to deoxidize. A 380 nm thick Si layer was further grown at 750 °C using pure Si_2H_6. After a short growth interruption to change growth temperature to 290 °C, a 60 nm thick Ge buffer layer was grown, followed by a 600 nm gradient boron doped Ge layer grown at 600 °C using pure GeH4 and diluted B_2H_6. The thickness of Ge layer was 0.6 μm. The concentration of boron atoms in Ge film was controlled by the flow of the gas source precisely.

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© 2015 SPIE · CCC code: 0277-786X/15/$18 · doi: 10.1117/12.2186742

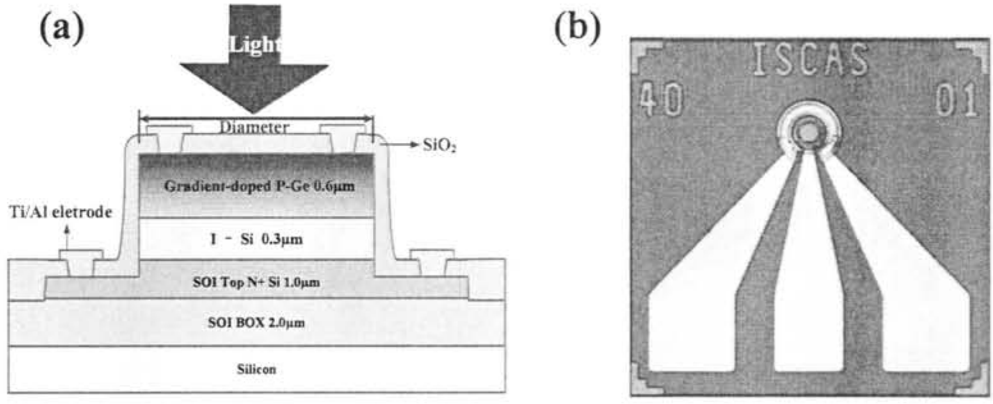

Figure 1(a) Schematic cross-sectional view of the reported Ge-on-SOI UTC photodetector; (b) Top view of a double-mesa structure of the Ge-on-SOI uni-traveling-carrier photodetector.

Circular mesas of Ge layer for normal incidence Si/Ge UTC photodiodes ranging from 20 to 40 μm diameter were defined by standard photolithography and inductively coupled plasma (ICP) etching. The second mesa was etched to the 2 μm thick buried oxide layer. The double mesa layout significantly reduced the parasitic capacitance. Top and bottom contacts were lithographically defined on evaporated Ti/Al and a rapid-thermal-annealing (RTA) process was followed for the impurity activation. A passivation/antireflection coating was deposited by plasma enhanced chemical vapor deposition. Windows for the metal contacts were opened by C_4F_8 ICP etching. The metal pad was evaporated and lifted off. The micrograph of a photodetector with a 40-diameter top mesa is shown in Fig.1 (b).

3. DIRECT CURRENT (DC) CHARACTERISTICS

The direct current characterizations of the photodetector include its dark-current and photocurrent responsivity. The dark current–voltage characteristic of the device was measured by an Agilent B1500A semiconductor parameter analyzer on a probe station without any illumination at room temperature. Moreover, the optical current–voltage characteristic of the device was obtained with a laser radiation at the wavelength 1550 nm and the power 1.2 mW.

3.1 Dark-current Characteristic

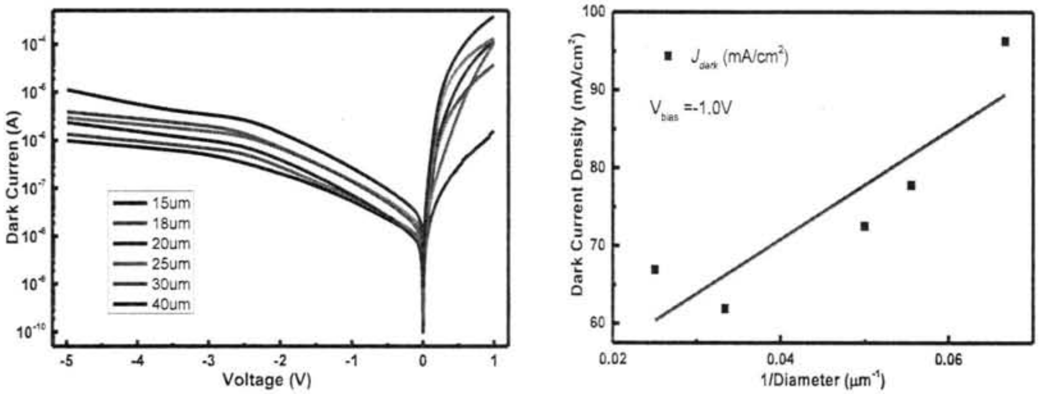

Figure 2(a) The dark-current-voltage characteristics of Si/Ge UTC photodetectors with different sizes. (b) Dark current density (J_{Total}) versus 1/D at 1-V reverse bias, where D is the device mesa diameter.

The dark current as a function of the applied bias voltage was measured for different mesa photodetectors. Fig. 2 shows the dark-current–voltage characteristics of the photodiodes with various mesa diameters at room temperature. For the photodiodes with a diameter of 15 μm, the dark current is 58 nA at a reverse bias of 1 V, corresponding to a current density of 96.3 mA/cm^2. For a 30-μm-diameter device, the dark current density was about 61.9 mA/cm^2 at −1 V.

Fig. 2 shows the total dark current density (J_{Total}) versus 1/d, where d is the device mesa diameter. For the photodetector operating at 1-V reverse bias, the bulk dark current density (J_{bulk}) is shown to be 42.9 mA/cm^2. The bulk dark current in a Ge photodetector has been proven to scale linearly with threading dislocation density N_{TDD} . Inserting a silicon film between germanium epitaxial layer and silicon substrate could increase the threading dislocation density around Si/Ge interface [7] and dark current bulk density. The dark current density can be reduced by appropriate thermal process [13].

3.2 Photocurrent Characteristic

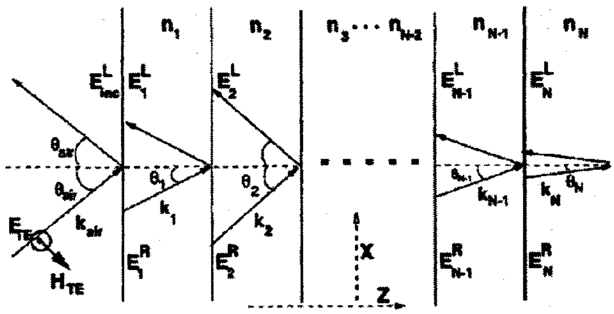

Figure 3 The schematic ID diagram of the multilayer structure. The light is typically incident in air. In each layer, the field can be defined completely by two cross-propagating waves with amplitudes E L and ER. The superscripts R and L point to the waves traveling to the right and left, respectively.

The main optical features of photodetector are the responsivity (R) and quantum efficiency (η). The ratio of light absorbed in the active region to the total incident light, assuming that all of the carriers generated by the absorption contribute to the photocurrent, indicate its absorption ability of optical power. The η are deduced from the electromagnetic (EM) field inside the device, which can be solved by applying Maxwell's equations with the appropriate boundary conditions [14]. In this paper, matrix techniques were used to calculate the reflectance and quantum efficiency, such as propagator matrix and transfer matrix methods, which are implicitly iterative and derive from the same basic EM principles as the recursive formulation. In the matrix method, the processed object is the local field, which is a sum of two cross-propagating waves. The elementary notion in matrix methods is to propagate the wave amplitudes at the input by a proper combination of 2×2 matrices. The information contained by the matrix depends on the formulation of the particular method, but nevertheless is derived from optical constants, wavelength, and polarization of the incident light.

In the perspective of Scattering Matrix Methods (SMM), the building blocks of the structure are the propagation element (the layers where the waves propagate freely) and the interface element (where the boundary conditions apply). As shown in Figure 3, at every point the field is a sum of two counter propagating waves.

$$E(x,z) = E^R e^{-in(k_{0x}x - k_{0z}z)} e^{-\kappa k_{0z}z} + E^L e^{-in(k_{0x}x + k_{0z}z)} e^{\kappa k_{0z}z} \quad (1)$$

Each element transforms the values of the wave amplitudes at its inputs into new values at its outputs. This operation is represented by matrices whose elements are determined by dielectric properties and boundary conditions:

$$\begin{bmatrix} E^R_{out} \\ E^L_{out} \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} E^R_{in} \\ E^L_{in} \end{bmatrix} \quad (2)$$

When the detectors are illuminated at normal incidence, the transfer matrix of single layer is:

$$\begin{bmatrix} E_{out}^{R} \\ E_{out}^{L} \end{bmatrix} = \begin{bmatrix} \dfrac{n_i + n_{i+1}}{2n_{i+1}} & \dfrac{n_i - n_{i+1}}{2n_{i-1}} \\ \dfrac{n_i - n_{i-1}}{2n_{i+1}} & \dfrac{n_i + n_{i-1}}{2n_{i+1}} \end{bmatrix} \begin{bmatrix} e^{ik_{0z}(n_i + i\kappa_i)d_i} & 0 \\ 0 & e^{-ik_{0z}(n_i - i\kappa_i)d_i} \end{bmatrix} \begin{bmatrix} E_{in}^{R} \\ E_{in}^{L} \end{bmatrix} \quad (3)$$

The physical cascade of the layers and the interfaces translate into a cascade of their matrices combined by simple matrix multiplication in the right order, which in turn yields the overall scattering matrix. The reflection (R) and transmission (T) of overall layers can be expressed as [15]:

$$R = \left|\frac{S_{21}}{S_{22}}\right|^2, \ T = \frac{n_N \cos\theta_N}{n_1 \cos\theta_1}\left|\frac{S_{11}S_{22} - S_{12}S_{21}}{S_{22}}\right| \quad (4)$$

Table 1. the parameters of each material layer for detector.

Layer (Top to Bottom)	Refractive index	Thickness (μm)	Absorption Coefficient ($\alpha=4\pi\kappa/\lambda$) ($\lambda$=1550nm)
SiO_2	1.47	0.65	0
Ge	4.0	0.6	4000 /cm [16]
Si	3.42	1.3	0
SiO_2	1.47	2	0
Si substrate	3.42	340	0

According to the SMM, the reflection (*R*) for these five layers was 0.50 and the transmission (*T*) was 0.32. Therefore, the quantum efficiency (η, $\eta=1-R-T$) was 0.18, and the theoretical responsivity for the Si/Ge UTC photodetector was 0.22A/W.

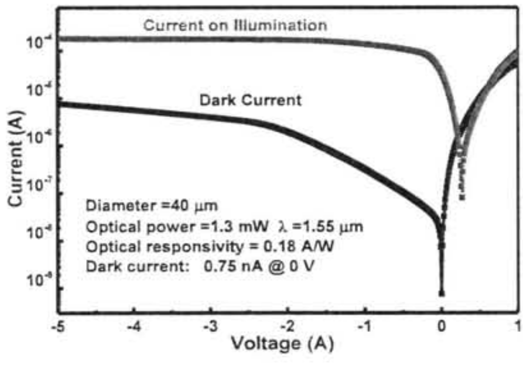

Figure 4 The current-voltage characteristics of the device without illumination and with laser radiation with input optical power of 1.3mW at 1550nm for the 40μm-diameter-device. The saturation of the optical responsivity values already at 0-V bias reveals that this photodetector configuration allows a complete photo-generated carrier collection without bias.and left, respectively.

The optical responsivity was measured by a setup, which consists of a semiconductor analyzer, a probe station and a special laser with a wavelength of 1550 nm. Light is coupled into the detector perpendicular to the surface with a single mode fiber probe. The DC responsivity was measured with a monochromatic light source at the wavelength of 1550 nm and power of 1.3mW, Fig. 3 shows the current of the device without the light and with the light normal incidence on the top surface. At a reverses bias of 1V, the optical responsivity was 0.18A/W at 1550nm. The quantum efficiency was 14.5%. The optical current at the zero bias indicates that this photodetector allows a complete photo-generated carrier collection even without any bias. The mismatch between dark and optical current at 0.7V~0.3V resulted from diffusion and collection of the photo-generated carrier because of the gradient doped of B and P atoms in actually epitaxial layers.

4. THE SATURATION

The device saturation current is obtained using a large signal measurement shown in Fig. 5. A heterodyne technique with two free-running lasers at 1550nm was used and a modulation index was finally obtained. A 100% modulation depth tone was fixed to 1GHz for the measurement of 40μm-diameter device whose 3-dB bandwidth was 2.7 GHz and the results are plotted in Fig. 5. The fabricated devices show high saturation photocurrents. For 40μm-dameter-device, -1dB compression current was measured 10.4, 13.7, 16.24 mA at -5V, -6V and -7V reverse-bias, respectively. There are three main effects limiting the photocurrent saturation of the devices.

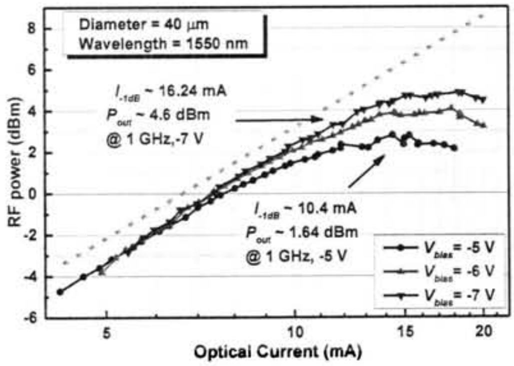

Figure 5 Large signal -1dB compression photocurrent measurement at 1GHz for the 40μm-dameter Si/Ge UTC-PDs with a 3-dB bandwidth of 2.7GHz.

5. CONCLUSIONS

In conclusion, the high-quality gradient doped germanium and intrinsic silicon materials were grown on top of silicon layer of the SOI substrate by the cold-wall ultrahigh vacuum chemical vapor deposition (UHV-CVD). High saturation Ge-on-SOI UTC photodetectors with different mesa diameters were fabricated by Si CMOS-compatible technology. The device performance was characterized by the dark-current, photocurrent responsivity, 3-dB bandwidth and 1dB compression current in the near IR range. This kind of photodetector had responsivity 0.18 A/W at the wavelength 1.55 μm, which has a good match with predicted value by SMM, and a dark current density 61.9 mA/cm^2 at the reverse bias 1V. And 3-dB bandwidth was 2.7GHz for 40 μm diameter at -5V bias voltage, which is limited by the transit-time of electrons in the absorber. Therefore, the optimization of the graded doping profile is imperative for increasing the response speed of the UTC photodetectors. The 1dB compression current of 40 μm-diameter device was 16.24mA at -7V, which approached to the predicted value by the three main effects of the photocurrent saturation.

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