ment of the collective excitations in two dimensions with respect to three dimensions. Furthermore, the minority-carrier correlation energy is found to be the dominant energy-gap narrowing term. On the other hand, an effective energy-gap widening occurs due to the upward shift of the electro-chemical potential into the conduction band (quantum-mechanical confinement). As a result the "effective" energy gap is found to be almost concentration-independent over a large electron-density range, and to increase at very high density values.

Growth and characterization of high-quality InP/$Ga_{0.25}In_{0.75}As_{0.5}P_{0.5}$ and InP/$Ga_{0.17}In_{0.83}As_{0.35}P_{0.65}$ grown by the LP-MOCVD technique. M. DEFOUR, F. OHMES, P. MAUREL and M. RAZEGHI. *Revue tech. Thomson-CSF*, **20–21**(3), 387 (1989) (in French). The purpose of this paper is the description of the growth and characterization of high-quality InP/$Ga_{0.25}In_{0.75}As_{0.5}P_{0.5}$ ($\lambda = 1.3\,\mu m$) and InP/$Ga_{0.17}In_{0.83}As_{0.35}P_{0.65}$ ($\lambda = 1.15\,\mu m$) grown by the LP-MOCVD technique using trimethylindium as indium source, triethylgallium as gallium source and the hydrides AsH_3 and PH_3 as V-elements sources, arsenic and phosphorus.

Models and experiments on degradation of oxidized silicon. C. T. SAH. *Solid-St. Electron.* **33**(2), 147 (1990). The concepts of electronic and protonic traps are introduced to delineate and classify the fundamental mechanisms of charging, generation, annealing and hydrogenation of electronic or electron and hole traps located in the interfacial (gate-conductor/oxide, oxide/nitride and oxide/silicon), insulator (oxide, nitride and oxynitride) and semiconductor surface layers of silicon MOS transistors and integrated circuits. Two matrix tables, one without tunneling (3 × 3) and one with tunneling (3 × 4) are used to classify the trap charging and electronic injection mechanisms according to the initial and final (band or bound) states of the electronic transition and the energy exchange mechanisms (thermal, optical and Auger-impact). The importance of tunneling to and from traps (TTT) as an oxide charge build-up mechanism is discussed. A theoretical tunneling rate to traps is given showing that traps shallower than about 2 eV from the oxide conduction band edge or 3 eV from the oxide valence band edge cannot be charged by the TTT transitions alone. Experimental examples illustrating the use of these mechanism tables as well as the importance of breaking hydrogen and strained intrinsic bonds by hot electron impact and by thermal hole capture are discussed, including: (i) annealing of the oxide/Si interface traps via hydrogenation during 38C chip bonding and during Fowler–Nordheim tunneling electron injection (FN-TEI) and avalanche electron injection (AEI) stresses, (ii) interface trap generation and positive oxide charge build-up during electron injection via FN-TEI or AEI, and (iii) electrical deactivation of boron and other group-III acceptors (Al, Ga, In) in the silicon surface layer during FN-TEI or AEI stresses. Examples at three d.c. bias conditions to delineate the dominant degradation mechanisms in silicon MOS transistors are given showing that trap charging via tunneling (FN-TEI, FNTHI and TTT) dominates below about 3.3 V in both *n*-MOS and *p*-MOS but trap generation via bond breaking by thermal hole capture may also occur in low voltage *p*-MOS. Higher than about 10 V, tunneling (FN-TEI, FNTHI and TTT) and avalanche injection (AEI and AHI) as well as hydrogen and intrinsic bond-breaking may all be important degradation mechanisms.

Growth and characterisation of high-quality GaAs/$Ga_{0.49}In_{0.51}P$ heterostructures grown by LP-MOCVD. F. OMES, M. DEFOUR, P. MAUREL and M. RAZEGHI. *Revue tech. Thomson-CSF* **20–21**(3), 407 (1989) (in French). We report in this paper the growth and characterization of high-quality GaAs/$Ga_{0.49}In_{0.51}P$ heterostructures grown by LP-MOCVD. The following results are presented: The first observation of a high-mobility two-dimensional electron gas in a GaAs/$Ga_{0.49}In_{0.51}P$ heterojunction is described. We measured a mobility of 80,000 cm^2/V.s.

Carrier multiplication and avalanche breakdown in self-aligned bipolar transistors. M. REISCH. *Solid-St. Electron.* **33**(2), 189 (1990). The extraction of the multiplication factor characterizing impact ionization in bipolar transistors is investigated in detail. In particular, two d.c. measurement methods, superior in measurement accuracy in comparison with any method published previously, are presented. These methods clearly separate the voltage dependence of the multiplication factor from the voltage dependence of the base Gummel number. The methods presented are shown to yield consistent results and are verified by a comparison with multiplication data derived from breakdown measurements. They allow easy experimental characterization of carrier multiplication effects in bipolar transistors, and provide a valuable tool for the on-chip investigation of inhomogeneities in space charge layers and for the identification of failure mechanisms. The analytical approximation for the multiplication factor due to Miller is found to provide a good description of carrier multiplication in epitaxial base collector junctions in the low-level multiplication regime if BU_{cbo} is substituted by the value $BU_{cbo,m} < BU_{cbo}$. The methods are applied but not restricted to self-aligned configurations and are of general interest for the precise characterization of impact ionization phenomena in reverse biased *pn* junctions.

The model of growth kinetics of very thin thermal silicon oxide layer. ROMUALD B. BECK and BOGDAN MAJKUSIAK. *Electron Technol. (Warsaw)* **21**(1/2), 65 (1988). In this paper the model of growth kinetics of silicon oxide in the beginning stages of thermal oxidation process is presented. This model is based on the balance between oxygen ion flux and two opposite electron fluxes flowing through the already formed oxide layer. The successful fitting to experimental data proved that this model may be used to describe the kinetics of thermal silicon oxide growth in the region within which the classical Deal–Grove formula is not valid (i.e. for $d_i \leqslant 20$ nm). The presented model enabled some conclusions to be drawn about the physical effects taking place during very thin oxide layer formation.

8. THICK- AND THIN-FILM COMPONENTS, HYBRID CIRCUITS AND MATERIALS

Hybrid IC technology leads to miniaturization. MITSUHARU TSUCHIYA. *J. Electron. Engng, Jpn*, 84 (October 1989). It has been 25 years since the hybrid IC was developed to meet the need for smaller and lighter products. Today it has given birth to SMT or surface mounting technology, which is used widely in a variety of applications. On the other hand, semiconductor ICs have displayed remarkable evolutionary progress both on a production and technical basis. The hybrid IC has opened the door to further development and growth.

New rules of resistance in small resistors. VIPIN SRIVASTAVA. *Solid St. Commun.* **73**(8), 541 (1990). The well-known rules of electrical resistance of macroscopic length scales that (i) it should increase monotonically as a narrow flat sample approaches one-dimensionality, and (ii) the resistances of two wires joined in series should add as $R_A + R_B$, do not hold at "mesoscopic" length scales (μm) as found in recent experiments. In place of (i) the resistance is found to be quantized as $h/(n2e^2)$ and (ii) is replaced by a simpler rule that the total resistance $R = R_A$ if $R_A > R_B$ or $R = R_B$ if $R_B > R_A$. These new results are explained in this paper.