CHAPTER 5

Readout Electronics for Infrared Sensors

John L. Vampola
Santa Barbara Research Center
Goleta, California

CONTENTS

5.1 INTRODUCTION

The readout integrated circuit (ROIC) is a highly integrated set of focal plane electronic functions combined into a single semiconductor chip. Its primary function is to provide infrared detector signal conversion and amplification, along with time multiplexing of data from many detectors to just a minimum number of outputs. ROICs can contain tens to hundreds of thousands of individual *unit cells,* each with critical detector amplifiers and multiplexer switches, as shown in Fig. 5.1. ROICs are normally processed using conventional silicon integrated circuit technology. They are most often implemented in complementary metal oxide semiconductor (CMOS) technology, allowing for higher resolution and greater sensitivity in today's sensors.

This chapter covers each of the ROIC functions shown in Fig. 5.1, including preamplifier, signal processor, multiplexer, and video amplifier sections. These functions are addressed in terms of major design drivers such as noise, dynamic range, and power. Since the signal-to-noise ratio (SNR) is the major driver in most sensor designs, each of the circuits is detailed in this context. The simplest circuits are introduced first to provide the basis for more advanced circuits. The resistor transimpedance amplifier (RTIA), which is most common in discrete configurations but also utilized in ROIC configurations, will be addressed initially to introduce many of the basic signal and noise concepts required for analysis of other preamplifier circuits in subsequent sections.

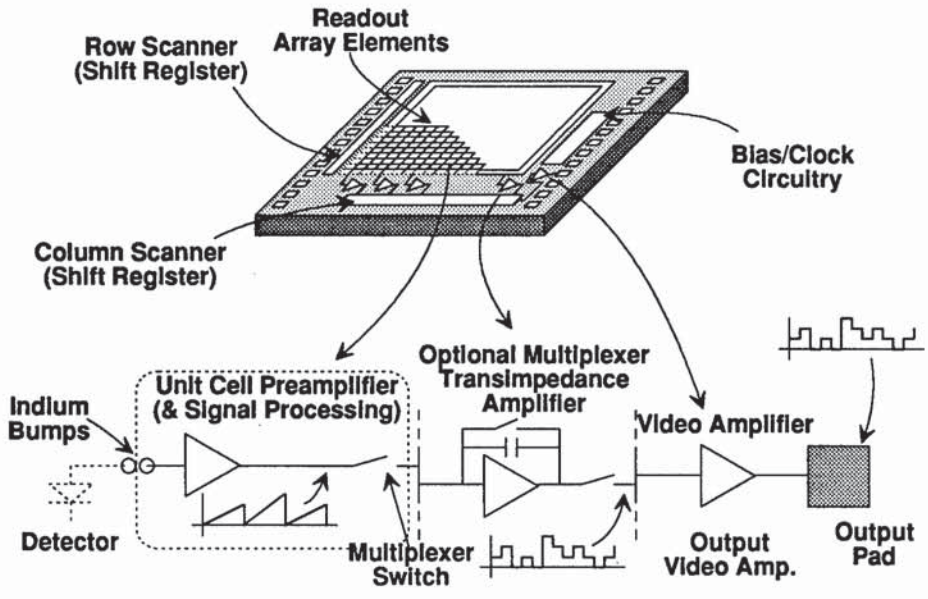


Fig. 5.1 The readout integrated circuit combines detector signal amplification, data multiplexing, and video output buffering of the infrared signal into a single chip. Shown is an example of a staring two-dimensional array.

High-impedance detectors, such as photovoltaics, extrinsic silicon, platinum silicide, and many photoconductors, are extremely sensitive to electromagnetic interference (EMI). A robust sensor design reduces EMI by locating the preamplifier as close as possible to the detector. Through the 1970s, preamplifiers were built up from discrete resistors, capacitors, and transistors into hybrids, which could be placed within inches of the detector. In the most sensitive applications, the front-end of the preamplifier, usually comprised of field effect transistors (FETs) and feedback resistors, was physically placed next to the detectors on the cold focal plane. Since a great amount of real estate would be required for such circuits, discrete amplifier designs put severe limitations on the number of detector channels that could be implemented in a given optical field of view.

The first integrated approaches to addressing both high-density scanning arrays and two-dimensional focal planes were designed in the 1970s. Visible sensors, the ancestors of today's camcorder focal planes, were demonstrated utilizing a single silicon chip composed of charge-coupled devices (CCDs) that served as both sensor and multiplexer. The advent of indium bump interconnect technology, whereby matching sets of small indium bumps are formed on the detector and the CCD, provided the mechanism for connecting a large array to its readout, forming a sensor chip assembly (SCA) as shown in Fig. 5.2. Because of this history, sensor users often refer to all ROICs as multiplexers or CCDs even though CCD devices may not be employed.

CCDs commonly utilize direct injection (DI) or gate modulation preamplifiers to buffer and accumulate the photon-induced current over a frame of scene data. These simple preamplifier types are covered in detail later in this chapter. Through the 1980s, as detector and integrated circuit densities increased, more elegant preamplifiers, as well as multiplexers and video drivers, were incorporated into the ROIC. These newer circuits expanded the use of SCAs to a broader set of applications by providing higher SNR, greater bandwidth, and better linearity. In addition to optimizing basic SCA functions,

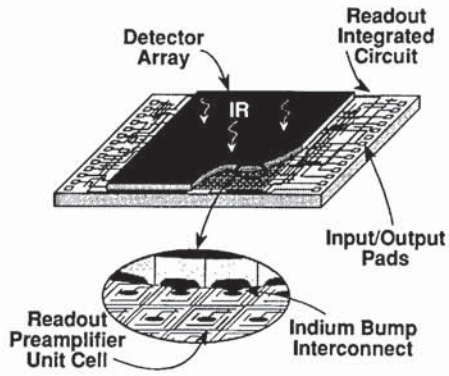


Fig. 5.2 The readout integrated circuit mates with the detector array via indium bumps to form the sensor chip assembly capable of integrating hundreds to millions of elements onto a single assembly.

many other signal processing functions have also been integrated into the SCA, such as detector frame store and circuits that eliminate amplifier drift.

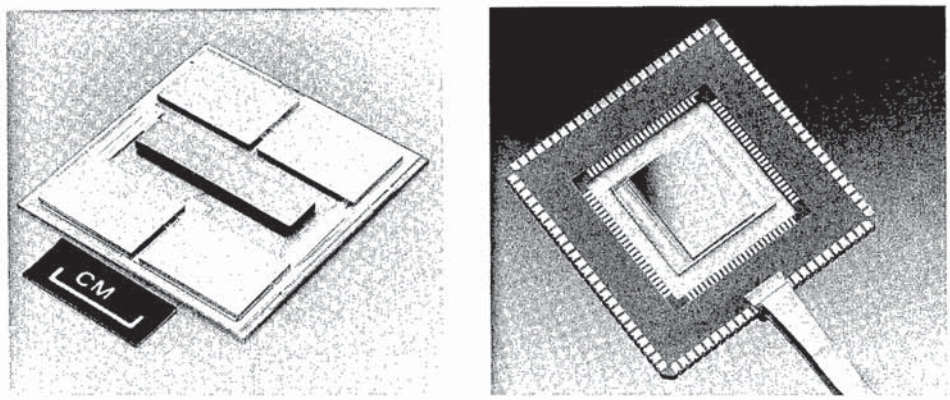
The ROIC, together with the detector, can be assembled to form various SCA configurations. The most common infrared configurations are the direct and the indirect hybrid SCAs of Fig. 5.3. A third type, the monolithic SCA configuration, is common in visible applications.

The direct hybrid SCA approach is common in high-density staring and scanning applications, which provide sufficient unit cell area under the detector element to accommodate a readout preamplifier and its associated circuitry. The direct hybrid SCA has fewer parts than the indirect and is therefore generally more producible.

Indirect hybrid SCAs can include one or more detector arrays fanned out to one or more ROICs via a single fanout board. Larger, more elaborate preamplifiers and signal processing electronics can be fabricated in the larger unit cells of indirect readouts, since the circuit area is no longer constrained to the real estate available under the detector element. The indirect hybrid can also reduce the stress caused by thermal mismatch between the detector and ROIC materials, thereby increasing the thermal cycle life of large SCAs.

A variation of the direct hybrid SCA design is the siderider SCA. This type of SCA includes additional signal processing circuitry, such as time delay integration (TDI), in the area of the ROIC adjacent to the detector array. The preamplifier signal, originating under each of the detector elements, is enabled to this siderider area of the ROIC for additional signal processing prior to being transmitted off the focal plane.

The monolithic device has both the detector and readout circuitry fabricated into a single semiconductor material. An example of a silicon monolithic device is the commercial camcorder SCA, which has the readout fabricated in the silicon adjacent to each of the detector elements. In this case the detector optical area is reduced to accommodate the readout circuitry, resulting in a low de-



(a) (b)

Fig. 5.3 (a) The 960 × 4 element detector with four readouts mounted on a motherboard is an example of an indirect scanning SCA. (Courtesy of DARPA) (b) The 640 × 480 element detector array coupled directly to the readout is an example of a staring direct hybrid SCA. (Courtesy of Santa Barbara Research Center)

tector (or optical) fill factor. Applications of the monolithic approach are also found in shorter wavelength infrared detector material, which utilizes CCD and FET devices.[1]

Common readout integrated circuit symbols, nomenclature, and units are given in Table 5.1.

5.2 MOSFET PRIMER

Although discrete preamplifiers can be designed with bipolar junction transistor (BJT) or junction field effect transistor (JFET) technology, integrated circuit forms of the preamplifier are most commonly fabricated in silicon CMOS technology because of the operating temperature range, power, and noise characteristics of the metal oxide semiconductor FET (MOSFET). Silicon CMOS devices can be designed[2] to operate from room temperature to below 10 K. This MOSFET primer is meant as an introduction only. Detailed explanations of semiconductor physics and MOSFET action are available through many sources.[3,4] Liu and Nagel[5] treat the modeling of MOSFETs.

The *N*-channel MOSFET, shown in Fig. 5.4, is composed of *n*-implanted drain and source regions isolated from each other by the *p*-doped silicon substrate, or *P*-well. A gate, usually composed of polysilicon, lies above a thin dielectric layer (usually SiO_2) on the semiconductor surface between the two diffusions. In the simplest transistor action, a positive gate-to-source voltage V_{gs} induces a field in the surface region of the semiconductor. If the gate voltage is above a specific threshold V_t, the resulting field repels majority mobile carriers (holes) and attracts electrons, forming a very thin inversion region, or *n*-channel, at the surface of the semiconductor. The *n*-channel then provides a current path between the source and drain. The *P*-channel MOSFET is the same as the *N*-channel device but it utilizes opposite doping and voltages.

A sample plot of the drain current versus drain voltage at several gate voltages is shown in Fig. 5.4. Higher gate voltages increase the density of electrons at the surface and thus increase the conductance of the channel between source and drain diffusions. This action is useful in ROICs, because MOSFETs can be utilized as switches for multiplexing signals and resetting integration capacitors. MOSFETs are dimensioned according to the width W and length L of the channel. A short channel length will result in a desirable lower "on" resistance. Lower "on" resistance also can be achieved by either connecting two switches in parallel or by simply increasing the channel width of a single device. When the switch is on, the voltage between the source and drain is very small, and the transistor acts as a voltage-dependent resistor:

$$I_d \text{ (linear)} \approx \frac{W}{L}\mu_n C_0(V_{gs} - V_t)V_{ds} \quad [\text{A}] \ , \tag{5.1}$$

where μ_n is the minority carrier mobility (electron in this case), C_0 is the gate capacitance per unit area, V_{gs} is the gate-to-source voltage, V_t is the threshold voltage, and V_{ds} is the drain-to-source voltage. The "on" resistance of the MOSFET in the linear region of operation is approximately

Table 5.1 Common Readout Symbols, Nomenclature, and Units

Symbol	Description	Units
A_{opt}	Optical area of the detector	cm^2
A_{sf}	Source follower buffer gain	V/V
A_v	Amplifier or buffer voltage gain	V/V
C_{clamp}	Clamp storage capacitor	F
C_{fb}	Feedback capacitance	F
C_0	MOSFET gate capacitance per unit area	F/cm^2
C_{sh}	Sample and hold storage capacitor	F
C_{st}, C_{stray}	Stray node capacitance	F
D^*	Normalized detector signal to noise	Jones
Δf	Power bandwidth	Hz
e_{in}	Input referred noise voltage	volts rms
e_n	Input noise voltage	volts rms
f	Frequency	F
g_m	MOSFET drain current to gate-source voltage (transconductance)	mohs
i_{det}	Detector noise current	amps rms
i_{in}	Input referred noise current	amps rms
i_{int}	Integrated photon-induced current	A
i_n	Input noise current	amps rms
I_d	MOSFET drain current	A
I_{dark}	Detector dark current	A
k	Boltzmann constant	J/K
L	MOSFET channel length	cm
m	MOSFET subthreshold factor	—
NEC	Noise equivalent charge	e^-
NEI	noise equivalent irradiance	$ph/cm^2\ s^{-1}$
q	Electron charge	C
q_c	Noise charge on a capacitor	e^- rms
r_{det}	Detector resistance	Ω
r_{in}	Amplifier input resistance	Ω
r_s	Source (detector resistance)	Ω
R	Resistor	Ω
R_{fb}	Feedback resistance	Ω
R_{on}	MOSFET "on" resistance	Ω
R_0	Zero bias detector resistance	Ω
t_{frame}	Period from frame to frame	s
t_{int}	Signal current integration time	s
T	temperature	K
T_{det}	Detector temperature	K
T_{Rfb}	Feedback resistor temperature	K
v_c	Noise voltage on a capacitor	volts rms
v_{out}	Output referred noise voltage	volts rms
V_{ds}	MOSFET drain-to-source voltage	V
V_{gs}	MOSFET gate-to-source voltage	V
V_t	MOSFET turn on threshold voltage	V
W	MOSFET channel width	cm
Z	Charge to voltage gain	V/C
Greek:		
η	Photon to electron conversion efficiency	e^-/ph
η_{ie}	Photon current injection efficiency	A/A
μ_n	*N*-channel MOSFET minority carrier mobility	$cm^2/V\ s^{-1}$
$1/f$ noise	Noise of $1/f$ power spectral density characteristics (drift)	

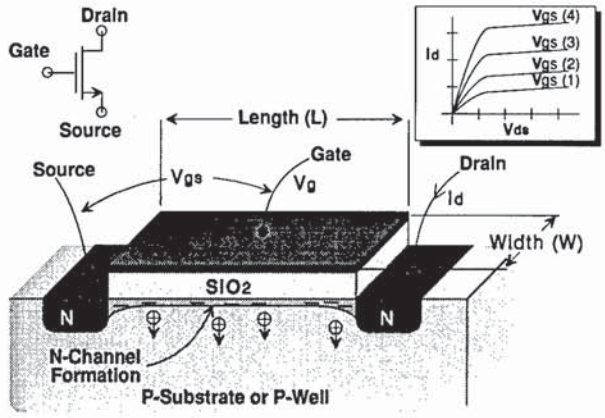


Fig. 5.4 Most ROICs utilize the MOSFET to perform as both amplifier and switch. Drain current is controlled by the gate-to-source voltage.

$$R_{\text{on}}\ (\text{linear}) \approx \frac{L}{W\mu^n C^0(V^{gs} - V^t)} \quad [\Omega] \ . \tag{5.2}$$

This simple explanation of transistor action is adequate, in the case of the switch, where the voltage between source and drain is driven to zero when the switch is on. When the drain-to-source voltage is increased, however, the drain current eventually saturates and no longer increases with the drain voltage. The transistor is then said to be in *saturation*, which is the case with most analog MOSFET amplifiers. The drain saturation current can be approximated as

$$I_d\ (\text{sat}) = \frac{W}{2L}\mu_n C_0(V_{gs} - V_t)^2 \quad [\text{A}] \ . \tag{5.3}$$

Analogous to the "on" resistance of a switch, the most important parameter describing the action of the MOSFET amplifier is its transconductance g_m, which is defined as the change in drain current for a given change in gate-to-source voltage

$$g_m\ (\text{sat}) \approx \frac{W}{L}\mu_n C_0(V_{gs} - V_t) \sim \left(2\frac{W}{L}\mu_n C_0 I_d\right)^{1/2} \quad [\text{mhos}] \ . \tag{5.4}$$

Equations (5.3) and (5.4) approximate the action of MOSFETs that are in strong inversion ($V_{gs} > V_t$). MOSFETs in weak inversion are discussed later in this chapter for the specific case of a direct injection preamplifier.

5.3 TRANSISTOR NOISE

Although most modern ROICs are comprised of MOSFETs and other components formed in CMOS integrated circuit technology, MOSFETs are not always

the best choice for low noise amplification of detector signals. There is a strong relationship between detector impedance and optimum readout technology. Although the silicon MOSFET covers most infrared applications, it is not well suited for all detectors. Specifically, discrete readout preamplifier implementations, popular in systems with few detector elements, can benefit from BJT, JFET, or MOSFET technology.

Detectors can be divided into two impedance categories: low-impedance sensors (lower than 10 kΩ), such as long-wave IR photoconductive HgCdTe detectors, and high-impedance sensors (greater than 10 kΩ), such as photovoltaic, extrinsic silicon, and platinum-silicide detectors. Noise in detectors is generated by the incident photon flux as well as inherent noise sources in the detecting element itself. The input active device of the ROIC preamplifier, a transistor, is usually the dominant noise contributor of the readout. The preamplifier should provide enough gain to balance, if not render negligible, downstream noise source contributions. If this is the case, the input transistor becomes the principal factor in readout noise performance.

The noise contribution of the input transistor is a function of the source impedance presented by the detector. Thus, it is important to match the detector with an appropriate readout input transistor. A schematic representation of a detector and the input transistor of an amplifier are shown in Fig. 5.5. The functions e_n and i_n are the equivalent input noise voltage and current of the transistor and are usually expressed in terms of noise power spectral density versus frequency. It can be generalized that a high transistor noise current, coupled with a high-impedance detector, can result in high-noise gain on the input node. Conversely, a low-impedance detector can tolerate high-noise current but will suffer from high-noise voltages. The equivalent input noise voltage e_{in} for a transistor or preamplifier in a voltage mode amplifier configuration is given by

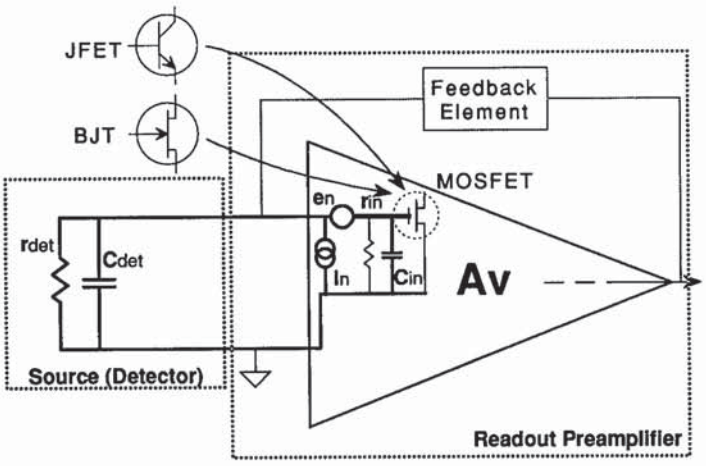


Fig. 5.5 Input referred noise of the preamplifier is usually driven by the input transistor. MOSFETs and JFETs have low i_n, while BJTs have low e_n.

$$e_{\text{in}} \approx \left\{\left[\frac{e_n r_{\text{in}}}{(r_{\text{in}} + r_s)}\right]^2 + (i_n r_{\text{in}} \| r_s)^2\right\}^{1/2} \approx [e_n^2 + (i_n r_s)^2]^{1/2} \quad [\text{V}/\sqrt{\text{Hz}}] \qquad (5.5)$$

for the nominal case where the voltage mode amplifier input impedance r_{in} is very high. The impedance $r_{\text{in}} \| r_s$ is the parallel combination formed by the input impedance of the amplifier (or transistor) and the source resistance. The output referred noise is the product of e_{in} and the voltage gain of the amplifier A_v. In current-to-voltage, or transimpedance, amplifiers, it is useful to express the noise in terms of an equivalent input noise current, i_{in}, instead of a voltage:

$$i_{\text{in}} \approx \left\{\left[\frac{i_n r_s}{(r_{\text{in}} + r_s)}\right]^2 + \left(\frac{e_n}{r_{\text{in}} \| r_s}\right)^2\right\}^{1/2} \approx \left[i_n^2 + \left(\frac{e_n}{r_s}\right)^2\right]^{1/2} \quad [\text{A}/\sqrt{\text{Hz}}] \qquad (5.6)$$

for the nominal case of a transimpedance amplifier where the input resistance is very low. The output referred amplifier noise is the product of i_{in} and the amplifier transimpedance Z_t.

Noise current and voltage for typical low-noise transistor technologies in the common source (or common emitter) configuration are plotted in Fig. 5.6. The noise is typical for low-noise devices such as discrete JFETS and BJTs, as well as for MOSFETs that might be found in a CMOS integrated circuit. Noise data for discrete BJT and JFETS are available from manufacturer's data books, whereas integrated circuit MOSFET noise is typically measured and modeled statistically for a given integrated circuit process and transistor geometry.

Within the system bandwidth of interest, the characteristics of e_n and i_n may not be flat with frequency, that is, white noise. These characteristics may

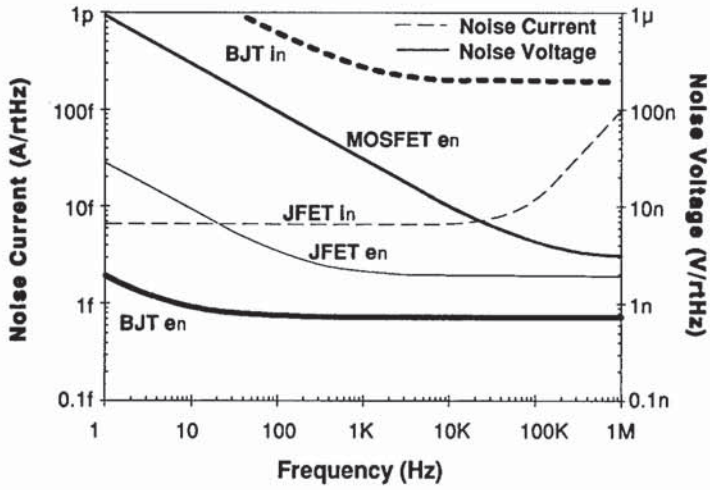


Fig. 5.6 Noise voltage and currents for typical low-noise BJTs, JFETs, and MOSFETS. MOSFET noise current is negligible.

be boosted at low frequencies, as is the case for $1/f$ noise, or boosted at high frequencies. Therefore, the total output rms noise must be calculated by integrating the power spectral densities, plotted in Fig. 5.6, for example, over the equivalent noise power bandwidth required, and then multiplying this by the gain of the amplifier:

$$v_{\text{out}}^2(e_n) = \int_{f_{\text{low}}}^{f_{\text{high}}} A_v^2(f) e_{\text{in}}^2(f)\, df \quad [\text{V}^2] \ , \tag{5.7}$$

or, for a transimpedance amplifier,

$$v_{\text{out}}^2(i_n) = \int_{f_{\text{low}}}^{f_{\text{high}}} Z_t^2(f) i_{\text{in}}^2(f)\, df \quad [\text{A}^2] \ , \tag{5.8}$$

where A_v and Z_t are the voltage gain and current transimpedance, respectively. The total rms output noise voltage from all noise components is summed in the power domain, for example,

$$v_{\text{out}}\ (\text{total}) = [v_{\text{out}}(i_n)^2 + v_{\text{out}}(i_{\text{det}})^2 + v_{\text{out}}(i_{\text{ph}})^2 + \ldots]^{1/2} \quad [\text{volts rms}] \ . \tag{5.9}$$

Figure 5.7 shows the ratio of amplifier (or input transistor) noise to detector thermal noise, as a function of detector source resistance, for the BJT, JFET, and MOSFET examples in the common emitter or source configuration. The calculations for detector (and resistor) thermal noise are covered later in this chapter. Notice that for photovoltaic detectors, which typically have impedances above 1 MΩ, MOSFET noise under the conditions given is lower than the detector thermal noise. MOSFETs, however, are not the optimum choice for detectors with impedance below 100 kΩ, such as some low-resistance photoconductors; bipolar transistors are the best choice in these cases. JFETS,

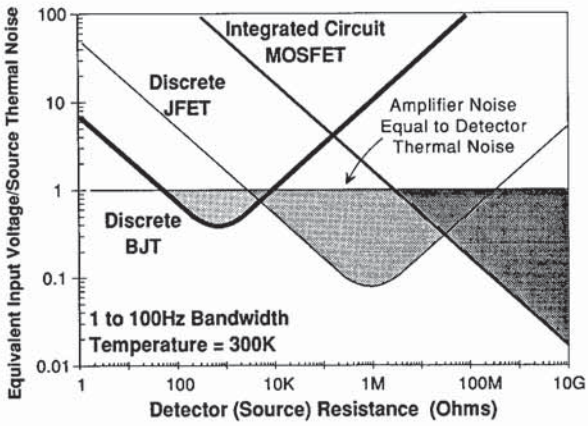


Fig. 5.7 Bipolar transistors offer low noise for low-impedance detector applications, while JFETs and MOSFETs offer low noise for high-impedance detectors.

common in discrete amplifier circuit configurations, offer greater performance than MOSFETs out to 100 MΩ, even at room temperature; and, although not shown, cooled JFETS have continued low-noise performance well beyond 100 MΩ, because shot-noise-inducing input bias current is significantly reduced with temperature.

There are two primary sources of noise in MOSFETs. The white (flat with frequency) channel thermal noise, usually input referred as a voltage from gate to source, is given as

$$e_n = \left(\frac{\frac{8}{3}k\,T\Delta f}{g_m}\right)^{1/2} \quad [\mathrm{V}] \tag{5.10}$$

for both MOSFETs and JFETs.[6] Unpublished data indicate that the actual channel thermal noise on some MOSFETs may be higher than that predicted here.

MOSFET $1/f$ noise comes primarily from current fluctuations caused by surface states at the interface of the MOSFET channel and the gate oxide.[7] These surface states capture an electron (or hole) and release it at a later time.[8] The $1/f$ noise is a strong function of the CMOS process and can vary significantly from one process lot to another. In general, $1/f$ for a given process can be reduced through circuit design by increasing the gate area, WL, or the gate capacitance, C_{0x}, of the MOSFET

$$e_{n(1/f)} \propto \left(\frac{1}{WLC_0 f^{\alpha}}\right)^{1/2} \quad [\mathrm{V}/\sqrt{\mathrm{Hz}}]\ , \tag{5.11}$$

where α is normally modeled as -1.0, but can vary between process lots.

5.4 ROIC PERFORMANCE DRIVERS

Sensor electronic designs, whether discrete or ROIC, are guided by requirements traceable to system performance parameters or input/output interface requirements. Key ROIC requirements are matched with respect to key system or interface requirements in Table 5.2.

The SNR is the prime design driver in most sensor systems. To achieve SNR objectives, trade-offs must often be made between detector temperature, circuit area, and power. Other important drivers include dynamic range, linearity, and operability. All requirements are interrelated and can usually be met given great enough real estate (detector size), power, and a low detector temperature. These conveniences are rarely allowed, resulting in designs requiring many trade-offs and compromises between parameters. The designer should develop a dialog with the sensor user so that the evolving design accurately reflects the users needs.

5.5 ROIC PREAMPLIFIER OVERVIEW

Most ROICs utilize preamplifiers that accumulate detector photon-induced current over a fixed integration time. The detector current, accumulated in an

Table 5.2 Relationships between Key Readout Circuit Requirements and System Performance and Interface Issues

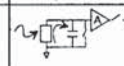
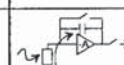
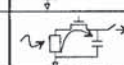
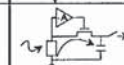
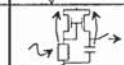
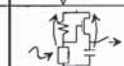
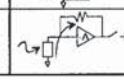
Major Readout Performance Parameters	Related System Parameter or Interface Impact	Comments
NEC (noise equivalent charge)	Sensitivity	Minimized to enhance SNR
Power dissipation	Cooldown time Life Weight	Limited cryogen/cooler life Cryogen weight/cooler size
Dynamic range	Maximum saturation signal	Loss of signal
Crosstalk	System MTF (resolution) Blooming of saturated elements	Element to element
Frequency response	System MTF (resolution) Latent images	Often related to crosstalk
Input impedance	Signal linearity Noise	Detector bias changes with signal Loss of optimum detector bias
Linearity reliability	Calibration Instrument life	Proper identification Confidence of success
Gain	Sensitivity	Signal amplified above system noise floor
Output video driver impedance	Sensitivity MTF	EMI from environment crosstalk between multiplexed elements

integration capacitor or CCD "bucket," results in a signal that is periodically sampled and multiplexed out of the preamplifier. The integration capacitor is reset and the process starts over again. A less common form of ROIC preamplifier provides continuous output voltage or current, which is proportional to the detector current, in lieu of an accumulated signal at the end of the frame time. The most common families of preamplifiers and their typical performance capabilities are given in Table 5.3. It is worth noting that the listed performance capabilities represent typical preamplifier applications and that it is possible, through careful design, to broaden the application space of the various configurations. Each of these configurations is briefly described here and then treated in detail in later sections. Many of these circuits and related topics are also addressed by Nelson, Johnson, and Lomheim.[9]

The self-integrator (SI) has the fewest unit cell components among all readout circuit configurations. Photon-induced charge is integrated over a given frame time directly onto the integration capacitance formed on the detector node, and is periodically transferred out of the unit cell via the multiplexer switch (MUX). The output of the SI is in the charge domain as opposed to the voltage domain. The action of the MUX, while enabled, resets the integration capacitor at the end of each frame.

A buffer amplifier can be added to the SI to provide voltage domain readout to the MUX. This implementation, normally a MOSFET source follower per detector (SFD), requires a reset switch on the detector node to reset the integration capacitor, because the MUX cannot provide reset through the buffer.

Table 5.3 Common ROIC Preamplifiers Selected According to the Limitations and Performance Requirements of the Specific Application

Circuit	Block Diagram	Circuit Description	Minimum Multiplexer Required (MUX)	Typical Noise (e^-) at Frame Rate**	Dynamic Range V_{sat}/V_{ns}	Frequency Response (KHz)	Power Per Cell (μW)	Non-Linearity	Detector Bias Uniformity	Minimum Unit Cell Area (μmxμm)	Irradiance Range at 1KHz F.R. (ph/cm²/s)
SI - Self Integrator		Reset Integrator	CCD or Active Amp. Prior to Video Amp.	400 at 1KHz	≥200 High Noise Low Signal	>200	<0.5μW	Tracks Detector I-V	~1mV to 10mV	<10 x <10	<1x10⁹ to ~3x10¹⁴
SFD - Source Follower/ Detector		Buffered Reset Integrator	Video Amplifier	50 - 100 at 10Hz	~2,000 Low Signal	>200	~0.5μW	Tracks Detector I-V	1mV	<20 x <20	<1x10⁹ to ~3x10¹⁴
CTIA - Capacitor Feedback TIA		Miller Reset Integrator	Video Amplifier	40 - 150 at 10KHz	>10,000 - Low Noise High Signal	>200	3μW - 40μW	Reduced By Amp. Feedback	<0.5mV* (to 40mV)	35 x 35	<1x10⁹ to ~3x10¹⁵
DI - Direct Injection		Injection Reset Integrator	Same as FEDI	80 at 10KHz	~2,500 Medium Noise	>20 at Higher Flux	<0.5μW	Tracks MOSFET & Det. I-V	10mV to 40mV	<20 x <20	1x10¹² to ~4x10¹⁵
FEDI - Feedback Enhanced DI		Injection Reset Integrator	CCD or Active Amp. Prior to Video Amp.	80 at 10KHz	5,000	>50	6μW - 30μW	Reduced By Open Loop Gain	<0.5mV* (to 40mV)	40 x 40	1x10¹¹ to ~3x10¹⁵
CM - Current Mirror		Gate Modulation Reset Integrator	CCD or Active Amp. Prior to Video Amp.	1,000 at 10KHz	~2,000 High Noise High Signal	>20	<0.5μW	Tracks MOSFET I-V	10 to 40mV	30 x 30	1x10¹³ to >5x10¹⁶
RL - Resistor Load		Gate Modulation Reset Integrator	CCD or Active Amp. Prior to Video Amp.	10,000 at 10KHz	~2,000 High Noise High Signal	>20	<0.5μW	Tracks Resistor I-V	10 to 40mV	30 x 30	1x10¹³ to >5x10¹⁶
RTIA - Resistor Feedback TIA		Current to Voltage Amplifier	Video Amplifier	60 - 150 at 1KHz	>10,000 Low Noise High Signal	>50	12μW - 500μW	Reduced By Amp. Feedback	<0.5mV* (to 40mV)	100 x 100	<1x10⁹ to >5x10¹⁶

* Lower Detector Bias Offset Achievable Utilizing Auto-Zeroing Type Amplifier
** Detector Capacitance in 0.3pf to 1pF Range

The detector bias of both the SI and SFD, although initially set at the beginning of a frame, changes as detector current integrates onto the input node. This detector debias results in signal output nonlinearity, since the signal characteristics of many detectors change as a function of bias. Neither the SI nor the SFD provides gain within the unit cell.

The capacitor feedback transimpedance amplifier (CTIA) solves the debias and gain limitations of the SFD and SI by incorporating the integration capacitor into the feedback loop of an inverting, high-gain differential amplifier, and thereby forcing charge to integrate into the feedback capacitor instead of the detector node capacitance. This results in a stable detector bias with a more linear signal transfer function. Because its gain is set by the feedback capacitor instead of the detector node stray capacitance, the CTIA can provide a high degree of signal amplification prior to multiplexing. The trade-off is that the CTIA requires significantly more area to implement than either the SI or the SFD.

Direct injection (DI) circuits provide a low-impedance detector interface, via the source of a MOSFET, that helps to keep the detector bias constant. Photon-induced charge integrates onto the capacitor at the drain of the MOSFET. The gain of the DI is set by the integration capacitor and, like the CTIA, gain can be quite high. The DI is limited to medium to high photon flux ranges. This is because the input impedance increases dramatically at low detector current levels, resulting in unstable detector bias, lower photon current integration, and reduced frequency response on the detector node. Also, since the input node of the DI is not reset at the end of each integration period, charge induced

in one frame of data can be integrated during the subsequent frame, resulting in reduced frequency response.

Feedback-enhanced DI (FEDI) incorporates an inverting amplifier between the detector node and the input MOSFET gate. This further reduces input impedance for applications at lower backgrounds. Like the SI, both the DI and FEDI provide charge domain output to the MUX; voltage mode output can be accomplished by adding a SFD to the output of the DI or FEDI.

Due to real estate constraints, it is not possible to accumulate all of the photon-induced charge at very high irradiance levels on a capacitor within the unit cell. Hence, the photon current must be scaled down before integration onto a reasonable size integration capacitor. For such applications, the current mirror (CM) preamplifier utilizes a load MOSFET, biased by the detector photon current, to induce or mirror a smaller current in the drain of a scaled down input MOSFET. The resistor load (RL) circuit provides a similar function by utilizing a resistor load in the detector to induce a lower current in the input MOSFET for accumulation onto the integration capacitor. Both CM and RL circuits suffer the same frequency response and detector bias stability issues as DI circuits.

The RTIA is similar to the CTIA but with the feedback capacitor and reset switch replaced by a resistor. The RTIA does not integrate detector current; rather, it provides a continuous output voltage that is proportional to the detector current. Since it is not reset after data are sampled, the RTIA has limitations in frequency response. It also requires high resistance feedback to provide gain comparable to the CTIA; large resistors require considerable unit cell area while tending to be high in $1/f$ noise or drift.

5.5.1 ROIC Preamplifier Signal-to-Noise Ratio

Sensitivity is normally the most important and challenging user-imposed requirement of a sensor design. Sensitivity can be expressed in terms of SNR or some other related parameter. The benchmark SCA performance parameters for SNR are typically functions of the sensor application, as given in Table 5.4. A common detector sensitivity parameter D^* is not a reasonable sensor flowdown, because high D^* can be achieved without fully addressing the system

Table 5.4 Useful Sensitivity Parameters Related to Sensor Applications

Parameter	Definition	Units	Common Application
NEdT	Noise equivalent temperature	K	Thermal imagers
NEI	Noise equivalent irradiance	ph/cm^2 s^{-1}	Radiometers and photon counters
NEP	Noise equivalent power	W	Imagers and radiometers
NEC	Noise equivalent charge (in a data frame)	e^-	Measure of ROIC, preamplifier, and CCD sensitivity Astronomy Visible imagers
D^*	Signal-to-noise normalized to photon energy, optical area, and system power bandwidth	A $\sqrt{\text{Hz}}$/W (Jones)	Comparison of detector technologies

SNR requirements. However, D^* is a valued tool for comparing one detector technology to another, since it is normalized to signal power, signal power bandwidth, and detector optical area.

Readout and SCA sensitivity are most often expressed in terms of any number of input referred noise quantities. Noise equivalent sensitivity parameters can be interpreted as the signal level that would result in a SNR of unity. The most universal measurement of readout sensitivity is noise equivalent charge (NEC); that is, the equivalent input referred noise electrons accumulated over a single frame or sample of data. NEC is specified with a given signal bandwidth or frame rate of interest. For a readout circuit that accumulates photon charge on an integration capacitor, NEC is the equivalent noise charge on the integration capacitor. The most commonly specified SCA level sensitivity parameter is noise equivalent irradiance (NEI), or the equivalent input irradiance for a SNR of unity; NEI holds the designer to a specific SNR at the sensor output. NEC can be referred to the input of the sensor, in terms of NEI through

$$\mathrm{NEI} = \frac{\mathrm{NEC}}{\eta A_{\mathrm{opt}} t_{\mathrm{int}}} \quad [\mathrm{ph/cm^2\ s^{-1}}] \ , \tag{5.12}$$

where η is the quantum efficiency of the detector, A_{opt} is the detector optical area, and t_{int} is the integration time over which photon charge accumulates.

5.5.2 System Sensitivity Flowdown

In general, the readout circuit is an integral part of the sensor design and should not be separated from the SCA or higher level assemblies. Therefore, sensor requirements must be partitioned into detector, readout, and other subcomponent parameters before design work can begin. Although subcomponents such as off-focal-plane amplifiers and digitizers require an allocation of the specification space, these parts are well understood and will be assumed to have negligible system impact in the following analyses.

An example flowdown of sensor sensitivity to the detector and readout begins by dividing the SCA level NEI into two equal noise contributors. This initial allocation is made after contributions from the photon flux Q_B are removed from the system NEI:

$$\mathrm{NEI_{SCA}} = (\mathrm{NEI_{sys}^2} - \mathrm{NEI_{ph}^2})^{1/2} = \left(\mathrm{NEI_{sys}^2} - \frac{Q_B}{\eta A_{\mathrm{opt}} t_{\mathrm{int}}}\right)^{1/2} [\mathrm{photons}] \tag{5.13}$$

for photovoltaic detectors. In this case, the sum of the readout contribution, NEI_{ro}, and the detector contribution, $\mathrm{NEI_{det}}$, yields the SCA total ($\mathrm{NEI_{SCA}}$). The initial detector and readout allocations are

$$\mathrm{NEI}_{ro} = \mathrm{NEI_{det}} = \frac{\mathrm{NEI_{SCA}}}{\sqrt{2}} \quad [\mathrm{photons}] \ , \tag{5.14}$$

which is an approximation, since it does not allocate NEI to other second-order noise contributors such as the multiplexer, video driver, off-focal-plane electronics, and the digitizer.

Detector NEI. The value of $\mathrm{NEI_{det}}$ is determined, to first order, from the noise contribution of a photovoltaic detector in reverse bias[6]:

$$i_{\mathrm{det}} = (2qI_{\mathrm{dark}}\Delta f)^{1/2} \quad [\text{amps rms}] \ , \tag{5.15}$$

where the detector noise current is assumed to be white thermal noise, q is the electron charge, Δf is the measurement bandwidth, and I_{dark} is the backbias dark current of the detector. The total (rms) detector noise is determined by integrating the noise and noise transfer function over all frequencies. For a photon integrating sensor, in which detector charge is accumulated and periodically read out before reset, the transfer function of the accumulator drops the noise power bandwidth and noise rolls off at a frequency of approximately

$$f \approx \frac{1}{2T_{\mathrm{frame}}} \quad [\mathrm{Hz}] \ , \tag{5.16}$$

where T_{frame}, the period between frames, is approximately equal to the integration time. (The shape of various transfer functions in a sampled system will be covered in a subsequent section.) Since the shot noise in Eq. (5.15) is white, i.e., flat over all frequencies, the noise power bandwidth of the accumulator can be substituted for Δf. The total number of noise electrons, or NEC, accumulated in a given integration time is

$$\mathrm{NEC_{det}} = \frac{i_{\mathrm{det}}t_{\mathrm{int}}}{q} \quad [\text{electrons}] \ . \tag{5.17}$$

To fit within the allocated NEI,

$$\mathrm{NEI_{det}} > \frac{\mathrm{NEC_{det}}}{\eta A_{\mathrm{opt}}t_{\mathrm{int}}} = \left(\frac{I_{\mathrm{dark}}/t_{\mathrm{int}}q\eta^2}{A_{\mathrm{opt}}}\right)^{1/2} \quad [\mathrm{ph/cm^2\ s^{-1}}] \ , \tag{5.18}$$

resulting in a maximum dark current of

$$I_{\mathrm{dark}} < \mathrm{NEI_{det}}^2\eta^2 qA_{\mathrm{opt}} \quad [\text{amps rms}] \ . \tag{5.19}$$

As a note, the NEI contribution from the photon-induced noise is calculated by replacing the dark current I_{dark} with photon current I_{ph} in the preceding equations.

For detector operation near zero bias, where dark current is negligible, the detector thermal noise can be expressed in terms of the small-signal detector resistance at zero bias, R_0, and the temperature of operation, T_{det}:

$$i_{\mathrm{det}} = \left(\frac{4kT_{\mathrm{det}}\Delta f}{R_0}\right)^{1/2} \quad [\mathrm{A}] \ , \tag{5.20}$$

where k is the Boltzmann constant. This yields a maximum detector noise contribution of

$$\mathrm{NEI_{det}} > \frac{(2kT/t_{\mathrm{int}}R_0)^{1/2}}{q\eta A_{\mathrm{opt}}} \quad [\mathrm{ph/cm^2\ s^{-1}}] \ , \tag{5.21}$$

and a minimum zero-bias resistance,

$$R_0 > \frac{2kT}{t_{\mathrm{int}}\mathrm{NEI}_{\mathrm{det}}^2 q^2 \eta^2 A_{\mathrm{opt}}^2} \quad [\Omega] \ . \tag{5.22}$$

Both of these expressions for detector thermal noise, Eqs. (5.19) and (5.22), are approximations that fit well in specific regions of detector operation. Equation (5.21) is most commonly used in infrared photovoltaics, because detector bias is usually minimized to reduce dark current and, therefore, detector $1/f$ noise (drift). Detector performance is often expressed in terms of R_0A_{opt}, or I_{dark}, and η due to their dependence on noise as expressed in Eqs. (5.18) and (5.21). If the selected detector technology shows significant margin in these parameters, more of the total noise budget can be allocated to the readout or other downstream noise sources.

Readout NEI. Readout noise, which is a function of the circuit configuration and layout details, is more difficult to analyze than detector noise. All readout circuits can be conceptualized in a format similar to that shown in Fig. 5.8, in which the readout noise sources are combined into an equivalent input referred noise voltage e_n and noise current i_n. Both parameters are usually dominated by the noise of the preamplifier input transistors and their sampled transfer function to the output. In determining the values of e_n and i_n, the folding, or aliasing, of high-frequency noise into the system bandwidth of interest must be considered.

Once the appropriate input noise contributions are determined, the readout amplifier noise current is handled in the same way as detector noise current in Eq. (5.17); however, the input referred noise voltage must be converted to an equivalent current prior to applying it to Eq. (5.17):

$$i_{en} = \frac{e_n}{r_{\mathrm{det}} \| r_{\mathrm{in}}} \quad [\mathrm{amps\ rms}] \ , \tag{5.23}$$

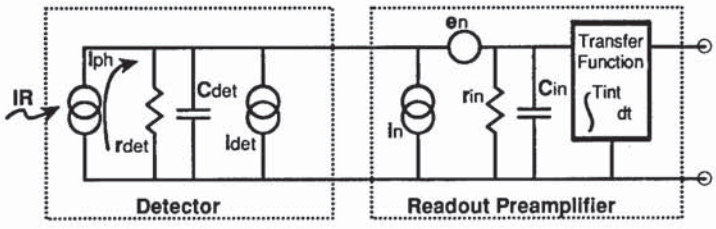


Fig. 5.8 Simple model of the sensor includes detector noise current and amplifier input referred noise voltage and current. Most preamplifiers can be conceptualized in this manner.

where $r_{\text{det}}\|r_{\text{in}}$ is the parallel combination of the small-signal detector and the amplifier input resistances. The NEC of the readout, with a fixed integration time of t_{int}, is

$$\text{NEC} = \left[i_n^2 + \left(\frac{e_n}{r_{\text{det}}\|r_{\text{in}}} \right)^2 \right]^{1/2} \frac{t_{\text{int}}}{q} \quad \text{[electrons]} \tag{5.24}$$

and is input referred to the detector as

$$\text{NEI}_{ro} > \frac{\text{NEC}}{\eta A_{\text{opt}} t_{\text{int}}} \quad \text{[photons]} \ . \tag{5.25}$$

Equations (5.24) and (5.25) can be utilized to determine the maximum noise contribution of the readout through Eq. (5.13). The results will guide the readout circuit type and design. Allocation of sensitivity should be made to detector drift, as well as to other less critical components not covered here, such as off-focal-plane electronics.

5.6 READOUT PREAMPLIFIERS

This section covers many of the most common readout preamplifier circuit families. Although the focus is on integrated circuit forms of the preamplifier, the RTIA is covered because it is utilized in sensors with few detector elements, it can be fabricated in ROIC format, and it provides an introduction to noise concepts necessary for subsequent preamplifier circuits.

5.6.1 Analysis of the Resistor Transimpedance Amplifier

The analysis tools discussed can be demonstrated and expanded by example for a common detector preamplifier circuit, the resistor transimpedance amplifier. The RTIA, usually employed in discrete rather than integrated circuit configurations, is useful in systems requiring only a few pixels (detector elements). The RTIA is also readily adaptable to ROIC format and may be combined with a sample/hold stage and multiplexers for application in sensors with larger numbers of elements. As with most photovoltaic readout amplifiers, the RTIA is a transimpedance or current-to-voltage amplifier. Unlike most preamplifiers, it does not accumulate, or integrate, signal charge over a given frame time; instead it presents a continuous output signal proportional to the input (photo) current. A schematic of a generic RTIA in a focal plane application, along with the predominant noise sources, is presented in Fig. 5.9.

The output response of the RTIA to a photon-generated current, or to any input current including noise, is

$$Z_t(f) = \frac{V_{\text{out}}}{I_{ph}} = \frac{R_{fb}}{[1 + (2\pi f R_{fb} C_{st})^2]^{1/2}} \quad \text{[V/A]} \ . \tag{5.26}$$

The in-band low-frequency transimpedance Z_t is set by R_{fb}, which is selected to provide sufficient gain to the system and to minimize its thermal noise contribution.

Noise contributed by the feedback resistor can be represented as a noise current across either the resistor or the input node by[6]:

$$i_{Rfb} \approx \left(\frac{4kT\Delta f}{R_{fb}}\right)^{1/2} \quad [\mathrm{A}] \ . \tag{5.27}$$

It is normally desirable to keep the feedback resistor noise below the detector thermal noise of Eq. (5.20); this results in a preliminary selection of R_{fb} as

$$R_{fb} > R_0 \frac{T_{Rfb}}{T_{\mathrm{det}}} \quad [\Omega] \ . \tag{5.28}$$

If the feedback resistor is on the focal plane and its temperature, T_{Rf}, is the same as that of the detector, T_{det}, then R_{fb} must be greater than the zero-bias resistance of the detector, R_0. If R_{fb} is too large, the very high amplifier transimpedance will result in saturation of the output signal.

If photon-induced noise is greater than detector thermal noise, then the feedback resistor is optimized to have lower noise than the photon-induced noise current i_{ph}:

$$i_{ph} = (2qI_{ph}\Delta f)^{1/2} \quad [\mathrm{A}] \ , \tag{5.29}$$

then

$$R_{fb} > \frac{2kT_{Rfb}}{I_{ph}} \quad [\Omega] \ . \tag{5.30}$$

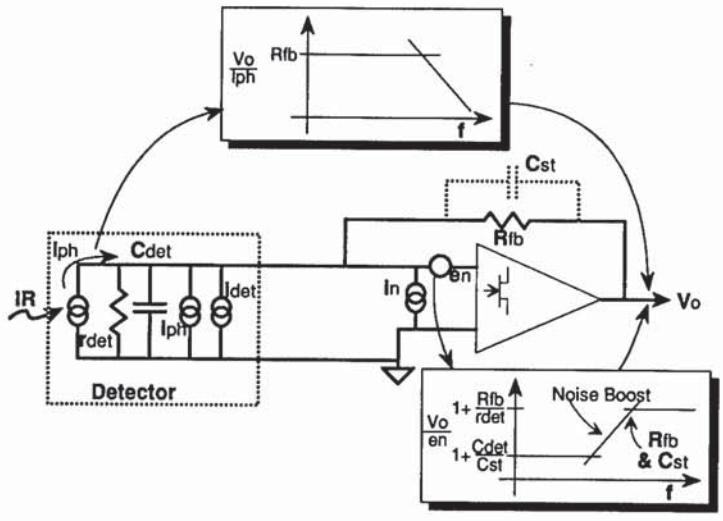


Fig. 5.9 The limits of the RTIA amplifier function are dominated by stray capacitance elements across the feedback resistor and on the input node.

Equations (5.29) and (5.30) can be used as guidelines for determining a reasonable transimpedance for the preamplifier. It may be desirable to have a higher R_{fb} than expressed above in order to further reduce its noise contribution and thus further limit its impact on the total noise, or to provide higher gain upfront and thus reduce the impact of downstream noise sources.

The feedback resistor must be selected with careful consideration to drift, or $1/f$ noise, which is common in high-ohmage resistors. In general, large surface area resistors exhibit low $1/f$ but, because of size, these are not easily integrated into cold focal plane configurations. Before committing to a final design, sample resistors should be measured both for $1/f$ and temperature stability, because any change in transimpedance with temperature can manifest as noise.

After selecting an appropriate transimpedance for the amplifier, the design should focus on selection of a low-noise-differential amplifier for RTIA implementation. Shot noise current of the amplifier, which is dependent on the input bias current of the input transistor, I_{in}, is governed by the same equation that predicts noise from photon current, and can be estimated at the input node as

$$i_n = (2qI_{in}\Delta f)^{1/2} \quad [\text{A}] \ . \tag{5.31}$$

Input bias current should be much less than the photon current, and in such cases shot noise is insignificant. For JFETs, this approximation can lose accuracy at very low frequencies where transistor $1/f$, or drift components, can dominate. Also, since input bias current is a strong function of temperature for JFETs, i_{in} can be negligible at cryogenic temperatures. Shot noise in MOSFETs is insignificant compared to the thermal noise of most detectors, provided no leaking p-n junctions or other stray current paths exist on the input node.

Transistor input referred noise voltage, e_n, does not have the same transfer function to the output as photon signal current in the RTIA. In the case of MOSFETs and JFETs, this noise is predominantly the channel thermal and $1/f$ noise described earlier in Eq. (5.10). The most straightforward way to analyze the impact of the input referred noise voltage is to refer to it as a noise current, by first determining its characteristics at the output node (through the amplifier) and then dividing by the circuit transimpedance. This allows all noise sources on the input node to be directly compared and summed as a single noise current. In Fig. 5.9, the transfer function of e_n to the output node is flat at low frequencies. At higher frequencies the stray capacitance on the input node "boosts" the voltage gain of the transfer function and noise gain increases. Eventually, the response goes flat again as parasitic or other capacitors across the feedback resistor become the dominant transimpedance element:

$$\frac{v_{\text{out}}}{e_n} = \left\{1 + \frac{R_{fb}}{R_{\text{det}}}\left[\frac{1 + (2\pi f C_{\text{det}} R_{\text{det}})^2}{1 + (2\pi f R_{fb} C_{fb})^2}\right]\right\}^{1/2} \quad [\text{V/V}] \ . \tag{5.32}$$

The input referred equivalent noise current caused by e_n of the RTIA is the ratio of Eq. (5.32) to Eq. (5.26):

$$i_{en}(f) = e_n\left(\frac{1}{R_{fb}} + \frac{1}{R_{\text{det}}}\right)\left[1 + (pfC_{\text{det}}R_{\text{det}})^2\right]^{1/2} \quad [\text{A}/\sqrt{\text{Hz}}] \ . \tag{5.33}$$

The total input referred noise current of the dominant RTIA noise sources is the sum of the photon, detector, feedback resistor, and transistor noises in the power domain:

$$i_{\text{total}} = (i_{ph}^2 + i_{\text{det}}^2 + i_n^2 + i_{en}^2)^{1/2} \quad [\text{A}/\sqrt{\text{Hz}}] \ . \tag{5.34}$$

The total noise should be compared to the system noise allocation discussed previously.

A detector and amplifier combination, such as the RTIA with a photovoltaic detector, are said to be "BLIP" (background limited performance) if the total noise is equal to the photon noise. The percent BLIP is calculated by dividing the photon noise by the total sensor noise, in this case Eq. (5.34),

$$\%\ \text{BLIP} = \frac{i_{ph}}{I_{\text{total}}} \times 100 \ . \tag{5.35}$$

The same BLIP can also be calculated via other sensitivity parameters such as D^*, SNR, and NEI.

5.6.2 Reset Integrators and Sampled Readout Circuits

The RTIA is commonly applied in a discrete component configuration in systems with few detector elements. However, the nature of most SCA applications is such that hundreds to thousands of detector elements must be amplified and multiplexed onto a few output lines in an integrated circuit configuration. In many cases, simple integrated circuit capacitors and switches act as the gain setting element in place of the resistor utilized in the RTIA. To design for and analyze the sensor sensitivity requires additional steps beyond those discussed in the previous section. A common problem encountered in switched circuit analysis is the aliasing of high-frequency signals or noise into the bandpass of the sampled signal, thereby producing a false signal or increasing noise beyond normal expectations.

An example of this aliasing effect can be seen in the spoked cartwheels of Western movies. The wheels appear to be moving slowly, stopped, or even reversed although the wagon is obviously moving forward at a high rate of speed. The cartwheel spokes are sampled by the film at a rate of 30 Hz. If the wheel passes a reference point in the camera's field of view at a rate of 29 spokes per second, the wheel will appear to be moving in reverse at about 1 spoke per second; this is because each subsequent spoke is imaged in a position slightly behind that of the preceding spoke in the previous frame. If the spokes are moving at exactly 30 or 60 per second, the camera will image subsequent spokes in the same position on each frame of film, giving the appearance of no spoke, or wheel, movement at all. These same effects are seen in sampled sensor systems, where undesirable high-frequency noise, signal, or interference appears at frequencies below half the scene sample rate, the so-called Nyquist rate or limit.

Sensors can be divided into two general classes of input preamplifier types: (1) those, such as the previously described RTIAs, that amplify or create a continuous output voltage representing the photon generated signal, and (2) those

that additionally accumulate and average (or integrate) the photon signal over a specified frame time. This second type of sensor is commonly referred to as a *reset integrator*. The resulting signal from either type of circuit can be multiplexed with other elements. In the analysis that follows, the reset integrators are assumed to integrate during the entire frame time except for a very short reset period.

5.6.3 Self-Integrating Readout

Integrating preamplifiers are most commonly used in ROIC designs where the charge accumulation element is a capacitor or a CCD. The capacitor accumulates photon-induced current over an integration period, resulting in a signal that can be multiplexed to the sensor output. Figure 5.10 shows one of the most basic integrating preamplifier unit cell designs, the self-integrator. The SI has advantages over all other designs in that it is composed of a single unit cell readout component, a small MOSFET switch, and thus requires minimum unit cell area. The drawback is that the SI does not provide signal gain in the unit cell and is thus subject to multiplexer and column amplifier noise.

Photon charge in the SI integrates onto the stray capacitance in the unit cell, which is formed primarily by the detector but also includes strays from the interconnect and the MOSFET switch. If necessary, additional capacitance can be added to the readout to increase storage capacity. After charge is integrated for an entire frame, the multiplexer is cycled and the stored charge is transferred onto the low-input impedance transimpedance column amplifier of gain Z. A reset switch on the multiplexer bus normally restores the detector to its pre-integration voltage bias after the amplifier drives the signal out of the multiplexer. However, the action of the transimpedance amplifier may be sufficient to perform the detector reset without the addition of a separate reset switch on the bus. The transfer function of the circuit from photon current to output of the column transimpedance amplifier, over the integration period t_{int}, is

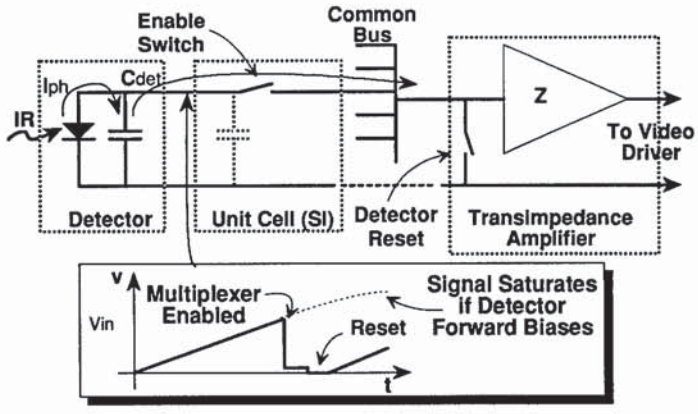


Fig. 5.10 The self-integrator accumulates photon charge on stray capacitance on the input node but provides no gain in the unit cell.

$$V_{\text{out}} = Z\int_0^{t_{\text{int}}} I_{ph}(t)\,dt + ZQ_r \quad [\text{V}] \,, \tag{5.36}$$

where Q_r is the initial charge stored on the input node and Z is the charge-to-voltage gain.

As the SI integrates photon and dark current onto the detector node capacitance, the voltage bias of the detector forms a ramp, as illustrated in Fig. 5.10. If allowed to integrate too long, however, the detector will become forward biased, resulting in response nonlinearity and additional detector shot noise, as photon-induced charge is shunted across the detector. The ramp on the detector node will follow the current to voltage (I-V) characteristics of the detector. For a photovoltaic detector, the voltage on the input node will follow the characteristics of a diode, which exhibits high nonlinearity as its voltage transitions from reverse to forward bias. The dynamic range of the SI is thus limited to the flat back bias signal excursion of the detector.

***kTC* Noise.** Thermal noise (commonly referred to as kTC noise) is stored on the detector node capacitance at the moment the switch or multiplexer of the SI is disabled (opened). This results in small variations in detector voltage or input node charge (ΔQ_r) from one reset time to the next, which in turn results in variation or noise at the end of integration according to Eq. (5.36). This variation in reset voltage is true for any switched capacitor. The thermal noise characteristics of the circuit, when the switch is closed, are the same as in any resistor-capacitor circuit with a resistance R_{on}:

$$e_R = (4kTR_{\text{on}}\Delta f)^{1/2} \quad [\text{V}] \,. \tag{5.37}$$

The rms noise on the capacitor can be calculated by integrating the thermal noise of the resistor over all frequencies through the transfer function of the RC circuit:

$$v_c^2 = 4kTR_{\text{on}}\int_0^{\alpha} \frac{1}{1 + (2\pi fCR_{\text{on}})^2}\,df \quad [\text{V}^2] \,, \tag{5.38}$$

which can be rewritten as

$$v_c = \left[4kTR_{\text{on}}\frac{\pi}{2}f(-3\text{ dB})\right]^{1/2} = \left(\frac{KT}{C}\right)^{1/2} \quad [\text{volts rms}] \,. \tag{5.39}$$

Notice that the noise produced by resetting a capacitor through a switch is not dependent on the resistance of the switch. In Eq. (5.39), the noise equivalent bandwidth [Δf, of Eq. (5.37)] is the product of $\pi/2$ and the -3-dB bandwidth of the circuit, which is true for all white noise sources acted on by a single pole filter. The noise voltage in Eq. (5.39) can also be expressed in terms of noise charge stored on the capacitor by multiplying by the node capacitance:

$$q_c = (kTC)^{1/2} \quad [\text{C}] \,. \tag{5.40}$$

Since kTC noise charge goes up with increased capacitance, it is normal practice to minimize these strays on the input node of the SI. In the case where photon noise dominates, Eqs. (5.29) and (5.40) can be combined to determine the maximum permissible stray capacitance on the input node

$$C\ (\max) \ll \frac{i_{ph} t_{\text{int}}^2}{kT} \quad [\text{F}] \ . \tag{5.41}$$

Unless special care is taken in the selection of capacitor size, kTC noise can be a dominant noise source in sampled integrated circuit applications. Minimizing this capacitance places special requirements on the detector capacitance; since the detector is normally the dominant contributor to input node capacitance, kTC noise must be considered in all switched capacitor circuits.

Integrated Noise Transfer Function. Individual contributions of all noise sources can be determined by applying the appropriate switched noise transfer function to each source. Noise current on the input node of any integrating amplifier, including the SI, is the simplest to analyze because it has the same transfer function as the signal current I_{ph}. For this example, the integrated current of the SI forms a voltage on the input node and is reset (transferred) at the end of the integration time, thus possessing the characteristics of the reset integrator. The change in voltage at the end of integration represents, for the SI, the total charge shifted out at the end of integration.

A reset integrator can be modeled as illustrated in Fig. 5.11. The voltage on the input node, shown as a continuous ramp, is the integral of the detector current $x(t)$. The resulting output voltage $y(t)$ can be expressed in terms of the convolution of the input current and the impulse response $h(t)$:

$$y(t) = x(t) * h(t) \quad [\text{V}] \ . \tag{5.42}$$

The impulse response of the reset integrator $h(t)$ over the integration period t_{int} is

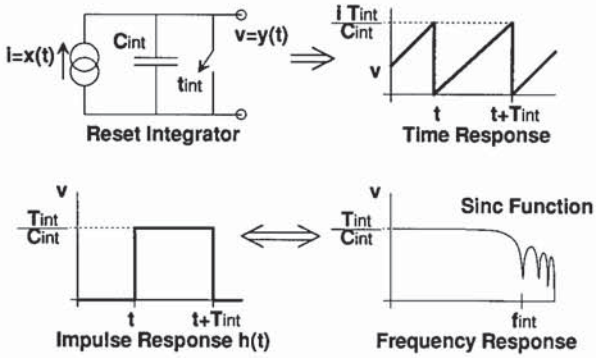


Fig. 5.11 The reset integrator action can be modeled as a continuous integrator that is sampled and subtracted as discrete time increments.

$$h(t) = 1/C_{\text{int}} \int_{t-}^{t-+t_{\text{int}}} \delta(x)\, dx \quad [\text{V}] \ , \tag{5.43}$$

which is simply a step to an amplitude of $1/C_{\text{int}}$ at time equal zero, and returns to zero (is reset) after t_{int}. The integral of the delta function is often referred to as a *window function,* because it applies only to a single integration time, and is zero before integration starts $(t-)$ and after the end of integration.

The frequency response of the reset integrator can be determined by evaluating the Laplace transform:

$$Y(f) = X(f)H(f) \quad [\text{V}] \ , \tag{5.44}$$

where the Laplace transform of $h(t)$ of Eq. (5.43) is

$$H(f) = \frac{t_{\text{int}}}{C_{\text{int}}} \frac{\sin(\omega t_{\text{int}}/2)}{\omega t_{\text{int}}/2} \quad [\text{V/A}] \ , \tag{5.45}$$

where

$$\omega = 2\pi f \quad [\text{rad/s}] \tag{5.46}$$

$$H(f) = \frac{t_{\text{int}}}{C_{\text{int}}} \frac{\sin(\pi f t_{\text{int}})}{\pi f t_{\text{int}}} = \frac{t_{\text{int}}}{C_{\text{int}}} \frac{\sin(x)}{x} \quad [\text{V/A}] \ . \tag{5.47}$$

The sine expression of the form $\sin(x)/x$ in Eq. (5.47) is commonly referred to as the *sinc function.* This derivation of Eq. (5.47) is strictly valid for an ideal reset integrator that is reset instantaneously in time. In practice, however, some dead time exists between the reset and the onset of integration (due to switching time). Equation (5.47) provides a good approximation in cases where the dead time is a small fraction of the integration time.

Signals that are integrated over time and then reset have the sinc transfer function shown in Fig. 5.12, and are in fact attenuated at frequencies higher than the Nyquist limit. Figure 5.13 shows the result of integrating a slowly changing (dc) photon signal with a high-frequency sine wave riding on it; the high-frequency ac component could be either signal, noise, or interference picked up on the input node. A large net accumulation of signal charge results in this case, through the integration of the dc signal over the entire integration time. The ac noise is also accumulated but tends to cancel out its own excursions above and below the dc signal, thus resulting in a significant reduction in amplitude. Since the integration time is assumed to be nearly equal to the time between frames, the only unaliased frequencies that can pass through the reset integrator are those less than half the frame rate. All other residual energy above the Nyquist frequency is attenuated and "folded" down between Nyquist and zero, thus resulting in higher noise than would otherwise be expected in the passband.

In addition to *kTC* noise, other noise sources of the SI include detector thermal noise and photon noise, as discussed previously. Also, the column amplifier is usually the major active noise source in most SI designs, although

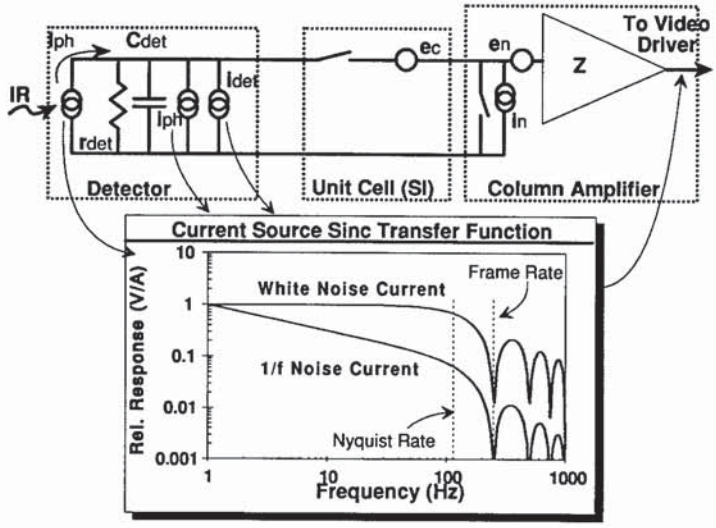


Fig. 5.12 Simple integrator of the SI provides basis of a sample noise model. Integrated current signal and noise sources have a sinc transfer function.

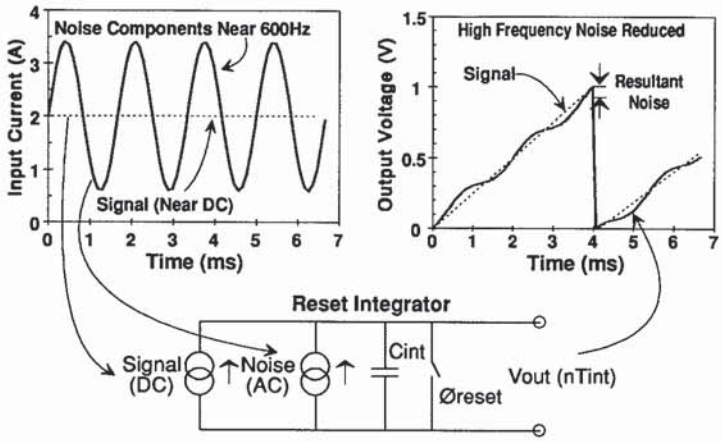


Fig. 5.13 Noise above the Nyquist frequency is attenuated in integrating amplifiers, reducing any aliasing effects in the passband.

it is outside the unit cell. The noise contribution of the column amplifier is dependent on its type, which can be any one of several unit cell amplifiers discussed later in this section.

5.6.4 Source Follower per Detector Readout

The source follower per detector readout preamplifier (SFD), shown in Fig. 5.14, is similar to the SI but with the addition of a MOSFET for voltage mode output and a reset switch. Only three components, other than the detector,

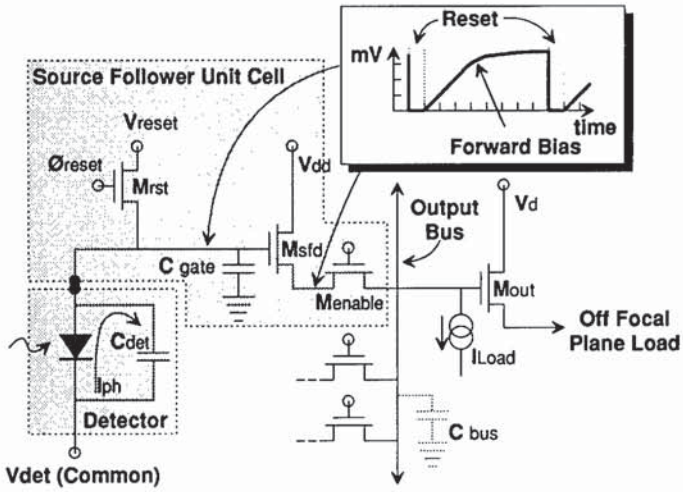


Fig. 5.14 SFD buffers the voltage resulting from photon charge integration to the video output driver via a source-follower MOSFET configuration. The SFD requires a reset switch on the input node.

are contained in the unit cell; this makes the SFD desirable for applications that require small unit cells.

Photon current is integrated onto the input node stray input capacitance formed by the gate of the source-follower MOSFET, the interconnect, and the detector capacitance. Unlike the SI, the ramping input voltage of the SFD is buffered by the source-follower MOSFET and then multiplexed, via an enable switch, to a common bus prior to the video output buffer. The SFD, which has a voltage mode output, requires no bus amplifier. After the multiplexer read cycle, the input node is reset and the integration cycle begins again. The dynamic range of the SFD is limited in the same way as that of the SI, by the current voltage characteristics of the detector. Charge on the input node creates a voltage at the end of integration according to

$$V_{\text{in}} = \frac{I_{\text{det}} t_{\text{int}}}{C} \quad [\text{V}] \ , \tag{5.48}$$

where I_{det} is the sum of photon and dark currents and C is the stray capacitance on the readout input node. The total excursion of input voltage should not exceed the detector forward bias, or severe signal nonlinearities and additional shot noise can occur. In photovoltaic sensors, this limit can be as low as tens of millivolts or as high as several volts. Additional charge storage can be accommodated by adding an integrated circuit capacitor to the input node.

The buffer MOSFET of the SFD is designed both for low noise and near unity gain. This gain, between the detector node and multiplexer, approaches unity as the MOSFET g_m and load resistance R_l are increased:

$$A_{sf} = \frac{1}{1 + (1/g_m R_l)} \quad [\text{V/V}] \ , \tag{5.49}$$

where R_l is the combined load resistance presented by the multiplexer, current source load, and video driver input circuits.

MOSFET drain current in the source follower is not driven by noise; rather, it is driven by g_m requirements and the signal bandwidth of the multiplexer. The current source load for the SFD is located opposite the multiplexer, outside the unit cell, so that power only dissipates in the unit cell MOSFET when it is enabled through the multiplexer onto the video buffer line. The source-follower load current must be large enough to drive, or slew, the capacitance of the multiplexer bus. This is covered in detail for the source-follower video driver in Sec. 5.9.

SFD Noise. The SFD is typically utilized in low background applications, such as astronomy,[10] where long integration times accumulate sufficient charge for readout. Gain is fixed by the near-unity gain of the MOSFET source follower and the integration capacitor, which is usually dominated by the detector. In high-sensitivity applications, the detector capacitance must be reduced to very low levels and thus provide high input node gain so that amplifier and multiplexer noise is overcome. Again the *kTC* noise caused through the reset of the input node must be considered. The major noise sources of the SFD are *kTC*, MOSFET 1/*f*, and MOSFET channel thermal noise.

It is important to address 1/*f* in the input MOSFET because this can often dominate the channel thermal noise to frequencies well above 10 kHz. MOSFET 1/*f* noise, as discussed in an earlier section, decreases as the product of the channel width and length (W and L) increases. The product of W and L also drive gate capacitance and, in Fig. 5.15, the relative total 1/*f* noise is shown as a function of the MOSFET gate-to-detector capacitance ratio. When gate capacitance is much lower than detector capacitance, the photon-to-voltage gain is high but the 1/*f* noise is also high. When gate capacitance is much larger than detector capacitance, the gain of the SFD is substantially reduced according to Eq. (5.48) and SNR is once again reduced. Optimum gate capacitance occurs at the point where it is equal to the detector capacitance. In practice, the detector capacitance is often sufficiently large such that the MOS-

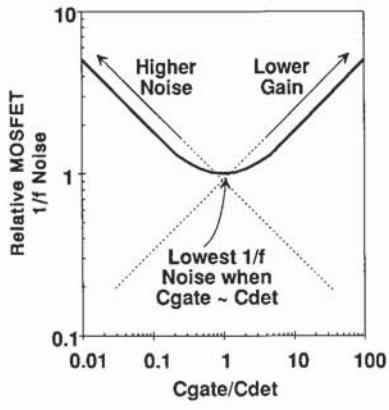


Fig. 5.15 Minimum MOSFET 1/*f* noise contribution occurs when gate capacitance is equal to detector capacitance.

FET size, and therefore gate capacitance, cannot be fully optimized due to area limitations in the unit cell.

MOSFET noise at the output of the SFD is the product of MOSFET input referred noise voltage (whether $1/f$ or channel thermal noise), source-follower gain (~ 1), and square root of the equivalent noise bandwidth of the noise, Δf. Periodic sampling through the multiplexer results in the folding of high-frequency noise below the Nyquist frequency of the circuit. In the case of channel thermal noise, the equivalent noise bandwidth, Δf of Eq. (5.10), is the only parameter to optimize for lowering noise.

The following discussion addresses the MOSFET channel thermal contribution to source-follower noise. MOSFET $1/f$ noise, to first order, is geometry and process dependent and not directly dependent on drain current or g_m. To reduce MOSFET channel thermal noise, the designer's degree of freedom is limited to reducing the noise bandwidth Δf since increasing g_m of the MOSFET does not have the obvious effect on noise that Eq. (5.10) implies. An increase in g_m, as a result of increased drain current, W/L ratio, or other means, results in a corresponding increase in the bandwidth Δf, thus canceling any low-noise benefit.

Noise Equivalent Bandwidth. Noise in the SFD can be controlled by reducing the noise equivalent bandwidth Δf of the circuit. The concept of noise equivalent bandwidth was mentioned previously in the analysis of capacitor kTC noise; here, noise equivalent bandwidth will be explained for the specific case of a single pole RC filter applied to white noise, as in Fig. 5.16. The output of the SFD can be conceptualized as such a circuit where the drive resistance R is $1/g_m$ of the MOSFET, and the load capacitance C is formed by strays on the multiplexer bus.

Noise equivalent bandwidth is a tool utilized to simplify circuit noise analysis, so the integral of noise sources and their transfer function need not be

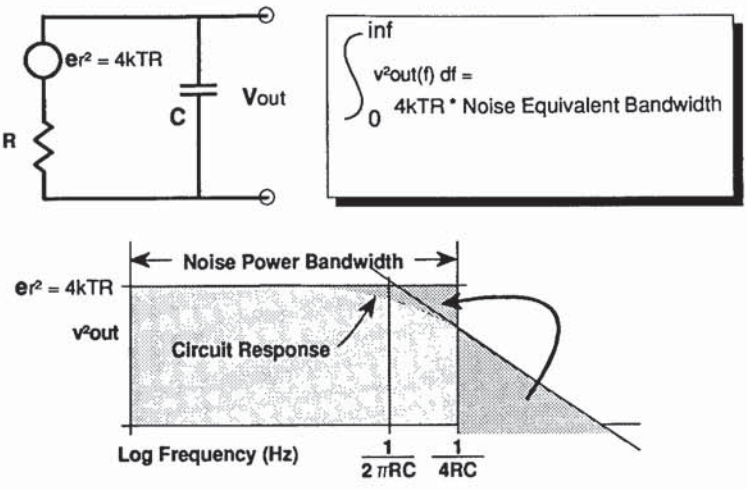


Fig. 5.16 Noise equivalent or power bandwidth is a brick wall approximation utilized in the estimation of total rms noise of a circuit.

evaluated to an infinite frequency. The white thermal noise voltage of the resistor circuit in Fig. 5.16 can be written

$$e_n^2 = 4kTR\int_0^{\alpha} A_v(f)\,df = 4kTR\int_{f_{\text{low}}}^{f_{\text{high}}} df \quad [\text{V}^2]\ , \tag{5.50}$$

where f_{high} and f_{low}, the equivalent noise bandwidth, are selected to provide the equivalence of the two integrals. In this expression, $A_v(f)$ is the transfer function of the single pole circuit comprised of a resistor and a capacitor. The integral of Eq. (5.50), over frequencies from zero to infinity through the filter, yields

$$e_n^2 = 4kTR\Delta f = \frac{4kTR}{4RC} = 4kTR\frac{\pi}{2}f(-3\text{ dB}) \quad [\text{V}^2]\ , \tag{5.51}$$

where $1/(4RC)$ is the equivalent noise or power bandwidth Δf. The term f_{high} of Eq. (5.50) is equal to the noise bandwidth if f_{low} is assumed to be at or near 0 Hz. The Δf of white noise acted on by a single pole filter is the product of $(\pi/2)$ and the half power response, or pole $f(-3\text{ dB})$:

$$e_n\ (\text{rms}) = e_n\ (\text{white})\left[\frac{\pi}{2}f(-3\text{ dB})\right]^{1/2} \quad [\text{V}^2]\ . \tag{5.52}$$

The equivalent noise bandwidth of a source can be dominated by a downstream single pole filter, such as the output impedance and load capacitance of the video amplifier, in which case, that pole would substitute into Eq. (5.52). If a system is ac coupled, and is consequently rejecting low-frequency noise and signal, Δf for a white noise source must be replaced by

$$\Delta f = f_{\text{high}} - f_{\text{low}} \quad [\text{Hz}]\ , \tag{5.53}$$

where f_{low} and f_{high} are the equivalent power bandwidth roll-on and roll-off frequencies, respectively. The result of Eq. (5.53) will be less accurate as f_{low} approaches f_{high}.

Also shown in Fig. 5.16 is the noise power spectral density as a function of frequency and the "brick wall" filter equivalent, or equivalent noise bandwidth, for the circuit. It should be noted again that Fig. 5.16 shows the derivation of power bandwidth for the common case of an RC circuit to a white-noise source. The equivalent noise bandwidth of noise sources other than white, such as $1/f$, applied to transfer functions different from the RC example can also be calculated.

In Eq. (5.53), f_{low} is a function of the data processing method and the implementation of ac coupling (if, in fact, ac coupling is implemented). For example, frame-to-frame differencing reduces or eliminates stationary or slowly changing elements of a scene. In data so processed, only high-frequency noise and scene changes are observed. Low-frequency noise and $1/f$ noise are sharply attenuated, and f_{low} in this case increases toward the Nyquist frequency. Systems that incorporate periodic scene recalibration will have a roll-on f_{low} on the order of half the recalibration frequency; all systems have a lower limit

on the bandwidth. Integration of $1/f$ noise from zero frequency has severe mathematical consequences, and it is important to determine the roll-on frequency of a focal plane system (or processing system). However, in most cases, the roll-on for white noise can be assumed to be zero with insignificant error in the analysis.

SFD Noise Equivalent Bandwidth. For the SFD, the bandwidth of the source follower during multiplexer read is

$$f(-3\text{ dB}) = \frac{g_m}{2\pi C_{\text{mux}}} \quad [\text{Hz}] \ , \tag{5.54}$$

where C_{mux} is the bus capacitance of the multiplexer plus other strays. The noise bandwidth of this single pole circuit is $\pi/2$ times the bandwidth of Eq. (5.54):

$$\Delta f = \frac{g_m}{4C_{\text{mux}}} \quad [\text{Hz}] \ . \tag{5.55}$$

Substituting Eq. (5.55) into (5.10) yields a total input referred channel noise contribution of

$$e_n = \left(\frac{2}{3}\frac{kT}{C_{\text{mux}}}\right)^{1/2} \quad [\text{V}] \ , \tag{5.56}$$

where g_m drops out, leaving C_{mux}, to first order, as the only noise-limiting parameter under the control of the designer.

Increasing the g_m of the source follower unfortunately does not change the thermal noise of the circuit, as expected in Eq. (5.56). If C_{mux} is too large, however, g_m must be increased to sustain a bandwidth large enough to pass the detector signal through the multiplexer. The SFD in this configuration has a MOSFET thermal noise contribution with a form similar to kTC noise in Eq. (5.39).

5.6.5 Capacitor Feedback Transimpedance Amplifier

This class of amplifier addresses a broad range of detector interface and performance requirements across many applications. The CTIA provides a highly stable detector bias, high photon current injection efficiency, high gain, and low noise, and has overall performance equal to and often better than most RTIA configurations. Further, the CTIA is readily integrated into silicon and has the high-frequency response and high modulation transfer function (MTF) advantages of most other reset integrators.

The CTIA, or reset Miller integrator, is shown in Fig. 5.17. Photon charge causes a slight change in voltage on the inverting input node of a differential amplifier. The amplifier, with open-loop gain in the hundreds to tens of thousands, responds with a sharp reduction in output voltage. This change in output is coupled back to the input node through the feedback capacitor, causing photon-induced charge to flow onto the feedback capacitor and oppose the initial

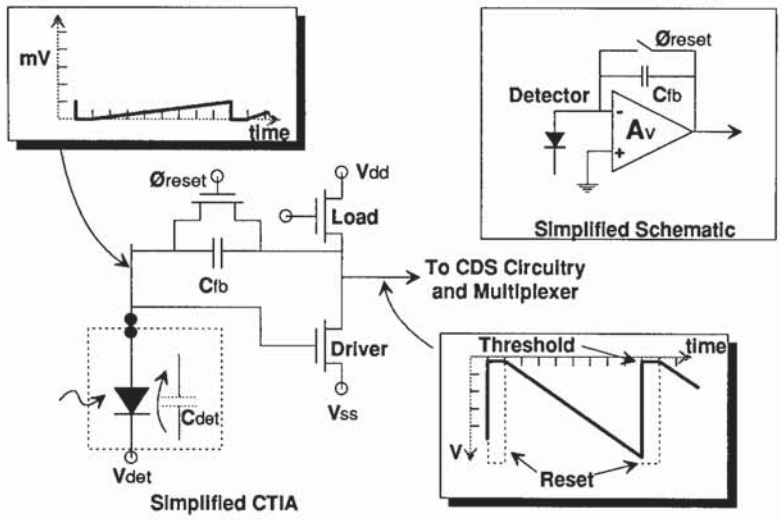


Fig. 5.17 The CTIA utilizes a high-gain inverting amplifier coupled via a feedback capacitor to achieve a high-gain linear dynamic range.

effects of charge on the input node. As detector current accumulates over the frame time, this results in a ramp at the output. At the end of integration, the output voltage is sampled and multiplexed to the output video drivers, and the switch across the feedback capacitor is cycled closed to achieve reset. Signal processing such as correlated double sampling (CDS) is often employed on the output of the CTIA, within the unit cell, primarily to reduce drift, but also to rereference the output signal to a more convenient voltage range. CDS is discussed in a later section of this chapter.

The CTIA gain, assuming a large open-loop amplifier gain, is

$$V_{\text{out}} = \frac{I_{ph} t_{\text{int}}}{C_{fb}} \quad [\text{V}] \ , \tag{5.57}$$

where C_{fb} is the feedback capacitor. This can be compared to gain of the RTIA, in which transimpedance is equal to the feedback resistor, while the CTIA transimpedance is often expressed over a single frame of data as

$$Z_t = \frac{V_{\text{out}}}{I_{ph}} = \frac{t_{\text{int}}}{C_{fb}} \quad [\text{V/A}] \ . \tag{5.58}$$

Given a feedback capacitor of 50 fF (5×10^{15} F) and a 100-Hz frame rate, this translates into an equivalent transimpedance of about 2×10^{11} Ω. This can be done in the CTIA without the careful resistor selection required by the RTIA, because transimpedance is achieved through the switched capacitor network in the amplifier feedback loop instead of a resistor.

The CTIA signal action can be modeled using the equivalent Miller capacitance on the input node, as shown in Fig. 5.18. The feedback capacitor, coupled with the high open-loop gain of the amplifier, results in an equivalent capac-

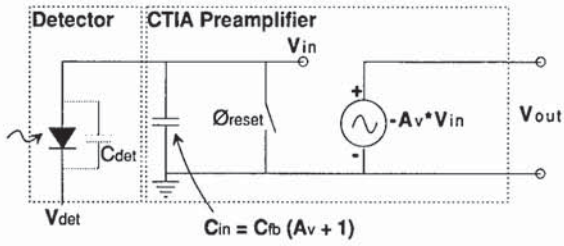


Fig. 5.18 The CTIA acts as a very large integration capacitor on the input node followed by a high-gain voltage amplifier.

itance on the input node that is orders of magnitude larger than the feedback capacitor itself. The excursion in detector bias, ΔV_{in}, can be determined from this model as

$$\Delta V_{\text{in}} = \frac{I_{\text{det}} T_{\text{int}}}{C_{fb}(1 + A_v)} \quad [\text{V}] \ , \tag{5.59}$$

thus providing a stable bias, and therefore a highly linear amplifier, for most reasonable open-loop gains A_v. The output voltage is

$$V_{\text{out}} = \frac{A_v I_{\text{det}} t_{\text{int}}}{C_{fb}(1 + A_v)} \quad [\text{V}] \ , \tag{5.60}$$

which reduces to Eq. (5.58) for the normal case of $A_v \gg 1$.

Like all reset integrators, the detector noise sources are integrated and follow the same sinc function described in Eq. (5.47) [after making appropriate substitution for Z_t, as described by Eq. (5.58)]. The CTIA does have major noise contributions from the input transistor(s) of the differential amplifier that would tend to cause undesirable drift and offset. Most CTIA implementations utilize on-chip CDS within the unit cell to reduce low-frequency noise ($1/f$) and drift, and eliminate the kTC noise caused by reset of the feedback capacitor. Also, a sample/hold circuit is often used to store the end of integration signal value from the CDS circuit. This stored value is then sequentially multiplexed to the video driver during integration of the next frame of data.

The output noise of the CTIA from the input MOSFETs is a function of the CDS circuit (if employed), the noise gain, and the noise bandwidth Δf. The voltage gain of the MOSFET white and $1/f$ noise sources is a function of the detector impedance, as shown in Fig. 5.19:

$$\frac{v_{\text{out}}}{e_n} \approx \frac{C_{fb} + C_{\text{det}}}{C_{fb}} \quad [\text{V/V}] \ , \tag{5.61}$$

which assumes detector node capacitance dominates detector impedance over the noise bandwidth of interest. The equivalent noise bandwidth Δf is a function of circuit implementation and generally determined through small-signal analysis of the specific implementation. Noise contributions from other MOSFETs

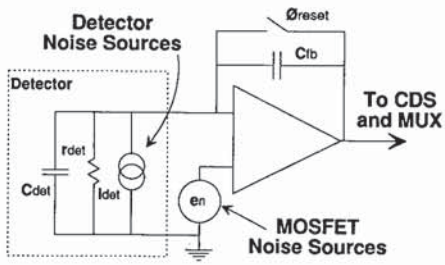


Fig. 5.19 The CTIA noise model must consider gain caused by detector capacitance and resistance. Detector capacitance must be minimized.

within the CTIA are normally negligible to the input MOSFET; however, they can be input referred as a noise voltage e_n.

5.6.6 Injection Circuits

A form of reset integrator, injection circuits perform integration through the channel of an active transistor or CCD channel. Usually the detector node is not directly reset; rather, charge accumulated on the integration capacitor (or CCD bucket), on the output of the injection transistor, is periodically reset or transferred. Since the detector is not directly reset, residual photon-induced charge from one frame time can be integrated into the next frame time causing frame-to-frame crosstalk. Figure 5.20 shows two of the more popular injection circuit configurations.

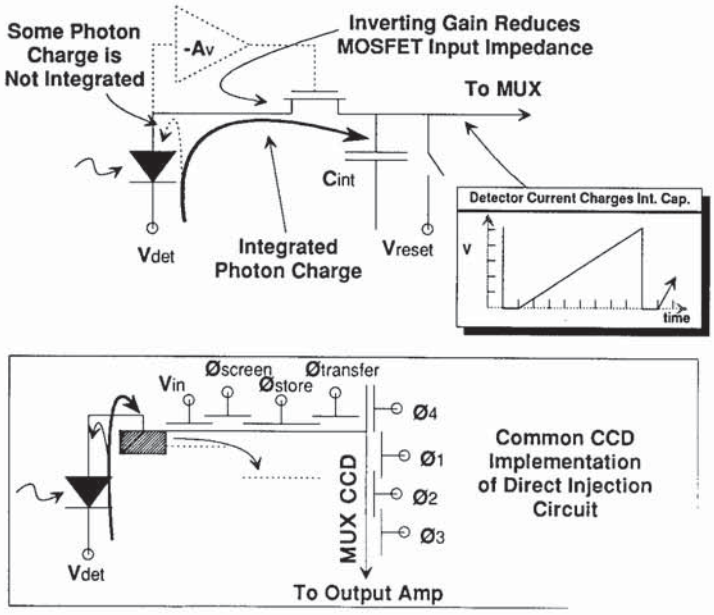


Fig. 5.20 The direct injection circuit is used in both CCD and conventional multiplexer designs. The FEDI is a DI with the addition of an inventor.

Direct Injection. The DI circuit of Fig. 5.20 has been used as an input to CCDs for many years. This readout configuration requires minimal area in the unit cell for implementation; it is perhaps second only to the SI in compactness. Its applications include medium to high proton irradiance conditions that provide sufficient photon current to maintain high MOSFET transimpedance g_m, therefore providing a low impedance and stable bias for the detector.

Photon current in DI circuits is injected, via the source of the input transistor, onto an integration capacitor that has been reset prior to the beginning of the frame. As the photon current integrates, it charges the capacitor throughout the frame; a multiplexer then reads out the final value and the capacitor is reset. In lieu of a multiplexer, a CCD can be utilized to pump the charge out of the unit cell. Unlike the SFD and SI, the gain of the DI, and the CTIA discussed earlier, is set by the integration capacitor, which can be quite small and is not dependent on the detector capacitance. The integration capacitor can be buffered by a source follower to provide voltage mode output. In the case of CCD implementation, the accumulated photon charge is clocked down the CCD to a sense gate, or floating diffusion, whose capacitance sets the gain.

Drain, or channel currents, in the DI are typically very low because they result from photon interaction with the detector. In many injection applications, the MOSFET operates in weak inversion, also known as the subthreshold region, in which drain current is exponentially related to the gate-to-source voltage, as described earlier.

To reduce detector noise, it is important that a uniform, near-zero-voltage bias be maintained across all the detectors. This is especially true for long-wavelength detectors, which can have significant dark current in reverse bias. Detector bias is not directly set on the DI circuits; instead, it is set through the node on the common side of the detector, and includes the MOSFET gate voltage plus the individual threshold voltage of each MOSFET. MOSFET threshold variations across a focal plane can result in bias variations (nonuniformities) of 10 to 50 mV or more between detector elements. Because of this broad range of detector biases, the detector common must be adjusted such that all detectors are biased away from the higher noise forward-bias region of the detector; however, this will cause some elements to receive tens of millivolts reverse bias and can result in higher detector $1/f$ noise and fixed pattern noise in the form of nonuniform detector dark currents.

The input to the readout should also provide a low impedance to the detector. This provides a stable detector bias and a high photon current injection efficiency. If the input impedance of the DI is too high, a fraction of the photon current will be shunted across the detector and not injected into the MOSFET, resulting in a loss of SNR. This injection efficiency, or ratio of integrated photon current I_{int} to photon current, is

$$\text{Injection efficiency} = \frac{I_{\text{int}}}{I_{ph}} = \frac{r_{\text{det}} g_m}{1 + r_{\text{det}} g_m} \quad [\text{A/A}] \ , \tag{5.62}$$

where r_{det} is the resistance of the detector and g_m is the inverse of the input impedance looking into the source of the MOSFET.

The term g_m is a strong function of drain current for MOSFETs in the weak inversion (or subthreshold) region, where most DI circuits operate. The rela-

tionship between drain current and gate-to-source voltage for a MOSFET in weak inversion was given by Swansen and Meindl[11] and can be written

$$I_d = \frac{W}{L}\mu_n K_1 \exp\left(V_g - \frac{mkT}{q}\right) \quad [\text{A}] \tag{5.63}$$

for an n-channel MOSFET, where K_1 includes geometry and operational characteristics of the MOSFET. For a transistor in subthreshold, the g_m is given by the first derivative of Eq. (5.63) with respect to drain current and gate-to-source voltage:

$$g_m = \frac{\delta I_d}{\delta V_{gs}} = \frac{I_d q}{mkT} \quad [\text{mhos}] \ . \tag{5.64}$$

Note that g_m in subthreshold is independent of the device geometry parameters. Because high g_m is a direct function of drain current (i.e., photon current), there are limitations in the background flux capability of the DI; at very low photon currents, g_m becomes very poor and the injection efficiency falls.

Low g_m not only affects the injection efficiency of the DI but also reduces the bandwidth of the detector element, thereby impacting frame-to-frame crosstalk and MTF. If g_m is the dominant impedance on the detector node, a condition required for high injection efficiency, the frequency response of the detector node becomes

$$f(-3\text{ dB}) = \frac{g_m}{\pi(C_{\text{det}} + C_{gs})} \quad [\text{Hz}] \ , \tag{5.65}$$

where C_{gs} is the MOSFET gate-to-source capacitance. Since g_m is directly proportional to the photon current, DI use is limited in high-speed low-photon-flux applications.

Noise in the DI includes the same detector, MOSFET, and kTC noise sources discussed earlier for other preamplifiers. MOSFET noise e_n can be output referred as a current i_o to the integration capacitor. Since i_o is integrated, it is acted on by the sinc function of the reset integrator discussed earlier. The transfer function of the input MOSFET noise sources to output current is

$$i_o \approx \frac{e_n g_m}{1 + r_{\text{det}} g_m} = \text{injection efficiency} \frac{e_n}{r_{\text{det}}} \quad [\text{A}/\sqrt{\text{Hz}}] \ . \tag{5.66}$$

Note that MOSFET noise is negligible for cases where r_{det} is high. The transfer function for all detector noise sources (thermal, $1/f$, and photon-induced) is the sinc function discussed for the SI; however, the DI detector noise is acted on by the charge injection efficiency and the input node bandwidth discussed above.

Feedback-Enhanced Direct Injection. Feedback-enhanced direct injection circuits (FEDI) address some shortfalls of the DI by introducing a feed-forward inverting amplifier off the detector node, as shown in Fig. 5.20. The inverting

amplifier, with gain of A_v, reduces the input impedance of the DI and therefore increases the injection efficiency and bandwidth. The effect is to reduce the minimum operating photon flux range of the FEDI by approximately an order of magnitude below that of the DI. All previously given equations for the DI can be utilized to estimate performance for the FEDI, with the substitutions of g'_m and C'_{gs} for g_m and C_{gs}, where

$$g'_m = g_m(1 + A_v) \quad [\text{A/V}] \ , \tag{5.67}$$

$$C'_{gs} = C_{gs}(1 + A_v) \quad [\text{F}] \ . \tag{5.68}$$

The detector bias uniformity across the array is dependent on the threshold variation of the inverting amplifier for the FEDI. Threshold nonuniformities from the inverting amplifier can be addressed through the use of auto-zeroing circuits, which utilize feedback during the zeroing period to reset the amplifier input. These zeroing circuits also reduce drift components of the amplifier.

The output referred MOSFET preamplifier noise for the FEDI is

$$i_o \sim \frac{e'_n g'_m A_v}{(1 + A_v)(1 + r_{\text{det}} g'_m)} \approx \text{injection efficiency} \, \frac{e'_n}{r_{\text{det}}} \quad [\text{A}/\sqrt{\text{Hz}}] \ , \tag{5.69}$$

where the dominant preamplifier noise is the input referred noise of the inverting amplifier e'_n. The noise contribution of the injection transistor of the DI, e_n, is negligible, because it is reduced by approximately A_v. Detector noise sources are treated in the same manner as they are for the DI.

5.6.7 Gate Modulation Circuits

Gate modulation circuits utilize photon current to modulate the gate voltage and thereby induce an output current in the MOSFET. The transistor output drain current accumulates onto an integration capacitor or a CCD bucket. Because of this gate modulation action, the detector bias is required to change, or debias, as scene-induced current changes. Thus, detectors utilized in gate modulation circuits must be operated in reverse bias where $1/f$ noise and dark current nonuniformity can be a problem. A reset switch may be incorporated onto the detector node to reduce crosstalk from one frame to the next, resulting in a higher MTF—in this special case of gate modulation circuits—than in their injection circuit counterparts. The gate modulation circuits discussed in this section are most commonly employed in high to very high background applications.

Resistor Gate Modulation. The resistor load gate modulation circuit (RL) is shown in Fig. 5.21. Detector bias is a function of detector (photon) current, load resistance R_l, and resistor bias V_d:

$$V_{\text{in}} = (I_{ph} + I_{\text{dark}})R_l + V_d \quad [\text{V}] \ . \tag{5.70}$$

The load resistor is designed for low $1/f$ noise,[12] high temperature stability, and for uniformity from cell to cell. Polysilicon resistors in integrated circuit form are commonly utilized as the load. The MOSFETs in gate modulation

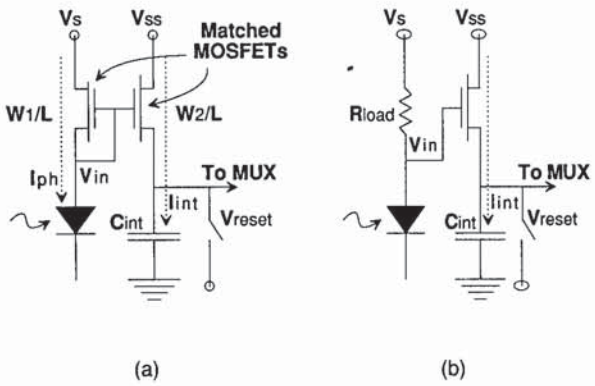


Fig. 5.21 The gate modulation circuit biases the detector through a high-impedance resistor or current mirror MOSFET: (a) current mirror input and (b) resistor load input.

circuits are normally run in weak inversion. Therefore, the resulting integrated drain current can be determined by applying Eq. (5.70) to the weak inversion (subthreshold) MOSFET of Eq. (5.63):

$$I_{\text{int}} = I_d = K_2 \exp(V_{\text{in}}) \quad [\text{A}] \ , \tag{5.71}$$

where K_2 is dependent on resistor bias, MOSFET threshold voltage, temperature, and other factors.

In high background applications, where the signal of interest is small compared to optics and scene background irradiance, the resistor gate modulation circuit provides a design that can reject much of these background components. When the background alone is present on the detector, the bias on the detector or the load resistor can be adjusted for negligible drain current or integration of charge. As signal is applied, the MOSFET drain current increases exponentially with photon current and thereby allows some level of background flux rejection.

The output uniformity from one element to another is dependent on variations in MOSFET threshold voltage, load resistance, and detector resistance. Because of these nonuniformities, a substantial amount of fixed pattern noise is characteristically presented at the output of the SCA.

Current Mirror Gate Modulation. In the current mirror gate modulation amplifier (CM), the resistor of the RL circuit is replaced with a MOSFET, as shown in Fig. 5.21. In CM operation, photon current flowing into the drain of the first of two closely matched transistors induces a common gate-to-source voltage change in both transistors; this results in a similar, or mirrored, current in the second transistor. If the source voltages, V_s and V_{ss}, of two matched MOSFETs are connected, both will have the same gate-to-source voltages, which will induce a current in the output MOSFET identical to the detector current flowing through the input MOSFET. In this specific case, the integration current is a linear function of the detector current (unlike the nonlinear case of the RL). This CM action can also be used to scale up or down the integration current in the second transistor by varying the transistor geometries according to

$$I_{\text{int}} = I_{\text{det}} \frac{W_2/L_2}{W_1/L_1} \quad [\text{A}] \ , \tag{5.72}$$

where W and L are the width and length dimensions of the two MOSFETs. The CM is frequently used in applications of very high background, where there is insufficient area in the unit cell to accumulate the detector current over an entire frame period; in this case, the width of the second transistor can be scaled down to a fraction of that of the load transistor, thereby scaling integrated current to a fraction of detector current. The current gain can also be set through the bias voltages V_s and V_{ss}:

$$I_{\text{int}} = I_{\text{det}} \frac{W_2/L_2}{W_1/L_1} \exp(V_s - V_{ss}) \quad [\text{A}] \ . \tag{5.73}$$

This analysis has assumed 100% injection efficiency of detector current into the input load MOSFET. Injection efficiency is a function of detector resistance and MOSFET g_m, which is dependent on detector current (photon current), and is calculated using the same equations as for the DI discussed earlier.

Nonuniformity from element to element can be quite large in CM designs. This is because the threshold voltages of the current mirror MOSFET pair are not identical and also because injection efficiency can vary due to detector resistance variations, factors that result in the high fixed pattern noise commonly observed in these designs. CM advantages over the RL include greater linearity and absence of a load resistor. The frequency response is calculated using the DI circuit equations discussed in the preceding subsection, unless the detector is reset each frame, in which case the frequency response follows the sinc function of reset integrators.

5.7 SIGNAL PROCESSING

Incorporation of signal processing on an ROIC is often desirable in order to reduce off-focal-plane electronics, reduce the data rate, or perform processing prior to sampling and multiplexing. The two areas where on-chip signal processing can occur are (1) within the unit cell itself and (2) in the multiplexer prior to the output video amplifier. The most common forms of ROIC signal processing are band-limiting (provided by all reset integrator preamplifiers), sample and hold, correlated double sampling, and time-delay integration. Other less common examples, not covered here, include gain and offset correction, signal digitization,[13] single event gamma circumvention (correction of corrupt signal), and frame-to-frame differencing to remove clutter and background offsets.

5.7.1 Sample and Hold

Simultaneous integration of all elements of the sensor is often required. The signal for simultaneous integration is accumulated over a given time period in a snapshot mode. To reset the detector and preamplifier to begin integration of the next frame, the signal from the previous frame must be sampled and stored temporally for sequential readout by the multiplexer. The most common form of this type of sample and hold is composed of a MOSFET sampling switch,

a hold capacitor, and a unity gain buffer amplifier. Figure 5.22 shows such an implementation on the output of a SFD preamplifier. A simple output MOSFET source follower and load serves as buffer amplifer prior to multiplexing. The sample and hold circuit resides in the unit cell, and therefore puts limitations on minimum cell size because ample area is required for the three transistors and capacitor.

The key design objectives of the sample and hold circuit are settling time and noise. Settling time is governed by the time required to charge or discharge the hold capacitor; it is also a function of the drive capability of the preamplifier or buffer circuit in front of the sampling switch. The output buffer must be able to drive or slew the multiplexer bus capacitance; the output current required for this is calculated in the same way as for the output source-follower video drivers, covered in a later section of this chapter.

Noise of the sample and hold circuit is governed by the kTC noise of the hold capacitor v_c, which must be significantly less than the output referred noise of the preamplifier, v_{out} (preamp). A kTC noise equal to $1/5 v_{\text{out}}$ (preamp) will result in less than a 2% increase in noise:

$$v_c = \frac{kT}{C_{sh}} \leqslant \frac{v_{\text{out}}\ (\text{preamp})}{5} \quad [\text{volts rms}] \tag{5.74}$$

for a minimum sample hold capacitance C_{sh} of

$$C_{sh} \geqslant \frac{25kT}{v_{\text{out}}^2\ (\text{preamp})} \quad [\text{F}]\ . \tag{5.75}$$

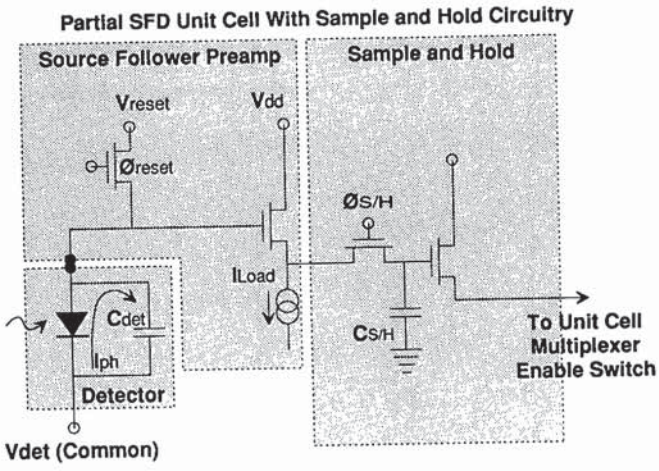


Fig. 5.22 The sample and hold function provides frame store in the unit cell. In the voltage domain configuration shown, the SFD is followed by a MOSFET switch and hold capacitor. The output is buffered with a MOSFET source follower.

5.7.2 Correlated Double Sampling

Drift and $1/f$ noise are often dominant noise contributors in readout preamplifiers. Therefore, it is often desirable to recalibrate, or rezero, the amplifier chain periodically in order to achieve lower noise and greater absolute accuracy. This is normally accomplished in reset integrators by rezeroing the output of the preamplifier at the beginning of integration.

Figure 5.23 shows a preamplifier, in this example the SFD, with a clamp circuit on the output. The output signal is initially sampled across the clamp capacitor during the onset of photon integration (after the detector is reset). The action of the clamp switch and capacitor subtracts any initial voltage from the output waveform. Because the initial sample is made before significant photon charge integrates onto the capacitor, the final integrated photon signal swing is unaltered; however, any offset voltage or drift present at the beginning of integration is removed, or subtracted, from the final value. This process of sampling each pixel twice, once at the beginning of the frame and again at the end, and providing the difference is called correlated double sampling (CDS). This process can be performed within the unit cell as shown in the figure, or it can be performed numerically off the focal plane in a digital processor.

CDS reduces or eliminates low-frequency noise but at the expense of increased noise at higher frequencies, as shown in Fig. 5.24. The value of the initial CDS sample represents dc offsets, low-frequency drift, and high-frequency noise; this initial value is subtracted from the final value, which also includes dc offset, low-frequency drift, and high-frequency noise. Since the two samples occur within a short period of time, the dc and drift components of each sample do not change significantly; hence, these terms cancel in the subtraction process. On the other hand, high-frequency waveforms (noise) change significantly between the two samples and bear little resemblance or correlation to each

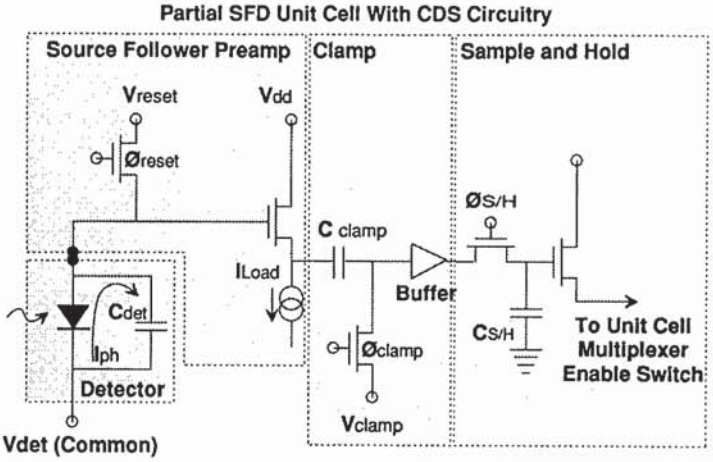


Fig. 5.23 Correlated double sample achieved in the unit cell with the addition of clamp and sample hold circuitry.

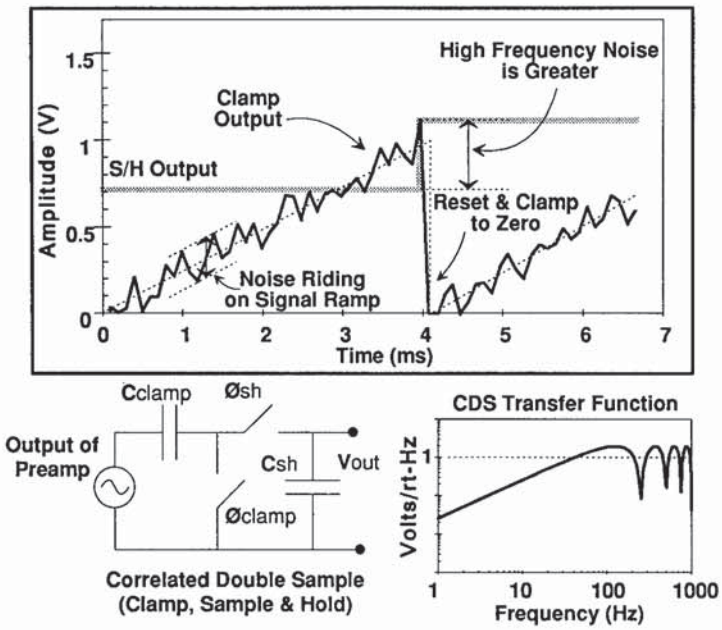


Fig. 5.24 CDS removes dc offsets and drift, but increases high-frequency noise.

other. The net effect is that these two uncorrelated high-frequency components sum to twice the noise power.

The sample transfer function of a noise source acted on by CDS processing can be calculated in the same manner as that for the reset integrator. The only difference is that the presampling input to the CDS, from the amplifier noise sources, is acted on by the band-limited gain of the amplifier, A_v, instead of an integrator,

$$V_{\text{out}}(t) = y(t) = A_v h(t) = A_v[\delta(t) - \delta(t - t_{int})] \text{ [V]} . \tag{5.76}$$

Then, using the Laplace transform,

$$V_{\text{out}}(\omega) = Y(\omega) = A_v H(\omega) = A_v[1 + \exp(-j\omega t_{\text{int}})] \text{ [V]} , \tag{5.77}$$

which results in

$$v_{\text{out}}(\text{f}) = A_v[2 - 2\cos(2\pi f t_{\text{int}})]^{1/2} \text{ [V/}\sqrt{\text{Hz}}\text{]} , \tag{5.78}$$

where it is assumed samples occur at the beginning and end of the frame. The sample function of Eq. (5.78) changes somewhat if significant time lapses between the end of one frame and the beginning of the next frame. The integral of Eq. (5.78) over all frequencies can be approximated for white noise by

$$v_{\text{out}}\,(\text{CDS}) = e_n A_v (2\Delta f)^{1/2} \text{ [volts rms]} , \tag{5.79}$$

provided the equivalent noise bandwidth of the noise source, Δf, is many times greater than the frame rate.

Noise in the CDS circuitry is dominated by kTC and buffer noise, as it was for the sample and hold case of the previous section. To minimize clamp capacitor kTC noise, C_{clamp} is scaled in the same manner as the hold capacitor. Additionally, C_{clamp} must be large enough to overcome any strays on its output side in order to maintain near unity gain. Stray capacitance, which includes the MOSFET switch and the gate of the output buffer MOSFET, together with the clamp capacitor, reduces the signal gain of the clamp, A_{clamp}:

$$A_{\text{clamp}} = \frac{C_{\text{clamp}}}{C_{\text{stray}} + C_{\text{clamp}}} \quad [\text{V/V}] \ . \tag{5.80}$$

It is desirable to have a clamp gain of at least 0.95 resulting in

$$C_{\text{clamp}} \geq 20\, C_{\text{stray}} \quad [\text{F}] \ , \tag{5.81}$$

although higher capacitance may be required to reduce kTC noise.

5.7.3 Time-Delay Integration

A simple scanning SCA includes a single row of detector elements that scan a scene and multiplex the resulting signal to the output. To generate an entire scene, the array is scanned from one side of the field of view to the other. Sensitivity is limited in a sensor of this type by the dwell time, or equivalent time that an element is "looking" at a specific point in the scene. To reduce flicker and provide reasonable scene refresh rates, this scene is typically scanned 30 to 100 times per second. The dwell time of a given element will tend to reduce if a short scan time, high scene resolution, or large field of view is required. Placing a second row of detectors next to the first row produces a second image of the scene that is displaced in time. The two images can be added (integrated), after the first is scene delayed, to double the signal level with only a modest increase in noise of the two frames. By adding rows of time-delay elements and performing the time-delay integration (TDI), the SNR of a scanning system can be improved by

$$\text{SNR improvement} = \sqrt{n} \ , \tag{5.82}$$

assuming the system is detector limited, where n is the number of elements or rows in TDI.

The TDI function can be performed off focal plane (normally after digitization) or on the ROIC. On-chip TDI requires temporary frame storage for each TDI row, and a multiplexer to transport the signal for the summing process. TDI can be performed via a large array of storage capacitors, however, it is most commonly implemented utilizing a CCD. The CCD transports the signal charge from one element to the next for accumulation with the next detector in TDI, as in Fig. 5.25. The transport time between cells provides the delay necessary for synchronization to the signal from the next detector. The CCD accumulates all TDI elements before the signal is buffered off the ROIC

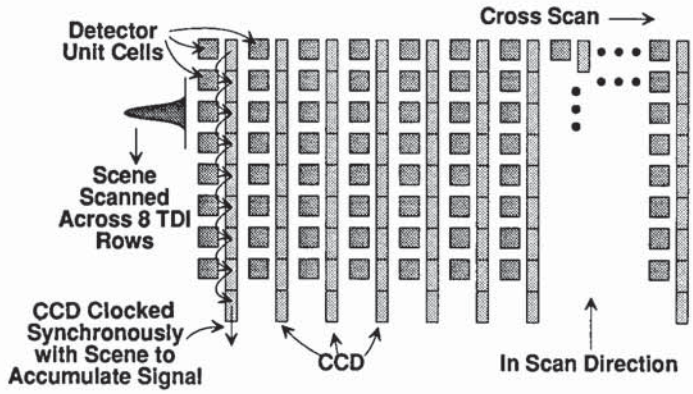


Fig. 5.25 TDI can be performed by utilizing a CCD, which provides delay between TDI detector before summing.

via the video amplifier. The CCD in this example provides both TDI and the multiplexer functions. More details on CCD operation are provided in the following section.

5.8 DATA MULTIPLEXERS

The multiplexer (MUX), in its simplest form, is a series of switches or transfer wells that sequentially transports sampled data from many pixel elements and encodes them onto a common bus. Signals from tens to hundreds of thousands of detector elements can be multiplexed through a video driver to a single output pad on the readout. Two common forms of multiplexers are available to the readout designer: (1) CCDs, which utilize a series of sequentially enabled potential wells, or metal insulator semiconductor (MIS) capacitors, to transfer charge to a floating gate or diffusion; or (2) a set of switches that is enabled sequentially to a common bus as shown in Fig. 5.26. Staring arrays utilize two multiplexers, one for the column and one for the row MUX. The column multiplexer shifts data at low speed from each unit cell to the end of the column; the data are then further multiplexed, at high speed, with other elements of the same row from subsequent columns. The output is thus formatted with pixel one of the first row through the last pixel in the first row followed by the data from pixel one in the second row through the last pixel in the second row, and so on. If multiple outputs are utilized, data can be formatted to address quadrants or interlaced columns of the ROIC unit cells.

5.8.1 CCD Multiplexers

The invention of the CCD in 1970 launched the optical industry, including infrared, into the area of high-density multielement solid-state focal planes. Evolution of most modern hybrid focal planes can be traced back to the introduction of CCD technology. Several detailed sources of information on the subject are available that provide a more in-depth review of CCD physics and

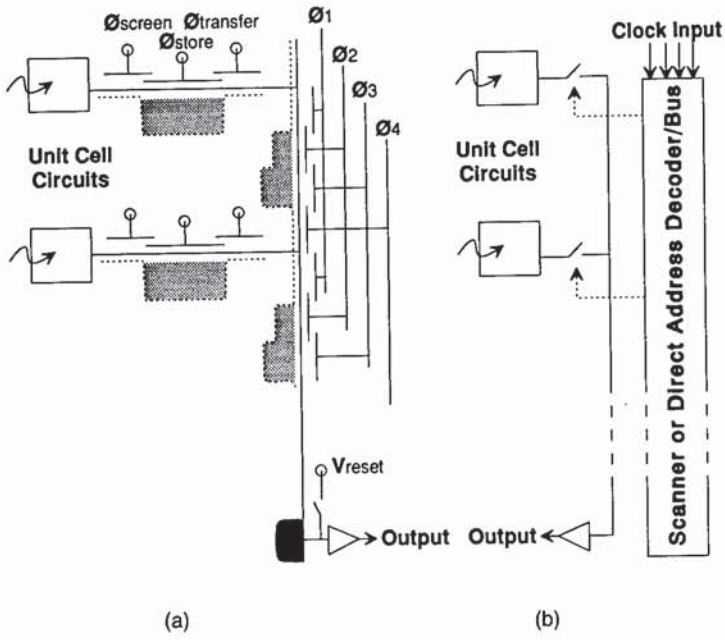


Fig. 5.26 Multiplexers include CCD and MOSFET enable switches: (a) CCD multiplexer and (b) direct readout multiplexer.

their wide range of applications and capabilities.[14–16] The following is a brief description of the CCD in ROIC applications.

The CCD basically provides charge storage and transfer along the surface of a semiconductor. Charge is manipulated through the attraction of carriers to a field set up between a gate and the substrate of the semiconductor. In MOSFETs, the application of a voltage, above a specific threshold, results in a channel formation under the gate between the source and drain diffusions, as discussed in the earlier MOSFET primer. In the absence of source/drain diffusion to attract carriers for channel formation, the area under the gate assumes a potential capable of storing localized minority carrier charge. The storage potential under the gate is referred to as a "bucket," and removal of the gate voltage results in the loss of charge storage capability in a manner analogous to a bucket being emptied. Charge is injected into a CCD through an adjacent diffusion or gate structure.

The action of the CCD is shown in the three-phase CCD multiplexer of Fig. 5.26(a). Charge, in this case minority carrier electrons in the *p*-type semiconductor, tends to flow toward the highest surface potential. In this case the surface potential is provided (and manipulated) by a positive gate bias on $\emptyset_1$. Charge is actually stored in a thin layer near the semiconductor surface, but is commonly depicted schematically as a bucket in the figure. The potential (voltage) on $\emptyset_2$ can be increased to attract charge from under the first gate. The voltage on $\emptyset_1$ is reduced to zero, thus forcing charge near the semiconductor surface to flow under $\emptyset_2$. This action can be repeated with $\emptyset_2$ and $\emptyset_3$ resulting in charge transfer to the right in the figure. Notice that additional charge "packets" in the CCD channel also flow in a similar manner. The CCD must

be capable of providing isolation between these signal charge packets as shown in Fig. 5.26. A two-phase CCD can be constructed as in Fig. 5.27(b). In this case, alternate gates are built on different thicknesses of gate oxide, thereby inducing a potential gradient across the surface under the two connected gates and providing charge transport from one gate to the next.

The CCD can perform both the detector and ROIC functions. Photon current can be accumulated directly into the CCD bucket or in an adjacent diode (detector). This monolithic approach is common in visible sensors, and has been demonstrated in the infrared.[1,17]

The charge is actually stored in a thin layer at the surface of the semiconductor in a MIS capacitor. The effective voltage applied to the MIS capacitor is

$$V_a = V_g - V_{FB} \quad [\text{V}] \ , \tag{5.83}$$

where V_{FB} is the voltage generated by the work function between the metal and semiconductor, and the fixed charge in the insulator.[4] The maximum storage capacity of a MIS capacitor is

$$N_{\max} = V_a \frac{C_{\text{gate}}}{q} = V_a \frac{qA_c\varepsilon_o\varepsilon_c}{T_{ox}q} \quad [\text{electrons}] \ , \tag{5.84}$$

where V_a is limited by the gate/oxide breakdown voltage.

As charge is transferred down a CCD the packet can gain charge through uncontrolled lateral dark currents, can lose charge, or can gain a random charge element (noise) through fluctuations resulting from surface state interactions or dark current noise. Charge lost through incomplete transfer can result in low signal at the output, or can result in crosstalk because the lost charge can appear in subsequent charge packets. Charge transfer efficiency

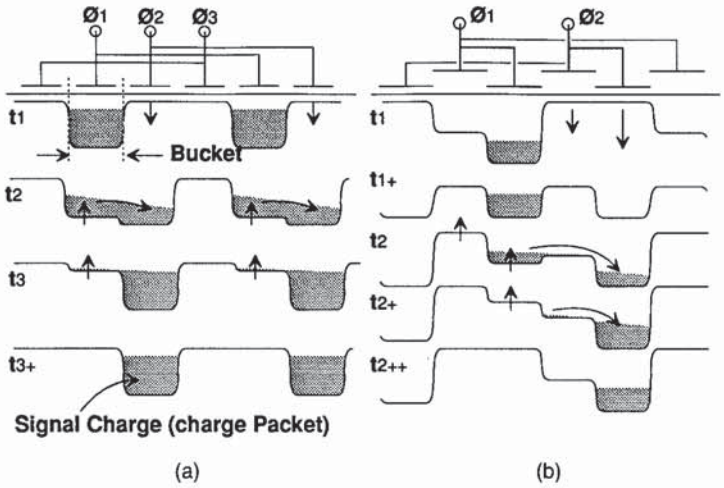


Fig. 5.27 Charge is transferred along a CCD as the surface potential is sequentially changed: (a) three-phase CCD and (b) two-phase CCD.

η_x, the ratio of charge transferred into the next CCD cell to the original charge prior to transfer, is related through

$$\eta_x + \varepsilon_x = 1 \ , \tag{5.85}$$

where ε_x is the transfer loss factor or charge transfer inefficiency; ε_x is related to the transfer time, because slower CCD clock rates allow for greater time for charge to transfer from one bucket to the next. Charge transfer efficiency for a good CCD is greater than 0.9999 per transfer. At low frequencies, <1 MHz, the major contributor to transfer inefficiency is interface-state trapping, whereby charge is trapped and subsequently released. This effect can be minimized through the injection of a constant current (dc) input to the CCD, or a "fat-zero" charge that fills most of these surface states. At high frequencies the charge transfer efficiency is limited by self-induced drift or repulsion of the carriers, by thermal diffusion, and by drift as a result of fringe fields such as those presented by adjacent gates and diffusions in the CCD.

Noise in the CCD manifests itself as fluctuations in the number of carriers in a charge packet. The major noise mechanisms in the CCD are related to those in MOSFETs and detectors:

1. as with $1/f$ noise in MOSFETs, fluctuations in surface state interaction with charge
2. analogous to channel thermal noise in the MOSFET, variation caused by thermally generated carriers in the semiconductor
3. noise generated through the absorption of photons (photon noise).

The input circuit to a CCD includes the charge domain preamplifier circuits discussed earlier: SI, DI, FEDI, RL, or CM. Voltage mode preamplifiers can be converted to charge mode by inserting a capacitor in series with the output. The output charge from the CCD can be transferred to a source-follower gate through a diffusion at the end of the CCD. The source-follower gate must be reset before the next signal is transferred. Additional input and output circuits are utilized for the CCD and are covered in Refs. 1 and 17.

5.8.2 Direct Address and Scanning Multiplexers

Direct address and scanning multiplexers became popular when CMOS technology was introduced into readout designs. Prior to this, NMOS or PMOS integrated circuits were commonly used and MOSFET multiplexer switches and their drivers, although not uncommon, were more difficult to implement. The MOSFET switch-type multiplexers are also simpler to interface to voltage mode preamplifier circuits, such as the CTIA and SFD, than CCDs, which operate in the charge domain.

The direct address and scanning multiplexers are shown in Fig. 5.28. In the direct address multiplexer, a digital code provides a unique address to each unit cell that is to be enabled onto the bus. This type of multiplexer requires several input address lines, but allows for random access to any element on the focal plane.

The scanner multiplexer utilizes a flip-flop-type scanner to pass sequentially an enable signal down a row or column of unit cell multiplexer switches. A simplified implementation, shown in Fig. 5.28, requires one line to reset, $\emptyset_r$,

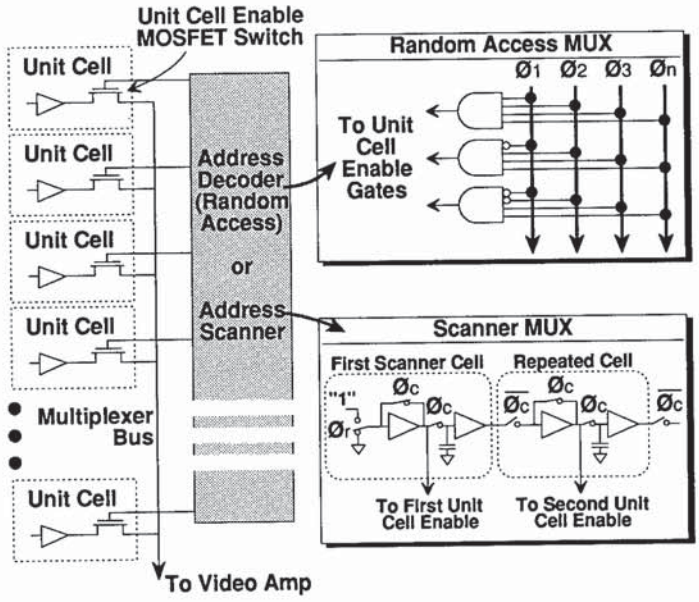


Fig. 5.28 Direct address and scanning multiplexers use MOSFET switches to enable detector-derived signals onto a common bus.

and another, $\emptyset_c$, to clock the scanner; $\emptyset_r$ resets the first scanner cell to a logical "1" at the beginning of the multiplexing sequence, $\emptyset_c$ and its inverse subsequently clock the logical "1" down the scanner, thus providing sequential unit cell enable.

The scanner multiplexer is easily integrated into readouts and can be utilized to generate other timing waveforms such as unit cell reset and sample/hold clocks. The on-focal-plane scanner has reduced the required number of input/output lines on large focal planes to fewer than 10.

The multiplexer itself does not produce noise, because the enable transistors are hard "on" or completely "off"; however, the kTC of the bus and noise of any buffer amplifiers must be considered in the design. Scanning multiplexers can achieve speeds upward of 10 million signals per second.

5.9 OUTPUT VIDEO AMPLIFIERS

The output video driver buffers the encoded signal string from the ROIC multiplexer off the focal plane, through the cryogenic and ambient interface cables, and finally to a set of warm electronics where any necessary signal conditioning is provided prior to digitization or display. The primary concern of the video driver is the cryogenic power dissipation required to provide adequate frequency response and dynamic range.

The limits of video driver power can be determined by evaluating the extremes in driver circuit configurations and output load capacitance. At the lower limit, power can be calculated from the energy required to charge and discharge the load capacitor presented by the cable of Fig. 5.29:

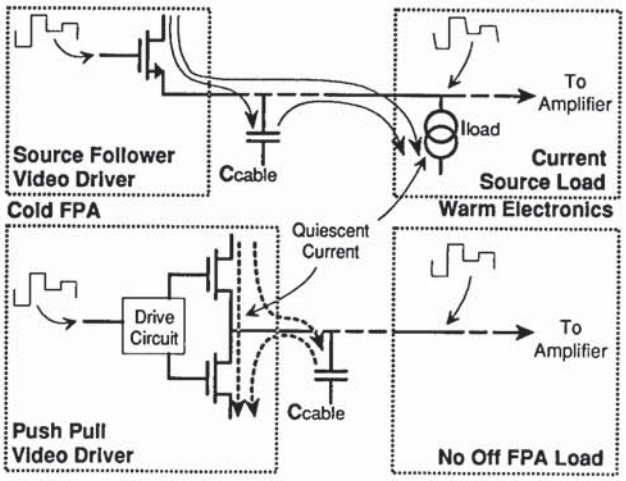


Fig. 5.29 Key drivers in video driver power are data rate, drive capacitance, and driver design. The lower power push-pull has greater ROIC complexity.

$$E(C_{\text{load}}) - \frac{1}{2}C_{\text{load}}\Delta V_{\text{max}}^2 \quad [\text{J}] \ . \tag{5.86}$$

The total power is the product of the energy and the repetition rate, plus the energy required to provide the idle current, I_{idle}, in the push-pull circuit:

$$P_{\text{out}}\ (\text{min}) > \frac{0.5\ C_{\text{load}}\Delta V_{\text{max}}^2 N}{T_{\text{frame}}} + (\Delta V_{\text{max}} + 1.5)I_{\text{idle}} \quad [\text{W}] \ , \tag{5.87}$$

where C_{load} is the total output capacitance, ΔV_{max} is the maximum output voltage swing, N is the number of elements, and T_{frame} is the time between two frames of data. The idle current required for the push-pull is in the 10- to 100-μA range.

A video driver circuit configuration that can approach this minimum power is the push-pull concept in Fig. 5.29. Push-pull circuits require several components to properly bias and drive the output transistors, as well as a quiescent current to keep them both active and linear. Although these push-pull circuits are somewhat complex, the near unity gain push-pull of Fig. 5.29 has advantages in speed and power over most other common video driver configurations.

The most common type of video driver for cooled focal planes is the source follower (in MOSFET implementations) of Fig. 5.29. The primary advantages of this circuit are simplicity, relative low power, and near unit gain; also, this configuration implements a current source load off the focal plane to minimize focal plane cryogenic power. The source follower responds to a positive change in input voltage by charging the stray load capacitor through the low-impedance source of the active N-channel MOSFET. Since the MOSFET in this configuration can only source current, or charge the load capacitance, an off-focal-plane current load is needed to discharge the capacitor for negative transi-

tioning signals. The current load required to discharge the capacitor is dependent on the time allocated for slewing the output T_{slew}, through the maximum output voltage swing $\Delta V_{\max}$:

$$I_{\text{load}} = \frac{\Delta V_{\max} C_{\text{load}}}{T_{\text{slew}}} \quad [\text{A}] \ . \tag{5.88}$$

To provide a reasonable time for downstream electronics to settle, T_{slew} is typically no more than one-third the total data valid time. The data valid time T_{data} for a given output is approximately

$$T_{\text{data}} < \frac{T_{\text{frame}}}{N} \quad [\text{s}] \ . \tag{5.89}$$

This gives

$$I_{\text{load}} > \Delta V_{\max} C_{\text{load}} \frac{3N}{T_{\text{frame}}} \quad [\text{A}] \ . \tag{5.90}$$

To keep the MOSFET operating in a linear fashion, the maximum voltage across the output transistor must be approximately 1 V greater than the maximum output voltage swing. The worst case video driver power occurs when the maximum voltage is across the video driver transistor:

$$P_{\text{driver}}\,(\max) = (\Delta V_{\max} + 1)\Delta V_{\max} C_{\text{load}} \frac{3N}{T_{\text{frame}}} \quad [\text{W}] \tag{5.91}$$

and for large voltage swings

$$P_{\text{driver}}\,(\max) \approx 3C_{\text{load}} \Delta V_{\max}^2 \frac{N}{T_{\text{frame}}} \quad [\text{W}] \tag{5.92}$$

or up to six times the minimum power of the push-pull. Knowledge of the typical infrared signal can result in a lower average power of the source-follower driver; the circuit should be designed so the MOSFET has lower voltage across it in the nominal signal output case, and has higher voltage across it only when there are infrequent large differences between the nominal output voltage and the maximum deviation from the nominal output. In Fig. 5.29, the nominal might be 1.5 V below the power supply V_{dd}, while the maximum deviation may occur at V_{dd} − 6 V.

5.10 POWER DISSIPATION

Power dissipation on any cryogenic focal plane, although very small when compared to conventional room temperature analog electronics, is a major system driver because it often translates into greater system weight, increased power in active coolers, larger cooler volume, and limitations in mission life. For example, the mission life of a space sensor can be driven by the consumption

rate of a cryogenic liquid or solid; or, where active cooling is utilized, cryogenic power can force the use of larger coolers, which in turn consume more electrical power and add greater weight. Passive cooler (radiative cooler) size also increases considerably as focal plane increases, and it is ultimately limited by space viewing issues as well as size and weight constraints. In view of these factors, it is not only important to reduce readout power, but to design sensors for the highest operating temperature that the selected detector technology can support.

Cold focal plane power often includes electrical power dissipation (I^2R) in the readout, detector, and cable; radiative power from the environment to the focal plane and interconnect cable; and power conducted through the interconnect cable to the focal plane. The readout design influences both I^2R losses in the readout and the thermal load of the cable, because this load is a function of the number of cable traces required by the readout. Of secondary importance are on-chip bias and clock generating circuits, such as the scanner multiplexer, which can be designed with minimal thermal impact for high-density sensor arrays. High-impedance detectors, such as photovoltaics, have negligible impact on focal plane power given that detector current is in the fempto-amp to nano-amp range.

Power dissipation occurs in two primary areas of the readout: the preamplifier section, with associated signal processing, and the video output driver. In some cases, where the preamplifier output is in the charge rather than the voltage domain, the multiplexer transimpedance amplifier must be considered. The drivers of power dissipation are (1) the data rate, which is set by the system specification, and (2) the linearity and sensitivity requirements of the readout, which drive the circuit design. The data rate, a combination of the detector element frame rate and the total number of elements, drives the slew rate and frequency response of both preamplifier and output video driver.

Total readout power, including the preamplifier, basic signal processing, and video driver, is a strong function of the detector unit cell preamplifier design. Unit cell power can be estimated, to first order, based on the number of active transistors within the unit cell. Estimates for typical power per unit cell were summarized earlier in Table 5.3.

Preamplifiers, such as the self-integrator, direct injection, current mirror, and resistor load types, have negligible current in the unit cell, that is, on the order of the detector current. Power for these circuits is in the nanowatt range and is also negligible. These circuits are normally current mode output and, as such, require a transimpedance amplifier on the output of the multiplexer or a CCD for charge transfer. In the case of CCD, power is very small and dominated entirely by the output video amplifier and on-chip clock and bias circuits. Transimpedance amplifiers, on the other hand, require power in the milliwatt range. The transimpedance amplifier is shared between the unit cells on the multiplexer bus and dissipates 1 to 10 nW per unit cell.

Preamplifiers such as the feedback-enhanced direct injection, capacitor feedback transimpedance amplifier, and source follower per detector types have amplifiers within the unit cell that require substantial bias current (on the order of 0.5 to 6 μA per amplifier). This results in a power of 3 to 40 μW per unit cell. In the case of the SFD, power can be cycled off except during the multiplexer read time.

Signal processing in the unit cell can also consume significant power if buffer amplifiers, such as the source follower, are utilized. These buffers consume about 1 to 3 μA per buffer. A typical bias voltage is 6 V, resulting in 5 to 20 μW of power per buffer.

Output video amplifier power is covered in Sec. 5.9.

5.11 DYNAMIC RANGE

Dynamic range (DR) is usually defined as maximum unsaturated photon flux, Q_{sat}, divided by NEI, as measured at the minimum specified background irradiance:

$$DR = \frac{Q_{sat}}{NEI} \tag{5.93}$$

or

$$DR = 20 \log\left(\frac{Q_{sat}}{NEI}\right) \quad [dB] \ . \tag{5.94}$$

Equation (5.93) defines instantaneous dynamic range, in which no user or external control is utilized to lower the gain for high-amplitude signals. Automatic gain switching, reduced integration time, and other methods can be used to achieve higher effective system dynamic ranges. Extremely high instantaneous dynamic ranges can be achieved through the use of nonlinear gain amplifiers in the readout circuit. The typical dynamic range of a focal plane can be calculated by dividing the maximum output voltage swing (on the order of 5 V) by the output noise floor of the sensor (typically on the order of 1 mV or less), and is usually in the range of 60 to 80 dB.

The maximum output voltage swing for any given ROIC is usually limited by either the integrated circuit process itself or the maximum acceptable focal plane power restrictions. The challenge of the readout designer is to achieve a large signal swing with the lowest possible noise floor. The minimum noise floor is a function of noise contributions of the preamplifier, multiplexer, and output driver, as well as external EMI. These noise sources can be filtered to some degree by on-focal-plane or off-focal-plane electronics. For example, the output of low data rate sensors can be filtered to reduce noise levels in astronomy applications.

For white noise, the rms noise contribution of a given source is proportional to the square root of the bandwidth. This relationship is useful in determining the dynamic range capability of a sensor. High data rate multiplexers and video drivers require high bandwidths. Therefore, one technique of increasing dynamic range is to decrease the corresponding bandwidth (data rate), and hence the noise of each output, by decreasing the number of elements multiplexed to a single output and then increasing the total number of outputs on the readout.

The general trend of minimum output noise versus multiplexer data rate is plotted in Fig. 5.30. The right axis shows dynamic range, in terms of digitizer

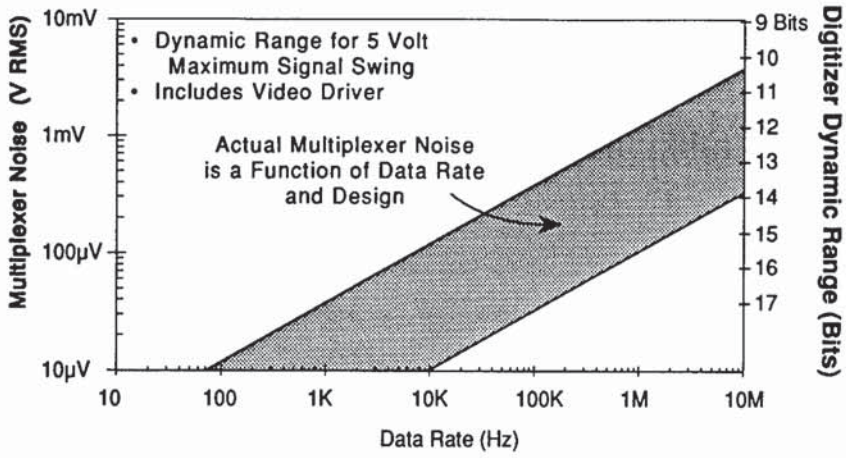


Fig. 5.30 Multiplexer noise floor and dynamic range are a function of data rate of a given output. A 12-bit dynamic range can be achieved in the 1- to 5-MHz region.

bits, for a maximum voltage swing of 5 V; the LSB (least significant bit) corresponds to the minimum sensor noise at the given data rate. The resolution of the focal plane falls to 12 to 13 bits in the 1-MHz data rate range, and is reduced to the 10 to 11 range at about the 5-MHz data rate.

5.12 CROSSTALK AND FREQUENCY RESPONSE

Two basic forms of signal crosstalk occur in SCAs. The first type is crosstalk from one physical detector element to another, which can be either electrical or optical in nature; the second is crosstalk on a detector element between one frame of data and its next frame of data (in time), which can also be expressed as frequency response in scanning sensors. Because a fraction of the photon energy striking a detector element is sensed in either an adjacent element or in a subsequent frame, both forms of crosstalk result in decreased image sharpness. Crosstalk can also manifest as a ghost or a latent image that fades with time. Poor frequency response in staring sensors can result in slow response to changes in the scene. Because frequency response of the detector channel is often a function of the specific readout preamplifier design, the use of preamplifier circuits that completely reset all storage elements (capacitors), prior to acquisition of a new frame of data, should be considered in critical applications where high-frequency response is required.

The output video amplifier is also a source of crosstalk problems in focal plane designs. The video amplifier, and all subsequent off-focal-plane circuits, must settle to a sufficient level prior to signal digitization. This settling level can be a source of confusion, because it is often specified to be within the system digitizers' least significant bit, which is in fact rarely required. Figure 5.31 shows a simplified representation of the output of a focal plane, where r_{out} is the video amplifier output impedance and C_{load} is the total output load capacitance including cables and other strays. Assuming the frequency response of the output data stream is dominated by a single pole of the circuit, the frequency response is

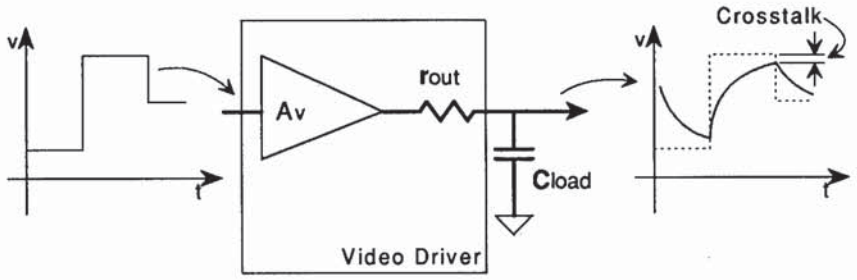


Fig. 5.31 The output configuration of a ROIC is designed to minimize crosstalk and on-focal-plane power.

$$f = \frac{1}{2\pi C_{\text{load}} r_{\text{out}}} \quad [\text{Hz}] \tag{5.95}$$

and the crosstalk between adjacent data stream elements is approximately

$$\text{crosstalk} = \exp\left(\frac{-t}{r_{\text{out}} C_{\text{load}}}\right), \tag{5.96}$$

where t is the elapsed time between the onset of new data being driven onto the output and when the digitizer acquires, or samples, the analog data. The crosstalk required for a typical sensor (including the detector) is normally on the order of 0.5 to 10%. If the video output circuit were designed to settle within half the least significant bit, on a 12-bit digitizer, the crosstalk of the video stage would be forced to less than 0.01%. Crosstalk this low would require a very high video circuit bandwidth and, since noise is related to bandwidth, this could result in increased noise. Settling time, or crosstalk, should be allocated in a reasonable fashion between the detector, the preamplifier, the video driver, and subsequent circuitry. The dominant output pole need not be the elements shown in Fig. 5.31, but could be characteristics of other downstream amplifier stages in the signal processing chain prior to digitization. The same analysis can be made for these other elements by appropriate substitution in Eqs. (5.95) and (5.96).

In most focal plane applications, significant crosstalk between elements that are not located optically adjacent to each other is unacceptable. An example is that in which subsequent columns of detector data are multiplexed to a single data stream; crosstalk occurs between the last element in one row of detector elements and the first element in the next row. In this case, a faster video settling time may be required at the expense of reduced noise bandwidth.

5.13 DESIGN METHODOLOGY

The full readout design includes many components not covered in the limited space of this chapter. This information, together with the references and bibliography, provides many of the tools required for successful circuit trades and designs. The circuit design approach is only a part of the overall procedure.

As mentioned, the design requires a well-understood set of requirements allocated to all sensor subcomponents. Circuit modeling and design is an iterative approach that leads to successful integrated circuit layout and processing. Performance of the resultant readout device is then fed back into the model to provide information for redesign or for future ROIC applications.

Acknowledgments

The author would like to recognize the following colleagues for the many discussions covering this subject: Will Frye, Mostyn Gale, Mark Goodnough, Mary Hewitt, Alan Hoffman, Joe Norworth, Terrence Lomheim, and Geof Orias. We also recognize support of the technology by the U.S. government, Santa Barbara Research Center, and Hughes Aircraft Company.

References

1. T. L. Koch, J. H. de Loo, M. H. Kalisher, and J. D. Phillips, "Monolithic n-channel HgCdTe linear imaging arrays," *IEEE Transactions on Electron Devices* **ED-32**(8) 1592–1598 (Aug. 1985).
2. M. E. McKelvey, C. R. McCreight, J. H. Goebel, N. N. Moss, and M. L. Savage, "Characterization of direct readout Si:Sb and Si:Ga infrared detector arrays for space-based astronomy," *Proceedings of the SPIE* **868,** 73–80 (1987).
3. S. M. Sze, *Physics of Semiconductor Devices,* 2nd ed., John Wiley & Sons, New York (1981).
4. A. S. Grove, *Physics and Technology of Semiconductor Devices,* John Wiley & Sons, New York (1967).
5. S. Lui and L. W. Nagel, "Small-signal MOSFET models for analog circuit design," *IEEE Journal of Solid-State Circuits* **SC-17**(6), 983–998 (Dec. 1982).
6. C. D. Motchenbacher and F. C. Fitchen, *Low-Noise Electronic Design,* John Wiley & Sons, New York (1973).
7. I. M. Hafez, G. Ghibauso, and F. Balestra, "A study of flicker noise in MOS transistors operated at room and liquid helium temperatures," *Solid State Electronics* **33**(12), 1525–1529 (1990).
8. W. V. Backensto and C. R. Viswananathan, "Bias-dependent 1/f noise model of an MOS transistor," *IEEE Proceedings* **127**(2), 87–92 (Apr. 1980).
9. M. D. Nelson, J. F. Johnson, and T. S. Lomheim, "General noise processes in hybrid infrared focal plane arrays," *Optical Engineering* **30**(11), 1682–1700 (Nov. 1991).
10. A. W. Hoffman, "Operation and calibration of self-integrating multiplexed arrays," *Proceedings of Workshop on Ground Based Astronomical Observations with Infrared Detectors,* C. G. Williams, B. E. Ecklin, Eds., March 1987, Hilo, Hawaii, p. 29.
11. R. Swanson and J. D. Meindl, "Complementary MOS transistors in low voltage circuits," *IEEE Journal of Solid-State Circuits* **SC-7**(2), 146–153 (Apr. 1972).
12. S.-L. Jang, "A model of 1/f noise in polysilicon resistors," *Solid State Electronics* **33**(9), 1155–1162 (1990).
13. D. E. Ludwig, N. D. Woodall, and M. M. Spanish, "On-focal plane analog-to-digital conversion with detector gain and offset compensation," *Proceedings of the SPIE* **1097,** 73–84 (1989).
14. G. S. Hobson, *Charge-Transfer Devices,* John Wiley & Sons, New York (1978).
15. M. J. Howes and D. V. Morgan, *Charge-Coupled Devices and Systems,* John Wiley & Sons, New York (1979).
16. C. H. Sequin and M. F. Tompsett, *Charge Transfer Devices,* Academic Press, New York (1975).
17. R. D. Thom, T. L. Koch, J. D. Langan, and W. J. Parrish, "A fully monolithic InSb infrared CCD array," *IEEE Transactions on Electron Devices* **ED-27**(1), 160–170 (Jan. 1980).

Bibliography

Bailey, R. B., L. J. Kozlowski, J. Chen, D. Q. Bui, K. Vural, D. D. Edwall, R. V. Gil, A. B. Vanderwyck, E. R. Gertner, and M. B. Gubala, "256 × 256 hybrid HgCdTe infrared focal plane arrays," *IEEE Transactions on Electron Devices* **38**(5), 1104–1109 (May 1991).

Capone, B., L. Skolnik, R. Taylor, F. Shepherd, S. Roosild, W. Ewing, W. Kosonocky, and E. Kohn, "Evaluation of a Schottky infrared charge-coupled device (IRCCD) staring mosaic focal plane," *Optical Engineering* **18**(5), 535–541 (Sep./Oct. 1979).

Carson, J. C., and S. N. Shanken, "High volume producibility and manufacturing of Z-plane technology," *Proceedings of the SPIE* **1097,** 138–149 (1989).

Celik-Butler, Z., and T. Y. Hsiang, "Spectral dependence of 1/f noise on GATE bias in N-mosfets," *Solid State Electronics* **30**(4), 419–423 (1987).

Cohen, J., *Introduction to Noise in Solid State Devices,* NBS TN 1169, National Bureau of Standards, Washington, DC (Dec. 1982).

Fang, Z.-H., A. Chovet, Q.-P. Zhu, and J.-N. Zhao, "Theory and applications of 1/f trapping noise in MOSFETs for the whole biasing ranges," *Solid State Electronics* **34**(4), 327–333 (1991).

Fleetwood, D. M., and J. H. Scofield, "Evidence that similar point defects cause 1/f noise and radiation-induced-hole trapping in metal-oxide-semiconductor transistors," *Physical Review Letters* **64**(5), 579–582 (Jan. 1990).

Forrest, W. J., A. Moneti, C. E. Woodward, J. L. Pipher, and A. Hoffman, "The new near-infrared array camera at the University of Rochester," *Astronomical Society of the Pacific* **97,** 183–198 (Feb. 1985).

Fowler, A. M., I. Gatley, F. Stuart, R. R. Joyce, and R. G. Probst, "The NOAO 1–5 micron imaging camera: a new national resource," *Proceedings of the SPIE* **972,** 107–121 (1988).

Fronen, R. J., and F. N. Hooge, "1/f noise in a p-i-n diode and in a diode laser below threshold," *Solid State Electronics* **34**(9), 977–982 (1991).

Grabowski, F., "Influence of dynamical interactions between density and mobility of carriers in the channel on 1/f noise of MOS transistors below saturation—I. mechanisms," *Solid State Electronics* **32**(10), 909–913 (1989).

Grabowski, F., "Influence of dynamical interactions between density and mobility of carriers in the channel on 1/f noise of MOS transistors below saturation—II. implications," *Solid State Electronics* **32**(10), 915–918 (1989).

Gustafsson, S., R. Sundblad, and C. Svensson, "Noise behavior of a static induction transistor between 77K and 300 K," *Solid State Electronics* **30**(4), 439–443 (1987).

Janesick, J. R., T. Elliott, S. Collins, M. M. Blouke, and J. Freeman, "Scientific charge-coupled devices," *Optical Engineering* **26**(8), 692–714 (Aug. 1987).

Johnson, J. F., and T. S. Lomheim, "Hybrid infrared focal plane signal and noise modeling," *Proceedings of the SPIE* **1541,** 110–126 (1991).

Lee, T. H., W.-C. Chang, W. A. Miller, G. R. Torok, K. Y. Wong, B. C. Burkey, and R. P. Khosla, "A four million pixel CCD image sensor," *Proceedings of the SPIE* **1242,** 10–16 (1991).

Lomheim, T. S., R. M. Shima, J. R. Angione, W. F. Woodward, D. J. Asman, R. A. Keller, and L. W. Schumann, "Imaging charge-coupled device (CCD) transient response to 17 and 50 MeV proton and heavy-ion irradiation," *IEEE Transactions on Nuclear Science* **37**(6), 1875–1885 (Dec. 1990).

McCreight, C. R., J. A. Estrada, J. H. Goebel, M. E. McDelvey, D. D. McKibbin, R. E. McMurray, Jr., T. T. Weber, J. Farhoomand, N. N. Moss, and M. L. Savage, "Low-background detector arrays for infrared astronomy," *Proceedings of the SPIE* **973,** 250–255 (1988).

McLean, I. S., *Electronic and Computer-Aided Astronomy,* John Wiley & Sons, New York (1989).

Mikoshiba, H., "1/f noise in n-channel silicon-gate MOS transistors," *IEEE Transactions on Electron Devices* **ED-29**(6), 965–970 (June 1982).

Mullens, R. S., and T. I. Kamins, *Device Electronics for Integrated Circuits,* John Wiley & Sons, New York (1977).

Norton, P. R., "Infrared image sensors," *Optical Engineering* **30**(11), 1649–1663 (Nov. 1991).

Oh, S.-Y., and R. W. Dutton, "A simplified two-dimensional numerical analysis of MOS devices—DC case," *IEEE Transactions on Electron Devices* **ED-27**(11), 2101–2110 (Nov. 1980).

Reimbold, G., "Modified 1/f trapping noise theory and experiments in MOS transistors biased from weak to strong inversion—influence of interface states," *IEEE Transactions on Electron Devices* **ED-31**(9), 1190–1198 (Sep. 1984).

Schiebel, R. A., "1/f noise in HgCdTe MISFETs," *Solid State Electronics* **32**(11), 1003–1007 (1989).

Skotnick, T., and W. Marciniak, "A new approach to threshold voltage modeling of short-channel MOSFETs," *Solid State Electronics* **29**(11), 1115–1127 (1986).

Swanson, R., and J. D. Meindl, "Ion-implanted complementary MOS transistors in low-voltage

circuits," *IEEE Journal of Solid-State Circuits* **SC-7**(2), 146–153 (Apr. 1972).

Van Der Ziel, A., "Integral expression for 1/f noise in MOSFETS at arbitrary drain bias," *Solid State Electronics* **29**(1), 29–30 (1986).

Van Vliet, C. M., "A survey of results and future prospects on quantum 1/f noise and 1/f noise in general," *Solid State Electronics* **34**(1), 1–21 (1991).

Wu, E. N., and A. Van Der Ziel, "On the influence of substrate doping on the input conductance and the induced GATE noise in MOSFETS," *Solid State Electronics* **27**(11), 945–946 (1984).

Zhu, X. C., A. Van Der Ziel, and K. H. Duh, "Low-frequency noise spectra in MOSFETS made by the DMOS process," *Solid State Electronics* **28**(4), 325–328 (1985).