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Functionalized Bonding Materials and Interfaces for Heterogeneously Layer-Stacked Applications

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Recently, heterogeneous integration has become more important in enhancing device performance and creating new functions. For this purpose, wafer bonding can provide a straightforward method to integrate different materials, regardless of lattice mismatch. Here, we review recent application spaces using low-temperature wafer bonding by classifying wafer bonding into direct bonding, oxide bonding, and metal bonding. We show that bonding materials and interfaces have an important role in achieving high-performance semiconductor devices.

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I. INTRODUCTION

Nowadays, heterogeneous integration is a key technology to achieve a multi-functional chip using several different nanoscale materials [1–14]. Heterogeneous integration provides not only performance enhancement but also new functionalities such as monolithic opto-electronic integration including 3D integration [14–18]. Actually, in terms of 3D heterogeneous integration, non-Si materials such as III-V and Ge provide better process compatibility. They can be processed at quite a low temperature, typically lower than 400 °C; therefore, multiple stacked devices can be fabricated without any damage to prefabricated devices to provide multi-functional and area-efficient semiconductor chips [14].

Despite the tremendous demands for heterogeneous integration, the sequential epitaxial growth of different materials is still quite challenging mainly due to the different lattice constants, thermal expansion coefficients, surface polarities, *etc.* [19–25]. On the other hand, wafer bonding-based material integration would be the most-straightforward method to integrate different materials on any materials because it provides high-quality material integration regardless of the material itself by bonding the active device layer grown on a lattice-matched substrate. Furthermore, due to recent progress in low-temperature wafer bonding using plasma surface activation [26–30], many more opportunities are available by functionalizing a bonding interface, which is critically important for various layer-stacked applications such as multi-junction solar cells [31–35], metal-oxide-semiconductor field effect transistors (MOSFETs) [36–51], optical sensing platforms [52–56], thin film photodetectors [57–65], semiconductor-insulator-semiconductor (SIS) optical phase shifters [13, 66–69], *etc.* In this paper, we review our recent activities about the low-temperature wafer bonding process to functionalize the bonding interface and extension to various applications with more detail on each application.

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II. WAFER BONDING PROCEDURE

Figure 1 shows the typical procedures of the wafer bonding process. Wafer bonding procedures can be diverse depending on the purpose and functions required at the bonding interface because each application needs different types of bonding media. Therefore, depending on the purpose, one can design a particular wafer bonding procedure. Table 1 shows the classification of wafer

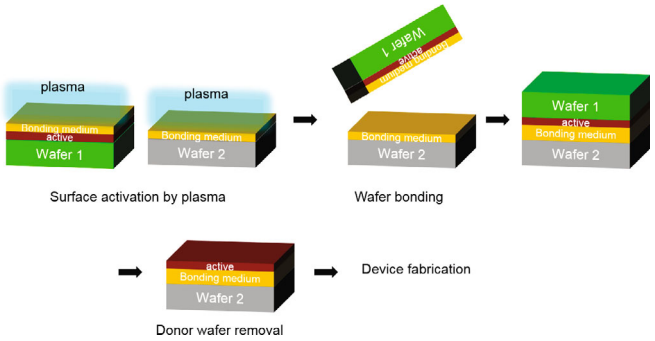

Fig. 1. (Color online) Typical process flow for the wafer bonding of two different wafers by using plasma surface activation.

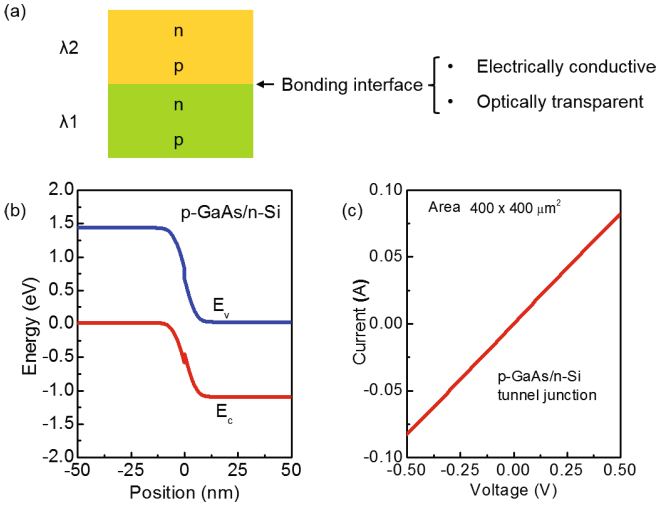

Fig. 2. (Color online) (a) Schematic cross-sectional image of a multi-junction solar cell and its requirements for bonding interfaces. (b) Band diagram of a p-GaAs/n-Si bonded heterojunction. (c) *I-V* curve of a directly bonded p-GaAs/n-Si junction.

bonding methods, their electrical and optical properties and their potential applications. Typically, the bonding media can be an oxide and a metal, but some applications do not need any bonding medium. Here, worth noting is the observation that the wafer bonding process at low-temperature has significant benefits such as the exclusion of unwanted/undesirable reactions of the bonded active device layers at the bonding interface, which can deteriorate the device performance. Low-temperature wafer bonding, even room temperature bonding enables interface engineering by means of new functions.

First, we activated the surfaces of the target wafers after a typical surface cleaning process. Here, Ar and O_2 plasmas were typically used for direct/metal bonding and oxide bonding, respectively [70,71]. The plasma irradiation time was 30 - 60 s. After the wafers had been bonded, the bonded wafers were pressed with 20 kgf/cm^2 without high-temperature thermal annealing. Afterwards, thermal annealing af a moderate annealing temperature can be applied to enhance the bonding strength.

Table 1. Classification of wafer bonding into direct bonding, oxide bonding, and metal bonding and their electrical and optical properties and potential applications.

Bonding method	Electrical properties	Optical properties	Potential applications
Direct bonding	Rectifying or conducting	Transparent	Multi-juncting solar cell
Oxide bonding	Insulating or conducting	Transparent	MOSFET Photonics platform SIS optical phase shifter
Metal bonding	Conducting	Reflective	Phoodetector

III. REQUIRED FUNCTIONS AT VARIOUS BONDED INTERFACES

1. Direct bonded interface

Using direct bonding, we developed electrically conductive and optically transparent bonding interfaces that could be used for multi-junction solar cells. As shown in Fig. 2, multi-junction solar cells should have a tunnel junction with different carrier polarities for different semiconductors. To achieve high-quality GaAs junction solar cells with Si junction solar cells, we developed GaAs/Si hetero-ohmic junctions by using direct wafer bonding [35]. Using the bonding between the heavily-doped p-GaAs and n-Si, we fabricated electrically conductive tunnel junctions with a very low interface resistance ($R_{\text{interface}}$) of 8.8 × 10^{-3} Ω·cm^2, as shown in Figs. 2(b) and 2(c). This value was much lower compared with other studies because native surface oxide formation was minimized before the wafer bonding [31, 72]. Because the refractive index was almost the same in both materials, the bonding interface in this junction was obviously optically transparent. Using a bonded Ohmic contact, we successfully demonstrated GaAs solar cells electrically connected to a Si substrate with a high energy conversion efficiency exceeding 13% even without an anti-reflection coating [35]. This result can be potentially extended to multi-junction solar cells using multiple materials covering multiple wavelength bands, but with lattice mismatch.

2. Oxide bonded interface

Various applications use oxide bonding. Both insulating and conducting bonding interfaces are possible by choosing the appropriate oxide materials [36–51,73,74]. Furthermore, an oxide is typically optically transparent,

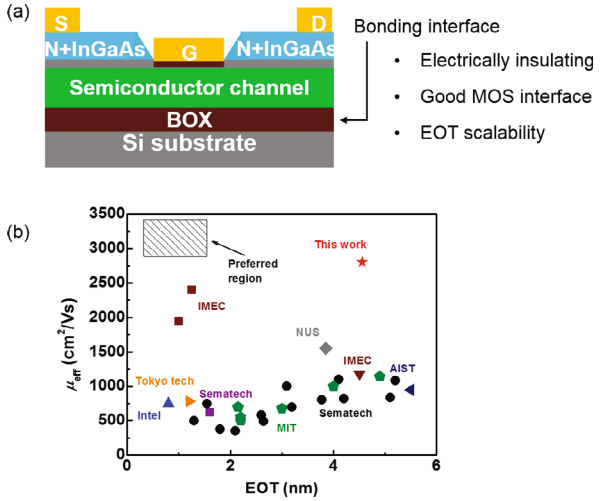

Fig. 3. (Color online) (a) Schematic cross-sectional image of an InGaAs-OI MOFET and its requirements for the bonding interfaces (b) Effective electron mobility for $N_s = 3 \times 10^{12}$ cm^{-2} for our InGaAs-OI MOSFET and from various other reports.

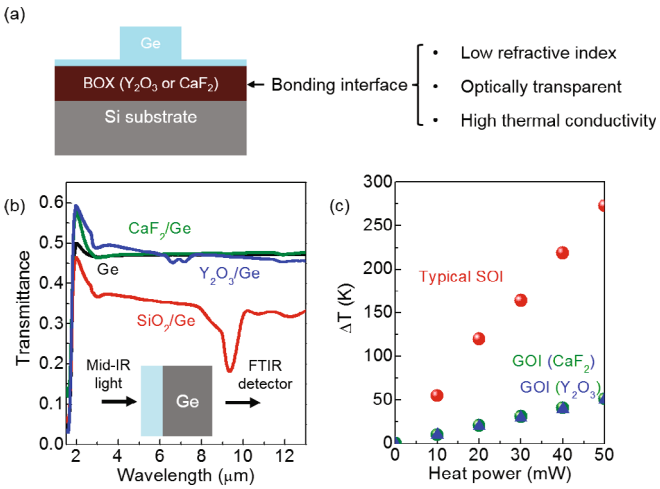

Fig. 4. (Color online) (a) Schematic cross-sectional image of the GOI photonics platform for Mid-IR sensing and its requirements for the bonding interfaces. (b) Transmittance of the oxide (SiO_2, Y_2O_3, CaF_2)/Ge samples in the mid-IR wavelength range. (c) Simulated temperature increase as a function of the power of the heat source on the SOI and the GOI platform.

which is one of the big advantages for many optical devices [56,67–74]. In addition, oxide bonding has recently become quite common and easy, if the surface roughness is low enough regardless of the material species.

Representative applications using oxide bonding would be semiconductor-on-insulator ("X"OI) MOSFETs shown in Fig. 3(a). If undesirable effects such as short-channel effects (SCEs) due to device scaling are to be avoided, a thin-body channel structure is mandatory in deeply scaled MOSFETs. In this sense, a tremendous numbers of studies have been published on Si-on-insulator (SOI) MOSFETs. Recently, III-V-on-insulator (III-V-OI) and Ge-on-insulator (GOI) MOSFETs have been studied much due to their high mobility properties [36–51, 75–82]. In these kinds of devices, a good MOS interface between the semiconductor and the buried oxide (BOX) and equivalent oxide thickness (EOT) scalability are, indeed, important to guarantee both a high carrier mobility over the whole carrier charge density (N_s) range and SCE control [51,82,83]. Here, a MOS interface at the semiconductor/BOX is formed by wafer bonding. Therefore, a surface treatment prior to oxide deposition, as well as any surface treatment of the oxide surface, would involve important process parameters for achieving good MOS interfaces [82]. Recently, the heat conducting properties of the BOX have become important for fast heat dissipation of devices [84]. Besides the general electrical characteristics, BOX engineering makes achieving a low subthreshold slope by using ferroelectric materials in the BOX possible [85]. Furthermore, a reconfigurable device can be achieved by introducing Oxide/Nitride/Oxide (ONO) charge trap layers in the BOX [86].

To achieve a good back MOS interface and EOT scalability of the BOX in InGaAs-OI MOSFETs, we carefully treated the surface before the oxide deposition and used a high-k Y_2O_3 BOX. We found that Y_2O_3 provided a good MOS interface for the InGaAs surface with proper pre-treatment and thermal annealing [36,87]. Due to the good MOS interfaces both for the top and the bottom, we obtained a record high electron mobility among the surface channel InGaAs MOSFETs (Fig. 3(b)) [88].

A photonics platform such as SOI and GOI is another representative application using a thick BOX that can be fabricated by oxide bonding. With SOI and/or GOI as a photonics platform, the BOX should be thick enough and its refractive index should be low enough to guarantee a good optical confinement in the core and to eliminate optical leakage to the substrate. Furthermore, the BOX should be optically transparent for the targeted wavelength of light. Finally, having a high thermal conductivity when considering light source integration, which typically has a weak thermal stability, is preferable [56]. All these requirements have to be satisfied during the wafer bonding process by manipulating the bonding materials and the interface. In the near-infrared (NIR) wavelength range, a common material and structure platform, which is SOI, exists. However, in the mid-infrared (Mid-IR) wavelength range, many suggested platforms are competing with each other in terms of device performance, cost, CMOS compatibility, *etc.* [52,89–92]. We also suggest GOI with a F- or a Y-based insulator as a BOX for a mid-IR photonics platform, as shown in Fig. 4(a) [56]. Using CaF_2 and Y_2O_3, we obtained a good optical transparency at wavelengths up to at least 13 μm (Fig. 4(b)). Furthermore, a significant thermal resistance reduction was achieved in our GOI platform compared

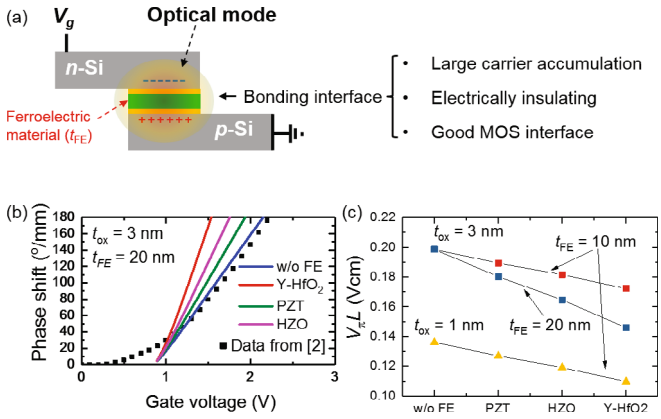

Fig. 5. (Color online) (a) Schematic cross-sectional image of the SIS optical phase shifter with FE materials and its requirements for the bonding interfaces. (b) Phase shift characteristics of the SIS optical phase shifter with various FE materials. (c) $V_\pi L$ as a function of FE materials with (t_{ox}, t_{FE}) sets of (3 nm, 10 nm), (3 nm, 20 nm), and (1 nm, 20 nm).

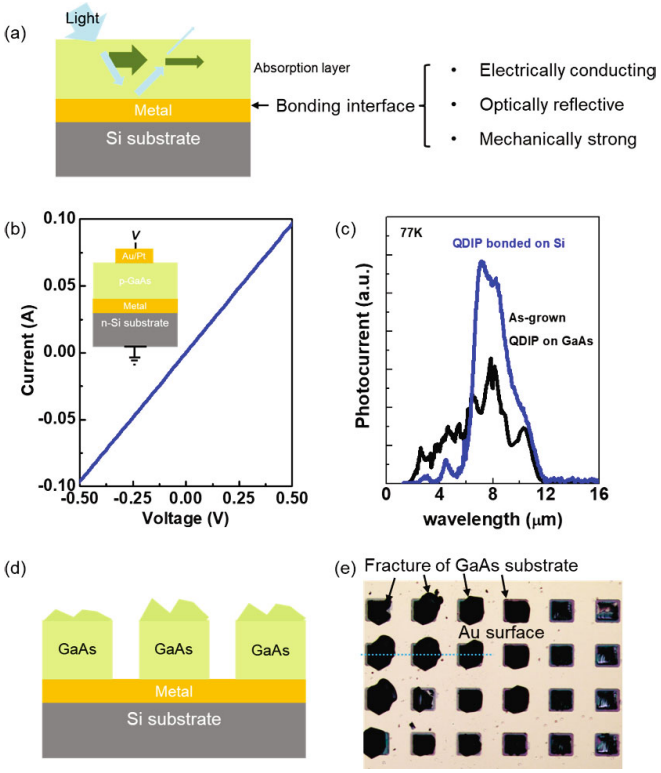

Fig. 6. (Color online) (a) Schematic cross-sectional image of the thin-film photodetectors and its requirements for the bonding interfaces (b) *I-V* curve of a metal bonded p-GaAs/n-Si junction. (c) Photocurrents of QDIP grown on GaAs and bonded on Si as a function of the wavelength. (d) Schematic cross-section of the detached GaAs substrate from the bonding interface across the line in (e). (e) A microscopic top-view image of the detached GaAs substrate.

with the SOI platform due to the high thermal conductivity of these oxides (Fig. 4(c)) [84]. The GOI structure was simply fabricated by using the low-temperature wafer bonding process described before.

Finally, a SIS optical phase shifter is a very promising application using low-temperature oxide bonding. Recently, the SIS structure for an optical phase shifter was actively studied as an optical modulator [13] and an optical switch [67] by using its inherent feature of strong carrier accumulation to achieve a high efficiency and speed and a low loss. The SIS structure can be fabricated by using oxide and poly-semiconductor deposition [93, 94], but the process temperature should be high in this case, resulting in integration difficulty and a limitation on the choice of material. Therefore, low-temperature oxide bonding would be a very favorable way to achieve a SIS structure. Using wafer bonding, people achieved hybrid integration [12, 13, 66]. III-V/Si hybrid optical modulators have been reported with both a very low voltage, length product ($V_\pi L$), which is one of the most important figures-of-merit of an optical modulator and a very low optical loss due to the high electron mobility and the low electron effective mass in the III-V semiconductor [12,13,66].

As shown in Fig. 5(a), a SIS optical phase shifter needs to have a good carrier accumulation efficiency, to be electrically insulating, and to have good MOS interfaces at the bonding interfaces. To meet these requirements, we recently suggested the use of ferroelectric (FE) materials in the insulator sandwiched by semiconductors [68]. Using the internal voltage amplification in the FE material, we were able to significantly enhance the carrier accumulation efficiency. There, we were able to increase the amount of optical phase shift at the same bias voltage, which is very beneficial for low power consumption (Fig. 5(b)). We also estimated the potential performances of optical phase shifters with various FE materials in terms of $V_\pi L$ by solving the Landau-Khalatnikov equation and the optical mode [93]. As shown in Fig. 5(b), quite a low $V_\pi L$ close to 0.1 V·cm is feasible with only Si when using a SIS structure that includes Y-HfO_2 FE. Here, we should emphasize that this structure can be achieved by using low-temperature wafer bonding; otherwise, a high-temperature process can induce interfacial damages and/or a leakage current through the insulators. At this moment, our research has predicted the performance through simulations, but experimental demonstrations will soon follow.

3. Metal bonded interface

Metal bonding is quite widely used in the semiconductor industry for applications such as 3D packaging [96]. Previously, metal bonding was done by thermo-compression bonding, which is a very stressful method for semiconductors. Another approach for metallic bond-

ing would be the indium bump process [97]. However, the indium bump process typically has a weak bonding strength and requires a very complicated process. Furthermore, the indium bump process limits the functional use of bonding metals in the application such as in thin-film photodetectors for recycling the incident light from the surface.

Metal bonding can be used in a thin-film photodetector application. As shown in Fig. 6(a), an electrically conducting feature provides easy integration with a readout integrated circuit, and an optically reflective feature enables photon recycling to enhance the photoresponsivity [98–100]. Furthermore, generally, a very strong metal bonded interface extends the use of these kinds of devices to space vehicles, which require mechanical stability to withstand the shock during launch. To meet the requirements shown in Fig. 6(a), we developed metal bonding techniques. Figure 6(b) shows the I-V characteristics of a metal bonded p-GaAs/n-Si junction. Here, 10-nm Pt/10-nm Au was deposited onto both substrates, and Au-Au was bonded using the bonding process described before with an Ar plasma. Figure 6(b) shows perfect Ohmic behaviors even after the bonding process, indicating the bonding interface was very clean without any unwanted insulators or air. Using metal bonding, we obtained an enhanced photo-response in a quantum-dot infrared photodector (QDIP), as shown in Fig. 6(c) [65]. The bonded QDIP shows a much higher photoresponse than the as-grown one on GaAs due to the light reflection from the bonded interface. Furthermore, to estimate the bonding strength of the metal bonding, we mechanically detached the bonded GaAs from the Si substrate. Surprisingly, the bonded GaAs was cut at the bulk region, not at the bonding interface, as shown in Fig. 6(d). Figure 6(e) shows a microscopic top-view image of the detached GaAs substrate. These results strongly indicate that the metal bonded interface is mechanically very strong, even stronger than the covalent bonding of the GaAs crystal. These features should further broaden the aerospace applications of metal bonding.

IV. CONCLUSION

In conclusion, we have developed a low-temperature wafer bonding technology to utilize bonding interfaces actively. Direct bonding, oxide bonding, and metal bonding have their own features based on the bonding materials and interfaces, which provide more functionality to devices. The various applications discussed in this study, which may not have been demonstrated enough, show how the bonding interface acts in a device and provides insight into how the wafer bonding process itself should be designed and the bonding interfaces manipulated.

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