International Technology Roadmap for Photovoltaic (ITRPV)

Results 2018 including maturity report 2019

Tenth Edition, October 2019

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1. Executive summary

The photovoltaic (PV) industry needs to provide power generation products that can compete with both conventional energy sources and other renewable sources of energy. An international technology roadmap can help to identify trends and to define requirements for any necessary improvements. The aim of the International Technology Roadmap for Photovoltaic (ITRPV) is to inform suppliers and customers about anticipated technology trends in the field of crystalline silicon (c-Si) photovoltaics and to stimulate discussion on required improvements and standards. The objective of the roadmap is not to recommend detailed technical solutions for identified areas in need of improvement, but instead to emphasize to the PV community the need for improvement and to encourage the development of comprehensive solutions. The present, tenth edition of the ITRPV was jointly prepared by 55 leading international poly-Si producers, wafer suppliers, c-Si solar cell manufacturers, module manufacturers, PV equipment suppliers, and production material providers, as well as PV research institutes and consultants. The present publication covers the entire c-Si PV value chain from crystallization, wafering, cell manufacturing to module manufacturing, and PV systems. Significant parameters set out in earlier editions are reviewed along with several new ones, and discussions about emerging trends in the PV industry are reported.

The global c-Si cell and PV module production capacity at the end of 2018 is assumed to be about 150GWp with utilization rates between 80% for Tier-1 manufacturers and 50% for Tier-2 [1, 2]; the market share of about 95% for the c-Si market and about 5% for thin-film technologies is assumed to be unchanged [3]. This roadmap describes developments and trends for the c-Si based photovoltaic technology.

The PV module market stayed stable in 2018 despite serious market uncertainties. At the same time c-Si PV production capacity increased to about 150 GWp [1]. To that effect the average module prices dropped significantly.

The consequent implementation of PERC and other improvements as well as the use of improved materials resulted in higher average module powers. The PV manufacturers expanded cell and module production capacities, upgraded existing production lines to increase cell efficiencies and continued cost reduction. The price experience curve continued with its historic learning with a further increase to 23.2%. The PV industry can keep this learning rate up over the next years by continuing the linking of cost reduction measures with the implementation of cell perfections, with enhanced and larger Si-wafers, improved cell front and rear sides, refined layouts, introduction of bifacial cell concepts, and improved module technologies. All aspects are again discussed in this revision of the ITRPV. Improvements in these areas will result 60-cell PERC modules with a mass production average module power-classes of 325 Wp for mc-Si 345 Wp p-type mono-Si, and 350 Wp for n-type mono-Si respectively by 2029. 144 half-cell PERC modules are expected to reach average module power-classes of up to 400 Wp with mc-Si, 420 Wp for p-type mono Si, and 430 Wp for n-type mono-Si respectively at that time. The combination of reduced manufacturing costs and increased cell and module performance will support the reduction of PV system costs and thus ensure the long-term competitiveness of PV power generation.

Roadmap activity continues in cooperation with VDMA, and updated information will be published annually to ensure comprehensive communication between manufacturers and suppliers throughout the value chain. More information is available at itrpv.vdma.org.

2. Approach

All topics throughout the value chain are divided into three areas: materials, processes, and products. Data was collected from the participating companies and processed anonymously by VDMA. The participating companies jointly agreed, that the results are reported in this roadmap publication. All plotted data points of the parameters reported are median values generated from the input data. As stated above, the topics are split into three areas: materials, processes, and products. Here, we address issues linked to crystallization, wafers, cells, modules, and PV systems for each of these areas respectively.

Color marking is applicable, as shown in Table 1. It is used for selected parameters to describe the maturity of a technology as of today: grey indicates that the technology is in mass production use and continuous cost optimization is done. Yellow means that an industrial solution is known but is not yet used in mass production and cost optimization has still to be done. Red means that an interim solution exists, but it is too expensive or not suitable for mass production while purple indicates that there is no known industrial solution available, only feasibility is known. In order to be comparable to the widely used technology readiness level (TRL) classification [36] we include in Table 1 a comparison between the color marking categories and the corresponding TRL values.

mass production	TRL 8-9	Industrial solution exists. Cost optimisation in mass production being done.
industrial solution	TRL 6-7	Industrial solution is known. Cost optimized mass production not done.
interim solution	TRL 4-5	Interim solution is known, but too expensive or not suitable for production.
feasibility	TRL 1-3	Feasibility is known. Industrial solution is not known.

Table 1: Color marking to visualize the maturity of technologies.

2.1. Materials

The requirements and trends concerning raw materials and consumables used within the value chain are described in this section. Reducing the consumption or replacing of some materials will be necessary in order to ensure availability, avoid environmental risks, reduce costs, and increase efficiency. Price development plays a major role in making PV-generated electricity competitive with other renewable and fossil sources of energy.

2.2. Processes

New technologies and materials, and highly productive manufacturing equipment are required to reduce production costs. By providing information on key production figures, as well as details about processes designed to increase cell efficiency and module power output, this roadmap constitutes a guide to new developments and aims to support their progress. The section on processes identifies manufacturing and technology issues for each segment of the value chain. Manufacturing topics center on raising productivity, while technological developments aim to ensure higher cell and module efficiencies.

2.3. Products

Each part of the value chain has a final product. The product section therefore discusses the anticipated development of key elements such as ingots, wafers, c-Si solar cells, modules and PV systems over the coming years.

3. PV learning curve

It is obvious that cost reductions in PV production processes should also result in price reductions [4]. Fig. 1 shows the price experience curve for PV modules, displaying the average module sales prices - at the end of the corresponding time period - (in 2018 US$/Wp) as a function of cumulative module shipments from 1976 to 12/2018 (in MWp) [2, 4, 5, 6, 7]. Displayed on a log-log scale, the plot changes to an approximately linear line until the shipment value of 3.1 GWp (shipments at the end of 2003), despite bends at around 100 MWp. This indicates that for every doubling of cumulative PV module shipments, the average selling price decreases according to the learning rate (LR). Considering all data points from 1976 until 2018 we found an LR of about 23.2% - a slight increase compared to the 22.8% in the 9th edition. The large deviations from this LR plot in Fig.1 are caused by tremendous market fluctuations between 2003 and 2016.

The last two data points indicate the module shipment volumes in 2017, and 2018. For 2017 we calculated the shipment to 105 GWp (99 GWp installation [8] + 6 GWp in warehouses [9]). The 2018 shipment value was calculated to 109 GWp: the installation of 2018 is about 102 GWp, calculated as average of the installation values indicated in [10-12], for shipments we added 7 GWp in warehouses and in transit until the end of 2018. Based on this data the cumulated shipped module power at the end of 2018 is calculated to be approximately 524 GWp. The calculated worldwide installed module power reached 505 GWp end of 2018 after 403 GWp in 2017 [8]. The corresponding module prices at the end of 2017 and 2018 were 0.34 US$/Wp and 0.24 US$/Wp respectively [7].

Learning curve for module price as a function of cumulative shipments

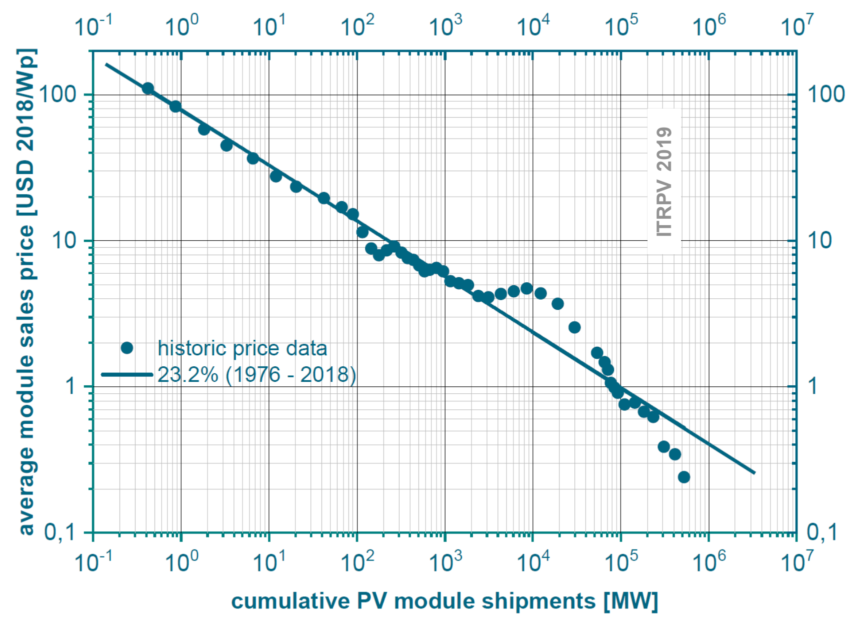

Fig. 1 : Learning curve for module spot market price as a function of cumulative PV module shipments.

4. Cost consideration

Fig. 2 shows the price development of mc-Si modules from January 2011 to January 2018 with separate price trends for poly-Si, multi crystalline (mc) wafers, and cells [7].

Module production capacity at the end of 2018 is assumed to be >150 GWp due to additional capacity expansions [1]. The limits on new PV installations announced by the Chinese government May 31 2018 have led to a reduction of PV installations in China in the second half of the year resulting in

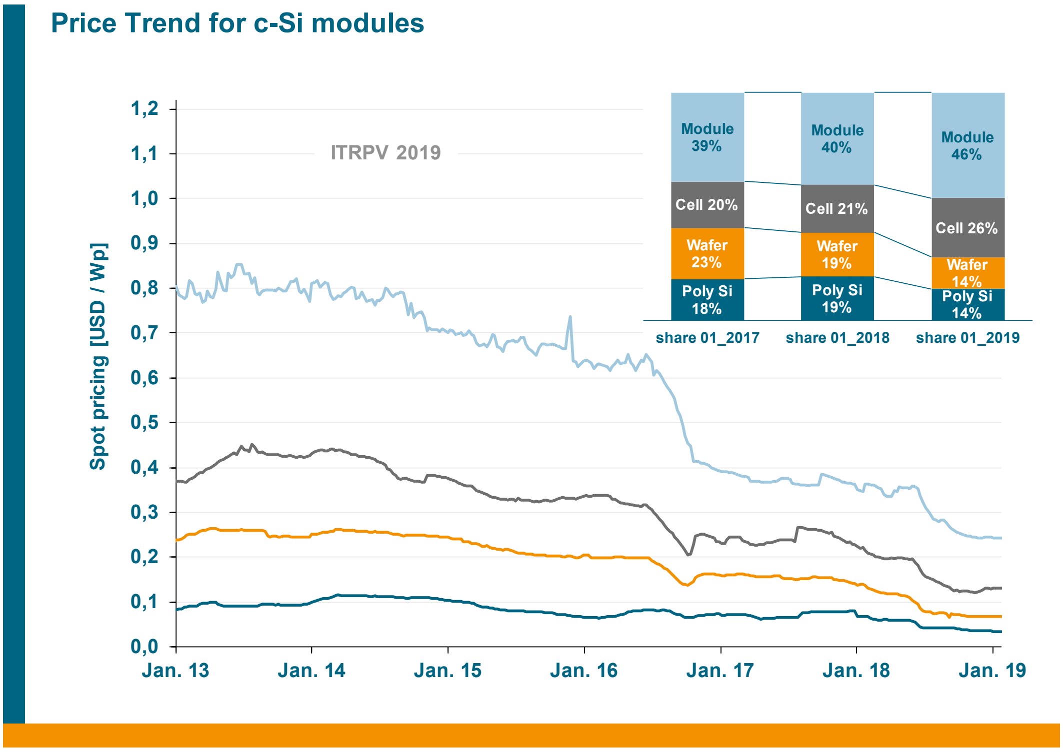

Fig. 2 : Spot market price trends for poly-Si, mc-Si wafers, cells, and c-Si modules (assumption 01/2019: 16g poly-Si per wafer(Fig. 5), average mc-Si cell efficiency: 19% {4.7Wp}, average mono-Si cell efficiency 21.5%, share mono/mc = 50/50 (Fig. 38)); inset: comparison of the proportion of the price attributable to different module cost elements between 01/2017, 01/2018, and 01/2019 (0.39, 0.354, and 0.244US$/Wp) [7].

40 GWp over all installation in 2018 vs. 54 GWp in 2017 [13]. These two facts led to a further price drop of about 30% and to an extremely challenging situation for all cell and module manufacturers. The inset of Fig. 2 shows the comparison of the proportion of prices attributable to silicon, wafer, cell, and module price since 2013. Average spot market prices for a representative mix of mc-Si and mono-Si modules on January 2017, 2018, and 2019 were calculated to 0.390 U$/Wp, 0.354 US$/Wp, and 0.244 US$/Wp respectively. The overall price level difference between 01/2017 and 01/2018 was only about 9% and the share of the different price elements remained nearly constant during 2017. But the price decrease between 01/2018 and 01/2019 was again about 30%. The fraction of poly-Si is now at about 14%. Cell conversion shares increased to 26%, as well as module conversion increased to 46% during 2018.

The non-silicon module manufacturing costs are mainly driven by consumables and materials as discussed in the c-Si PV module cost analysis in the 3rd edition of the ITRPV. Taken into account the fact that the anticipated global PV module production capacity of about 150 GWp in 2018 will further increase in 2018 due to continued capacity expansions, the production capacity will again at no account exceed the predicted global market demand of ≈120 GWp in 2018 [14]. Therefore, prices will not compensate for any cost increases as there is no shortage expected — in other words, the pressure on wafer, cell and - more painful - on module manufacturing – will persist unchanged. Achieving cost reductions in consumables, and materials will be more difficult but have to be continued. Improving productivity and product performance will become even more important.

The known three strategies, emphasized in former ITRPV editions help to address this challenge:

- Continue the cost reduction per piece along the entire value chain by increasing the Overall Equipment Efficiency (OEE) of the installed production capacity and by using Si and non-Si materials more efficiently.
- Introduce specialized module products for different market applications (i.e. tradeoff between cost-optimized, highest volume products and higher price fully customized niche products).
- Improve module power/cell efficiency without significantly increasing processing costs.

The latter implies that efficiency improvements need to be implemented with lean processes that require minimum investment in new tool sets, including the extension of the service life of depreciated tool sets in order to avoid a significant increase in depreciation costs.
It will remain difficult to introduce new, immature technologies that do not show reductions of the cost per Wp from the beginning. Nevertheless the Toprunner Program in China will motivate to follow this track [15].

5. Results of 2018

5.1. Materials

5.1.1. Materials – crystallization and wafering

With ≈25% price share poly-Si remains the most expensive material of a c-Si solar cell as discussed in 4. The Siemens and the FBR (Fluidized Bed Reactor) processes remain the main technologies to produce poly-Si. Despite FBR processing is consuming less electricity it is assumed that its share will not increase significantly against the well matured Siemens processing. Other technologies like umg-Si or direct wafering technologies are not expected to yield significant cost advantages compared to conventional poly-Si technologies over the coming years but are expected to stay available in the market.

The landscape in wafering technology changed completely during the last years. The introduction of diamond wire sawing (DWS) was a significant improvement in terms of wafering process stability and cost reductions. The predicted change from slurry-based wafering to diamond wire-based wafering was finished in 2018 for mono-Si and for mc-Si.

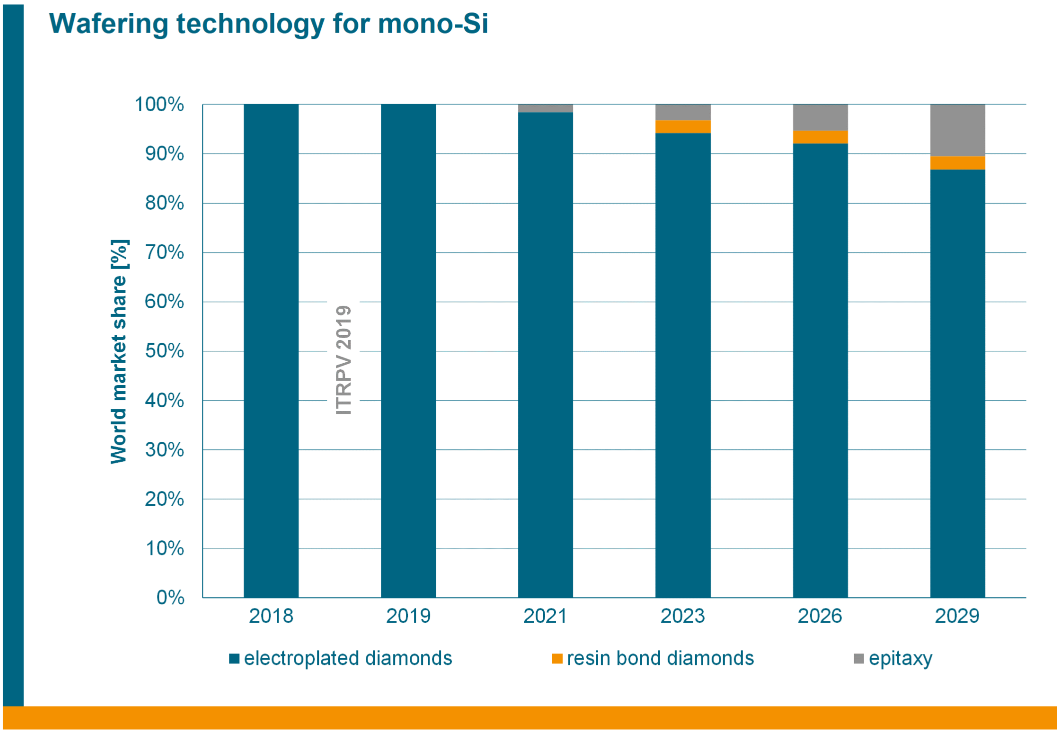

Fig. 3: Market share of technologies for mono-Si wafer manufacturing.

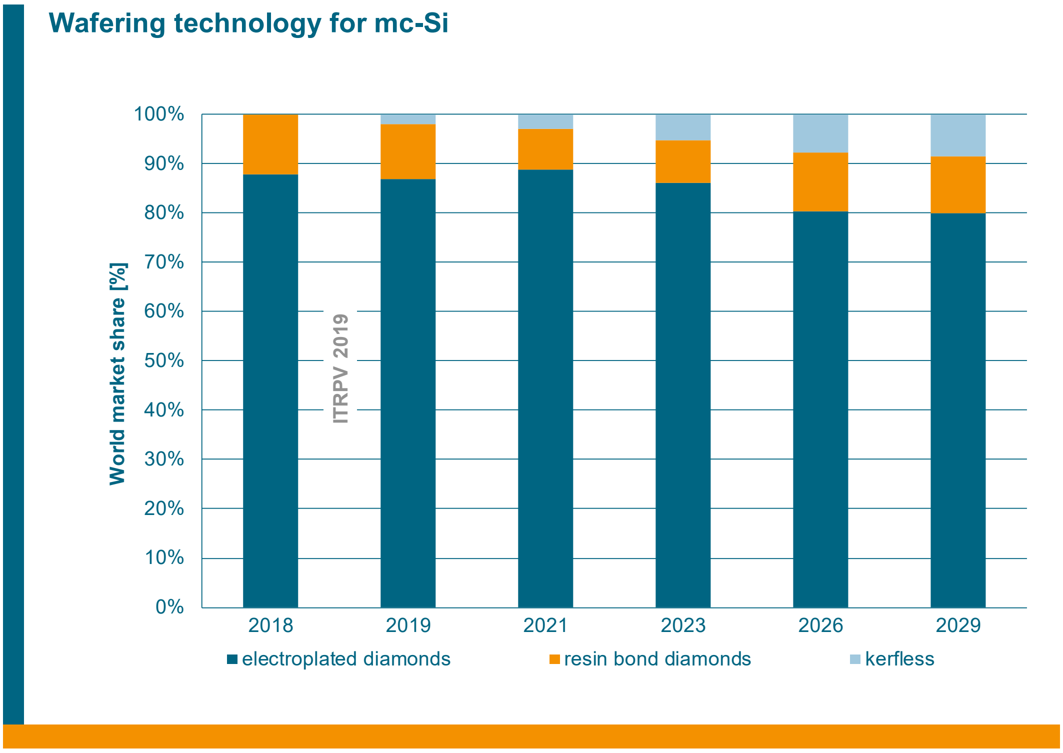

Fig. 4: Market share of technologies for mc-Si wafer manufacturing.

Fig. 3 shows that the switch to DWS was completed in 2018 for mono Si wafering. As new technology epitaxy is expected to appear in mass production from 2021 onwards.

Fig. 4 reveals that DWS is the only wafering technology also for mc-Si wafering. This change was supported by the fast introduction of wet chemical texturing methods for DWS mc-Si as will be discussed in 5.2.2. Electroplated diamond wire is considered as the dominating wire material. We do not expect that other kerf less wafer manufacturing techniques, especially kerf less technologies, will gain significant market shares, mainly due to the maturity of the DWS.

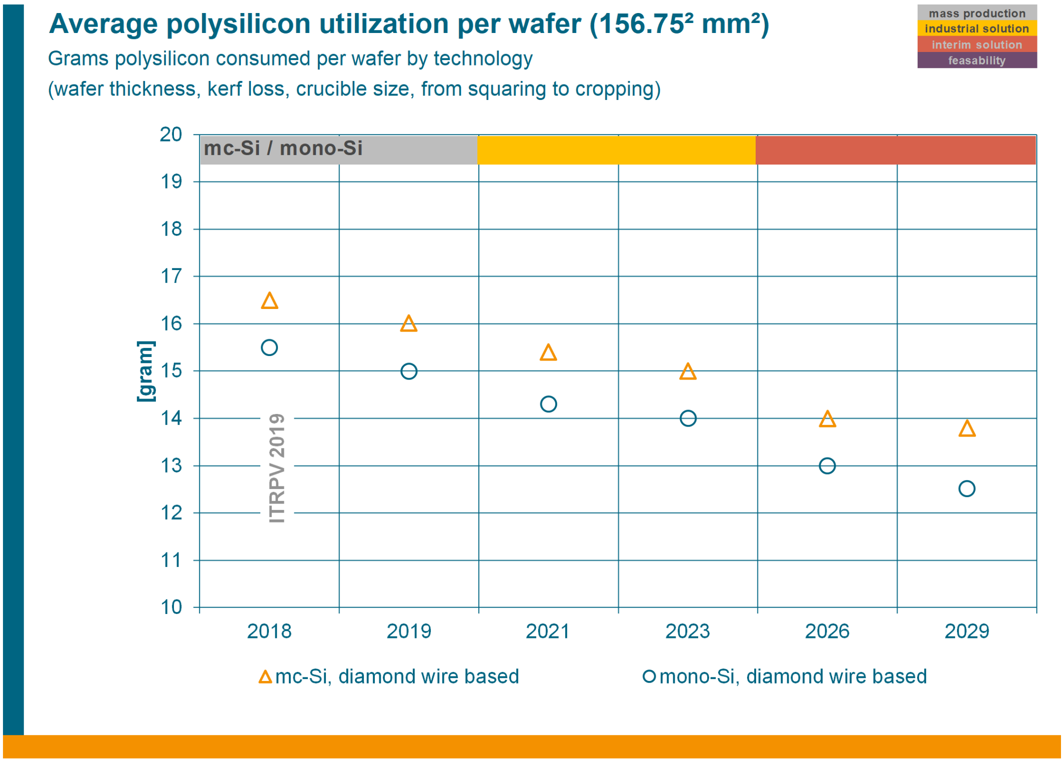

Fig. 5: Average poly-Si consumption for mc-Si and mono wafers with diamond wafer sawing technology.

Producing thinner wafers, reducing kerf loss, increasing recycling rates, and reducing the cost of consumables, can yield savings. Wire diameters will be reduced continuously over the next few years and there will be more recycling of Si and diamond wire over the next years.

Fig. 5 shows the average utilization of poly-Si to produce silicon wafers. The weight of a 180 µm M2 156.75 mm x 156.75 mm mono-Si or mc-Si wafer is about 10 g. Up to 165% poly-Si was used in 2018 to produce a standard M2 wafer. Mono-Si wafers consume about 7% less poly-Si than mc-Si wafers. It is assumed that the poly-Si usage will be improved further during the next years. The yellow color marking for 2021 and 2023 indicates that industrial solutions exist today to reach 15 g for mc-Si wafers and 14g for mono-Si wafers respectively.

5.1.2. Materials – cell processing

Si wafers account for approximately 52% of today's cell price, as shown in Fig. 2. Reducing the as-cut wafer thickness will lead to more efficient use of silicon. The developments anticipated in previous editions of the roadmap did not materialize. A thickness of 180 µm is still preferred for mc-Si and mono-BSF as shown in Fig. 6a. Nevertheless, we see that mono-Si wafers used in contemporary cell and module production lines for PERx cells have an as-cut thickness of about 170 µm, it is assumed that the thickness of mc-Si wafers will slowly approach a minimum value between 160 and 150 µm until 2026. Mono-Si wafer thickness will follow a reduction down to 140 µm in 2029 for PERx wafers.

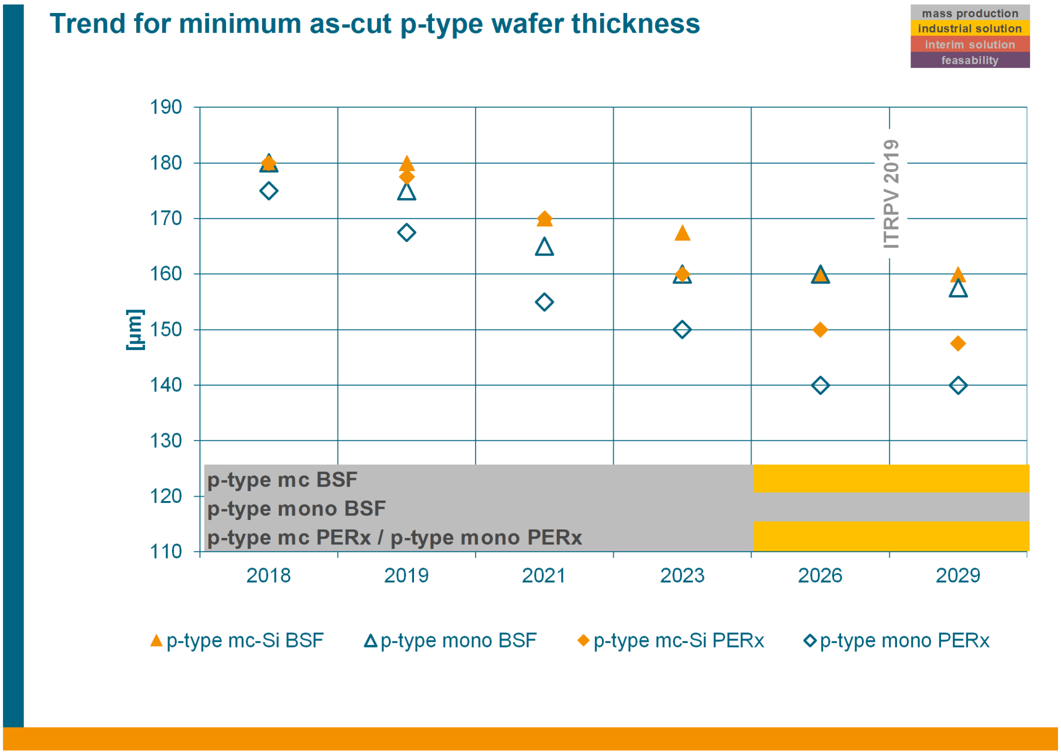

Fig. 6a: Predicted trend for minimum as-cut wafer thickness p-type c-Si solar cell concepts.

The color marking in Fig. 6a indicates that the thickness reduction for p type may be realized even faster as industrial solutions have been known.

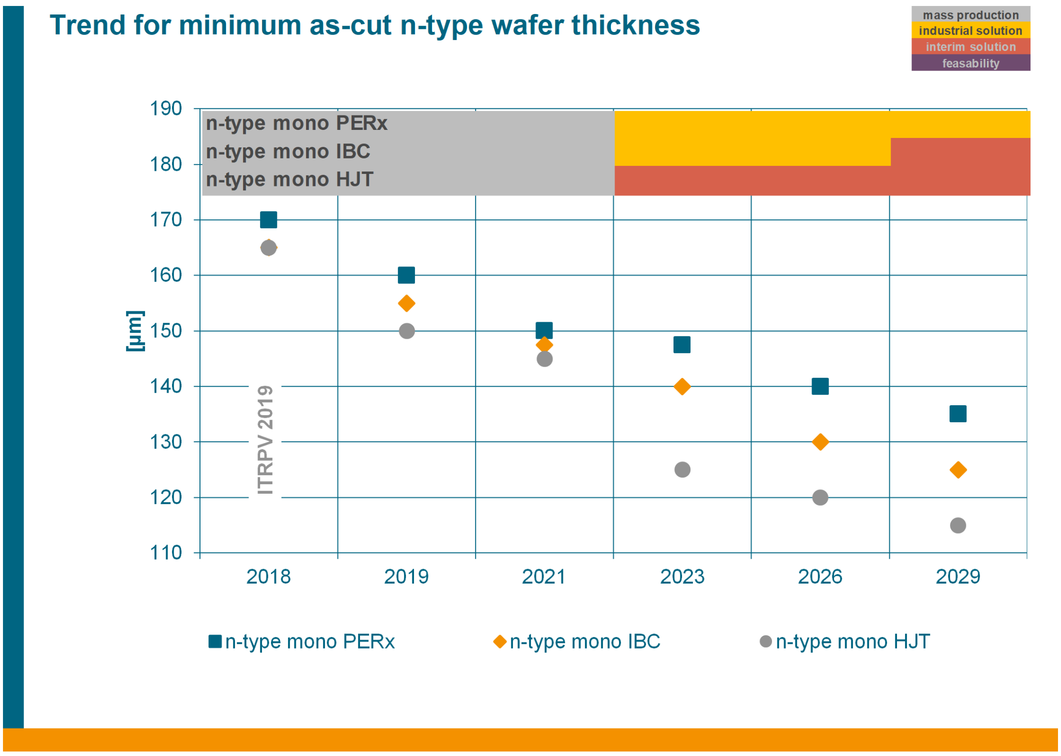

Fig. 6b: Predicted trend for minimum as-cut wafer thickness n-type c-Si solar cell concepts.

Fig. 6b shows the predicted trend of as cut wafer thickness for n-type wafers. Current thickness is around 170 µm with a much faster reduction trend to below 120 µm for HJT cell concepts and 130 µm for IBC cells. N-Type PERx cells follow a similar trend then p-type cells. Nevertheless, going below 130 µm requires further development as only interim industrial solution has been known so far.

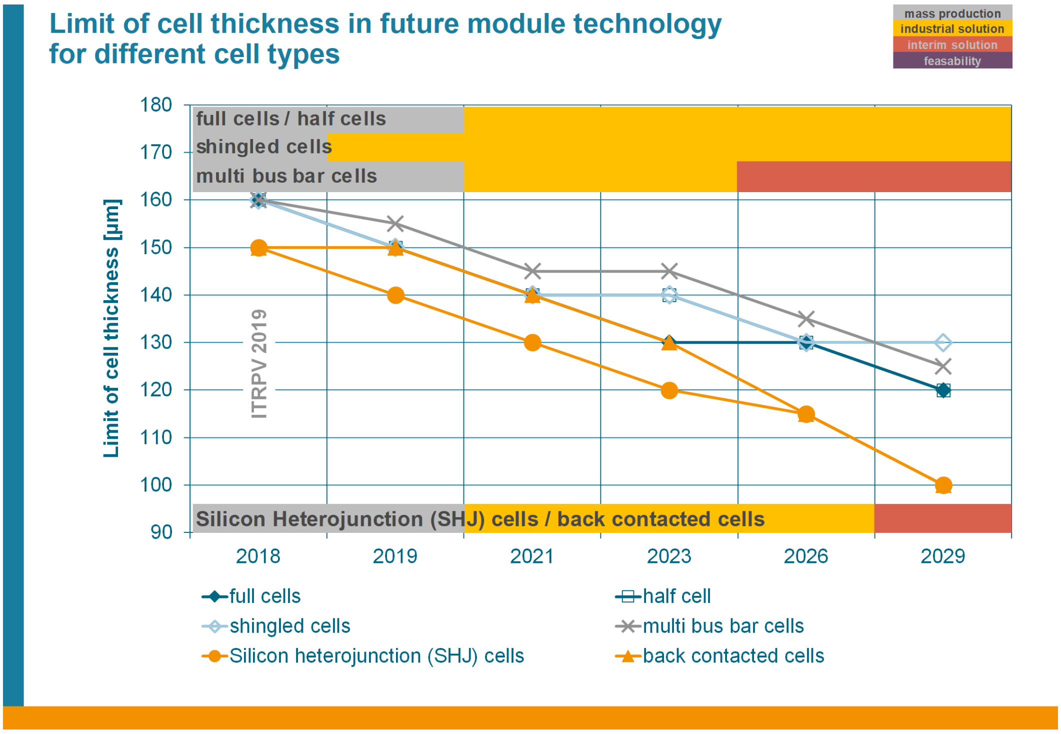

Fig. 7: Predicted trend of cell thickness in different module technologies.

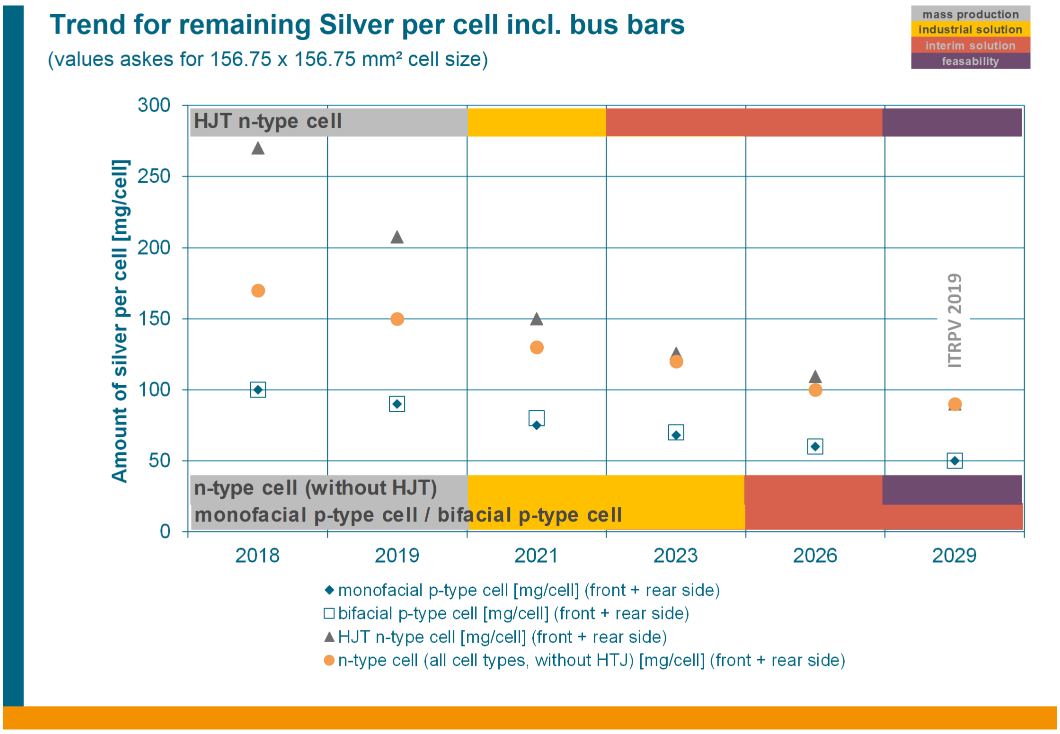

Fig. 8a: Trend for remaining Silver per cell for different cell concepts (156.75 x 156.75 mm²).

The corresponding cell thickness limit trend in module technology is shown in Fig. 7. Module technology appears to be ready for thinner cell types. Module technology will follow the cell reduction requirements as indicated by the color marking. Further development is required multi bus bar cell concept-based module technologies.

Metallization pastes/inks containing silver (Ag) and aluminum (Al) are the most process-critical and most expensive non-silicon materials used in current c-Si cell technologies. Paste consumption therefore needs to be reduced. Fig. 8a shows our estimations regarding the future reduction of the silver that remains on 156.75 x 156.75 mm² cells of different p- and n-type cell concepts after processing. N-type cell concepts using busbars show a significant higher silver consumption than p-type cells. Bi facial concepts show no difference in Silver consumption. Industrial solutions to meet the required thickness reductions are available for p- type concepts to reach laydowns below 80mg and for n- type concepts to go below 130 mg. Further development is required for lower lay downs and HJT asks for industrial solutions to go even below 150mg as indicated by the red marking.

The reduction of remaining silver per cell is expected to continue during the next years. The current study found 100 mg as the median value for 2018 and 90 mg for 2019 – again slightly above the estimation in the last edition. A reduction down to 50 mg per cell is expected to be possible by 2029 – also more conservative then in last year's survey. New developments in pastes and screens will enable this reduction, and this clearly shows the reaction of suppliers to the needs of cell manufacturers. The average silver price of 500 US$/kg beginning of February 2019 [16] results in costs of 4.5 US$ cents/cell (0.85 US$ cents/Wp, for a 21.5% mono PERC cell), or about 13.6% of the non-Si cell price, discussed in 4.

Because silver will remain expensive due to the world market dependency, it is extremely important to continue all efforts to lower silver consumption as a means of achieving further cost reductions.

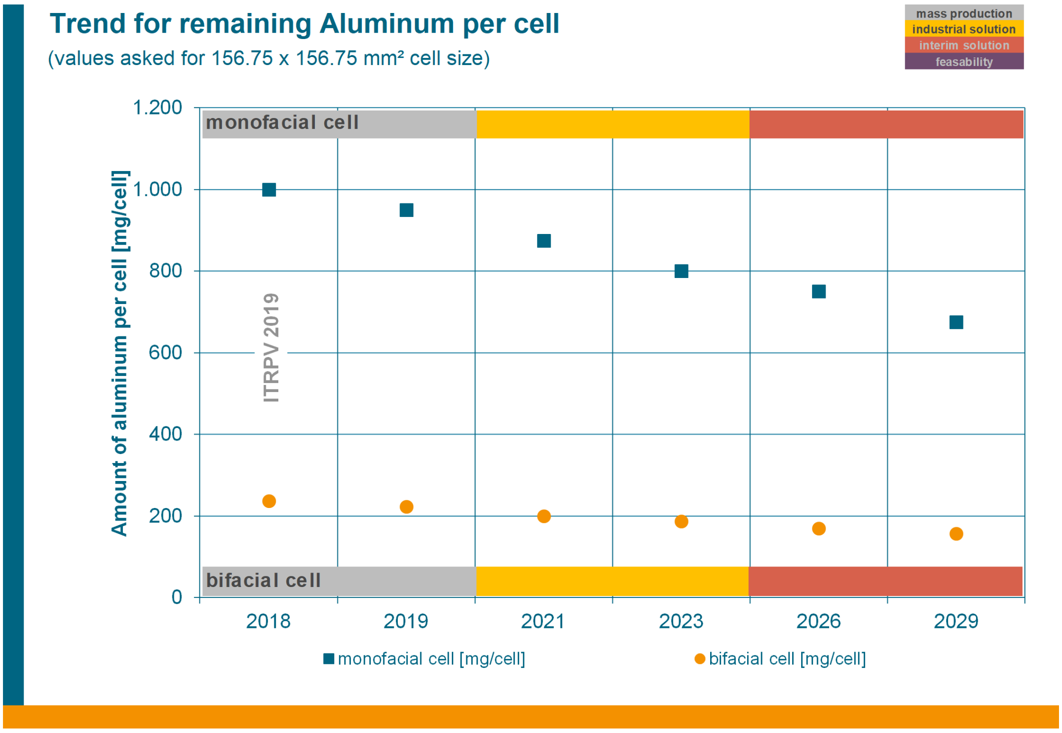

Fig. 8b: Trend for remaining Aluminum per cell for monofacial and bifacial PERC concepts (156.75 x 156.75 mm²).

Despite a continuous reduction of silver consumption at the cell manufacturing level, silver replacement is still considered as we will discuss in chapter 5.2.2. Copper (Cu), as less expensive material, applied with plating technologies, is the envisioned substitute. It is still assumed that it will be introduced in mass production, but the market share is considered more conservative than in the last edition with a market share of ≈10% in 2029 – a further delay versus former ITRPV expectations. Technical issues related to reliability and adhesion have to be resolved before alternative metallization techniques can be introduced. Appropriate equipment and processes also need to be made ready for mass production. Silver is expected to remain the most widely used front side metallization material for c-Si cells in the years to come.

The trend of remaining Aluminum is shown in Fig. 8b. We distinguish in this figure between bifacial and monofacial cell concepts using BSF or PERC technologies. Bifacial cells need much less Al – only about 22% of the corresponding monofacial cell type. The reduction is assumed to reach down to 650 mg for monofacial and 180 mg for bifacial cell concepts respectively. A faster reduction down to 800 mg for monofacial cells and down to 200 mg for bifacial cells respectively seems possible as industrial solutions exist, following the roadmap further down requires development efforts.

Pastes containing lead are restricted in accordance with legislation that went into effect in 2011 under the EU Directive on the Restriction of Use of Hazardous Substances (RoHS 2). This restriction affects the use of lead and other substances in electric and electronic equipment (EEE) on the EU market. It also applies to components used in equipment that falls within the scope of the Directive. PV panels are excluded from RoHS 2, meaning that they may contain lead and do not have to comply with the maximum weight concentration thresholds set out in the directive[1]. PV's exclusion from the

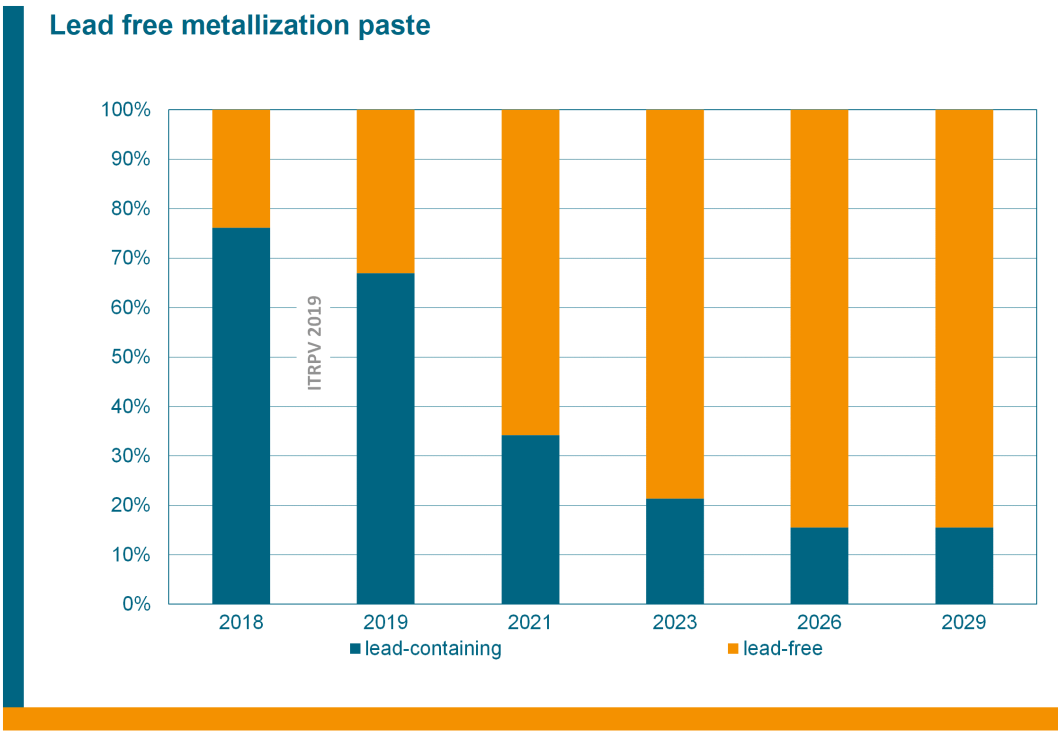

Fig. 9: Trend for implementation of lead free pastes in different cell technologies.

[1] Article 2(i) of the RoHS Directive [2011/65/EU] excludes from the scope of the Directive "photovoltaic panels intended to be used in a system that is designed, assembled and installed by professionals for permanent use at a defined location to produce energy from solar light for public, commercial, industrial and residential applications."

directive will remain in effect for the next few years — a review of RoHS 2 will likely take place by mid-2021 at the latest[2]. Cell manufacturers should act carefully, especially, as the exclusion in question is limited to PV panels installed in a defined location for permanent use (i.e. power plants, rooftops, building integration etc.). Should the component in question also be useable in other equipment that is not excluded from RoHS 2 (e.g. to charge calculators), then the component must comply with the Directive's provisions.

We anticipate lead free pastes to become widely used in the mass production of c-Si cells in 2019/2020. Fig. 9 shows that during the next years the cells will become more and more lead free.

5.1.3. Materials – modules

Module add-on costs are clearly dominated by material costs. Improvements in module performance as shown in Section 5.3 and reductions in material costs are therefore required if module add-on costs should be reduced. Approaches for increasing performance include the reduction of optical losses (e.g. reflection of front cover glass) and the reduction of interconnector losses. Approaches for reducing material costs include:

- Reducing material volume, e.g. material thickness.
- Replacing (substituting) expensive materials.
- Reducing waste of material.

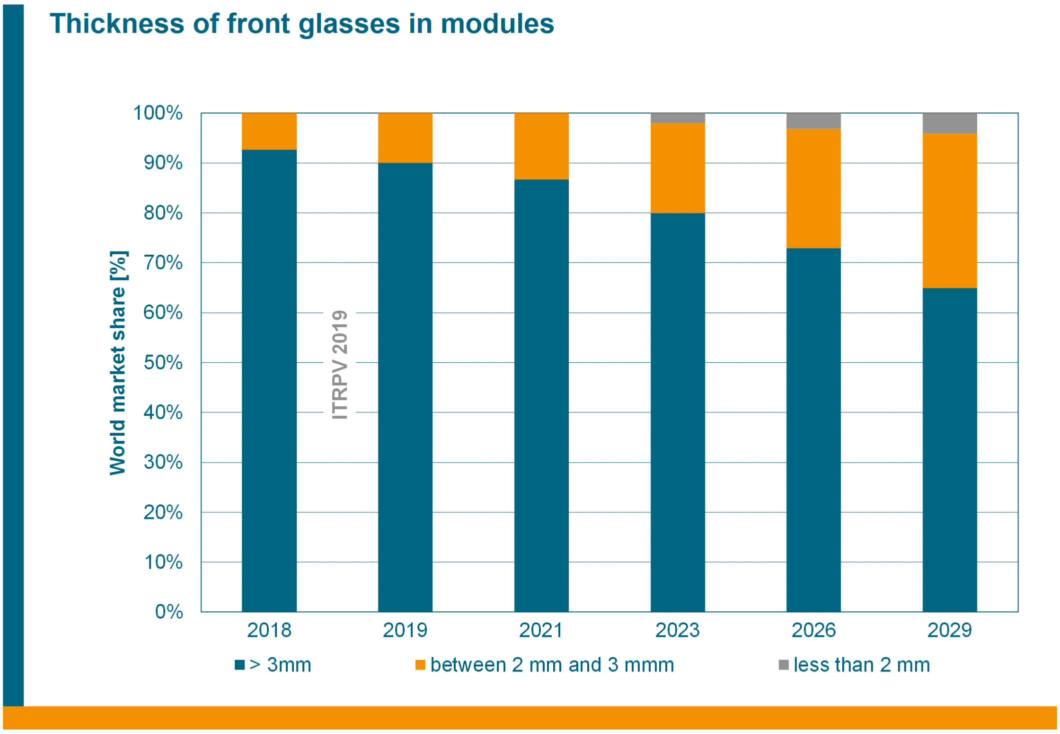

Fig. 10: Expected trend of front side glass for c-Si modules.

[2] Article 24 of the RoHS Directive [2011/65/EU] requires an evaluation and possible revision of the Directive, including its scope, by July 22, 2021.

The most important material of a module is the front side glass. It mainly determines weight and light transmission properties. The thickness is also important regarding mechanical stability.

Fig. 10 summarizes the expected trend in front side glass thickness. It is expected that a reduction to 2 mm thickness will appear over the next years. A thickness below 2 mm is not expected to have significant market share.

The use of antireflective (AR) coatings has become common to improve the transmission of the front cover glass. AR-coated glass will remain the dominant front cover material for c-Si PV modules in the future, with market shares well above 90%.

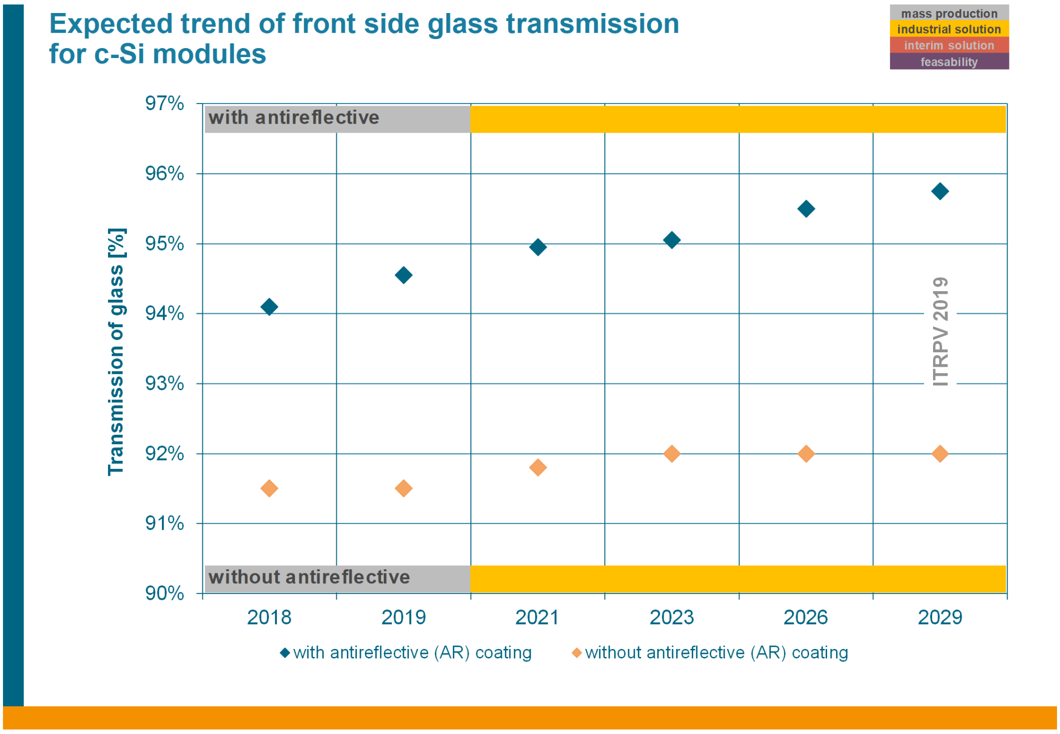

Fig. 11: Expected trend of front side glass transmission for c-Si modules.

Since AR-coated glass will be the most commonly used front cover, it is important that the AR coating remains effective and stable under various outdoor conditions during the entire lifecycle of the module. All AR-coatings on the market meet an average lifetime of at least 15 years, and, there is a clear trend indicating that the average service life of these coatings will improve over the next years.
The transmission of AR coated glasses appears to be today around 94% - 3% higher than for non-coated glasses. A continuous improvement of the glass is expected to reach up to 95% transmission within the next 10 years as shown in Fig 11.

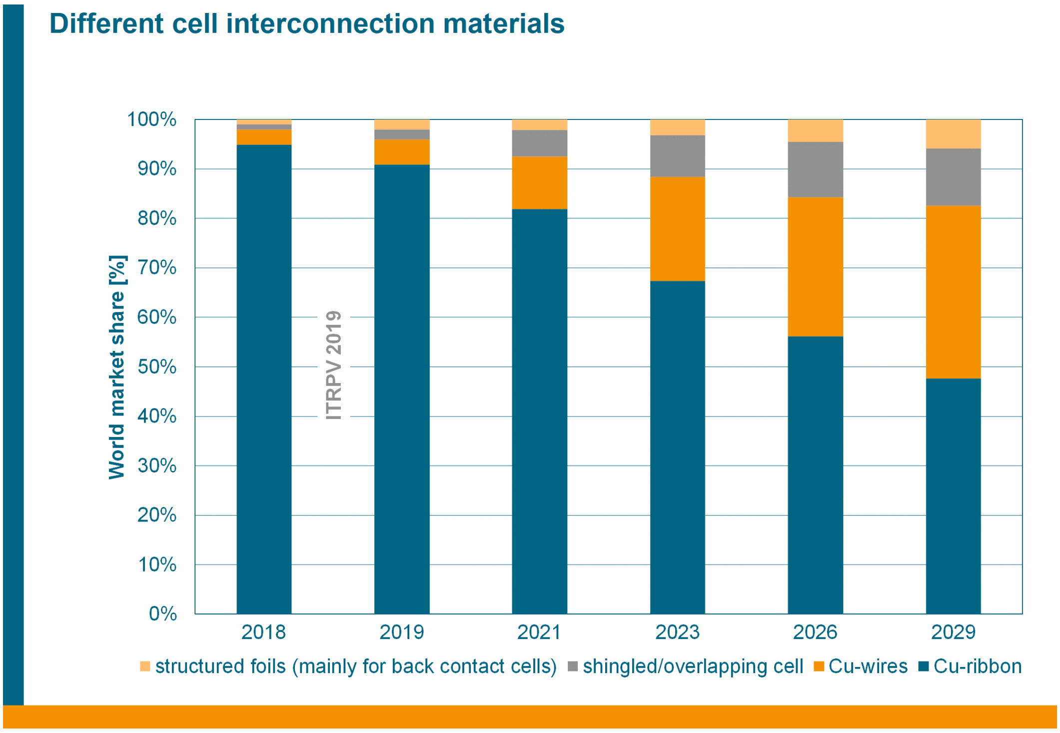

Fig. 13: Expected market shares for different cell interconnection materials.

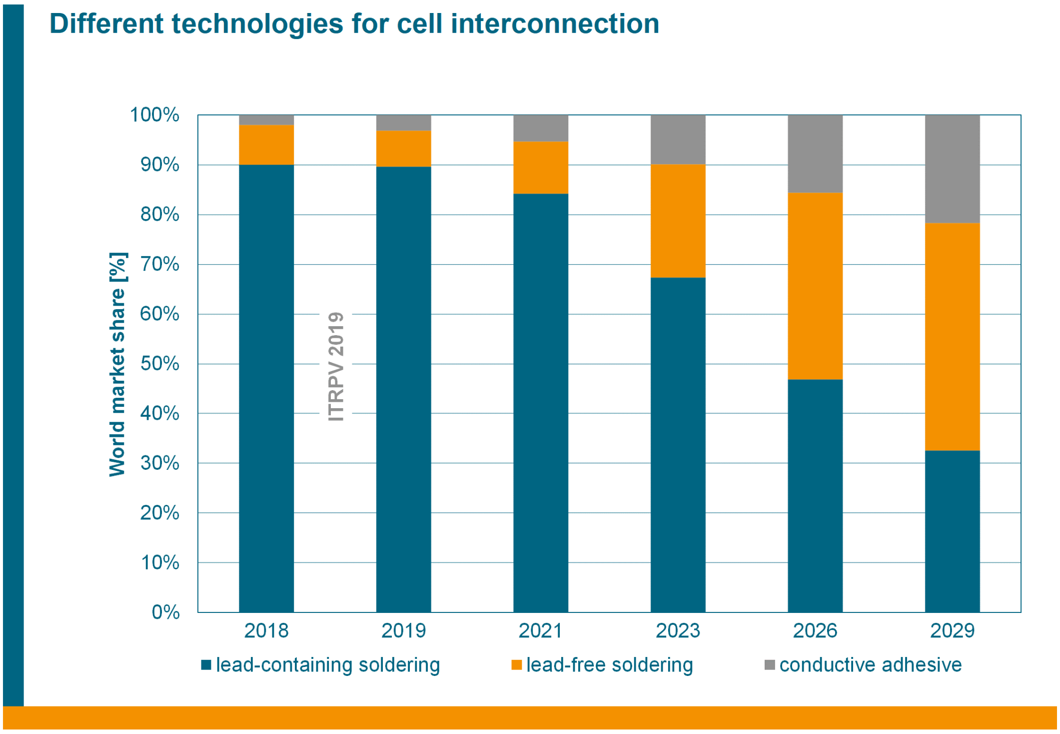

Fig. 12: Expected market shares for different cell interconnection technologies.

Today, solders that contain lead are the standard interconnection technology for solar cells in module manufacturing. Due to environmental and other considerations as discussed in chapter 5.1.2, more and more PV manufacturers are striving towards lead-free alternatives, as can be seen in Fig. 12.

With regard to the interconnector material, copper ribbons will remain the dominating material as shown in Fig. 13. Copper-wires are expected to gain over 30% market share during the next decade.

Structured foils mainly used as an interconnection of back contact cells are expected to stay at a market share of <8% while shingled or overlapping cell interconnection technology might gain a market share of up to 10% until 2029.

It is important to note that the upcoming interconnection technologies will need to be compatible with the ever-thinner wafers that will be used in the future. In this respect, low-temperature approaches using conductive adhesives or wire-based connections have an inherent advantage due to the lower thermal stresses associated with them.

Similar to the cell interconnection we find a clear trend towards lead-free module interconnection covering all interconnections between the cell strings and the junction box, as shown in Fig. 14. Conductive adhesives and lead-free interconnects are expected to become dominating alternatives to currently used lead containing technologies.

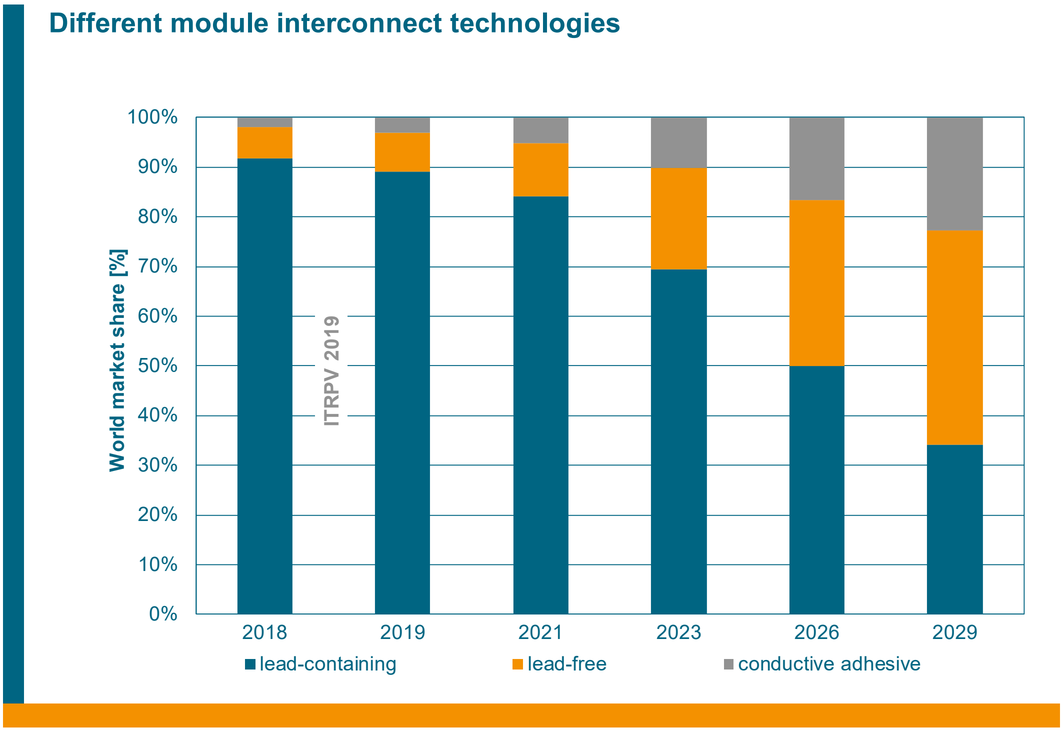

Fig. 14: Expected market share of different module interconnection material.

The encapsulation material and the back sheet are key module components. Both are also major cost contributors in module manufacturing. Intensive development efforts have been made to reduce the cost of these materials.

At the same time maintaining or even improving the properties of this key components is mandatory to ensure the module service lifetime. This has led to a trend toward new materials, as shown in Fig. 15a for encapsulation materials. Polyolefins are an upcoming alternative with a predicted market share of up to 25% in 2029. However, it is also assumed that EVA will remain the dominant encapsulant material with a market share well above 60% over the ten-year period of this survey.

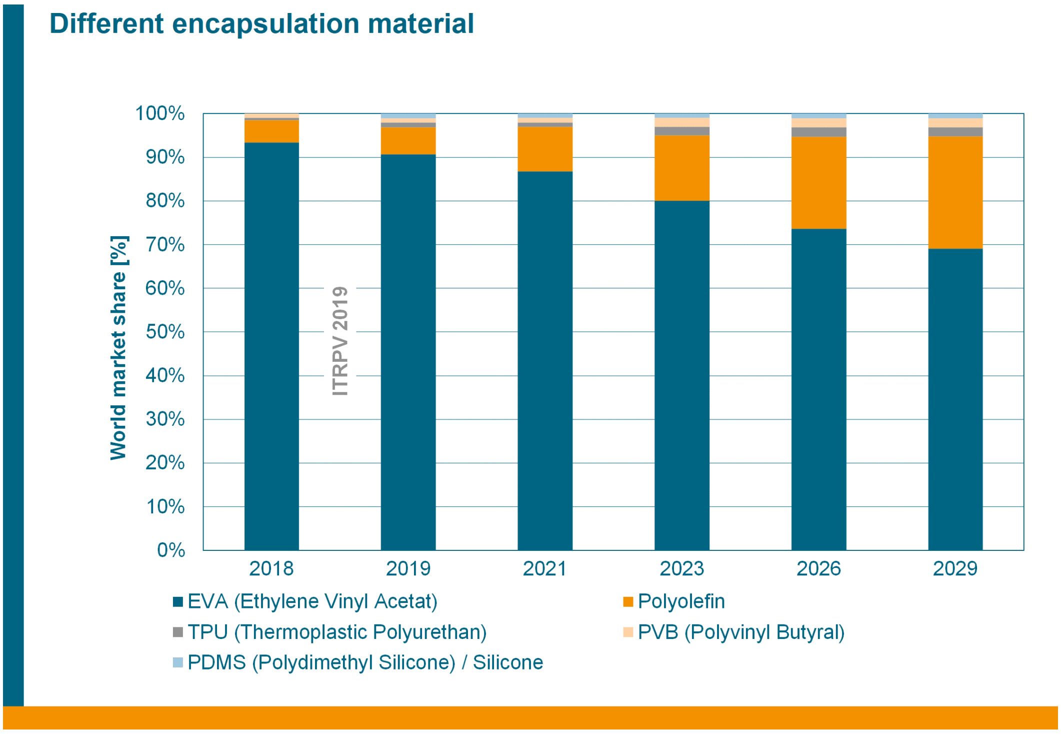

Fig. 15a: Expected market shares for different encapsulation materials.

Fig. 15b shows the expected trend in thickness of the different encapsulant materials. We see a clear trend to a considerable thickness reduction by up to 25% within the next 10 years.

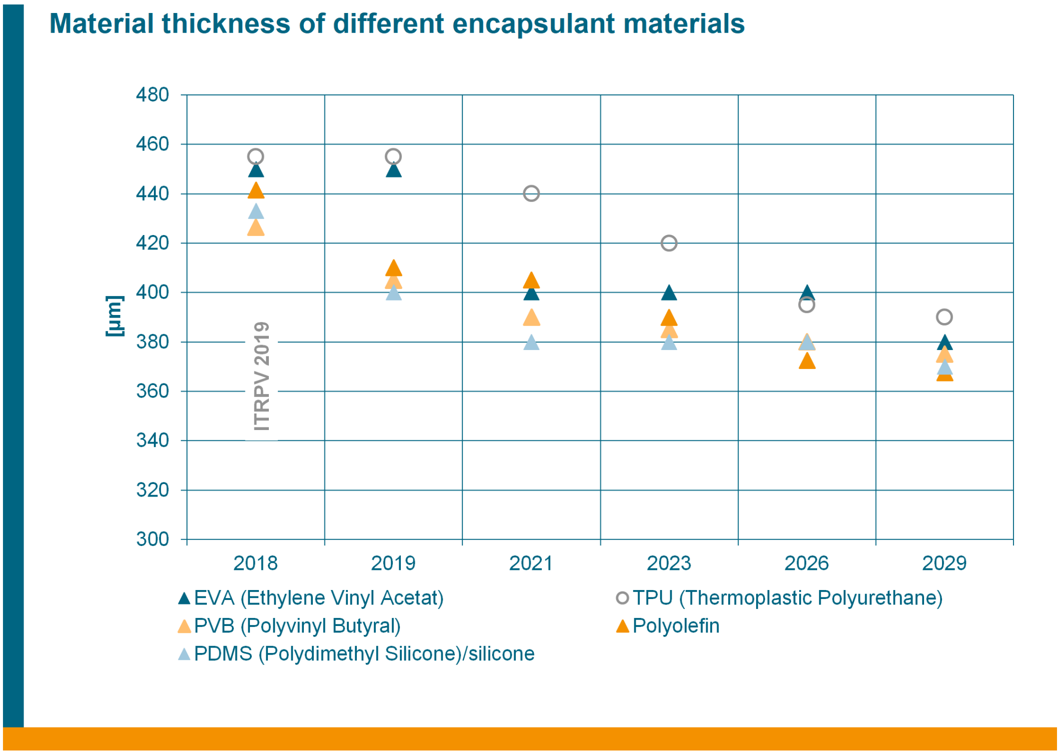

Fig. 15b: Expected thickness reduction trend for different encapsulant materials.

As can be seen in Fig. 16, foils will stay mainstream as back cover material, but glass is expected to gain a significant higher market share as backside cover material for c-Si modules over the next decade and increase its market share from 6% in 2018 to above 30% in 2029. If bifacial cell concepts will fast gain market share this share would increase.

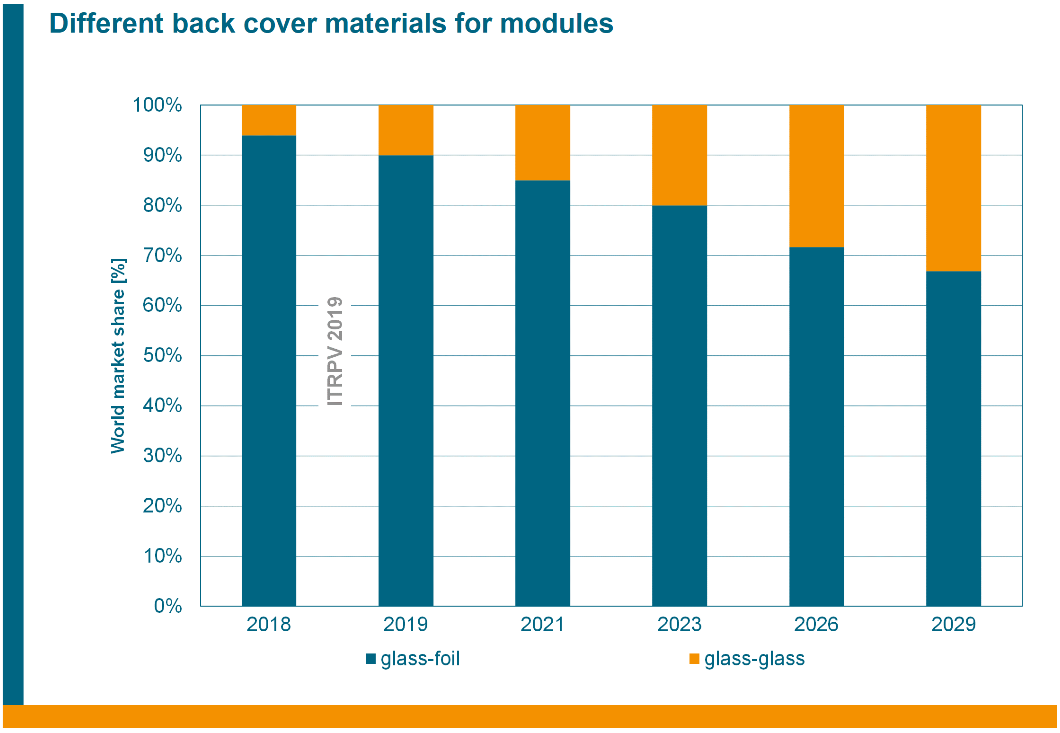

Fig. 16a: Share of glass-foil and glass-glass as back cover technologies.

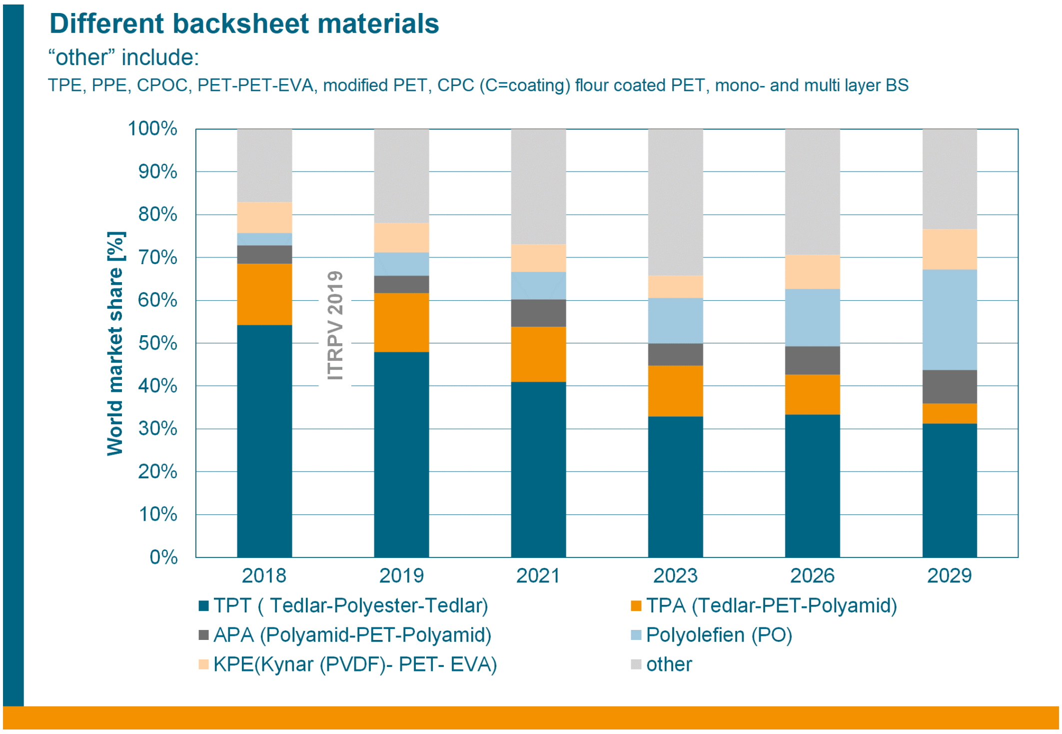

Fig. 16b: Back cover foil materials trend: "others" include TPE, PPE, CPOC, PET-PET-EVA, modified PET, CPC (C=coating) flour coated PET, mono- and multi layer BS.

The thickness of the back glass is expected to stay in the range between 2 mm and 3 mm in the mainstream.

The expected share of different back cover foils is summarized in Fig. 16b. Tedlar based foils, mainstream today, are expected to lose market share while a lot of new materials are expected to appear. We do not see a clear new mainstream material but a trend towards new alternatives for TPT and TPA.

The mainstream color of the backsheet foils will stay white. Black colored backsheets will stay a niche application whereas transparent backsheets are considered as an upcoming trend – especially for bifacial cell applications.

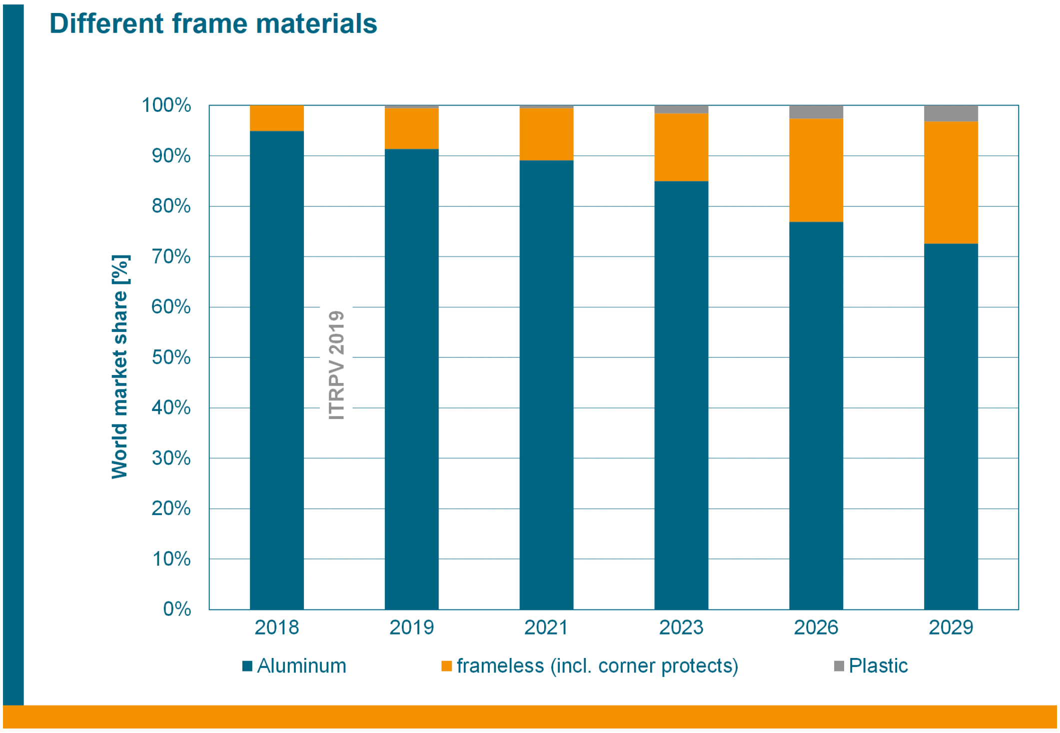

Fig. 17: Expected market shares for frame materials.

Fig. 17 shows the trends of different frame materials. Currently modules with aluminum frames are clearly dominating the market.

Frameless modules are expected to increase its market share to above 20% in 2028. Plastics are considered as niche application with market shares of <2%. In order to maintain quality (for thinner cells as well), the solar cells used for module assembly should be free of micro cracks. The contributing companies are considering testing all the products during the manufacturing process with EL inspection as standard. Among other things, the contributors consider Potential Induced Degradation (PID)-resistant cell and module concepts also as market standard.

Higher level of stress testing for PID is still common. Many test labs employ test conditions beyond the minimum levels described in IEC TS 62804. Currently IEC TC82 is working on a next edition of IEC 61215 which will likely include testing for PID. The test conditions are still under discussion. At the same time, there has been no industry-wide accepted and applied definition of micro-cracks.

5.2. Processes

5.2.1. Processes – manufacturing

It is possible to increase the throughput of the crystallization process by changing the common sizes of the ingots. Fig. 18 shows the increase in ingot mass for casted silicon materials and for Czochralski/Continuous Czochralski (Cz/CCz) growth of mono-Si, as predicted by the roadmap. Gen6/7 ingoting is mainstream with ingot masses of 1100 kg in 2019. Starting in 2021, the transition to Gen8 will be executed, by realizing ingoting with masses of up to 1300 kg in 2026. Casted ingot mass will increase further towards 1500 kg and will mark the move to Gen8+ after 2026. But transition to Gen9 in mass production may go even faster but requires further development work as indicated by the red color marking.

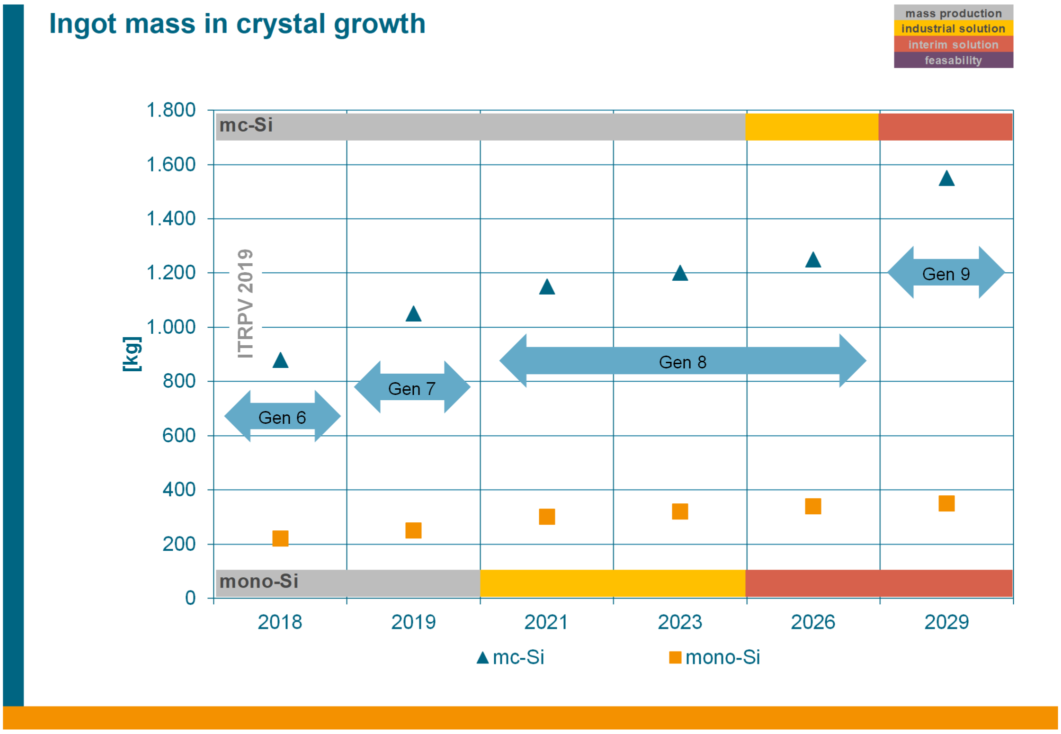

Fig. 18: Predicted trend for ingot mass for mc-Si and for mono-Si.

The ingot mass of mono is expected to increase within the next 10 years. CCz is expected to have a considerable increase in market share over classical Cz and is assumed to become mainstream after 2023. Going beyond will not be possible right now as indicated by the red color marking for ingot mass above 270kg.

For the first time we asked about the power consumption of crystal growth. Fig 19 shows that mono ingot growth consumes about 5 times more energy per kg than mc-Si ingot growth. Consumption for mono crystallization is expected to be reduced over the coming years while mc-Si crystallization consumption is expected to stay at between 6 kWh/kg and 7 kWh/kg. Reduction to 25kWh/kg has not been ready soon for industrialization as indicated by the red color marking.

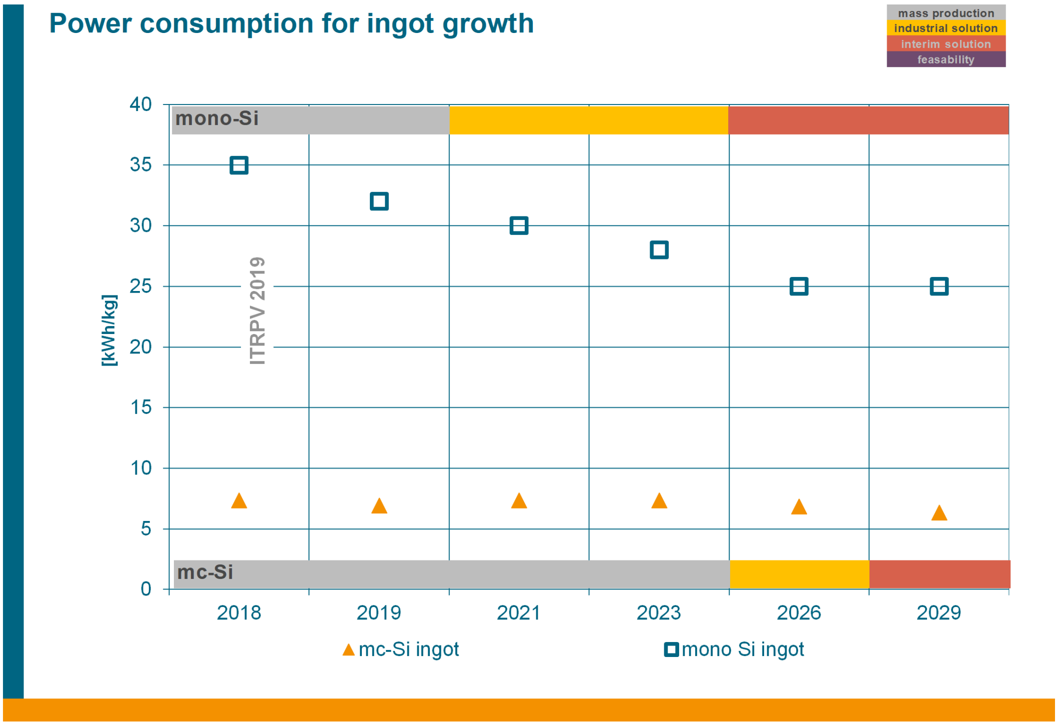

Fig. 19: Trend of power consumption for ingot growth.

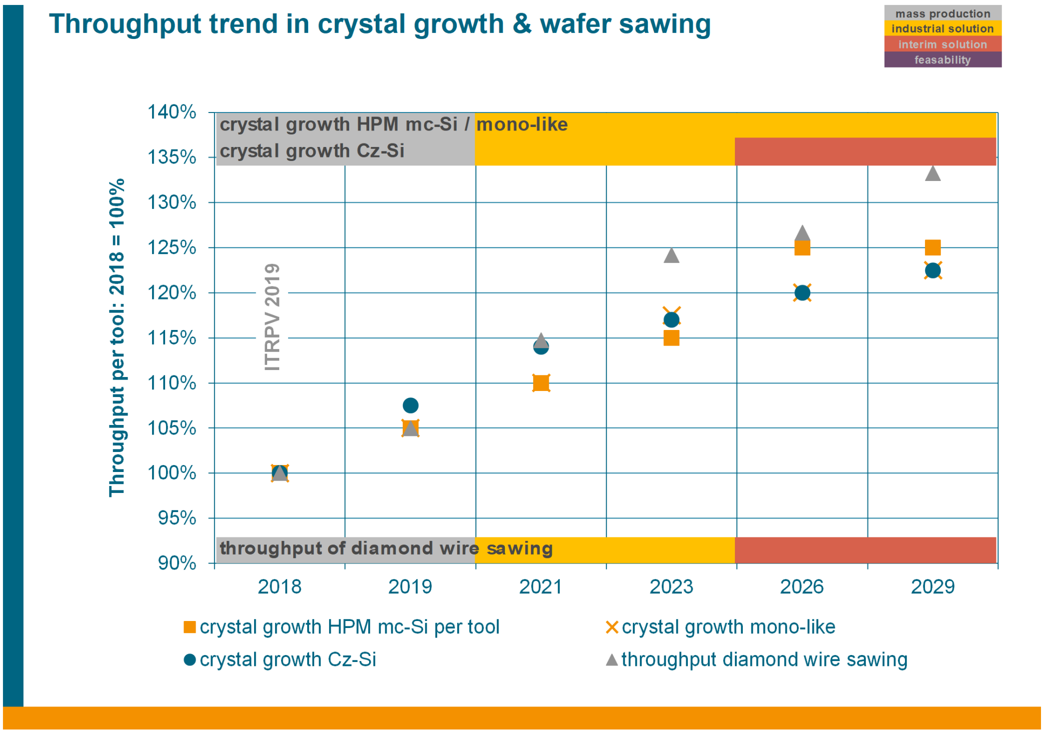

Fig. 20: Predicted trend for throughput per tool in crystal growth & wafer sawing technologies.

Fig. 20 summarizes the anticipated throughput developments of crystal growth and wafering technologies. The throughput of crystal growth for both types, casted and mono, will be continuously increased by up to 35% for casting and up to 20% for pullers over the next 10 years.

Casting throughput may increase faster as industrial solutions exist as shown while increasing of Cz growth speed to 120% and beyond needs further development as indicated by the red color marking. A similar trend is visible for wafering. Diamond wiring will increase the throughput above 130% within the next 10 years while industrial solutions have been ready only for a throughput increase close to 125% as indicated by the red color marking for a higher throughput increase.

Yield enhancement by reducing the kerf loss will further improve productivity in wafering on top of the effect of the increased throughput. This is important to improve the usage of poly-Si as discussed in 5.1.1. Fig. 21 describes the trend for kerf loss and for Total Thickness Variation (TTV). A kerf width of about 80 µm is standard in diamond wire-based sawing. It is predicted to decline to 60 µm until 2029. The realization of down to 70 µm may go faster as an industrial solution exist, indicated by the yellow marking. Reaching a Kerf loss of <63µm has not been ready yet. Today's TTV is 20 µm for it is expected to stay constant in the future.

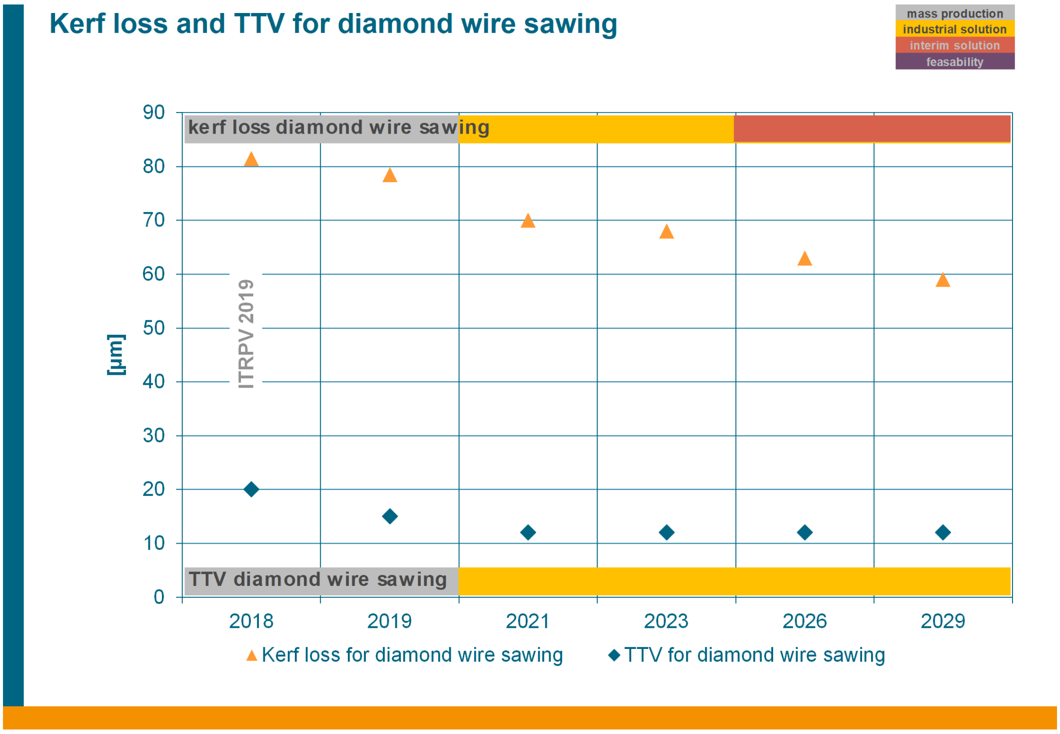

Fig. 21: Kerf loss and TTV (Total Thickness Variation).

Fig 22 shows the resulting cost reduction trends for the discussed crystallization and wafering technologies. All technologies are expected to realize about 25% cost reduction, this may be implemented much faster than predicted as industrial solutions have been available by today, indicated by the yellow color marking.

Optimizing productivity is essential to remain cost competitive. Increasing the throughput of the equipment in order to achieve maximum output is therefore a suitable way to reduce tool related costs per cell. In order to optimize the throughput in a cell production line, both, front-end (chemical and thermal processes) and back-end (metallization and classification) processes should have equal capacity.

Fig. 23a summarizes the expected throughput of cell production equipment, until 2029.

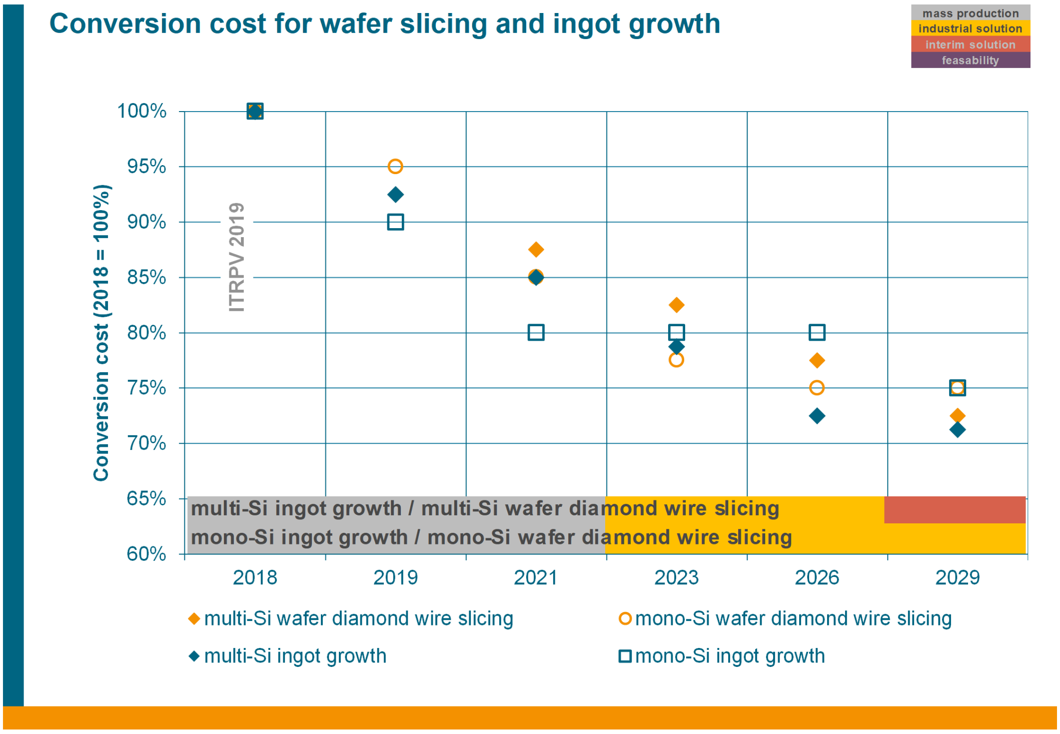

Fig. 22: Trend of conversion cost for crystallization and wafering technologies.

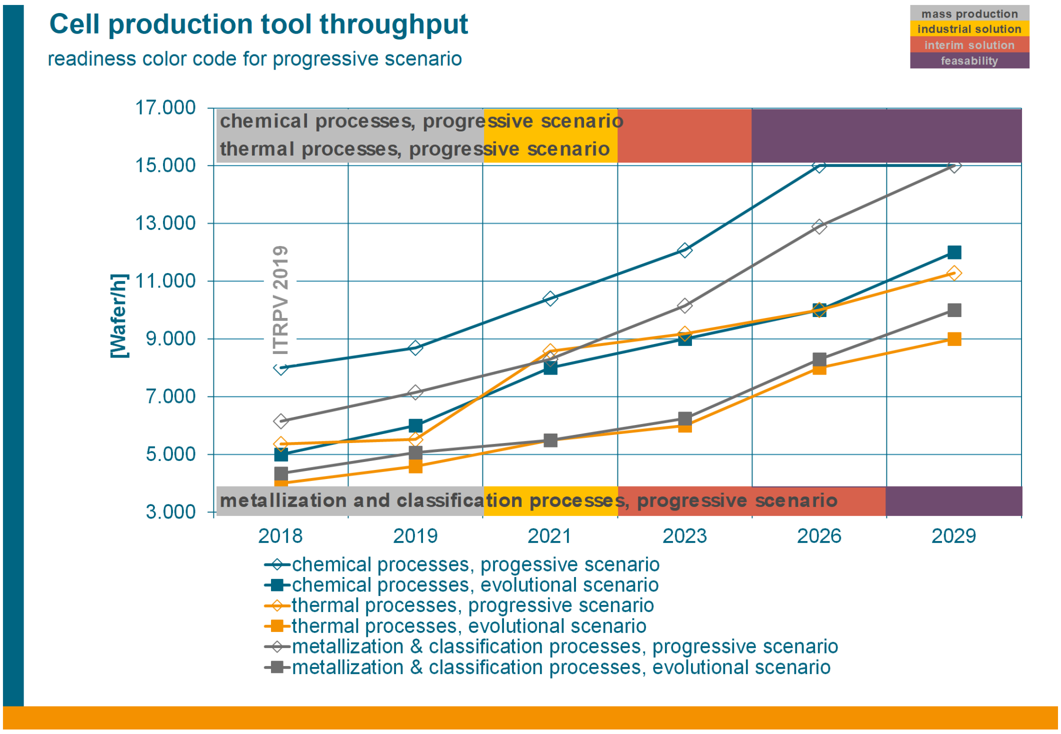

Fig. 23a: Predicted trend for throughput per tool cell production tools.

Two scenarios are considered for a discussion of this topic in more detail. The standard scenario reflects the evolutional optimization approach, which is suitable for batch as well as in-line equipment (the evolutionary scenario).

The progressive scenario also enables in-line or cluster line layouts but combines this with fairly new automation concepts and potentially higher process throughputs. Both scenarios are based on the achievement of substantial improvements through new tools, which are necessary to reduce depreciation and labor costs. More optimistic forecasts in previous editions have been offset by the current investment cycle. New “high throughput” equipment has been installed since 2016 on a large scale in mass production during the current investment cycle. Nevertheless, manufacturers are also working in existing lines on continuous process improvements by improving existing tool sets. In addition, the implementation of PERC process upgrades is also accompanied by implementing new machines.

Single tools with increased throughput in chemical and thermal processing can be implemented, especially in cluster lines as replacements or upgrades as for PERC. New lines will be equipped from the beginning with the new tool concepts that matured during the last years in newly built production lines.

Metallization tools with throughputs of >6.000 wafers/h are available on the market today. Further improvements in this field will depend strongly on the progress made with the screen printing technology that currently focuses on smaller line width and lower paste consumption. The color marking indicates that industrial solutions have been available today for up to 8000 wafers/h. Wet chemical processing is leading with 8.000 wafers/h today and is expected to continue leading the throughput per tool with up to 15.000 wafers/h by 2029 as well. A maximum of > 10.000 wafers/h is expected by 2023 for metallization and test equipment, but this will require significant engineering efforts as indicated by the color marking. Thermal processing is expected to somewhat lag in terms of throughput. So innovative equipment/process solutions for increased throughput in thermal processing are required.

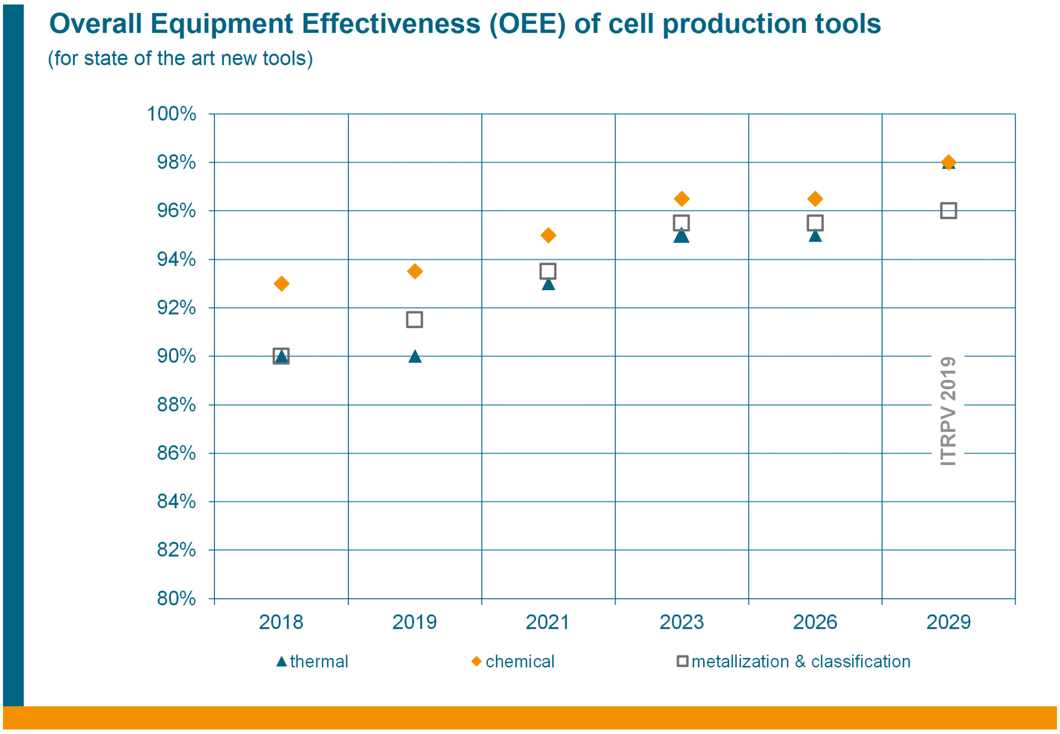

Fig. 23b: OEE trend of state of the art new cell tools in new production facilities.

Using the tools in an efficient way is mandatory to keep path with required cost reductions. Fig 23b summarizes the status of Overall Equipment Efficiency (OEE) according to SEMI E10 [17] in state of the art cell production facilities. Current values around 90% for backend and thermal have to be increased during the next years.

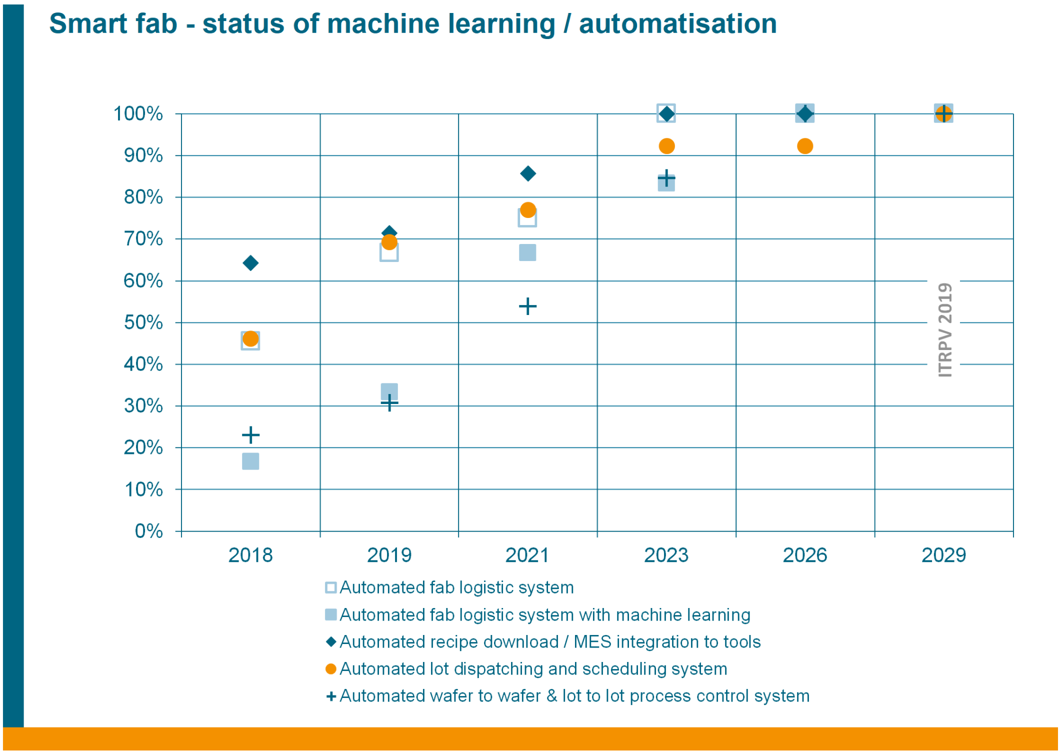

Fig. 23c: Machine learning status and implementation of MES outlook for new cell fabs.

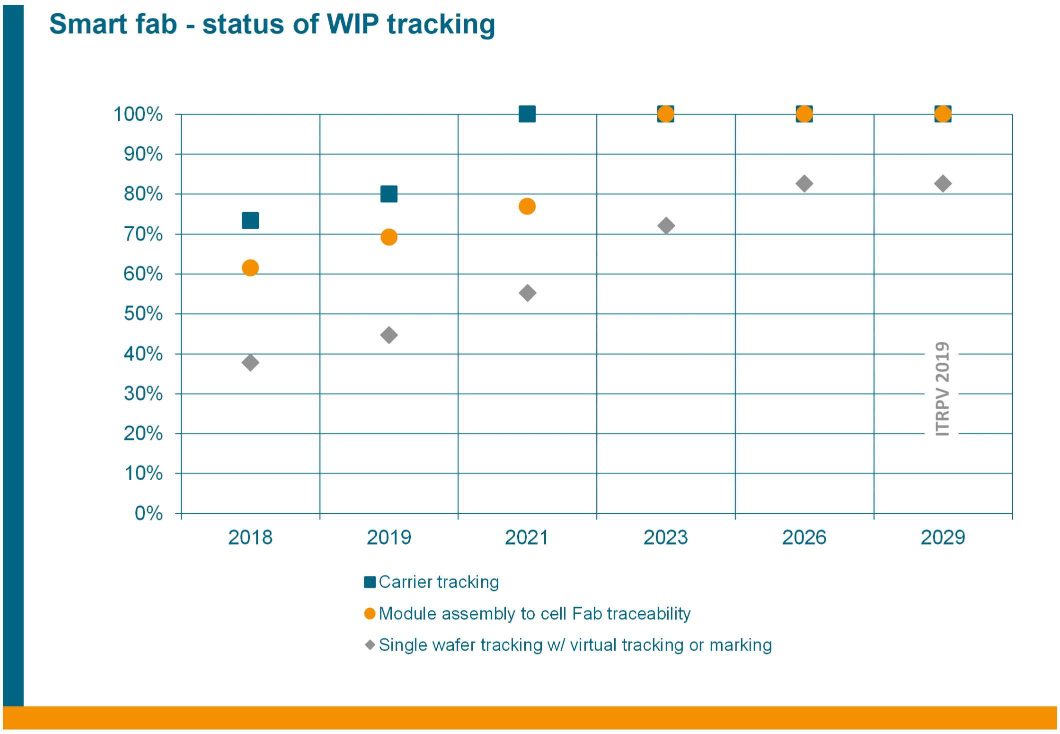

Fig. 23d: Status and trend of WIP tracking methods in state of the art cell and module production lines.

OEE Improvements will also be realized by improved tool and fab automation, automatic recipe downloads via integration of the tools into Manufacturing Execution Systems (MES) and automatic dispatching systems as well as automated wafer-to-wafer and lot-to-lot process control systems. Fig.23 c shows the status and an outlook about the machine learning and automation. Machine learning will be implemented not only at metallization and test but also in front-end machines within the next years.

Fig 23d shows the expected trend of measures regarding production tracking. It has to be emphasized that the tracking from cell to module manufacturing will increase to 100% within the next years.

Increasing the tool throughput is also a measure for manufacturing cost reduction in module manufacturing. The expected throughput trends of key equipment in module front end and back end are summarized in Fig. 24a and 24b. We expect a continuous throughput increase in the next years. Industrial solutions are available by today for a fast introduction also for multi bus bar product implementation as indicated by the yellow color marking.

In 2029 the throughput of stringing and lamination tools is expected to increase fast to up to 140% and by about 20% respectively of the 2018 values. Solutions are available for mass production and first industrial implementation as indicated by the color marking. In order to reduce the floor space and hence the cost of module manufacturing, the equipment should occupy less floor space and achieve higher throughput. This should be possible by combining continuous improvements and new developments, particularly for connection and encapsulation processes. For the latter process, new encapsulation materials with shorter processing times would be desirable. Stringing of multi bus bar and half cells will also require significant tool improvements.

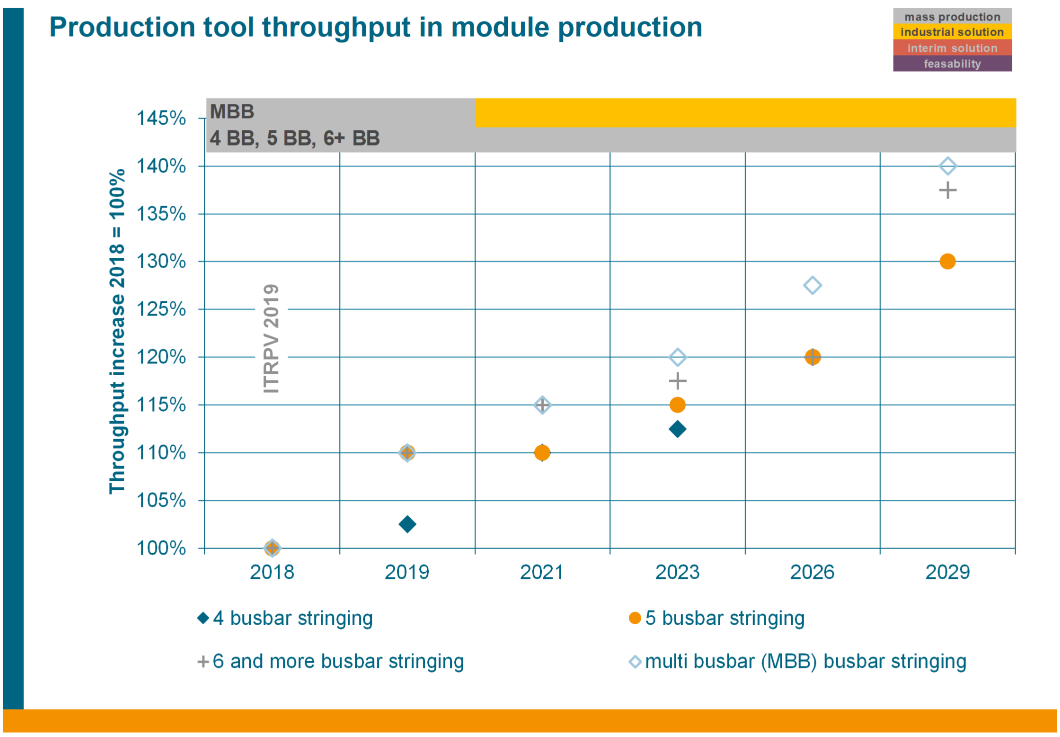

Fig. 24a: Trend of tool throughput in stringing.

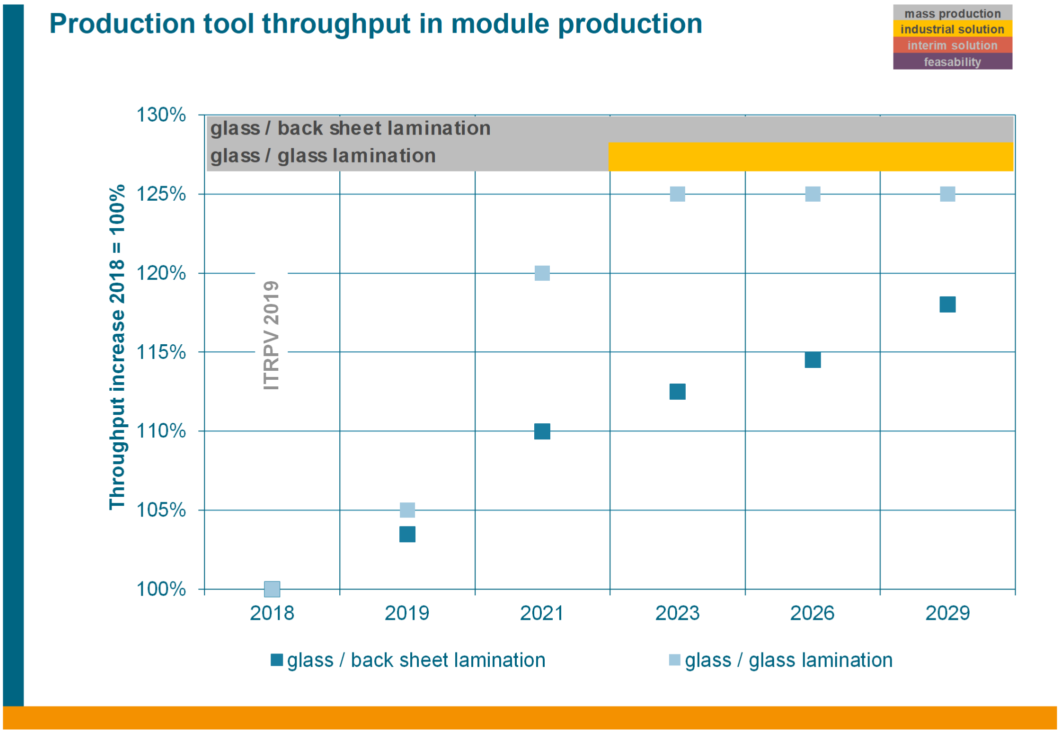

Fig. 24b: Trend of tool throughput for module lamination.

5.2.2. Processes – technology

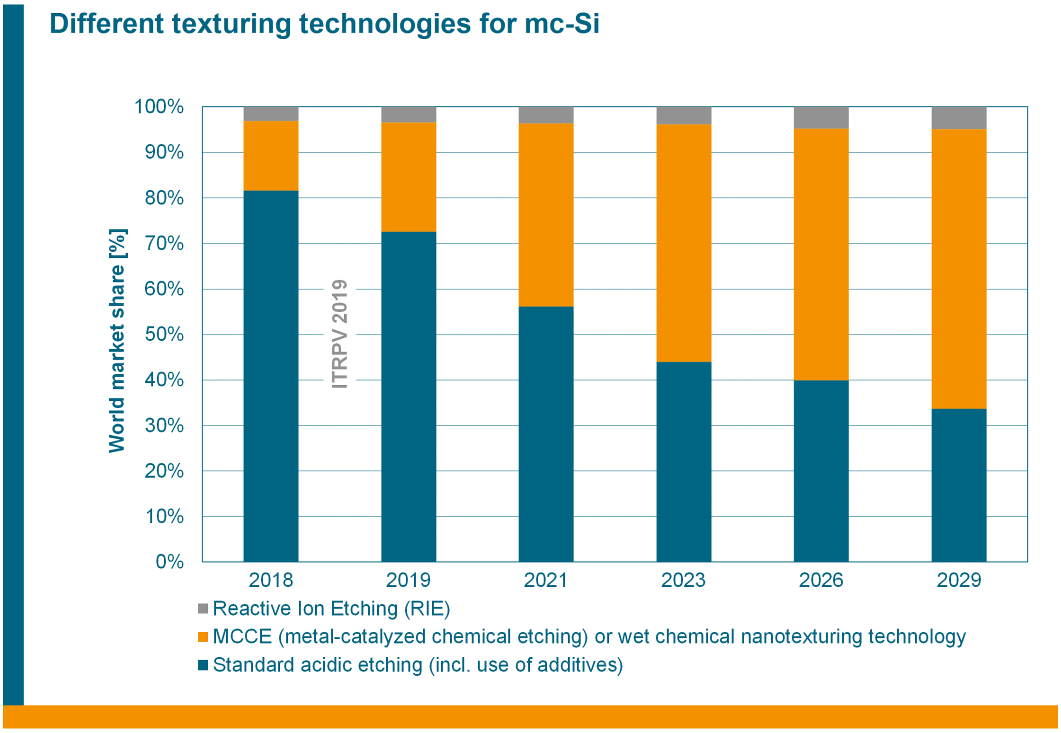

Fig. 25: Expected market share of different texturing methods for mc-Si.

The first production process in cell manufacturing is texturing. Reducing the reflectivity is mandatory to optimize cell efficiency. The expected market share of different texturing methods for mc-Si is shown in Fig. 25. Acidic texturing, a wet chemical process, is mainstream in current mc-Si cell production and is expected to stay mainstream. Wet chemical processing is a very efficient and cost optimized process especially due to its high throughput potential as discussed in Fig. 23a. Standard acidic texturing including the use of additives is expected to stay the mainstream until 2021. Especially the application of additives enables good texturing of DWS mc-Si material. Progress in metal catalyzed chemical etching (MCCE) or wet chemical nano-texturing technologies is causing the expectation that MCCE will become dominant after 2022. Reactive ion etching (RIE) is not expected to exceed 5% market share in 2028 due to the higher cost.

Solar cell recombination losses on the front and rear sides of the cell, as well as recombination losses in the crystalline silicon bulk material, must be reduced in line with high-efficiency cell concepts. The recombination currents J0bulk, J0front, J0rear, indicating the recombination losses in the volume, on the cell's front and rear side respectively, are a reasonable way to describe recombination losses. Fig 26a and 26b show the expected recombination current trends for p-type and n-type materials respectively. The values are in line with the assumptions of former ITRPV editions.

Recombination currents can be measured as described in the literature [18], or they can be extracted from the IV curve if the other J0 components are known.

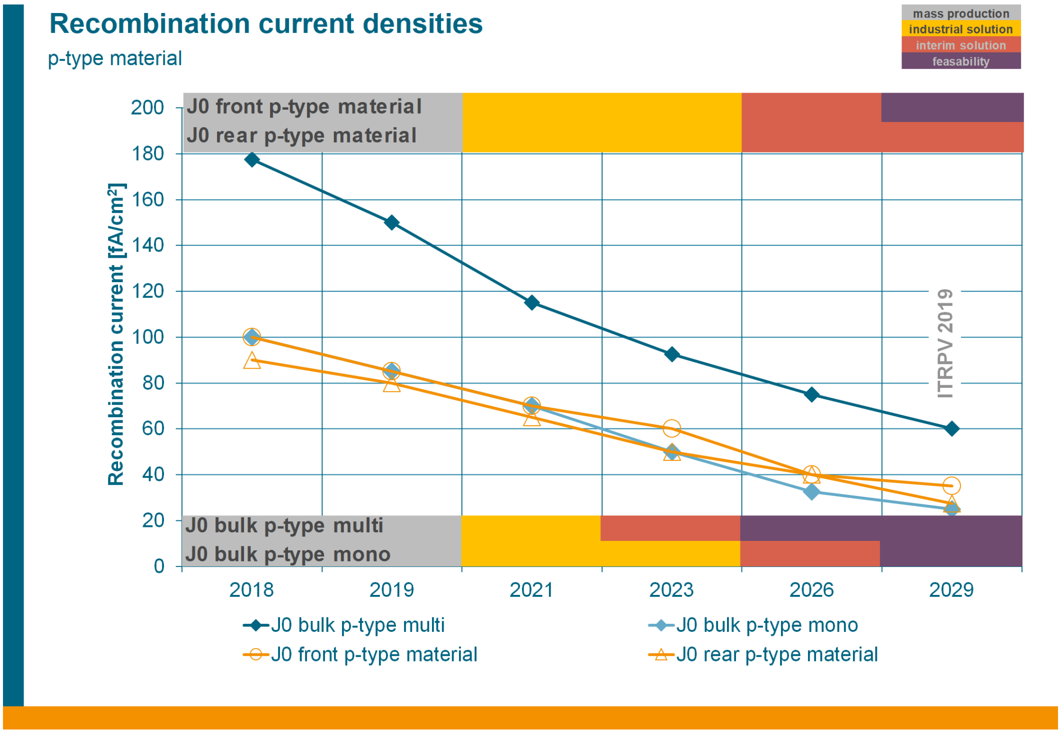

Fig. 26a: Predicted trend for recombination currents J0bulk, J0front, J0rear for p-type cell concepts.

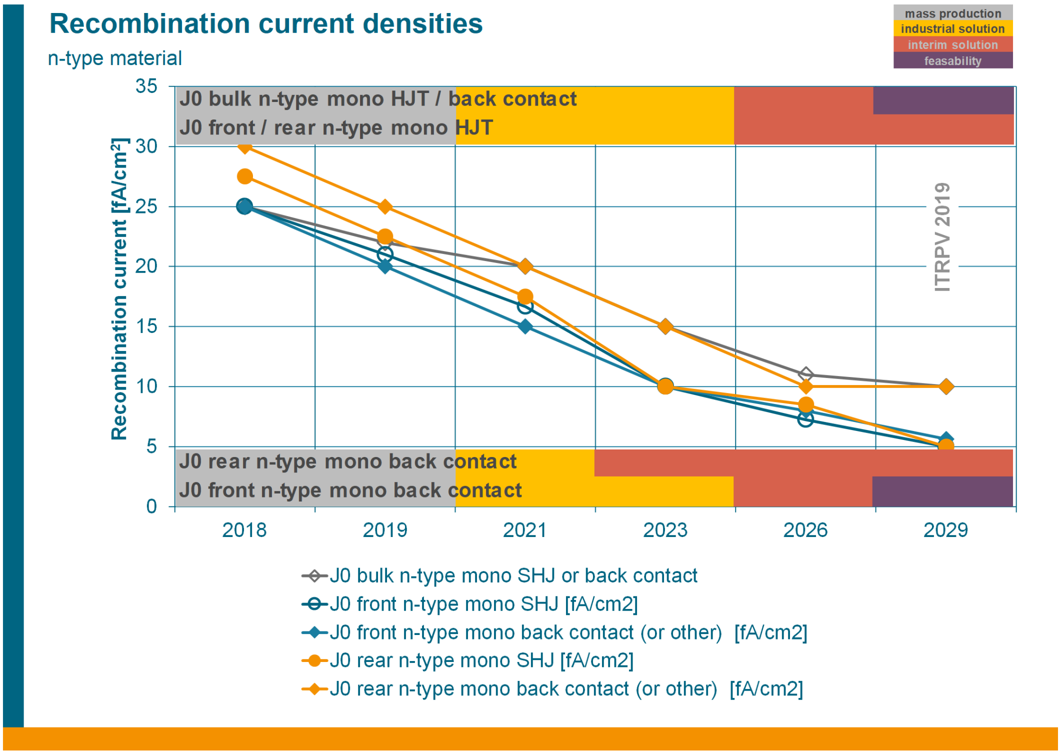

Fig. 26b: Predicted trend for recombination currents J0bulk, J0front, J0rear for n-type cell concepts.

The improvement of the silicon material quality for both, mono and multi will continue. This should result in a reduction of the J0bulk value to 60 fA/cm² for p-type multi and around 30 fA/cm² for p-type mono. J0 front and J0 rear are expected to improve similar like J0 bulk of p-type mono to below 40 fA/cm² in 2029.

Improvements for J0 rear are expected to be implemented faster than for J0 front. The improvements of J0 bulk for p-type mc-Si material is expected to progress slower than for mono, emphasizing the current domination of mono material in the industry.

N-type mono wafers display a J0bulk value of <30 fA/cm², which is expected to be further reduced to about 10 fA/cm² within the next 10 years.

Reductions of J0bulk will result from improvements of the crystallization process (see 5.3). The introduction of improved casted silicon materials (e.g. HPmc-Si, mono-like-Si) resulted in lower bulk recombination currents for this material type.

J0 values of front and rear surfaces are similar for different bulk materials. This J0 values are expected to be reduced by up to 70% of the current values by 2029, nevertheless significant improvements are required to go below 10fA/cm² as there have not been industrial solutions available as indicated.

Rear side recombination current values below 200 fA/cm² cannot be attained with an Al Back Surface Field (BSF). Therefore, J0back improvement is linked directly to cell concepts with passivated rear side. Since 2012, several cell concepts using rear side passivation with dielectric layer stacks have been introduced to production processes (PERC/PERT/PERL technology). Fig. 27a shows the predicted market shares of different rear side passivation technologies suitable for n-type and p-type cell concepts.

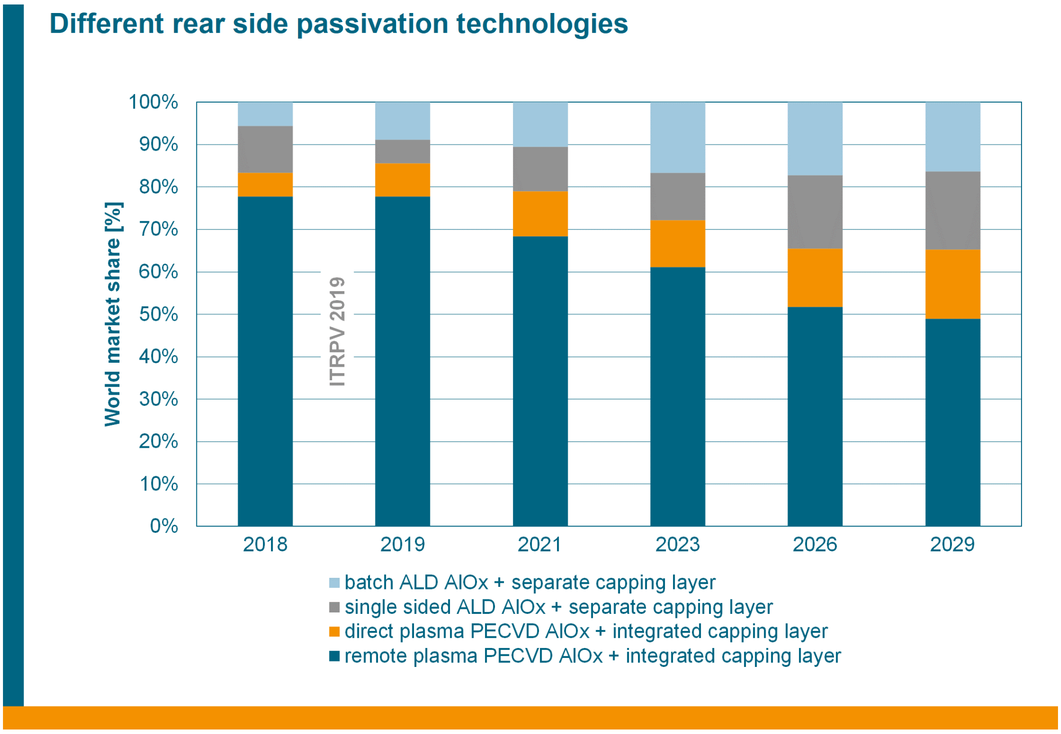

Fig. 27a: Predicted market shares for AlO_x-based rear side passivation technologies.

Remote plasma PECVD Al_2O_3 in combination with a capping layer is and will be the most widely used technology for PERC cell concepts. Beside this, direct plasma PECVD Al_2O_3 in combination with a capping layer is gaining market share. Another technology, ALD Al_2O_3 deposition in combination with separate capping layer deposition, is now expected to gain market share. PECVD $SiON_x$/SiN_x is considered as niche process.

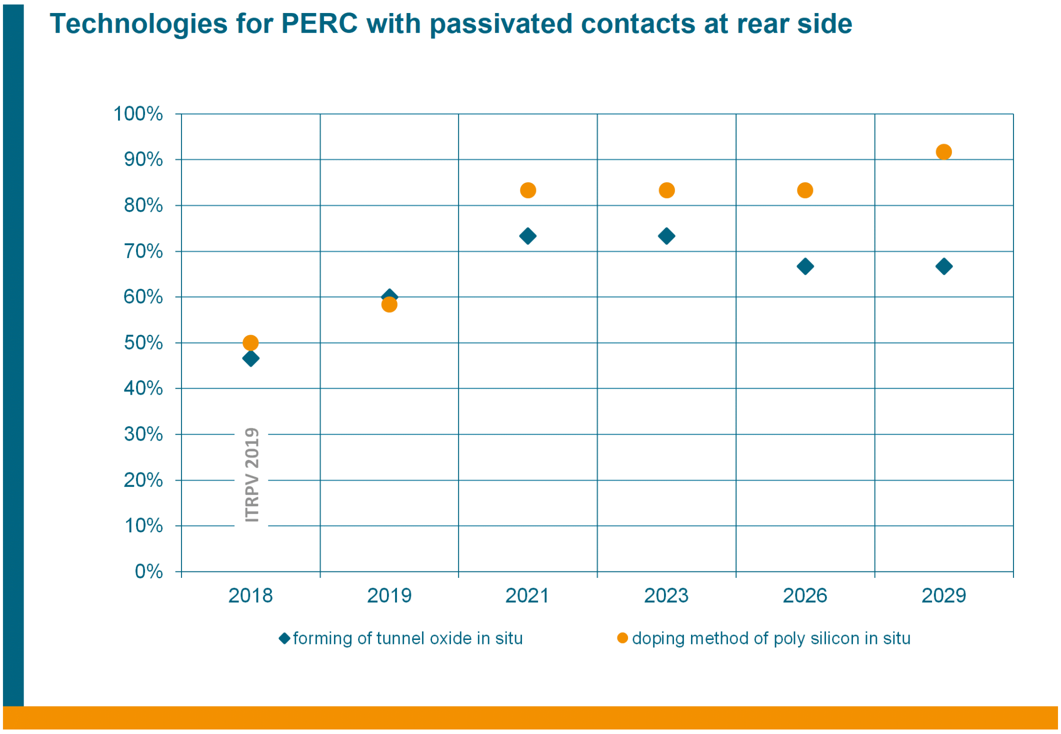

Fig. 27b: Expected trend for forming the tunnel oxide and doping the ploy Si capping layer in passivated contact forming.

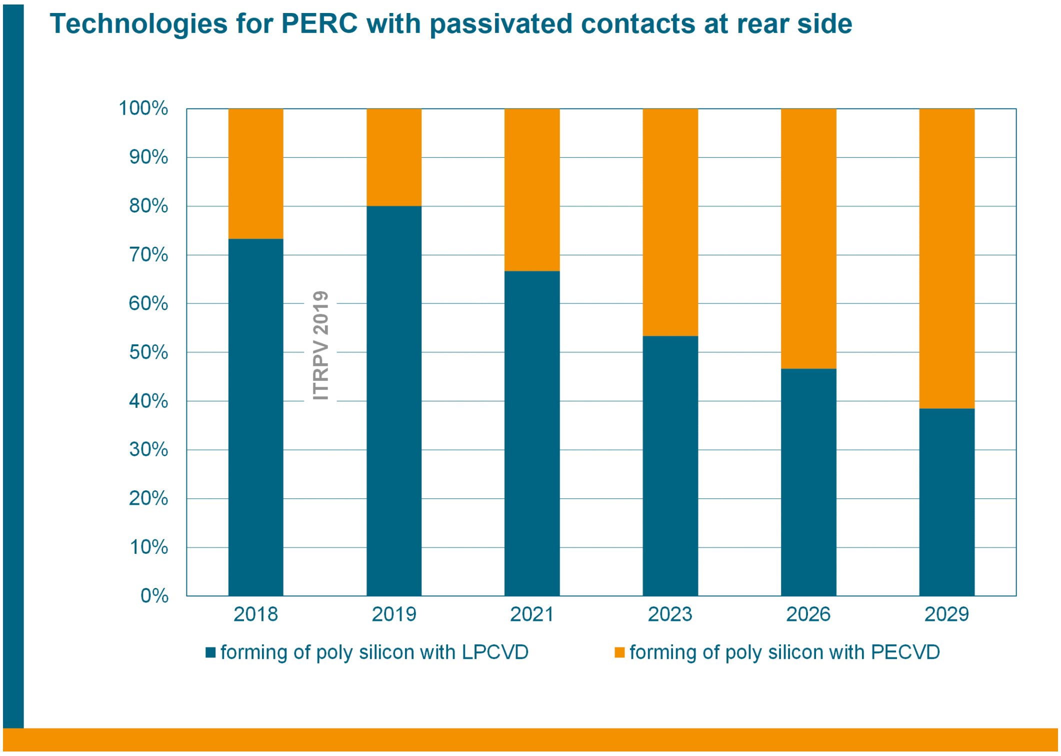

Fig. 27c: Expected technology preference for deposition of the poly-Si capping layer for cells with passivated contact.

A new upcoming method for rear side passivation uses a thin tunnel oxide layer with a conducting polysilicon cap layer. Instead of forming contacts to the bulk Si the contacting is done via the tunneling. This technique avoids the forming of undesired recombination centers. Fig 27b shows the expected trend for the forming of the tunnel oxide and the method of doping the conducting poly-Si layer. In situ processing is expected to become the preferred technique. Market shares of this new technology will be discussed in section 5.3.

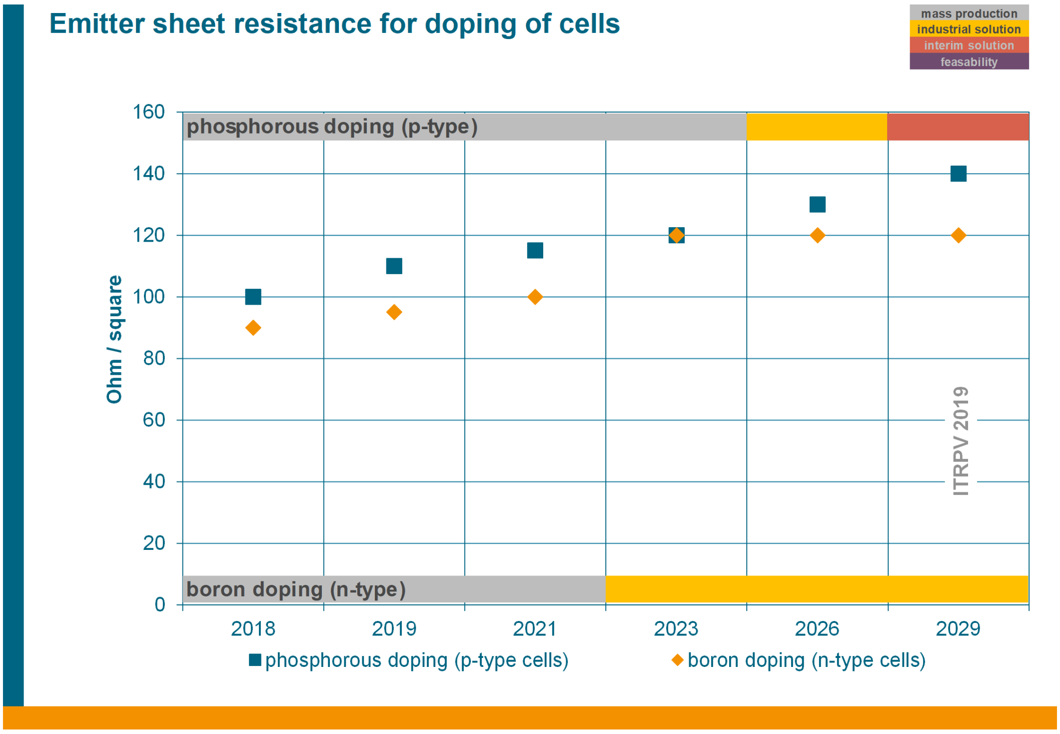

Fig. 28: Expected trend for emitter sheet resistance.

The forming of the poly-Si layer can be done by LPCVD or by PECVD. The trend shows that the both techniques are currently in use – a long term winner is not yet clear.

One parameter that influences recombination losses on the front surface is the emitter sheet resistance. The predicted trend for n-type emitters is shown in Fig. 28. An emitter sheet resistance of about 100 Ohm/square is mainstream in today's industry.

Increased sheet resistances above 100 Ohm/square can be realized with and without selective emitters. If a selective emitter is used, sheet resistance shall refer only to the lower doped region, whereas J0front includes all relevant front side parameters (emitter, surface, contacts). Industrial solutions are available for 130 Ohm/square and might be implemented quite fast, going beyond will require further engineering as indicated by the red marking.

The sheet resistance of p-type emitters is with 90 Ohm/square slightly lower today, it is expected that p-type emitter sheet resistances will increase up to 120 Ohm/square quite fast as the industrial solutions are available.

Fig. 29 shows the expected world market share of different technologies for phosphorous doping in p-type cell processing. Homogeneous gas phase diffusion is a mature, cost efficient doping technology and will remain the mainstream for the years to come. Nevertheless, we see that selective emitter processes are commonly used in mass production with shares of 10% in 2018. This share of laser doped selective emitters will increase significantly over the next years to above 40%. Etch back selective emitter techniques or ion implantation will disappear.

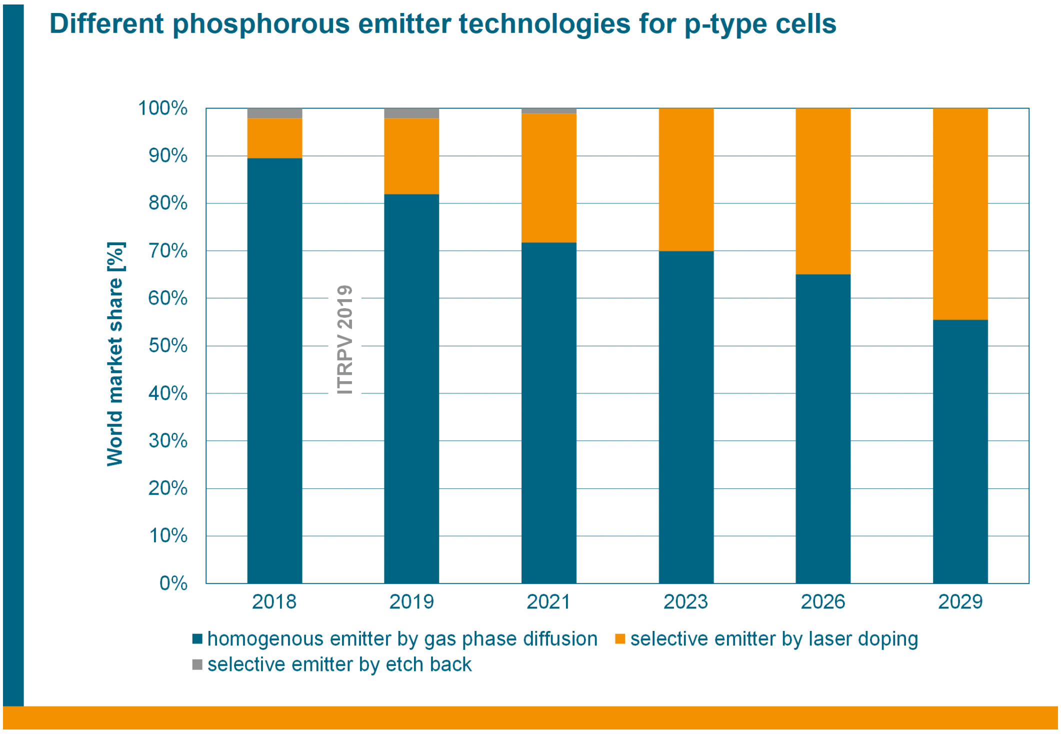

Fig. 29: Expected world market share for different phosphorous emitter technologies for p-type cells.

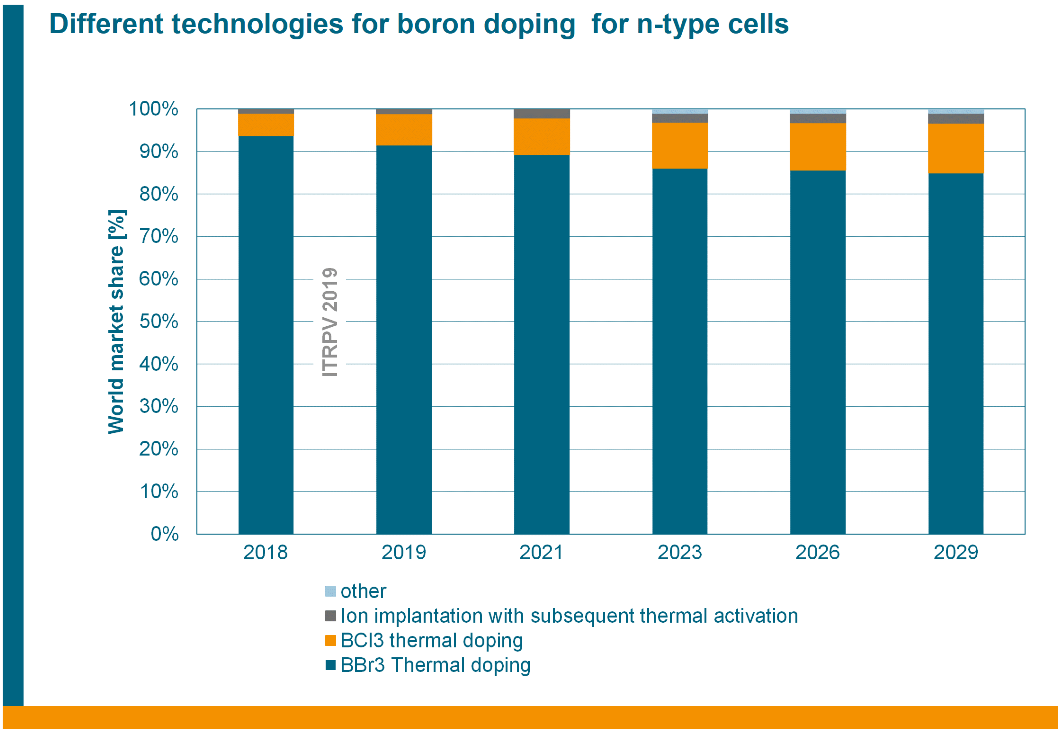

Fig. 30: World market share for different technologies for boron emitter doping (n-type cells).

Nevertheless, Fig 30 shows the expected market share for different boron doping technologies. In line with the findings of the last editions we expect that the currently most widely used BBr_3 thermal diffusion technique will stay mainstream. Ion implantation is supposed to be at low market share of 1%. BCl_3 doping will gain market share. Alternative processes are not seen with high market share so far.

Front metallization is a key process in the production of c-Si solar cells. New front side metallization pastes enable the contacting of the previously discussed low doped emitters without any significant reduction in printing process quality.

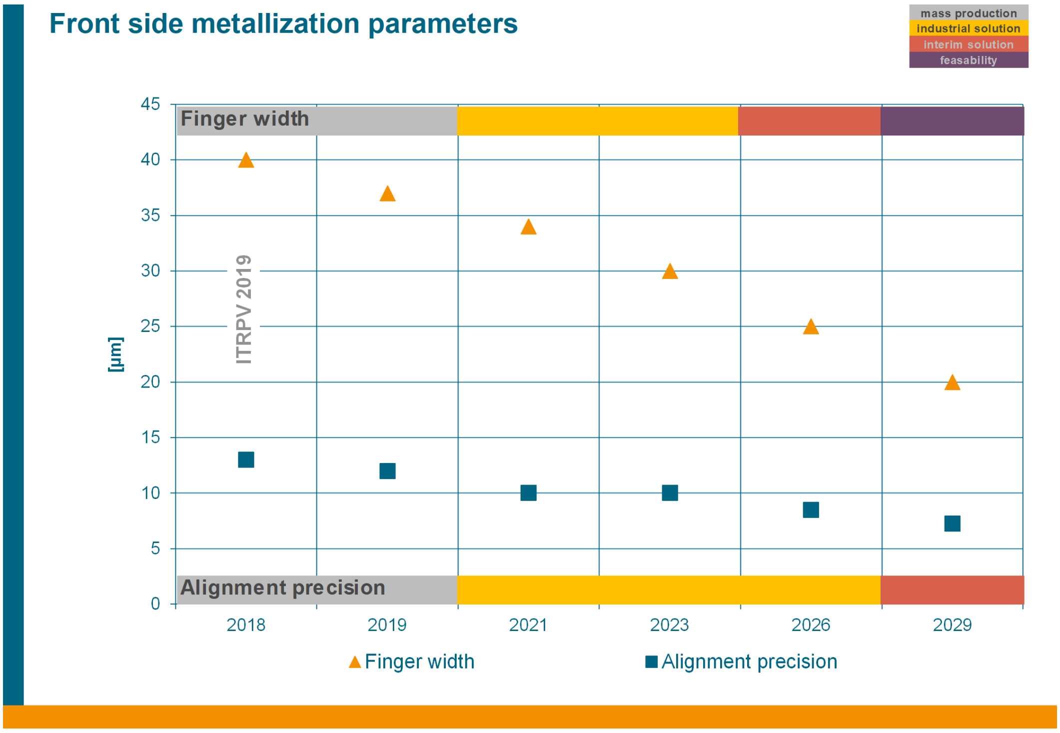

Fig. 31: Predicted trend for finger width and alignment precision in screen printing. Finger width needs to be reduced without any significant reduction in conductivity.

A reduction in finger width is one method yielding in efficiency gain and cost reduction, but only if it is realized without significantly increasing finger resistance. Furthermore, contact with a shallow emitter needs to be established reliably. One possible way to achieve these goals is to use a selective emitter structure, preferably without increasing processing costs.

Finger widths of 40 µm were standard in 2018. 30µm will be implemented quite fast as new screen solutions are available for industrial solutions. Reaching <30µm requires significant development. A further reduction to 20 µm appears possible over the next 10 years. Reducing finger width reduces shadowing, but a trade-off has to be made to maintain conductivity if the roadmap for silver reduction as discussed in 5.1.2 will be executed.

Different approaches for high quality front side print exist. Fig. 32 summarizes the available technologies and their estimated market share during the next 10 years.

Single print technology is mainstream, followed by double printing. Double printing requires an additional printing step and exact alignment. A third, more robust technology — the dual print — separates the fingerprint from the busbar print, enabling the use of busbar pastes with less silver. New busbar less cell interconnect techniques can even omit the busbars completely. Therefore, for reliable module interconnection, and for future applications as bifacial cells, a good alignment accuracy is important in metallization — an alignment accuracy of about 10 µm (@+/- 3 sigma) will be required from 2021 onwards as shown in Fig. 31.

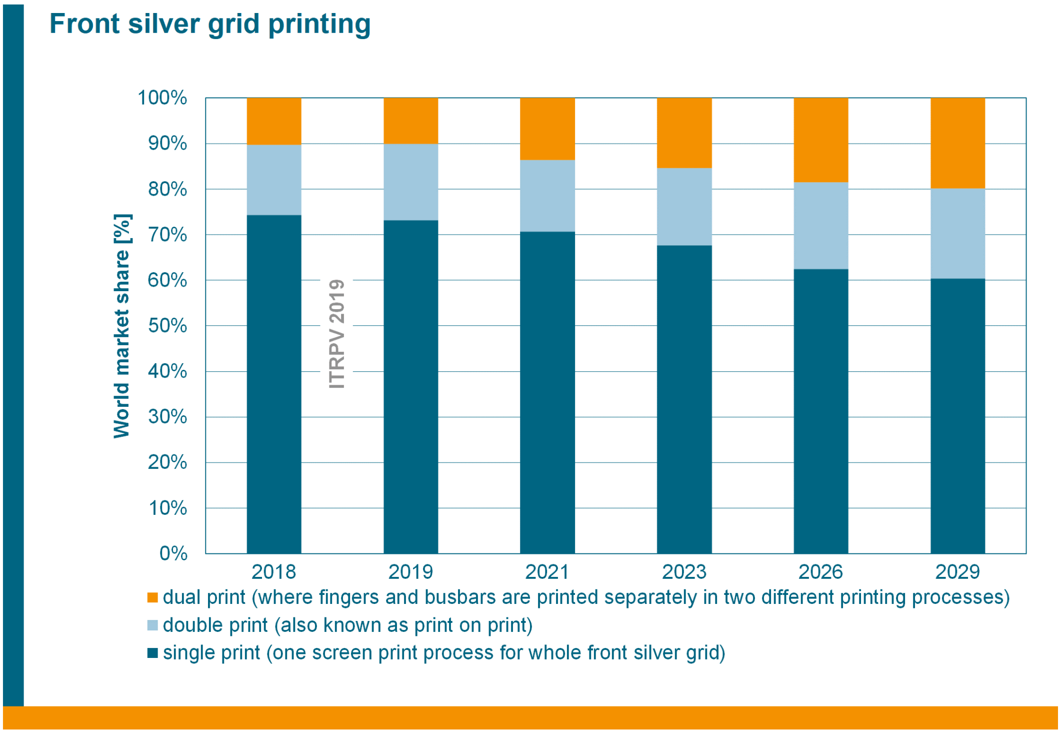

Fig. 32: Expected market share of different front side printing techniques.

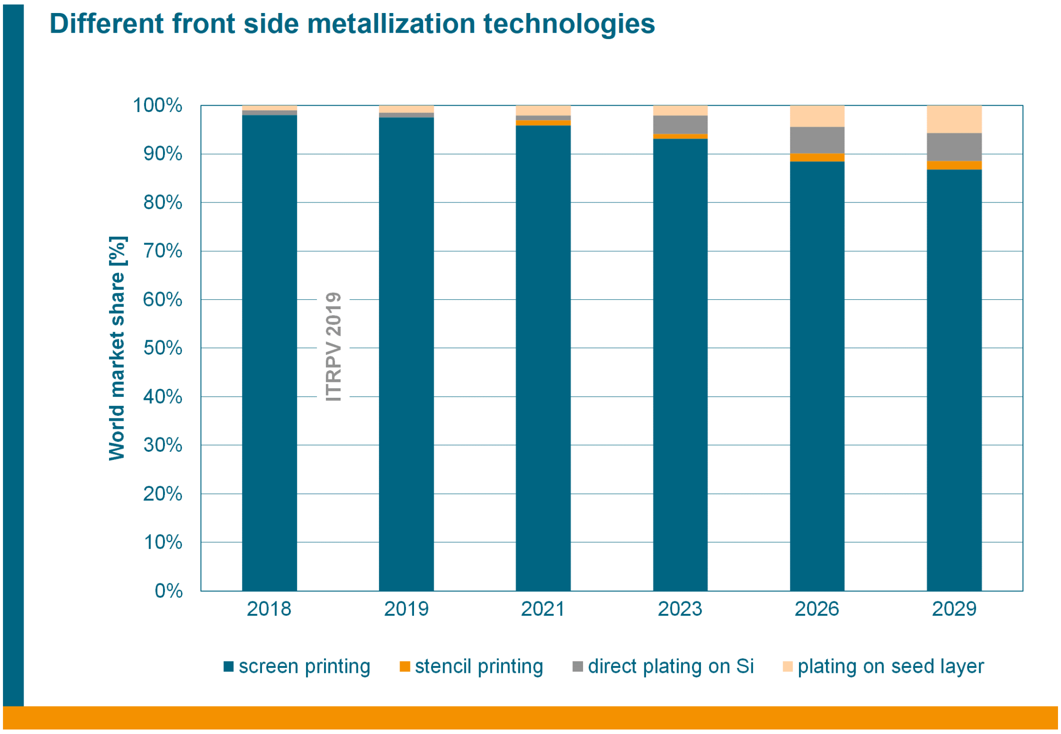

Fig. 33a: Predicted trend for different front side metallization technologies.

The expected share of different technologies for front side and rear side metallization are shown in Fig. 33a and 33b respectively. Fig. 33a shows that classical screen printing is expected to remain the mainstream technology for the years to come in front side metallization. Stencil printing, which can be used with existing screen printing equipment, is expected to be introduced in mass production in

2021, a market share of only 2% is expected for 2028 – again a delay regarding former ITRPV editions. Again, plating appears to be introduced with market shares of 5% from 2021 onwards.

Screen printing as well is expected to stay mainstream in rear side metallization for the next years as shown in Fig. 33b. Plating, especially used for rear side contact cells, is expected to gain slowly market

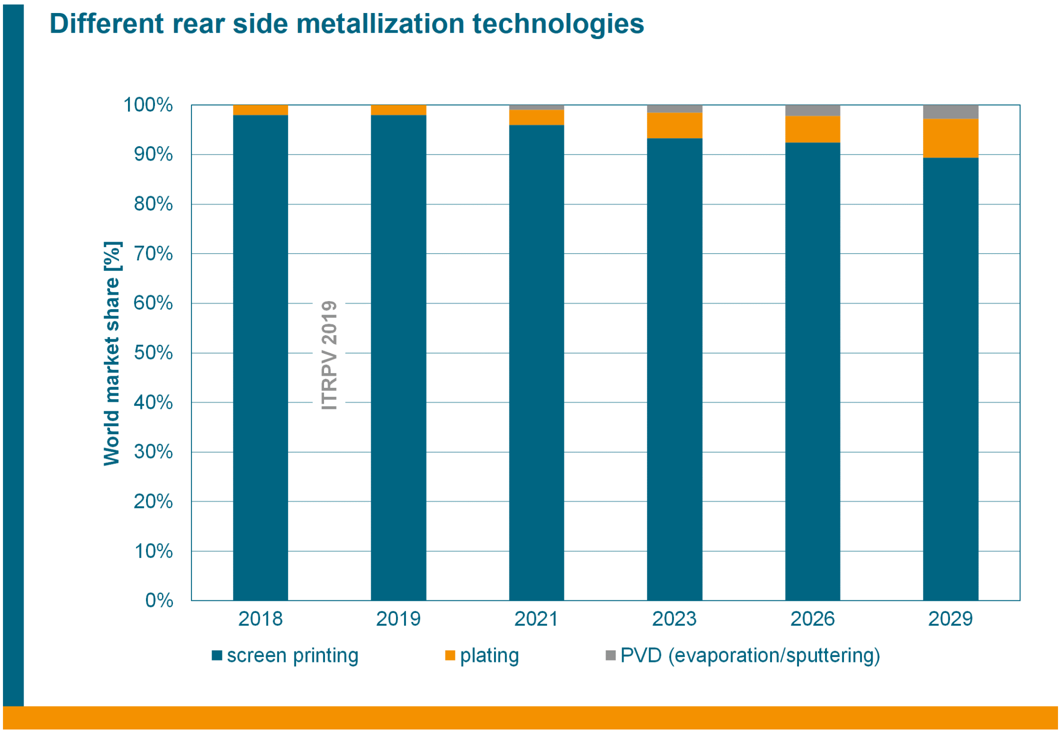

Fig. 33b: Predicted trend for different rear side metallization technologies.

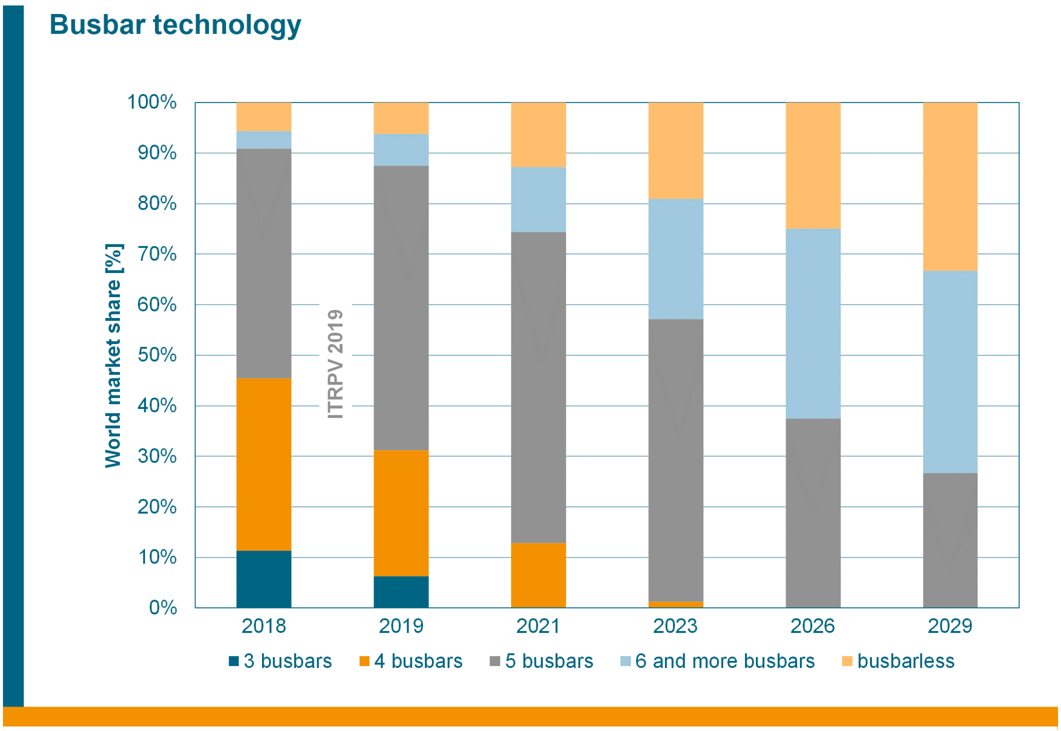

Fig. 34: Worldwide market share for different busbar technologies.

share of around 10% in 2029. Physical vapor deposition (PVD) by evaporation or sputtering is still expected to appear as new application.
As mentioned above, reducing the finger width requires a tradeoff – a current trend in metallization that is direct related to the number of busbars (BB) used in the cell layout. Fig. 34 shows the expected trend. We see that the 3-BB layout, is disappearing and will be fast replaced over by layouts with 4, 5, 6 and more BBs - and by BB-less layouts. BB-less technologies support minimum finger widths as shown in Fig. 31. Nevertheless, this will require new interconnection technologies in module manufacturing that cannot be implemented by simple upgrading of existing stringing tools. It is crucial to get as much power as possible out of the assembled solar cells. The cell-to-module power (CTM) ratio is a good parameter to describe this behavior. It is defined as module power divided by cell power multiplied by the number of cells (module power / (cell power x number of cells)).
Fig. 35 distinguishes in CTM for half cell and full cell applications. The CTM for full cell modules was 2018 at 99% for mc-Si cell technology (acidic texturing) and at 98% for mono-Si cell technology (alkaline texturing), 101.5% and 100% respectively for the corresponding half cell modules.

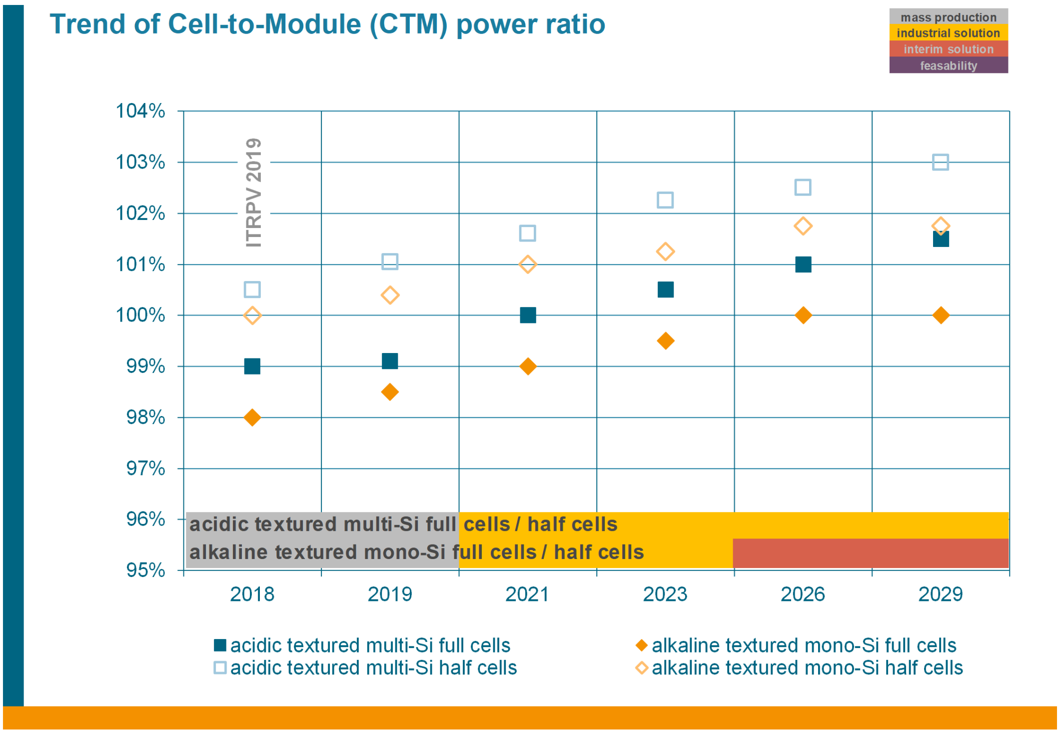

Fig. 35: Expected trend for the cell-to-module power ratio.

CTM exceeding 100% imply that the power of the finished module will exceed the power of the cells used in the module. Using of half cell technology is one method to realize this. Smart interconnection techniques and further improvements of light management within the module as a means of redirecting light from inactive module areas onto active cell areas are possible measures to improve the CTM. The introduction of new interconnection and encapsulation technologies (e.g. narrower ribbons, encapsulation materials with improved UV performance, etc.) will result in further improvements that will enable additional power gains. While CTM improvements for mc-Si may be implemented faster (industrial solutions are known), meeting the CTM roadmap for mono full and half cell requires more development work as no industrial solution has been available so far, indicated by the red color marking.

The junction box is the electrical interface between the module and the system. We found that the internal electrical connection of the bypass diodes is and will be done mainly by soldering, welding is gaining market share over the next years whereas clamping, the third technology, will be used less in the future. Also, we found that the current single junction box concept is expected to shift to multiple junction box as mainstream from 2021 onwards.

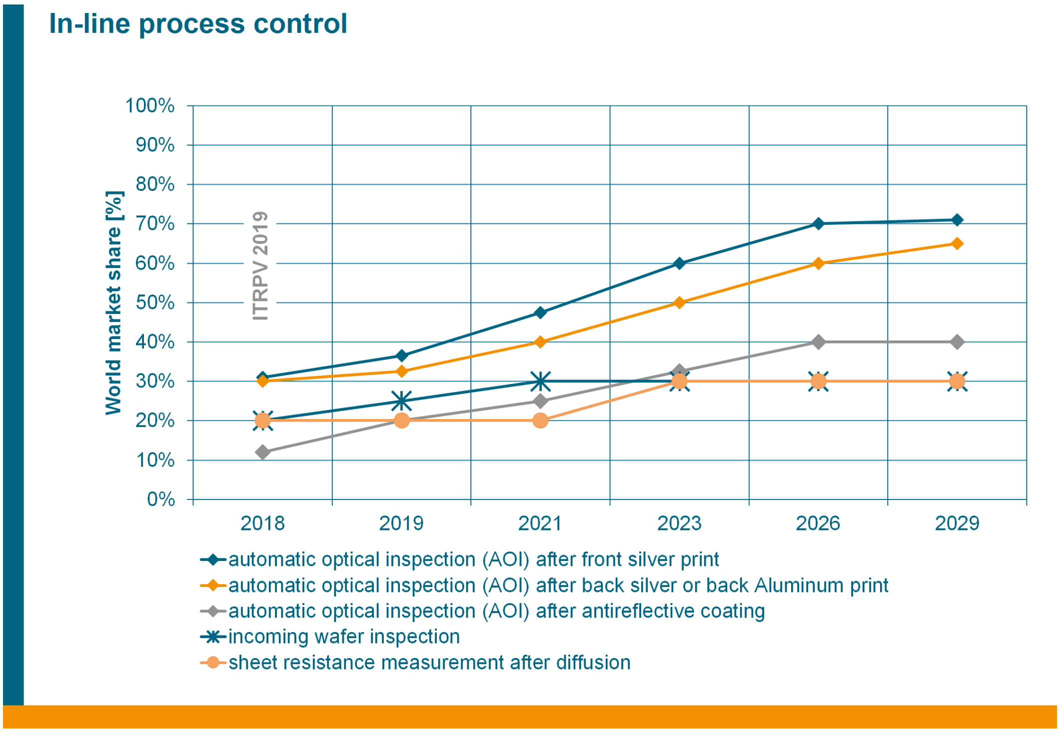

Fig. 36a: Market share of in-line process control for incoming wafer quality, sheet resistance, antireflective coating, and for printing quality at rear and front side printing.

In-line process control in cell and module production lines becomes more and more important to ensure high production yields, high average efficiencies, perfect optical appearance and longtime product reliability. Fig.36a and Fig. 36b summarize the assumptions about in-line cell process control of selected key process parameters. Automatic inspection (AI) of incoming wafer is assumed to be in use in about 20% of all cell production lines. Sorting out of spec material is important to ensure high cell production yields. Nevertheless, incoming inspection is in use on sampling base measurement systems for sheet resistance may be implemented in contemporary production lines for diffusion process monitoring, 20% of the production lines will be using them in 2023. The control of the front side antireflective (AR) layer is in use at about 10% of production lines. Nevertheless, the penetration in 2025 is expected to reach 40%. AOI in print inspection is also expected to be implemented more in the future.

All numbers in Fig. 36a are below the values of the last edition. We assume that in-line process control is becoming more important in modern production lines, nevertheless it is a question of capex spending. Intelligent sampling will be in use anyway for process monitoring. The trends for AI at cell test are summarized in Fig. 36b.

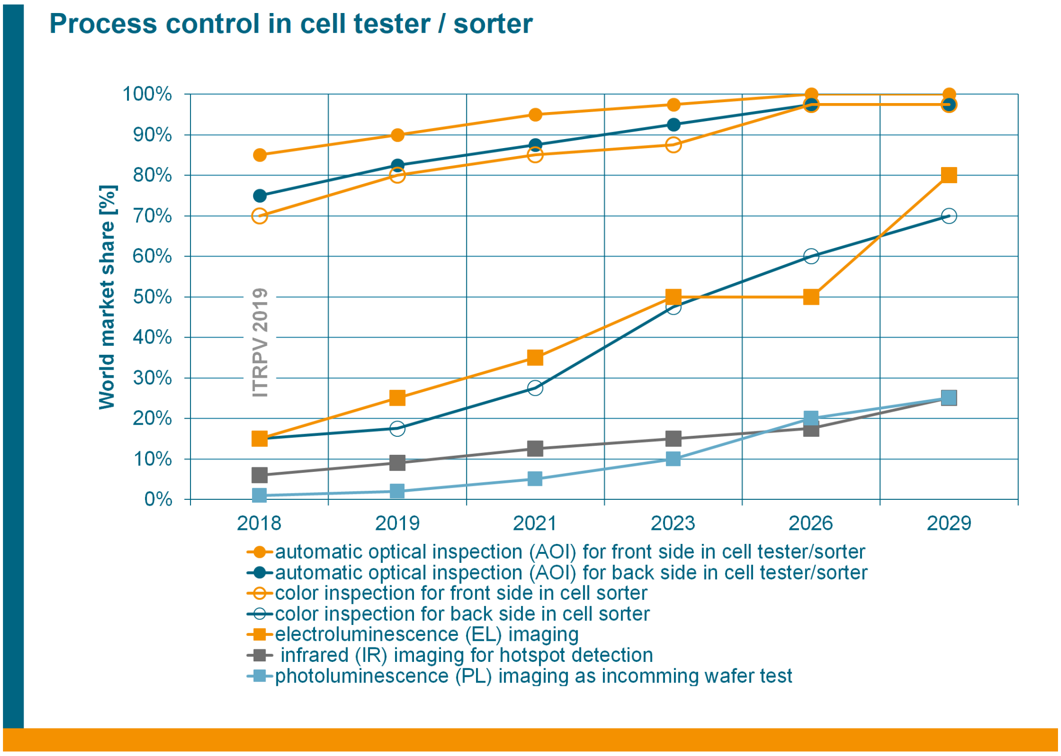

Fig. 36b: Market share of different in-line Automated Inspection (AI) systems for process control at cell test.

AOI incl. front side color inspection at cell test is standard in new cell production lines. It is expected that in this year about 80% of all lines will be equipped with AOI for front and rear side inspection. The trend is clear to be close to 100% from 2026 onwards.

On top of optical inspection, we see an increasing share of rear side color inspection for bifacial cells, EL, IR, and PL systems. The latter two are considered to have the lowest implementation share with <5% today and only 20% in 2029.

The trends for in-line testing and manufacturing execution systems (MES) in module production lines are summarized in Fig. 37. EL inspection of modules is standard even today and will reach 100% from 2021 onwards. A similar trend is visible in AOI of cells in the stringers. IR and cell color inspection in module production are expected stay on very low level as those inspections are already done at cell test.

The implementation of MES progresses – today's share of 30% is predicted to increase systematically to above 80% in 2029. This is a clear sign towards further automation in module manufacturing.

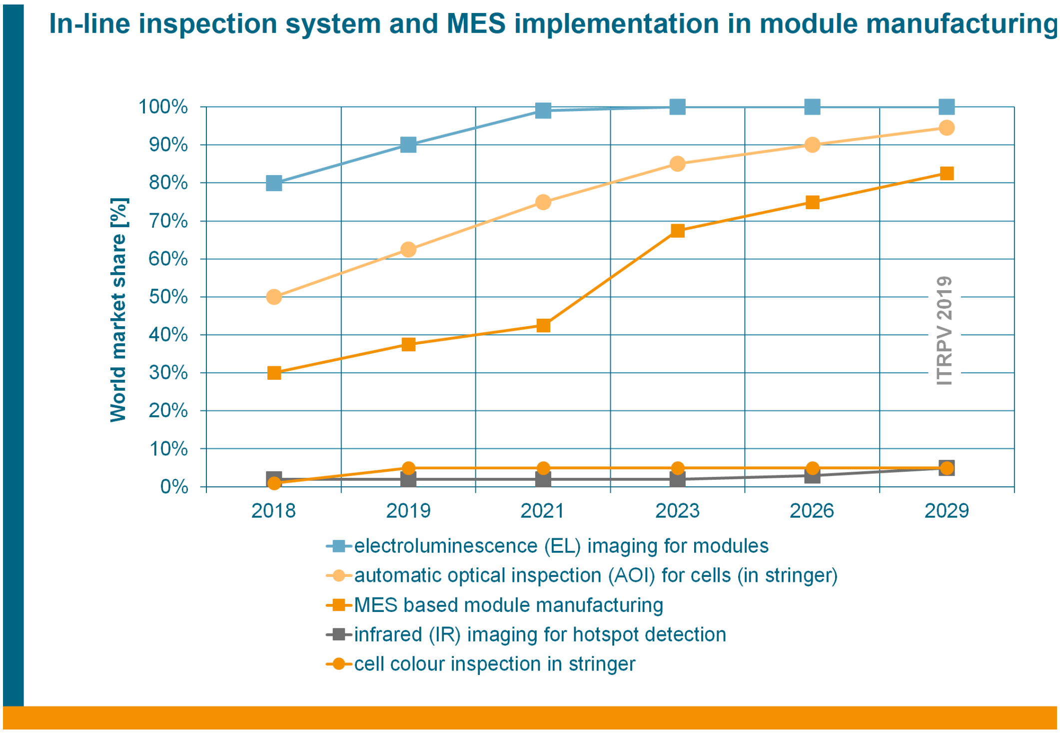

Fig. 37: Trends of in-line inspection systems and MES implementation in module production lines.

5.3. Products

Casted c-Si materials had in 2018 a market share of about 50% vs. 50% for mono [19, 20]. Fig. 38 shows that the ITRPV results are in line with these facts. This market share of casted wafer materials is assumed to shrink fast to below 40% of the world wafer market for c-Si solar cell manufacturing and it is assumed that this share will further shrink to around 10% in 2029. Simply distinguishing between mono-Si and mc-Si, as it was done some years ago, is insufficient. The c-Si materials market is further diversifying, as shown in Fig. 38. N-type mono Si material is expected to gain about 40% in 2029. High-performance (HP) mc-Si material will be the only casted silicon material. Mono-like-Si will stay present but at a negligible share.

Mono-Si is expected to gain fast significant market share over casted materials and will attain an assumed share of ≈80% in 2029. This trend of increased mono-Si market share is in line with the assumptions of the past ITRPV editions, but it is assumed to take place much faster. We expect in 2019 a market share of p-type mono-Si of about 50% and 10% for n-type mono-Si - slightly higher as expected in the 9th edition. For 2029 we see a market share for p-type mono of 40% and 40% for n-type mono. Kerfless crystallized materials are expected to have a market share of up to 10% in 10 years.

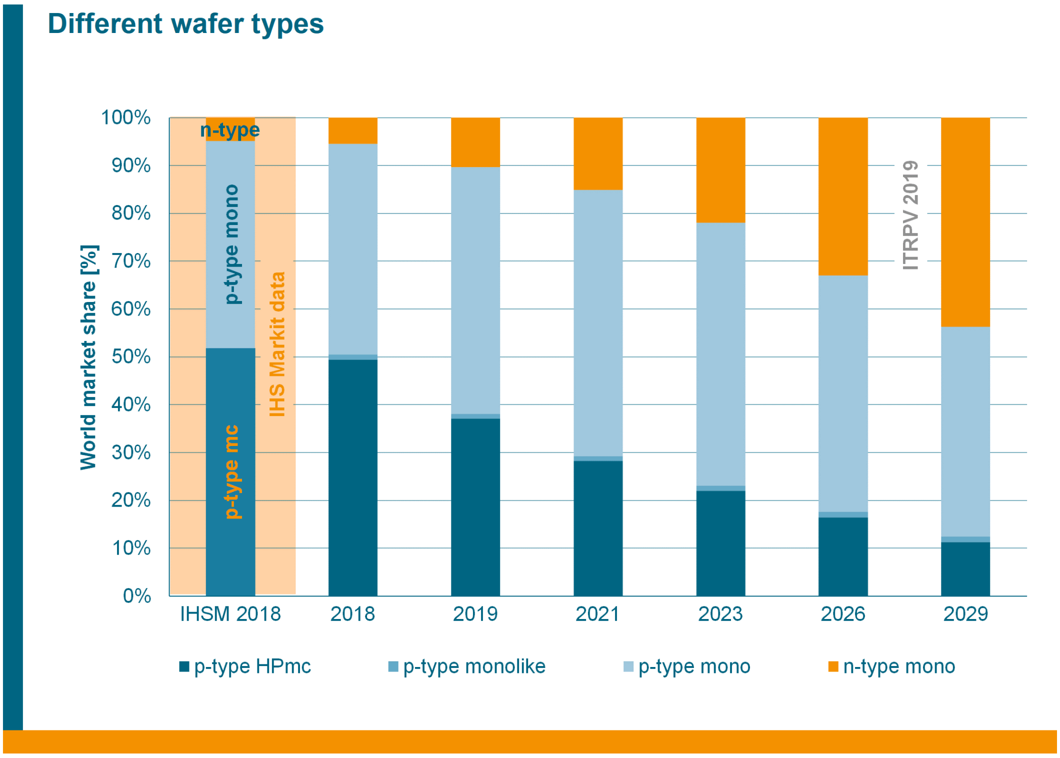

Fig. 38: World market shares for different wafer types. IHS Markit data are indicated for 2018 as reference, not distiguishing between HPmc and mc material [19].

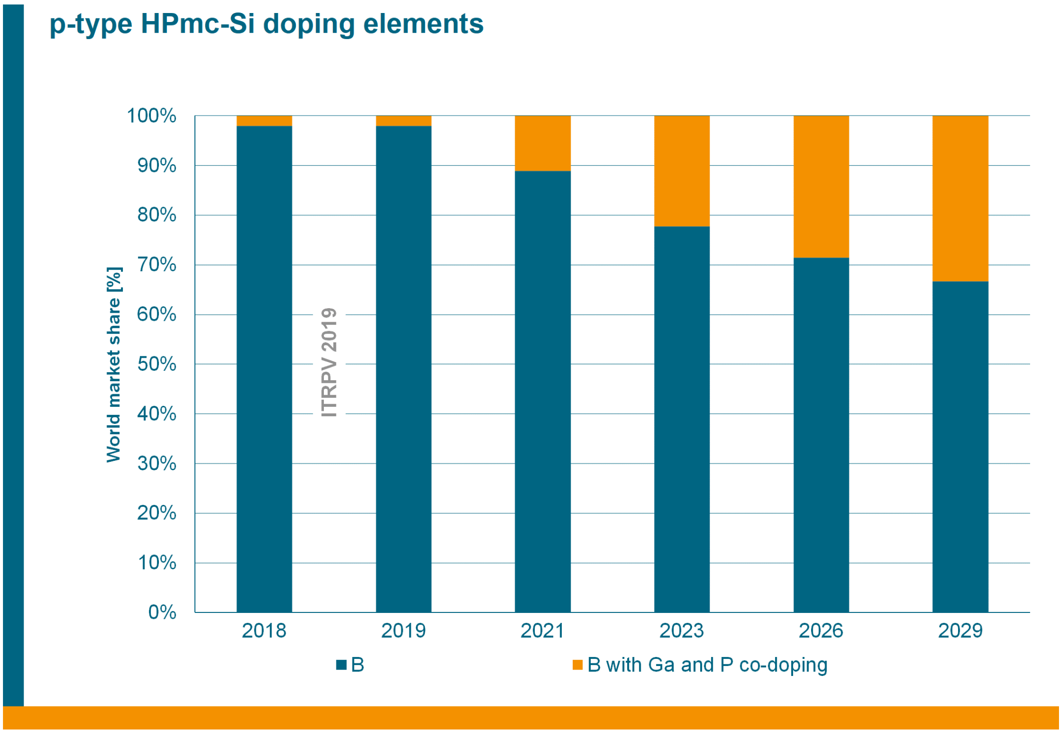

Fig. 39: Expected market share of dopands used for doping of p-type mc-Si material.

Further engineering is done to improve mc-Si material properties despite an expected shrinking market share. Fig. 39 shows that the share of p-type mc-Si material doped with Boron and additional co-doping with Ga and P is expected to be more intensively used in the coming years resulting in improved material performance of mc-Si PERC especially regarding improved doping homogeneity [21].

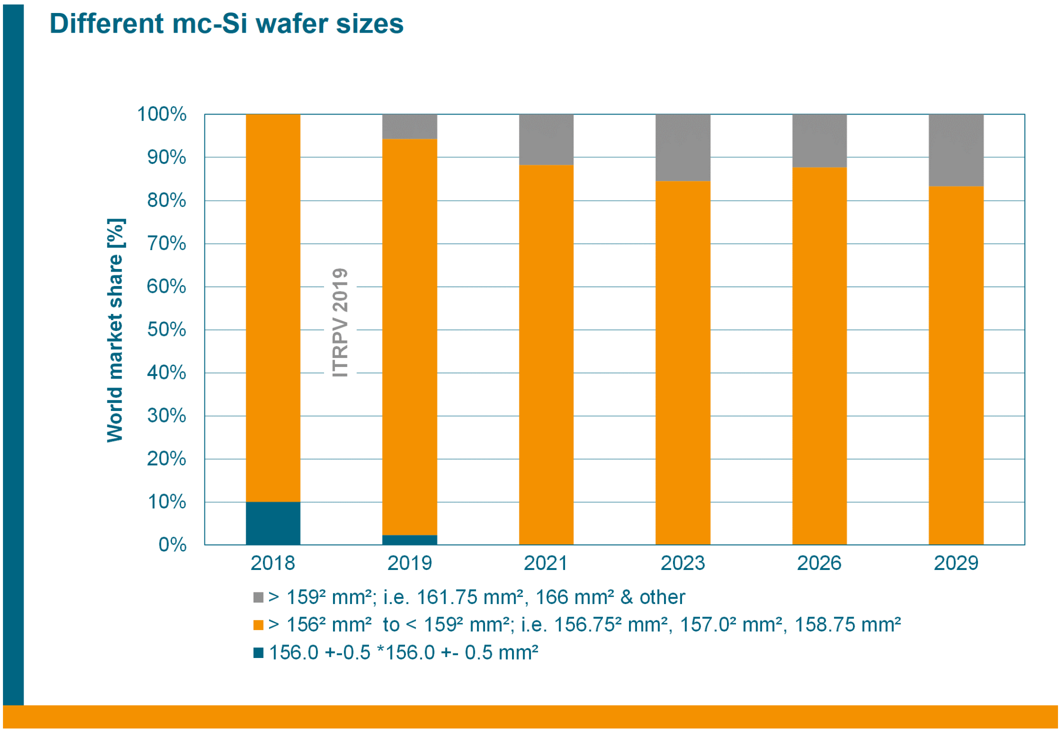

Fig. 40a: Expected trend of mc-Si wafer size in mass production.

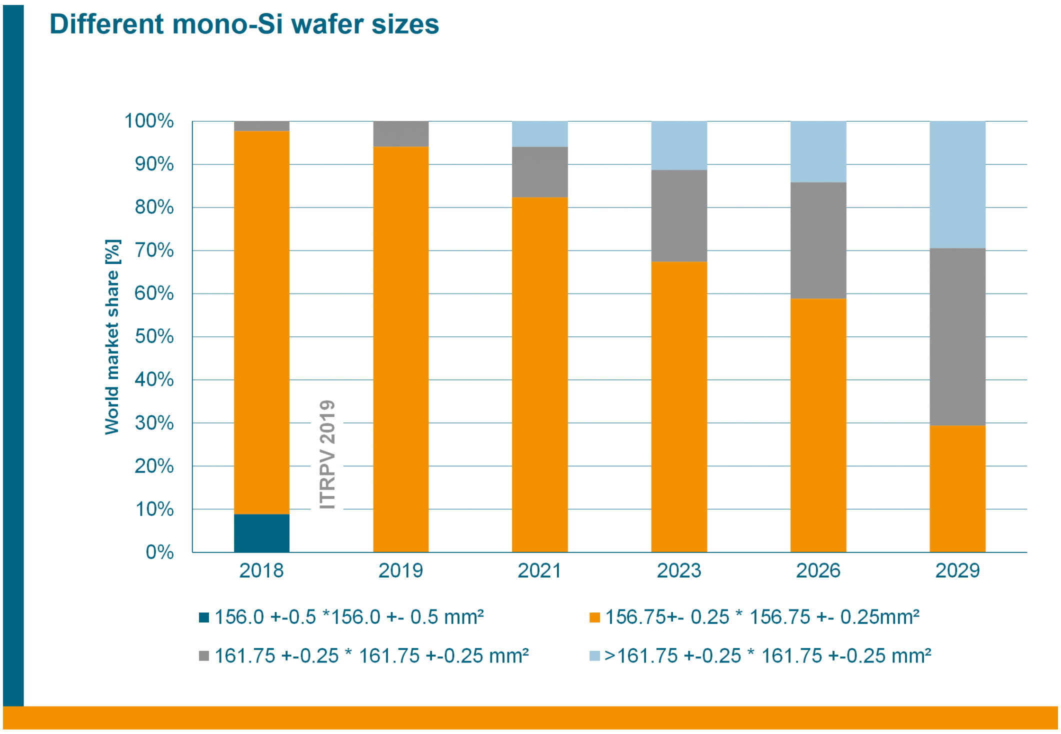

Fig. 40b: Expected trend of mono-Si wafer size in mass production.

Fig. 40a and 40b show the ITRPV survey results about the market share of different wafer dimensions for mc-Si and mono-Si wafers respectively. New wafer formats first appeared in 2015.

The move from 156 x 156 mm² to the larger formats of 156.75 x 156.75 mm² in mass production started 2016. The old 6" format with 156 x 156 mm² will disappear in the market completely by the end of 2019. We see a wide diversification in mc-Si wafer formats, powered by the shrinking mc-Si wafer market. The dominating format is and will be wafers with 156.75 x 156.75mm², but also 157.0 x 157.0 mm² and up to 158.75 x 158.75 mm² are in use. Larger wafers with formats of 161.75 x 161.75, 166.0 x 166.0 mm² and even larger are expected to appear with a market share of up to 15% within the next 10 years.

The transition to 156.75 x 156.75mm² was faster for mono-Si: the old 6" will be gone in 2019 and the share of this larger format is expected to be at ≈95%. The format is mainstream in the industry for both material types. An even larger format was introduced by a cell and module manufacturer first in 2016. We assume that the larger format of 161.75 x 161.75 mm² will gain significant market share in mono-Si within the next years. In addition, we found that even larger formats will appear with increasing market shares. Standardization of wafer dimensions is highly recommended in order to enable tool manufacturers to provide the right tools and automation equipment. The dimension change for mono-Si is assumed to go in parallel with an increase in diameter of the pseudo square wafers: 210 mm are mainstream today with >75% market share. It is expected that larger diameters >211 mm will be implemented within the next years.

Implementation of new Wafer Size in Production

Wafer manufacturing mc-Si	158.75 (+/-0,25) mm²	in existing lines possible
	161.7 (+/-0,25) mm²	possible with upgrades
	≥ 166 (+/-0,25) mm²	possible with new lines
Wafer manufacturing mono-Si	158.75 (+/-0,25) mm² (full- & semisquare)	in existing lines possible
	161.7 (+/-0,25) mm² (full- & semisquare)	possible with upgrades
	166 (+/-0,25) mm² (semisquare)	possible with upgrades
	≥ 166 (+/-0,25) mm²	possible with new lines
Cell manufacturing	158.75 (+/-0,25) mm² (incl. semisquare)	in existing lines possible
	161.7 (+/-0,25) mm² (incl. semisquare)	possible with upgrades
	166 (+/-0,25) mm² (incl. semisquare)	possible with new lines
	> 166 (+/-0,25) mm²	possible with new lines
Module manufacturing	158.75 (+/-0,25) mm²	in existing lines possible
	161.7 (+/-0,25) mm²	possible with upgrades
	≥ 166 (+/-0,25) mm²	possible with new lines

Tab. 2.: Implementation status of new wafer formats.

Table 2 summarizes the current status of implementation for new upcoming wafer formats at different levels of the value chain. All formats up to 161.7 x 161.7 mm² can be implemented in existing fabs with upgrades. Larger formats will be introduced with new equipment in new built fabs.

The roadmap also confirms that pseudo square wafers will dominate the market over full square wafers. Nevertheless, we expect that the share of full square wafers will increase and stay at a low level below 10% over the next years.

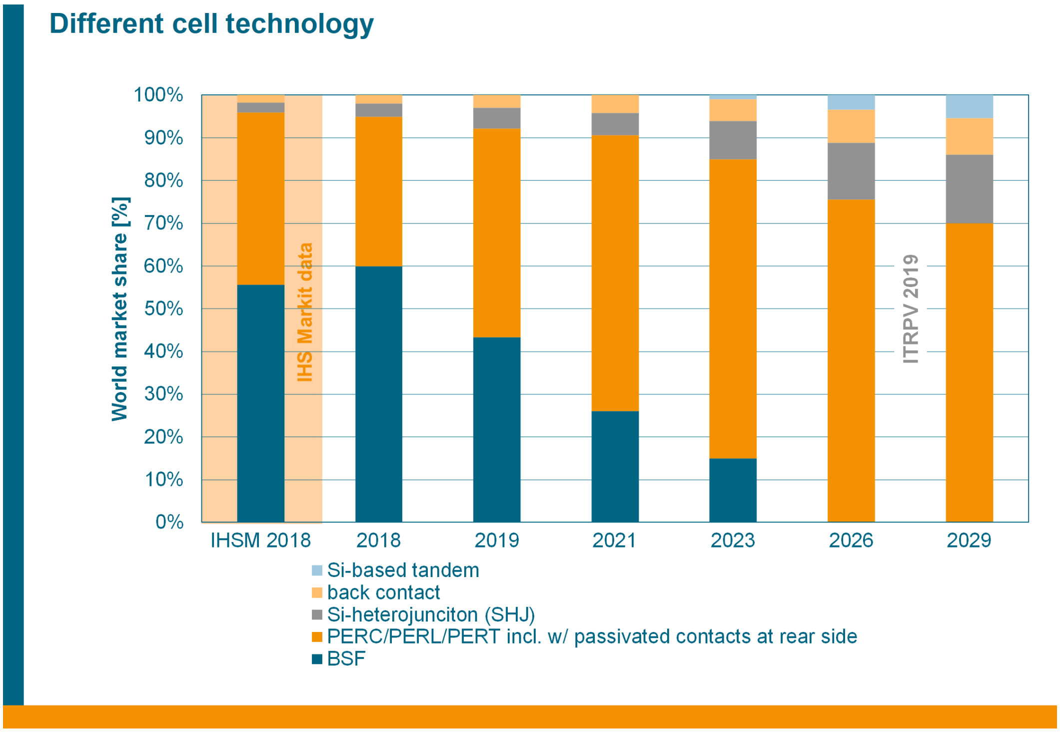

Fig. 41a: Worldwide market shares for different cell technologies. IHS Markit data are indicated for 2018 as reference for 2018 [19].

We found for 2018 a share of 35% for PERC technologies and 60% for BSF – despite slight differences, in line with the assumptions of IHS Markit as shown in Fig. 41a [19]. PERC/PERT/PERL cells are assumed to become mainstream in 2019 with 50% market share over BSF cells with 42%. Heterojunction (HIT/HJT) cells are expected to gain a market share of 12% in 2026 and 15% by 2029. Fig. 41a confirms again the market dominance of double-sided contact cell concepts. Rear-side contact cells are not expected to have significant market share: we assume a change from 2% in 2018 to nearly 10% in 2029. Si-based tandem cells are expected to appear in mass production after 2021. BSF is assumed to be produced mainly on cost efficient mc-Si and will probably disappear until 2026. Fig. 41b highlights trends in PERC technology, the current and future mainstream cell technology.

There are different approaches to realize passivated emitter and rear cells. The most common process sequence is using p-type material with a passivating layer of Al_2O_3 and a SiN_x cupping layer. In 2019 about 15% of PERC cells will be produced in this technology with mc-Si material, 80% with p-type mono-Si. About 4% are produced with n-type material and 1% is using n-type material with a tunnel oxide based rear side passivation – called passivated contact technology. The passivated contact rear side passivation technology is expected to gain significant market share at the expense of p-type PERC mainly on n-type material, but also on p-type material. The share is expected to grow to up to 30% in 2029.

PERC cells can trap the light from the front and from the rear side if the electrical contacts are designed accordingly, so this cell types can be used for bifacial light capturing. Fig. 42 shows the expected market trend for bifacial cells. The 2019 market share of about 13% is expected to increase significant to more than 60% within the next 10 years.

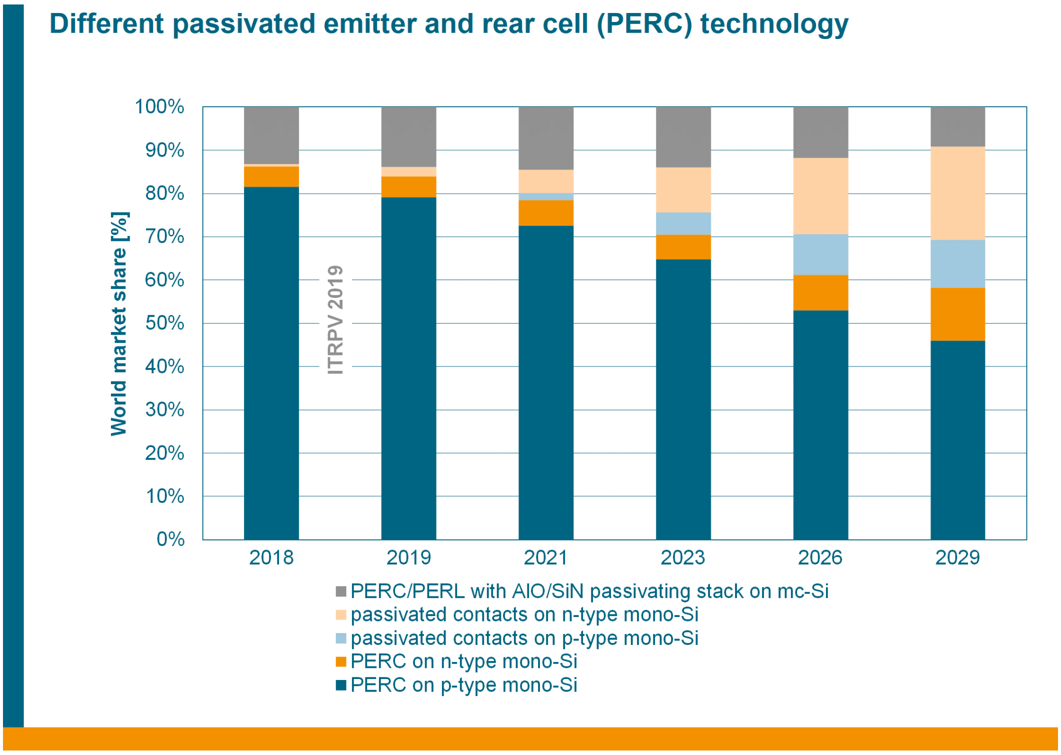

Fig. 41b: Worldwide market shares for different cell technologies.

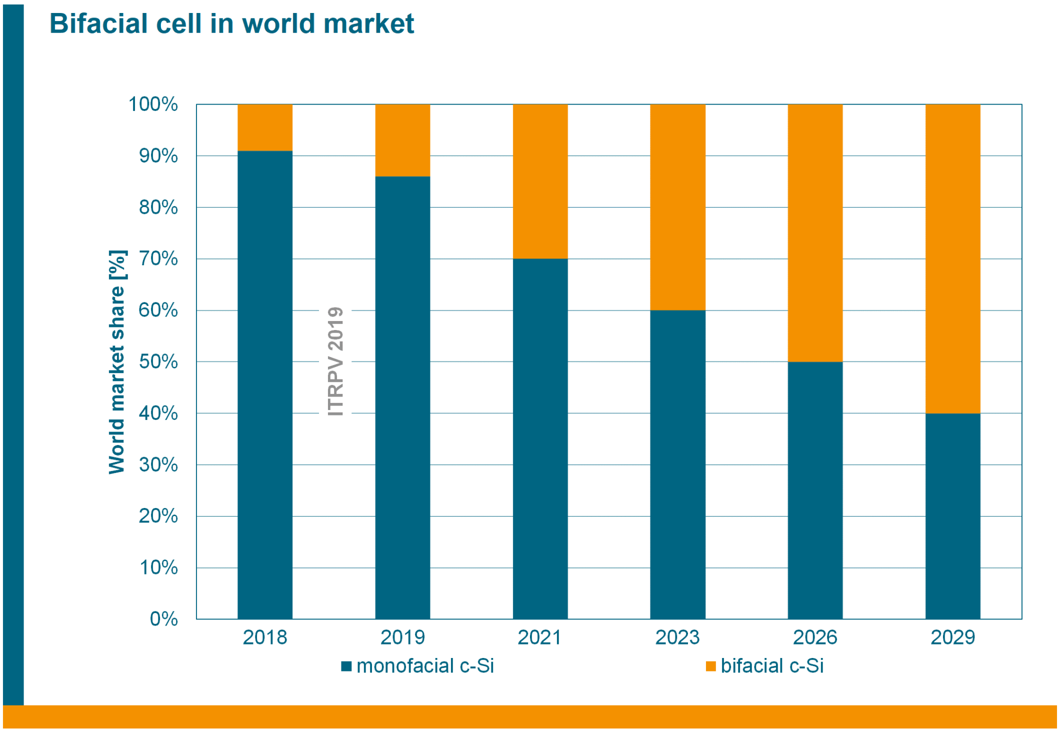

Fig. 42: Worldwide market shares for bifacial cell technology.

Today most of modules are monofacial modules. Bifacial cells can be used in bifacial modules as well as in conventional mono facial modules so bifacial cells will also be used in both module concepts.

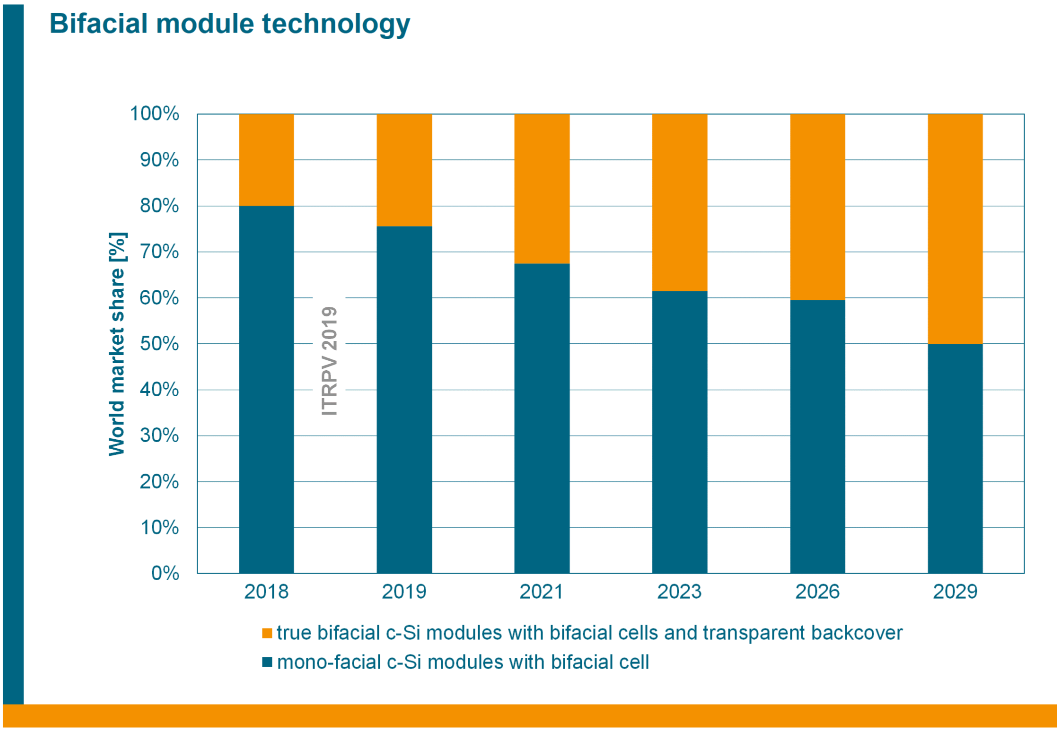

Fig. 43: Worldwide market shares for monofacial and "true" bifacial c-Si modules.

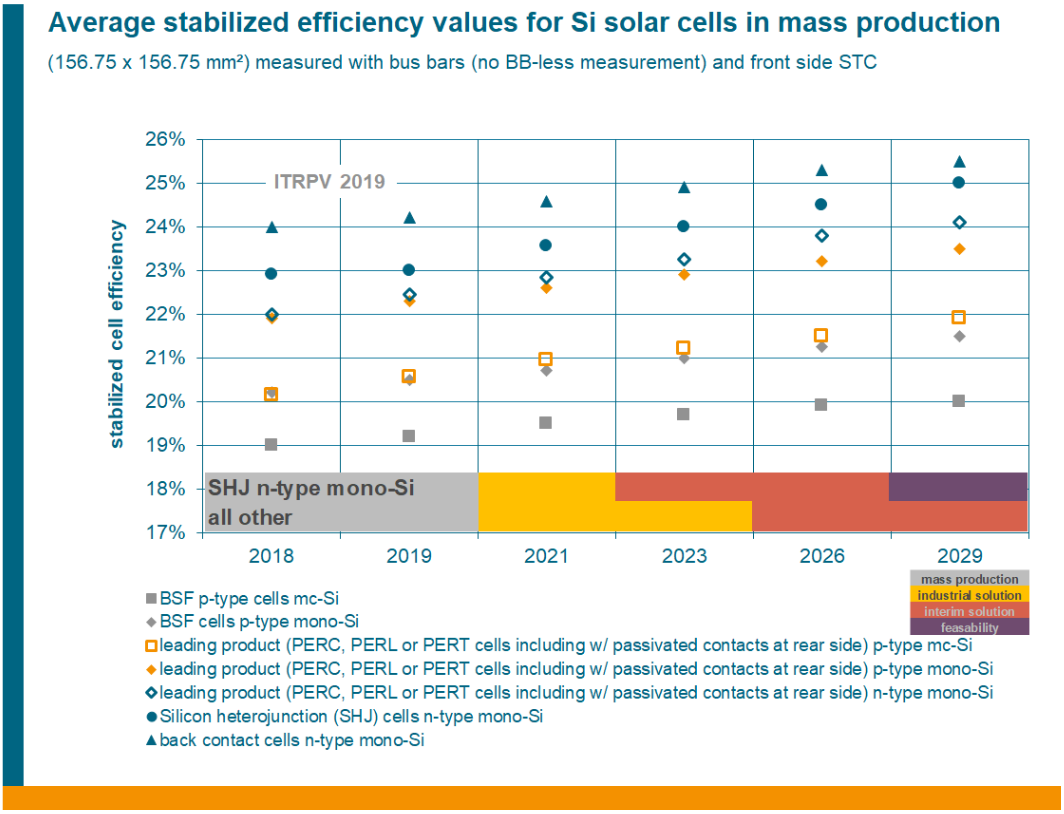

Fig. 44: Average stabilized efficiency values of c-Si solar cells in mass production (156.75 x 156.75 mm²).

As shown in Fig. 42 bifacial cells will gain market share. Fig. 43 shows the expected share of true bifacial modules. Nevertheless, we expect that the market share for bifacial modules will increase to more than 30% or that more than 50% of all bifacial cells will be used for true bifacial modules in 2029.

Fig. 44 shows the expected average stabilized front side cell efficiencies of state-of-the-art mass production lines for double-sided contact and rear-contact cells on different wafer materials. The plot shows that there is potential for all technologies to improve their performance. N-type cells show the highest efficiency potential. N type PERC, PERL, or PERT cells are expected to show a higher efficiency potential than p-type cells compared to the 9th edition. This is mainly due to the expected introduction of passivated contact cell concepts as discussed in Fig. 41b. We found that p- and n-type mono cells will reach 23.5% and 24.1% in 2029 with PERC, PERL, or PERT processes. Other n-type-based cell concepts like SHJ and back-contact cells, will reach higher efficiencies of up to 25.5%. Nevertheless, the color marking shows for HJT that reaching 24% and beyond in mass production is not yet ready for roll out whereas the improvements for all other cell concepts might be rolled out faster as indicated by the color marking. BSF cell techno-logy is expected to approach an efficiency of up to 20% with mc-Si and 21.5% with mono-Si material.

Fig. 45a, Fig. 45b, and Fig. 45c show the corresponding development of module power of typical 60-, 72- and 144 half-cell modules respectively for 156.75 x 156.75 mm^2 cells, considering the cell efficiencies shown in Fig. 44 and the cell-to-module power ratios shown in Fig. 35.

We assume acidic texturing for mc-Si and alkaline texturing for mono-Si. In addition, we consider pseudo-square mono-Si wafers with diagonals of 210 mm as discussed above in this chapter. Changes in module size are not considered.

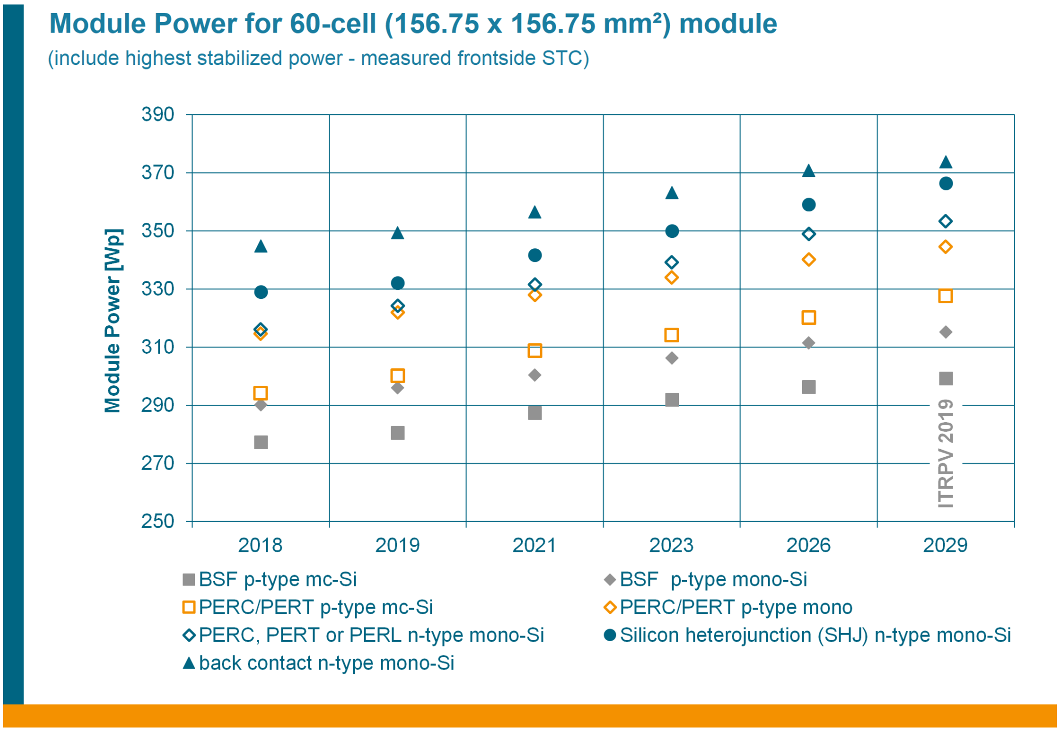

Fig. 45a: Predicted trend curve for module power of 60-cell modules for different c-Si cell types.

It should be noted that for modules with high efficiency back-contact cells, which are not yet available on 156.75 x 156.75 mm² wafers, the module power values given in Fig. 45a and 45b represent equivalent values in order to enable a better comparison with double-side contact technologies. 60-cell Modules with mc-Si PERC cells will achieve module power classes of 330 W by 2029. Modules with mono-Si p- and n-type PERC cells have today about 315 W and will achieve a power output of 345 W for p-type and 352 W for n-type by 2029, as shown in Fig. 45a. Modules with SHJ cells have today 330 W and in 2029 358 W.

The calculated corresponding module power of 72 cell modules is visualized in Fig. 45b. P-type PERC modules will surpass in 2029 395 W for mc-Si and 415 W for mono-Si. N-type PERC cells will enable power classes up to 425 W in 2029.

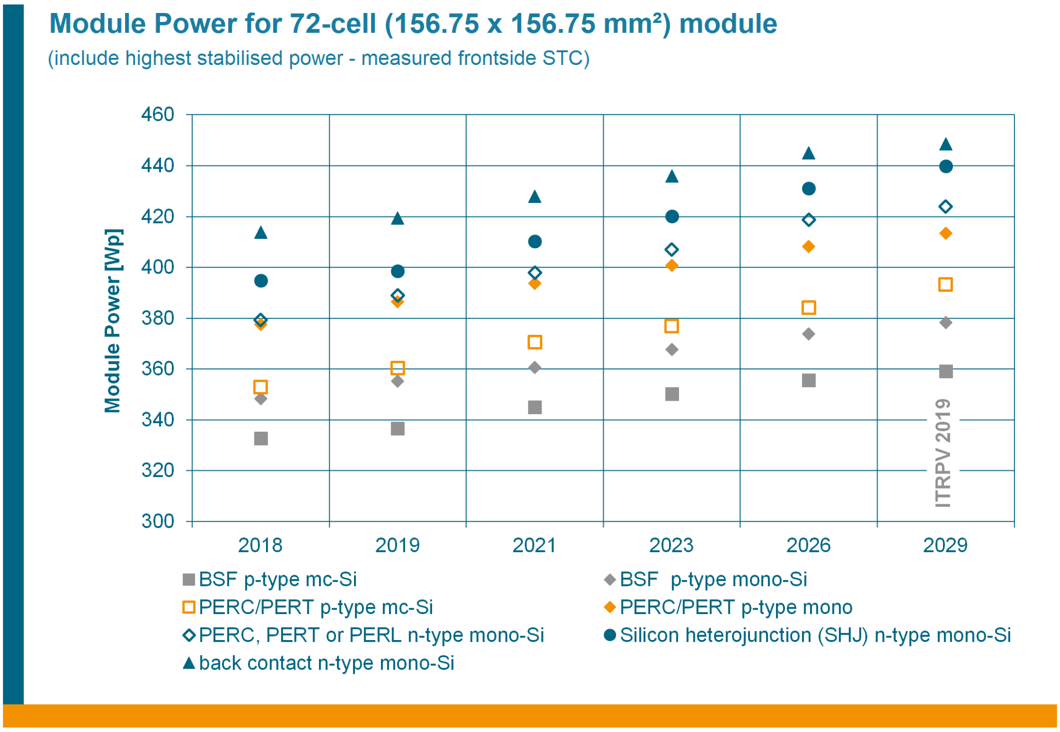

Fig. 45b: Predicted trend curve for module power of 72-cell modules for different c-Si cell types.

Modules that use half-sized cells were introduced in the market in order to reduce interconnection losses and therefore improving the CTM. Since this technology requires an additional process step for cutting the cells, as well as a modification of the stringer equipment, it has an impact on the module manufacturing process. Nevertheless, the benefit in module power is remarkable. Fig 45c compares the module power trend of 72-cell and 144-half-cell modules with 156.75 x 156.75 mm² PERC cell concepts. Half-cell modules will reach between one and two power classes more than full cell modules of the same PERC cell type. So, 395 Wp power class are expected to be common in 2019 mass production for p- and n-type PERC 144 half-cell modules.

As shown in Fig. 46, it is expected that the market share of half cells will continue to grow from 13% in 2019 to nearly 40% in 2029. In addition, we expect the appearance of modules with quarter cells after 2021.

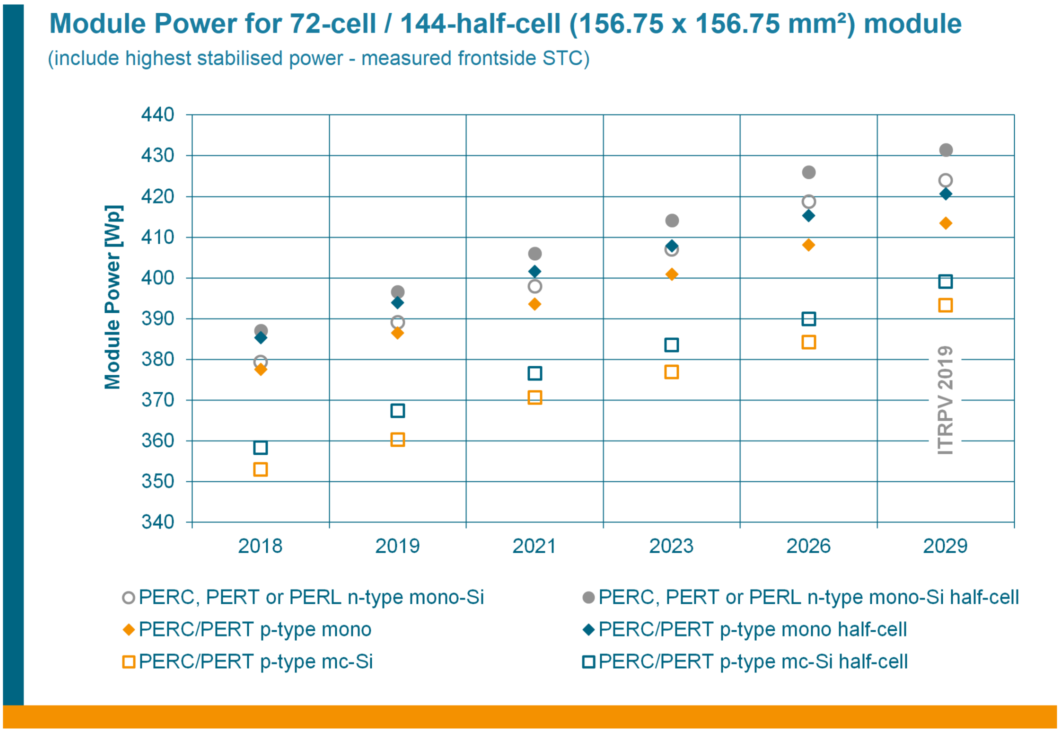

Fig. 45c: Module power trends of 72-cell and 144-half-cell modules with different PERC c-Si cell types.

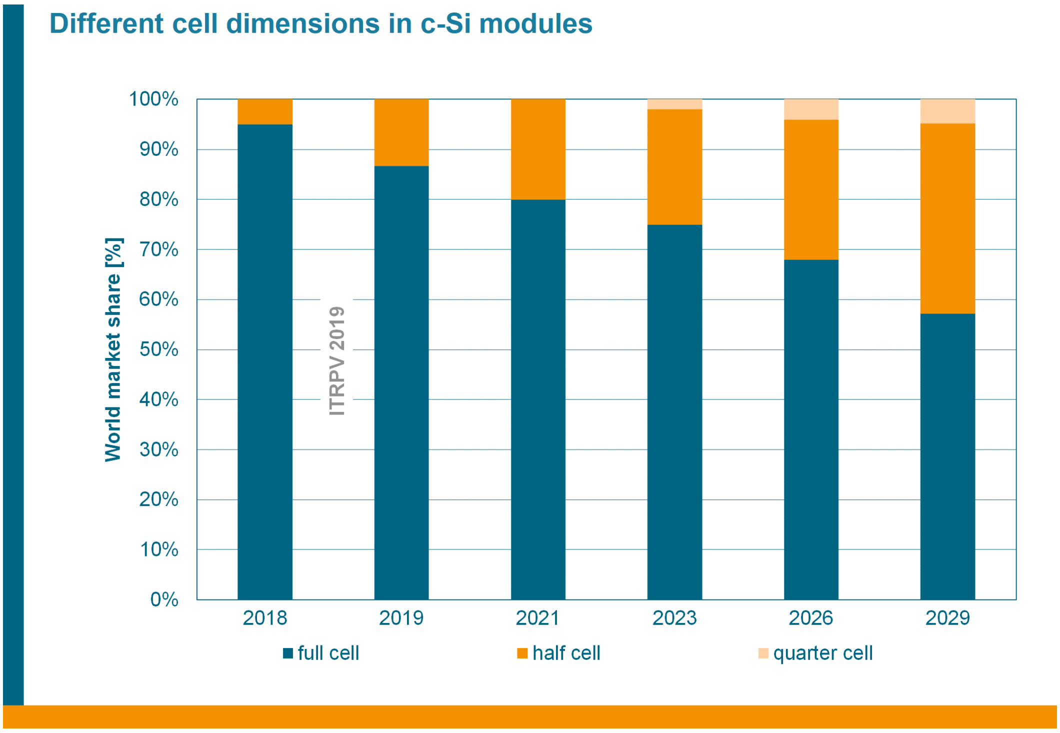

Fig. 46: Predicted market shares for modules with full, half, and quarter cells.

Fig. 47 shows that the module market splits into two main sizes: 60-cell and 72-cell modules. 96-cell modules are for special markets. The larger module sizes are mainly used in utility applications. Other module sizes for niche markets (e.g. 48 and 80 cells) are expected to account only for less than 2% of the market during the next years. Today´s mainstream modules (60-cells) will lose market share.

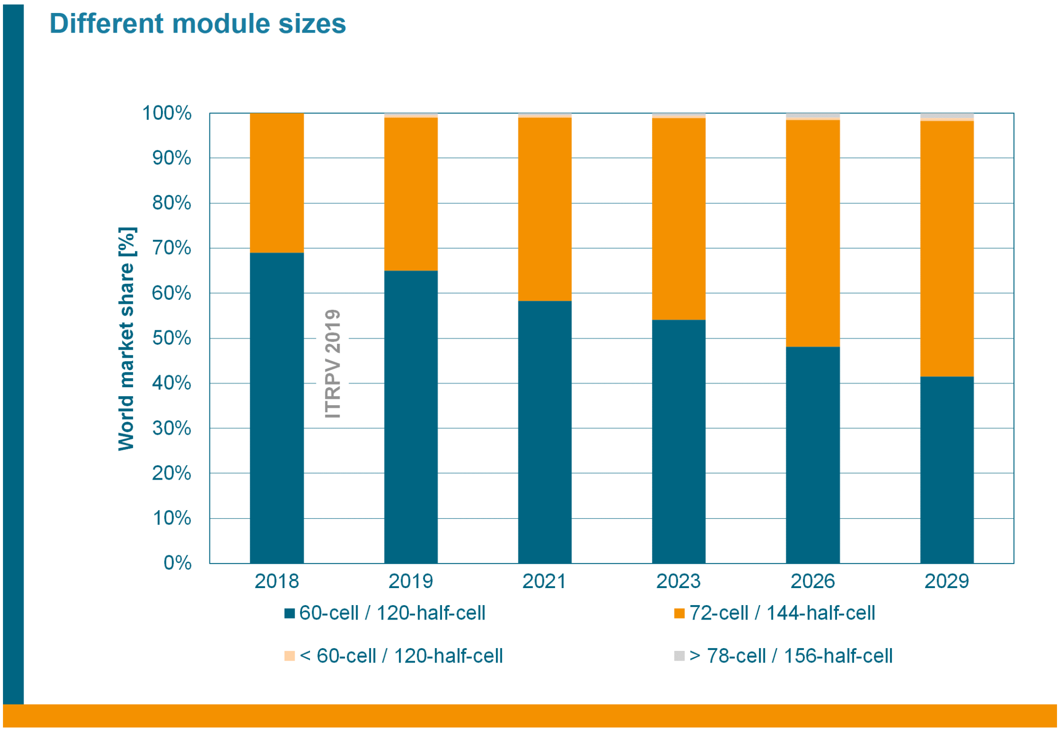

Fig. 47: Market shares of different module sizes with 156.75 x 156.75 mm² cells.

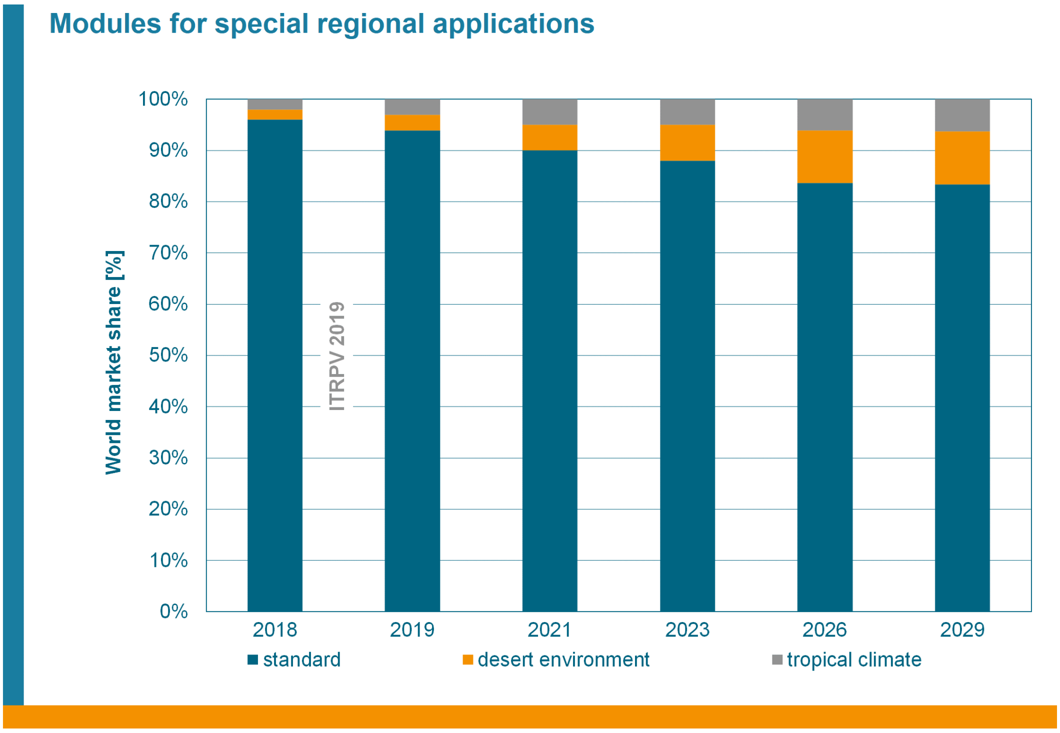

Fig. 48: Market share for special regional applications.

Another trend is the development of modules for special markets and environmental conditions. Fig. 48 shows the assumed market share of modules for special environmental conditions like for desert and for tropical climate conditions. It is still expected that the main market in 2029 will be for standard modules and that below 20% will be produced for special regions.

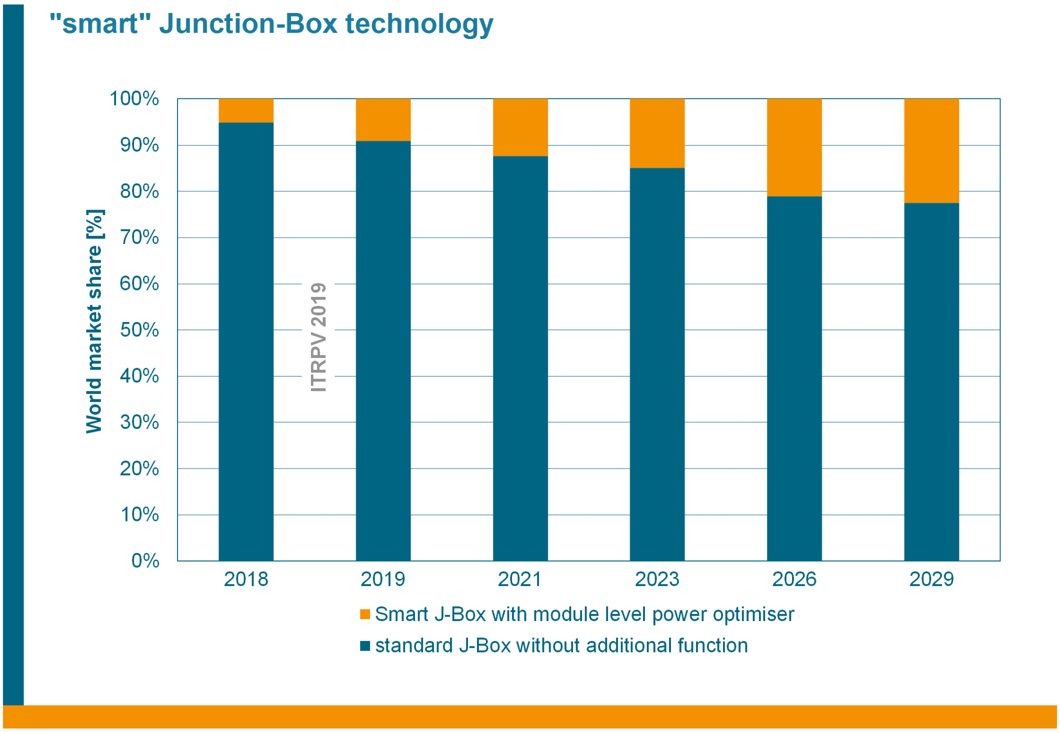

Fig. 49: Market trend for different J-Box functionalitie - smart vs. standard junction box.

So-called smart J-Box technologies are anticipated to improve the power output of PV systems. As can be seen in Fig. 49, the participants in our survey believe that standard J-Box without any additional function except the bypass diodes will clearly dominate the market over the next 10 years.

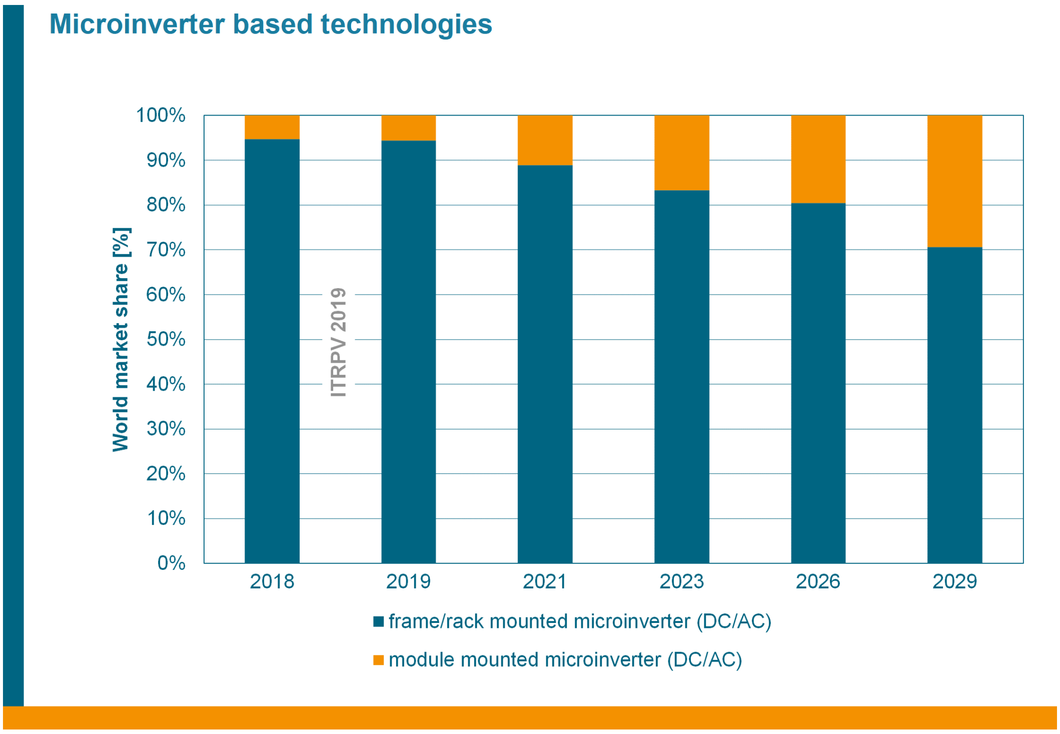

Fig. 50: Market trend for microinverter technologies (10% of the modules in 2028 are expected to include microinverters).

Standard junction boxes will stay mainstream. Fig. 51 describes the expected trend of additional cost for smart junction boxes with different functions.
The installation of new capacities for c-SI cell and module production will continue. In order to benefit from the economy of scale the construction of larger fabrication units is expected.

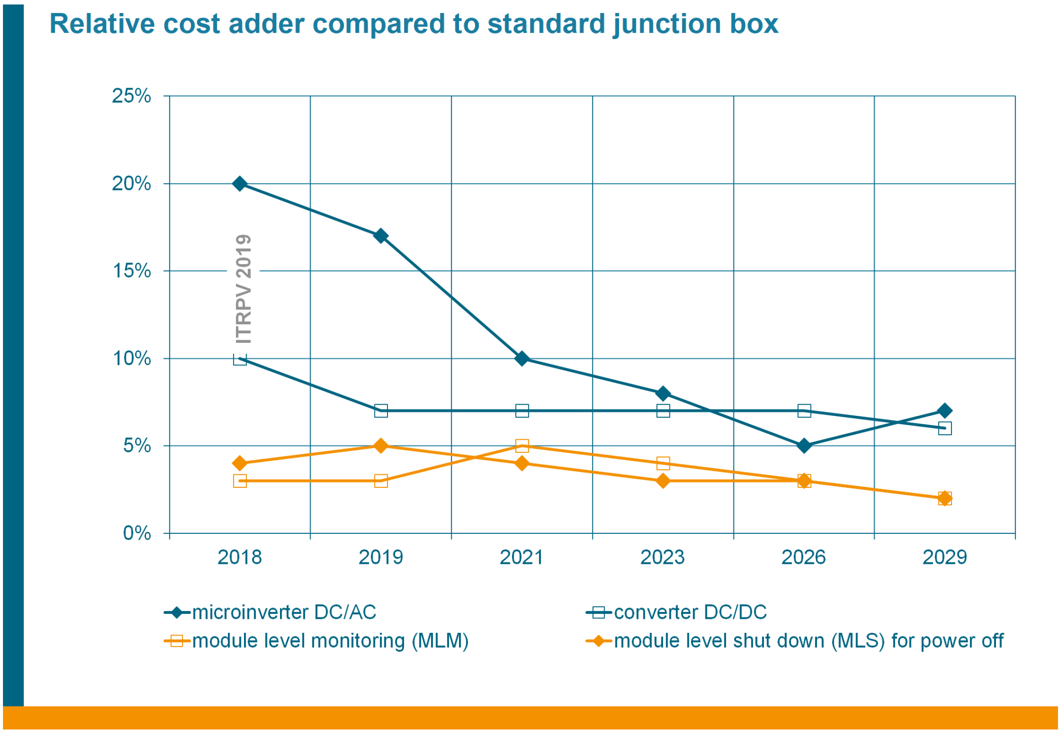

Fig. 51: Trend of cost adder for special junction box applications.

We find a dominating market share of factories with a production capacity >2 GW. Fabs with <500 MW production capacity will disappear during the next 10 years as shown in Fig 52a.

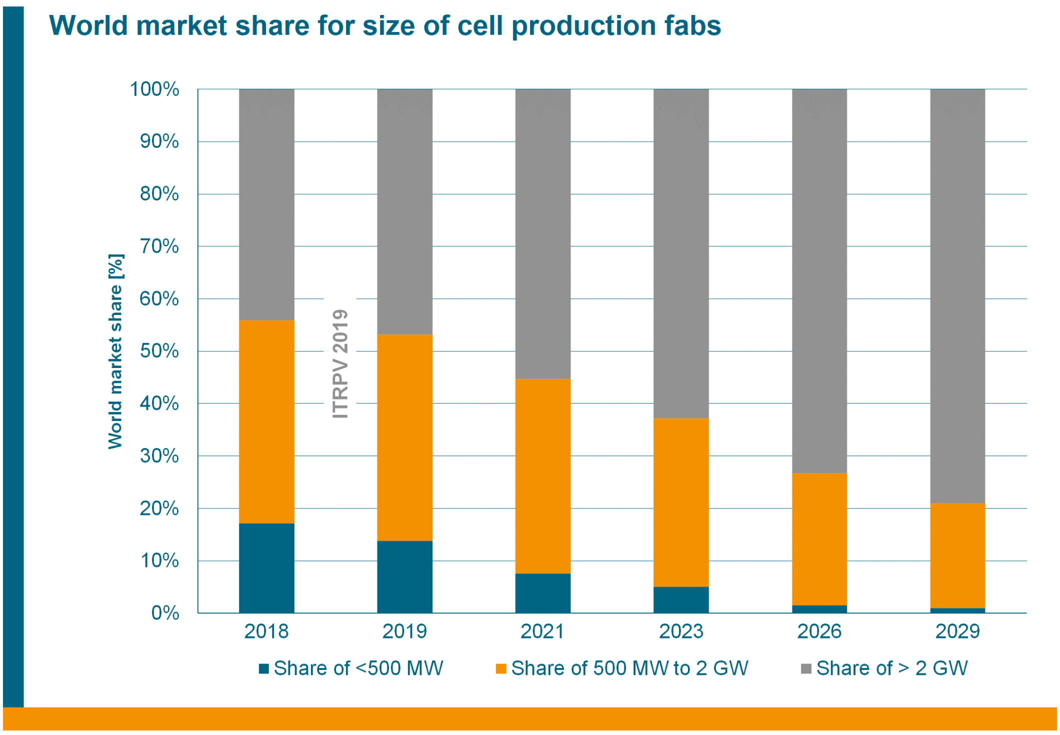

Fig. 52a: Trend for name plate capacity of cell manufacturing fabs.

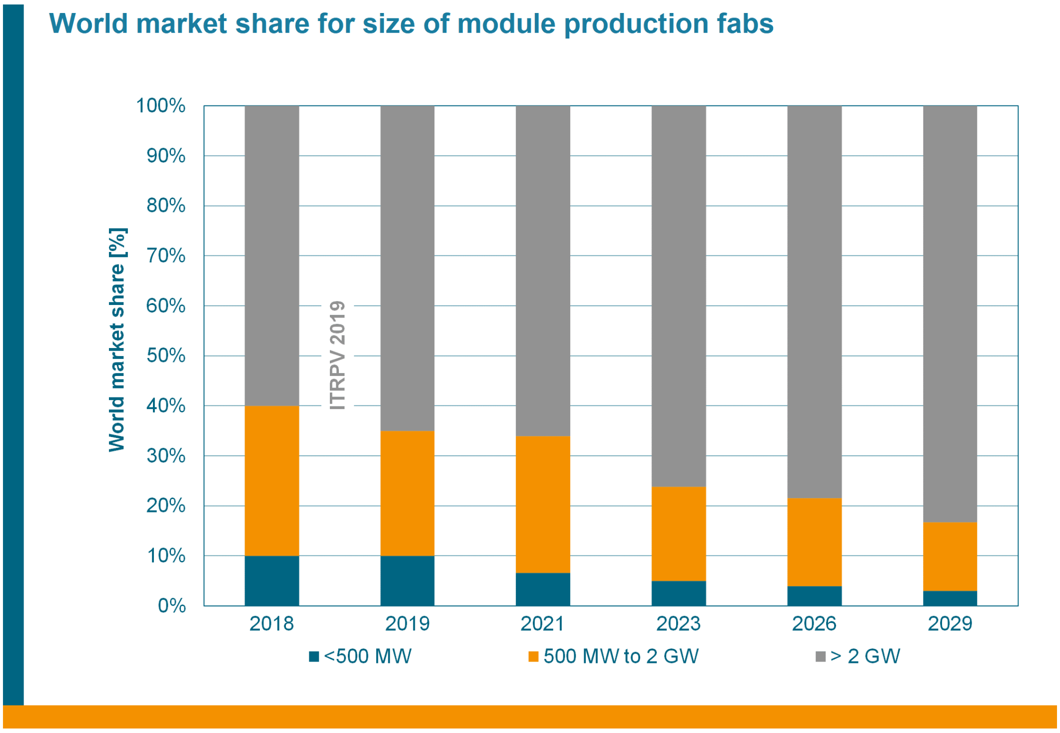

Fig. 52b: Trend for name plate capacity of module manufacturing fabs.

The trend for module production fabs is similar as shown in Fig. 52b. Nevertheless, smaller module fabs with <500MW are expected to be used for special applications with a share of about 2% in 2029.

6. PV systems

Due to the significant reduction of PV module prices over the last few years, balance of system (BOS) costs have become a crucial factor in overall system costs and thus the levelized cost of electricity (LCOE) as well. Besides warranties for the product and the product performance as well as the degradation of the modules during the operation lifetime an increase in system voltage and the trend to install more 1-axis tracking systems are important parameters to reduce LCOE.

Fig. 53 shows the estimated trend of warranty requirements and degradation parameters for the next years. The product warranty is expected to increase from 10 years to 12 years and perspectively to 15 years in the long run whereas the performance warranty is considered to increase to 30 years from 2021 onwards. The degradation after the 1st year of operation will be reduced from currently 2.5% to 2% from 2021 onwards. This is mainly linked to the control of light induced degradation (LID) and light and elevated temperature induced degradation (LeTID), latter especially in the case of module products with rear side passivation cell. Understanding the degradation mechanisms and a tight control of the degradation are mandatory to ensure this warranty [22, 23]. Standards for LeTID testing are about to be developed.

Yearly degradation is expected to be reduced slightly from 0.7% today stepwise to 0.5% over the next years. The color marking in Fig. 53 indicates, that first year degradation of 2% and the annual degradation limit of 0.5% may be implemented faster as industrial solutions are known by today.

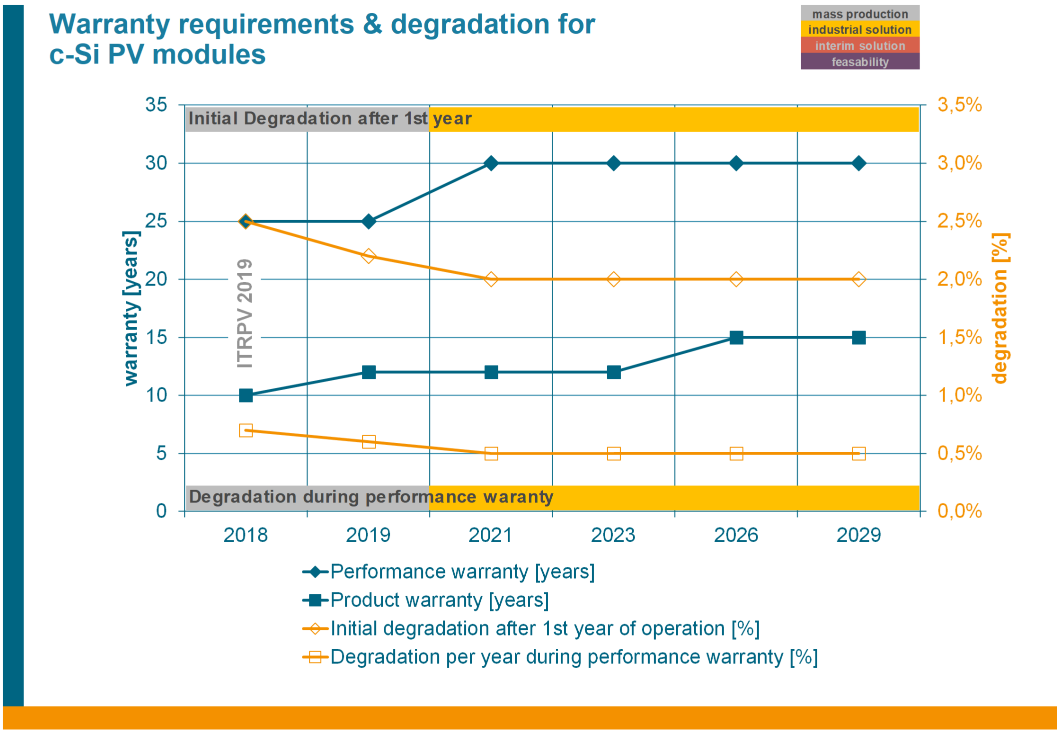

Fig. 53: Expected trend for product warranties and degradation of c-Si PV modules.

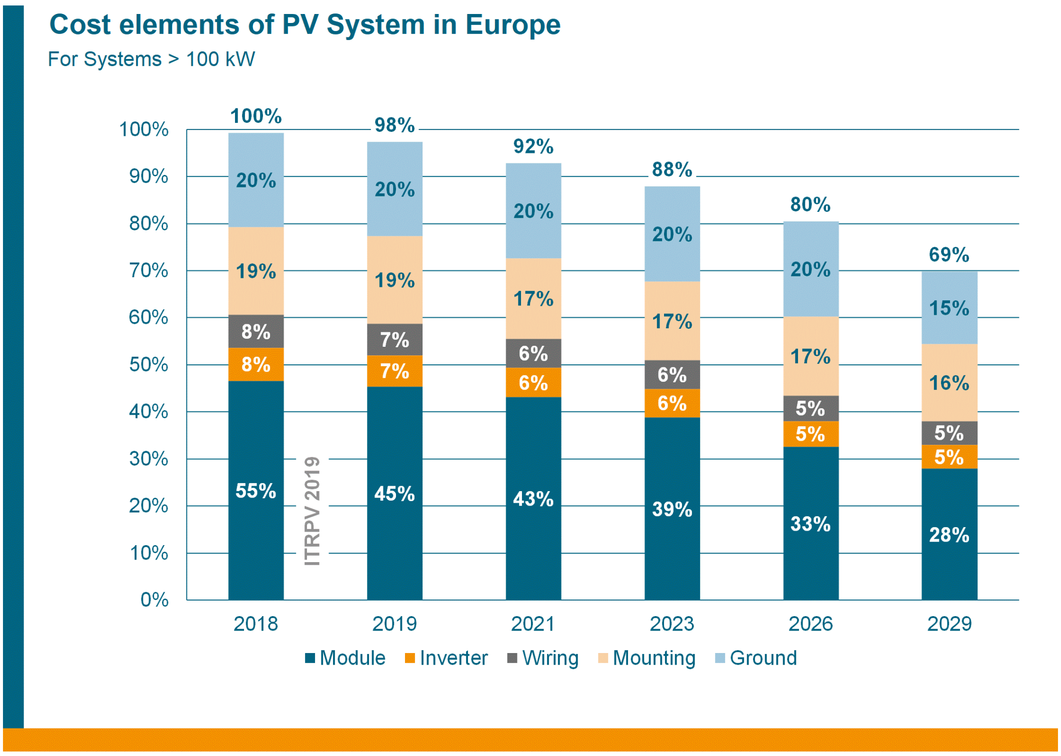

Fig. 54a: Relative system cost development for systems > 100 kW in Europe (2018 = 100%).

In Figures 54a, 54b, and 54c, the relative developments of system costs for large systems >100 kWp in Europe, the US, and Asia are shown. It should be noted that no “soft costs,” such as costs for permits or costs for financing, are included, as these costs may vary significantly from country to country. Excluding the "soft costs," the distribution of system costs as well as the development over time are expected to be comparable in Europe and Asia.

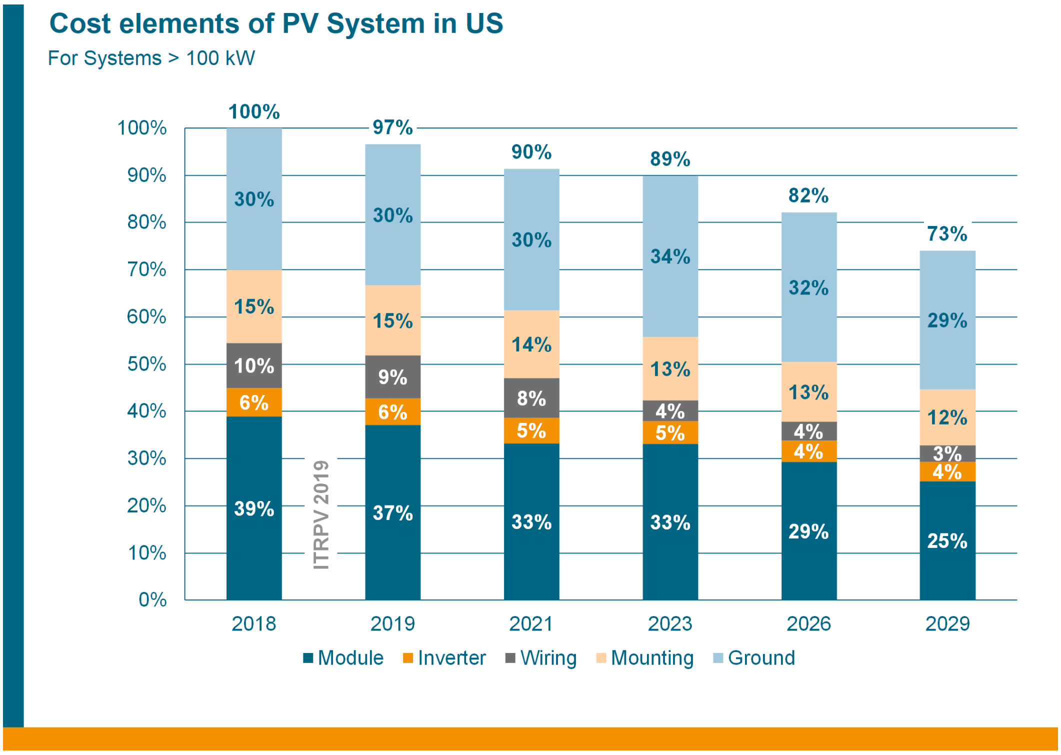

Fig. 54b: Relative system cost development for systems > 100 kW in the U.S. (2018 = 100%).

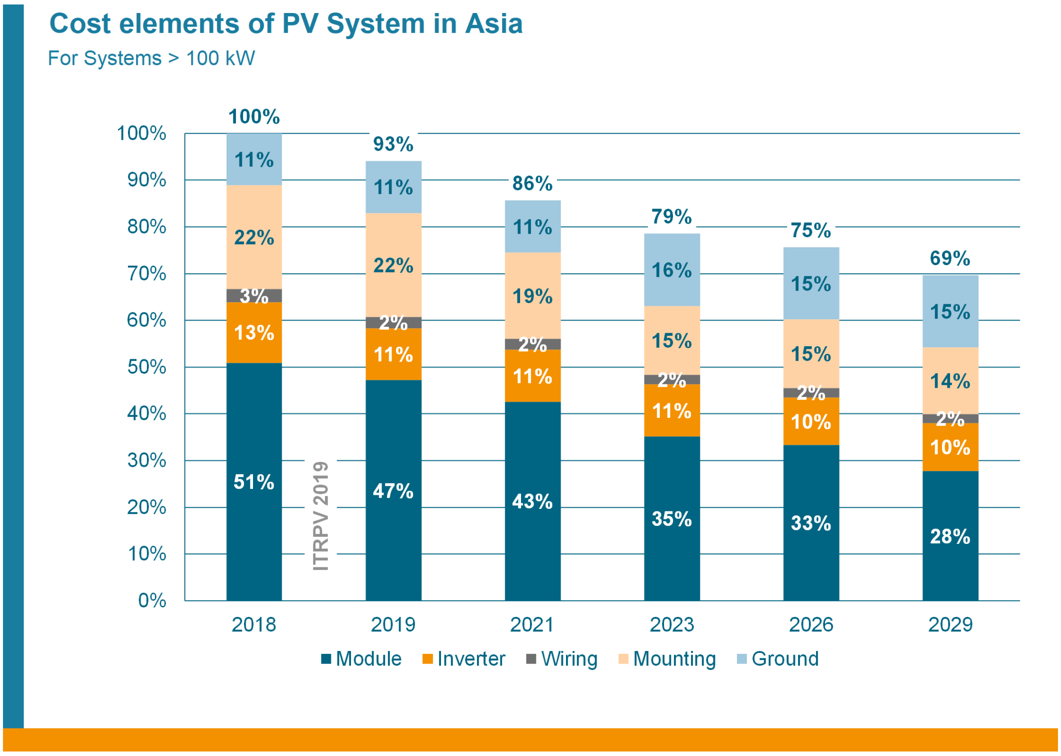

Fig. 54c: Relative system cost development for systems > 100 kW in Asia (2018 = 100%).

As can be seen by comparison of Fig. 54a-c, the overall trend for system cost reduction during the next ten years is expected to be similar for Asia, Europe, and the U.S. with a slightly higher decrease for Europe and Asia. Due to differences in absolute system costs, the relative distribution between the cost components of module, inverter, wiring, mounting, and ground is expected to be different. The major differences can be seen in the share of the ground costs as compared to the system costs. It is expected that the ground costs share will constantly stay higher in the U.S. compared to Europe and Asia. This also explains the lower overall system costs in Europe and Asia.

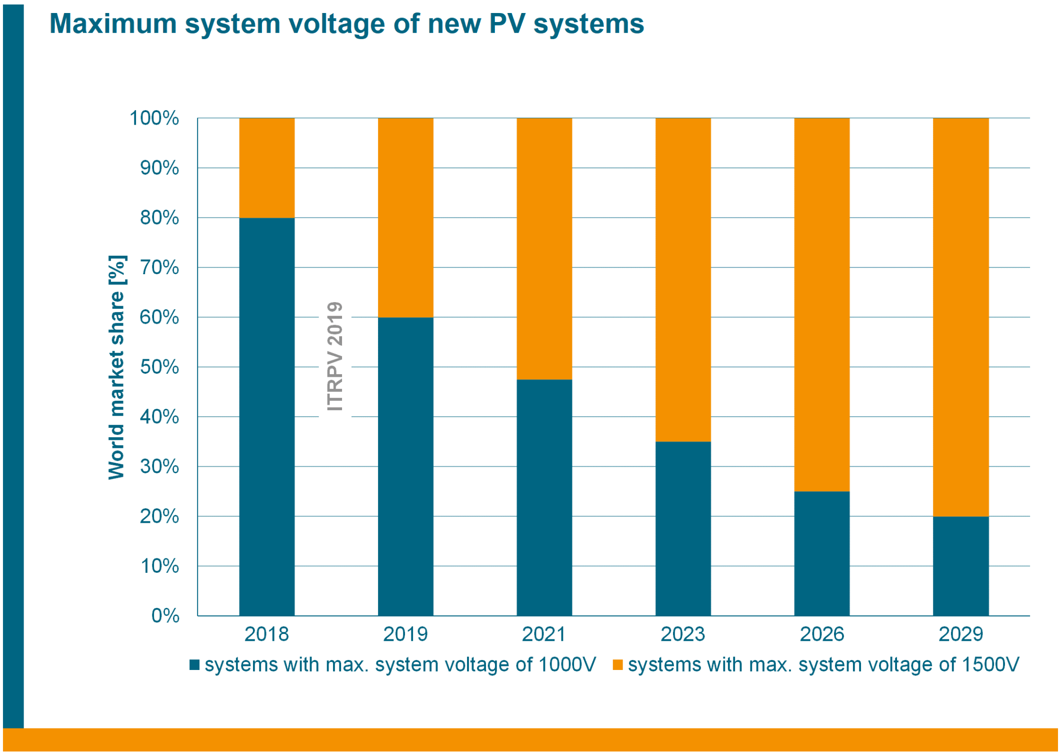

Fig. 55: Trend of maximum system voltage for systems >100kW.

One trend to be expected on system level is the trend toward an increase of system voltage from 1,000 V to 1,500 V – from 2021 onwards the market for 1500V systems will be >50%, attaining a market share of >75% from 2026 onwards (see Fig. 55). The increase in system voltage represents an important measure for lowering resistive losses and/or BOS costs by reducing the required diameter of the connection cables within a PV system.

Furthermore, the average module power class for systems >100 kWp is expected to increase from 290 Wp in 2018 to about 350 Wp for 60-cell modules, and from 340 Wp to 400 Wp for 72-cell modules (see Fig. 56). This also should significantly support the reduction of all area-dependent BOS costs.

Another long-term trend on system level is to use tracking systems in order to maximize the energy output of PV-systems. The market share of tracking systems in large scale c-Si based PV-systems is shown in Fig. 57. 1-axis tracking systems will increase the market share from approximately 30% in 2018 to >50% from 2023 onwards. In contrast, 2-axis tracking will remain negligible for c-Si technology with a (constant market share of around 1% during the next decade).

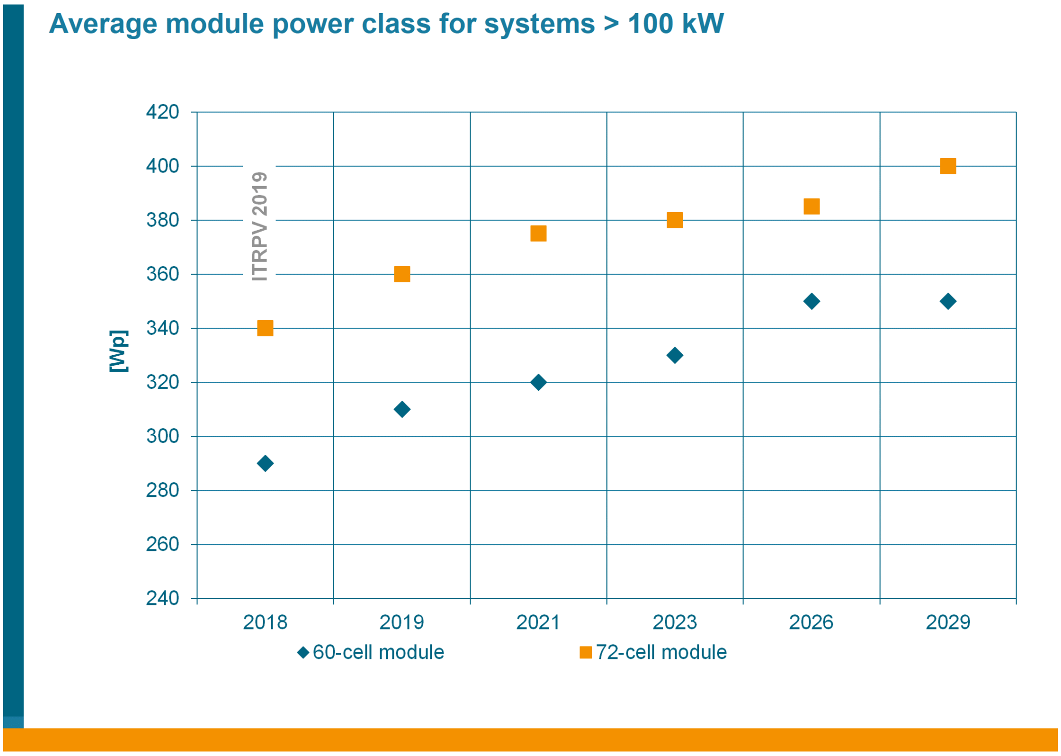

Fig. 56: Trend of average module power class for utility applications with >100kW.

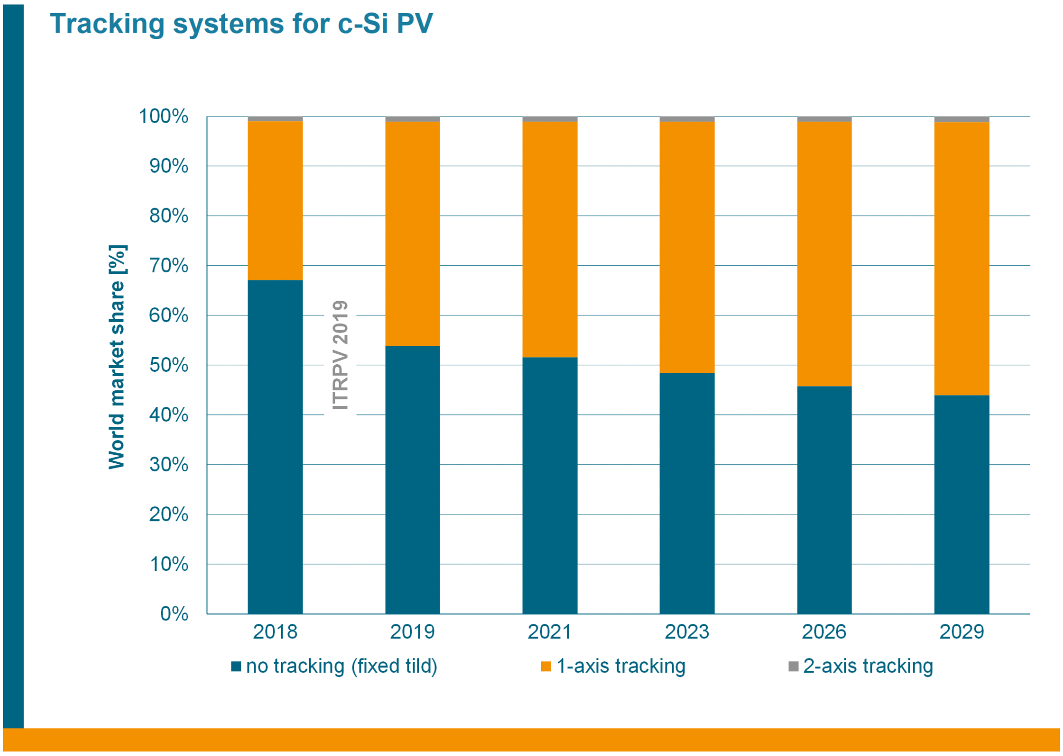

Fig. 57: Market share of tracking systems for c-Si PV installations.

This year for the first time we include the new trend chart with regard to the application of PV systems into the ITRPV. While the fraction of roof top systems will remain between 30% and 40% for the next decade the fraction of ground-based power plants will reduce from 60% to 50% related to the emerging trend of floating PV. Building-integrated PV is expected not to exceed 5% in the next 10 years timeframe.

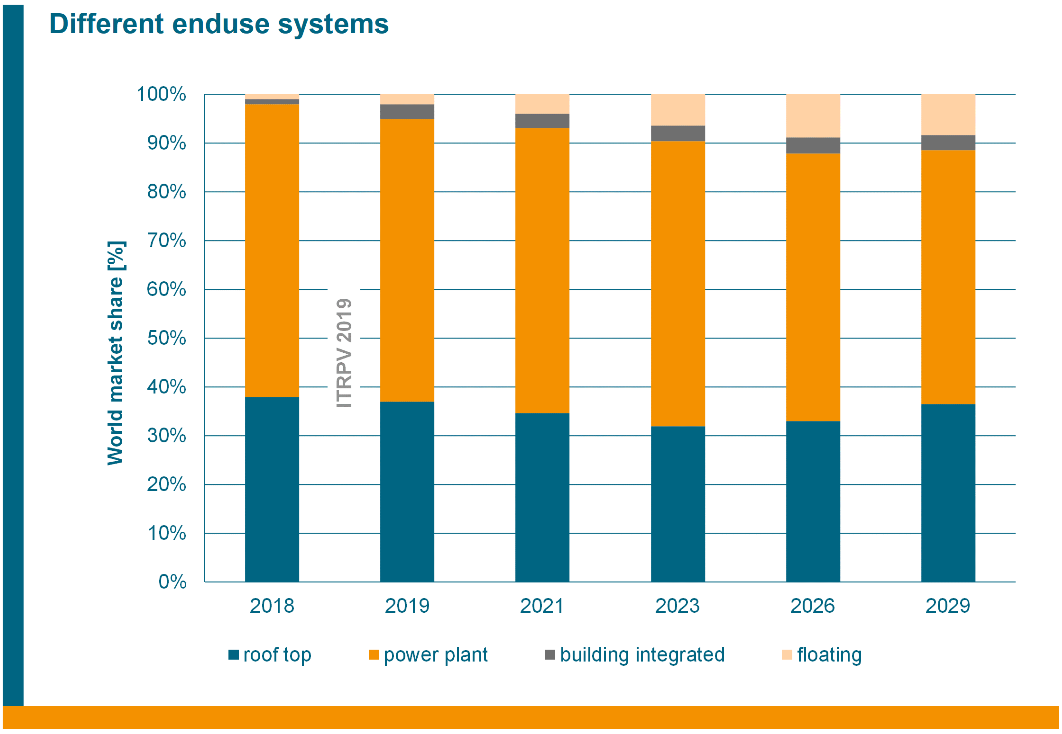

Fig. 58: Share of PV system applications in enduser markets.

System levelized cost of electricity (LCOE) is a commonly recognized economic metric for comparing the relative costs of different renewable and non-renewable electricity generation technologies. To estimate 2018 benchmark and future scenarios of PV power generation costs, we have used NREL's System Advisor Model (SAM) to calculate the LCOE in USD for large PV systems deployed in different insolation conditions (see Fig. 59) [23, 24]. Actual system prices and cost drivers are strongly dependent upon location. We have assumed a total 650 USD/kW$_{(DC)}$ system capital costs in 2018. The so-called 'soft costs' including project developer and installer overhead and profit, sales tax, contingency, and interconnection and permitting fees could add around another 250—400 USD/kW$_{(DC)}$ for large-scale systems in the U.S. and Europe in 2018. Project soft costs and labor costs typically have the greatest variance across the globe and from project-to-project. The system cost trends depicted in Fig. 52 assume that total direct costs will decline to around 450 USD/kW$_{(DC)}$ in 2029.

As can be seen in Fig. 58, LCOE values between 0.026 and 0.066 USD are calculated to be feasible today, depending upon the insolation level. Considering the system price trends anticipated by the ITRPV (see Fig. 52, 53, 54), PV LCOE in the range of 0.02 to 0.05 USD are predicted by the year 2028. It is important to note that, along with the system price and the insolation level, LCOE is also strongly dependent upon operations and maintenance issues, the project financing structure and the usable service life of the system. For our calculations we have assumed 25 years of usable system service life; however, it is expected that advances in module and BOS technology as outlined in the ITRPV could enable an extension of the system service life to 30 years or maybe even more. Advances in system life would make it possible to reduce LCOE levels even further. Lower financing rates due to PV becoming a lower risk electrical energy generation technology may also allow the 2028 LCOE levels to be reached earlier. This could make PV power generation a more cost-competitive and valuable contributor to the world's future energy mix, as will be discussed in the next section.

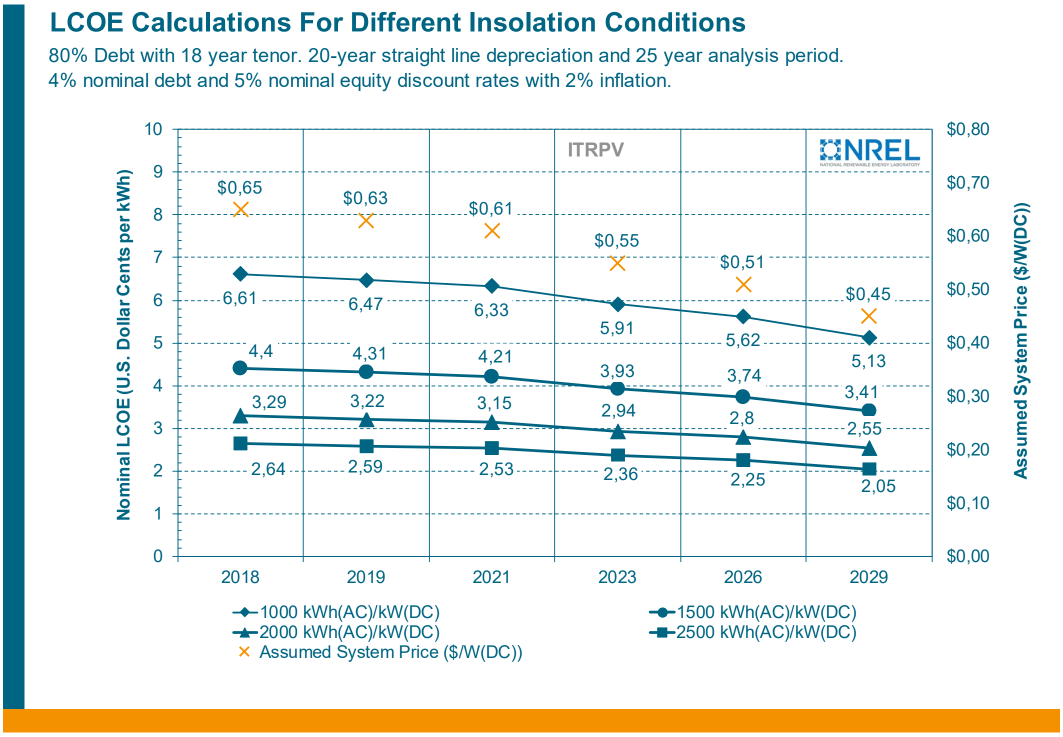

Fig. 59: Calculated LCOE values for different insolation conditions. Financial conditions: 80% debt, 18-year loan tenor, 20-year straight line depreciation and 25 years usable system service life. 4%/a nominal debt rate, 5%/a nominal equity discount rate, 2%/a inflation rate. The calculations were performed using NREL's System Advisor Model (SAM)[23].

7. Outlook

7.1. PV learning curve

We discussed in Chapter 3 the current learning curve situation. Fig. 1 shows the price learning curve and the calculated price learning rate. The learning rate was calculated to be 23.2% by using all data points between 1979 and 2018. However, considering only the data points since 2006, the learning rate is 39.8% as shown in Fig. 60a.

2006 was the last year of a longer period of Silicon shortage. It marks the beginning of c-Si PV mass production in China and thereby the entry into a period of continues capacity extensions after the scarcity situation of silicon and modules during the period between 2004 and 2006.

Based on the above findings we started in the 8th edition the analysis about the breakdown to the two basic learning contributors – module power learning and reduction of price (cost) per piece.

Table 3 summarizes average module efficiencies at different years. The price values were taken from the learning curve while module efficiencies were assumed as average module powers of p-type mc-Si and mono-Si modules of ITRPV reports (3rd to 10th edition) the module efficiency of 1980 was found in [26]. A 64% increase in module power was realized during the 30-year period from 1980 to 2010. The yearly average power learning from 2010 to 2018 was between 1% and 4% while per-piece learning varied between -9% and up to 35%.

Learning curve for module price as a function of cumulative shipments

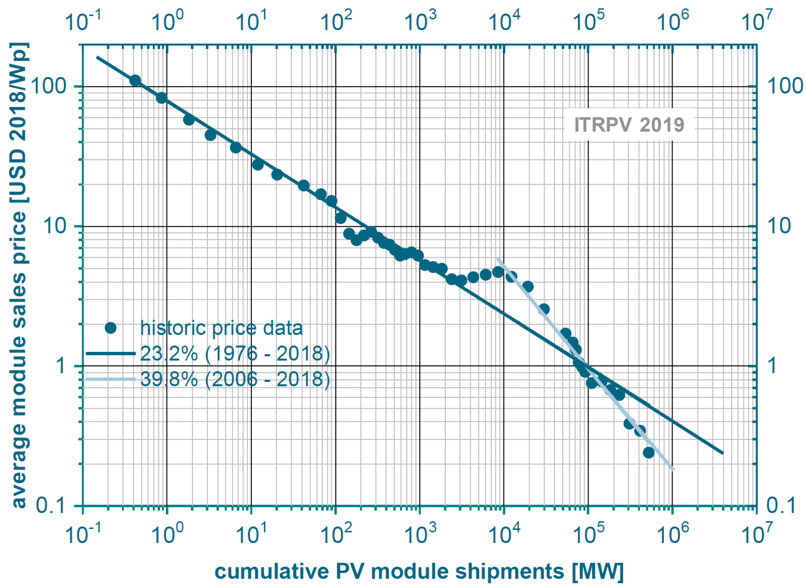

Fig. 60a Learning curve of module spot market price as a function of cumulative PV module shipments and calculated learning rates for the period 1979 to 2018 and 2006 to 2018 respectively.

Year over year learning

Year	1980	2010	2011	2012	2013	2014	2015	2016	2017	2018
avg. Module power p- type (ITRPV-data)	147.6	241.5	248	253	262	267.5	278.5	287.5	290	302.5
Module efficency [%], avg. Mod. area: 1.64m²	9 [25]	14.7	15.1	15.4	16	16.3	17	17.5	17.7	18.4
Module price [$2018]	36.57	1.7	1.06	0.75	0.78	0.67	0.62	0.39	0.34	0.24
relative module price reduction [%]		95.34	37.77	28.84	-2.84	13.21	7.83	37.65	11.08	30.27
Module price (Wp-increase only) [USD(2018)/Wp]		1.7	1.66	1.63	1.57	1.54	1.47	1.43	1.42	1.36
Module price (cost reduction per piece only) [USD (2018)/Wp]		1.7	1.11	0.83	0.91	0.84	0.85	0.660	0.63	0.59

Table 3. Yearly learning for module efficiency and price per piece based on module price data (2010 = 100%) [5, 6, 7], module efficiencies calculated from ITRPV module power values (3rd to 10th edition); 1980 module power is calculated from efficiency in [25].

Fig. 60b shows the plot of data points for Wp learning and per piece learning according to Table 1. The calculated corresponding learning rates of 6.7% for Wp learning and 24% for per piece learning indicate that the main contribution of the price learning arose from per piece reductions. This is in line with the findings in [4] and emphasizes again that only the combination of Wp learning and cost re-

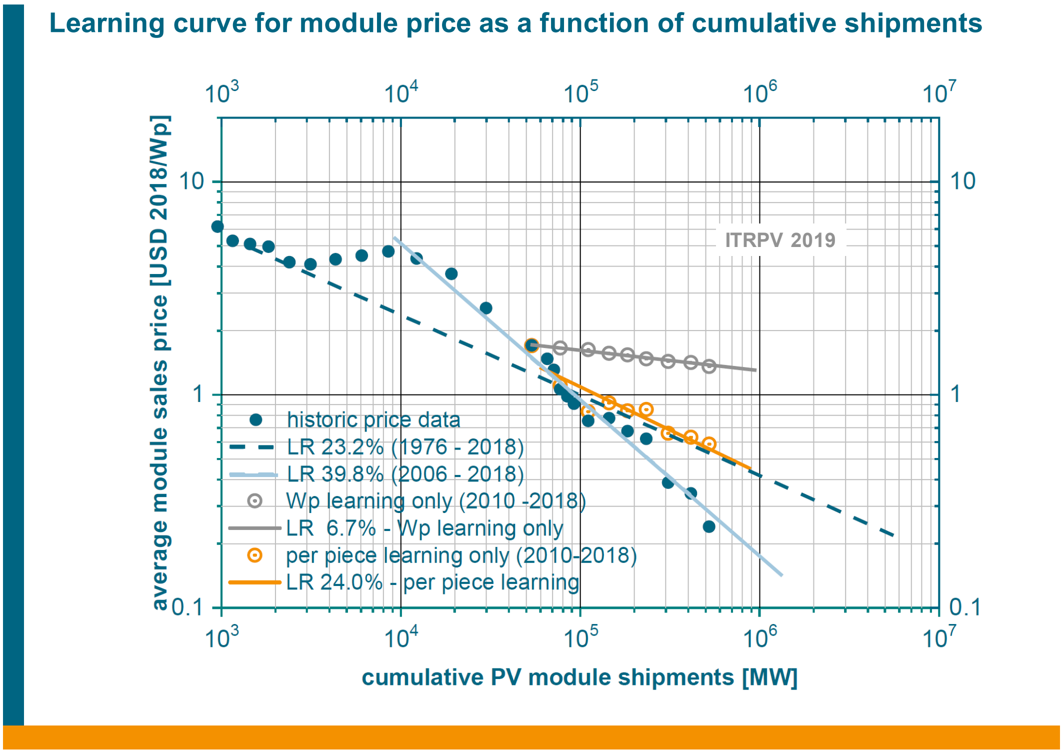

Fig. 60b Learning curve of module spot market price as a function of cumulative PV module shipments, update on calculated learning rates for the period 1979 to 2018 and 2006 to 2018, calculated rates for Wp learning and per piece learning according to table 3.

duction grants the resulting learning. Nevertheless, it can be concluded that the current price situation is not only due to cost learning but also caused by the market situation. Manufacturers are struggling with low margins as prices are expected to remain close to the manufacturing cost as was stated in [27].

7.2. PV market development considerations

The most widely publicly discussed PV-related topics and trends are installed PV module power, module shipments, as well as scenarios about the PV generated electricity. PV will play a key role in a future net zero greenhouse gas emission energy system that has to be installed around 2050 [28].

A look at the supplier side, to follow the market development of PV modules, cells, wafers and polysilicon, is less spectacular, but it is essential for investment planning. The analysis of the annual PV market development until 2050 was started in the ITRPV 6th edition. In the following section, analyses of previous ITRPV editions and results of a recent study about a global energy system based on 100% renewable energy is discussed in view of 2018 PV installation results.

We consider four scenarios that superimpose the calculated results for different world regions:

1. Low scenario: (power sector) — 4.5 TWp installed PV in 2050, generating 7 PWh ≈16% of global electricity [27, 28].

2. Progressive scenario: (all sectors) — 31 TWp installed PV in 2070, generating 41 PWh ≈27% of global primary energy demand [31].

3. Electricity scenario: (power sector) — 22.0 TWp installed PV in 2050, generating 38 PWh ≈69% of global electricity [28].

4. Broad electrification: (all sectors) — 63.4 TWp installed PV in 2050, generating 104 PWh ≈69% of global primary energy demand (including power & heat, transport, and desalination) [32].

Details of the scenarios and the corresponding considered regions are summarized in Tab. 2.

Summary of regional results for the different scenarios

Scenario	Region	Installed power 2050 [TWp]	PV Power generation 2050 [PWh]
Low scenario	Africa	0,2	
	Americas	0,8	
	Asia	3,1	
	Europe	0,3	
	total	4,5	7,1
Progressive scenario	Africa	2,1	
	Americas	2,8	
	Asia	7,1	
	Europe	2,1	
	total	14,1	18,7
Electricity scenario	Sub-Saharan Africa	1,3	
	MENA	1,4	
	North America	2,5	
	Northeast Asia	7,4	
	SAARC	3,7	
	South America	0,8	
	Southeast Asia	2,4	
	Eurasia	0,4	
	Europe	2,0	
	total	22,0	38,1
Broad electrification	Sub-Saharan Africa	2,9	
	MENA	4,6	
	North America	7,0	
	Northeast Asia	17,8	
	SAARC	11,9	
	South America	2,3	
	Southeast Asia	5,3	
	Eurasia	2,6	
	Europe	8,9	
	total	63,4	104.3

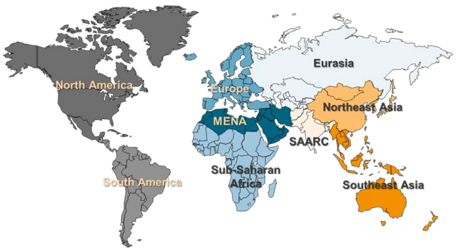

Table 4: Summary of regional results for the different scenarios.

Fig. 61 – 64 display these scenarios showing the calculated cumulated PV installation in 5-year steps, the corresponding 5-year average annual PV market without and with replacement after 25 years, and the historic annual shipments according to Fig. 1.

Fig. 61 illustrates scenario 1 - the most optimistic scenario out of three IEA approaches for the energy consumption and generation until 2050, based on assumptions about population growth and energy consumption behavior [29]. It considers the limitation of global temperature increase to 2°C at the end of the 21st century. This scenario assumes a PV installation of about 4.5 TWp being enough to cover 16% of global electricity demand in 2050. It was calculated with the logistic growth approach discussed in the 9th edition of the ITRPV [33]. Energy yield in this scenario is assumed to be about 1.6 kWh/kWp. The maximum addressable market is calculated to 273 GWp as 5 years average in 2030 (peaks at 350 GWp in 2028 and 600 GWp in 2050 were calculated in the 9th edition with annual calculation [33])

The logistic growth approach is limited due to the existence of a growth target – in our case the Installation volume. Looking at a timeframe of 40 years in the future a fix growth target seems uncertain despite the fact that there will never be unlimited growth. Electricity consumption per capita and heat demand will increase so considering a floating growth target within the next 40 years will be a smarter approach.

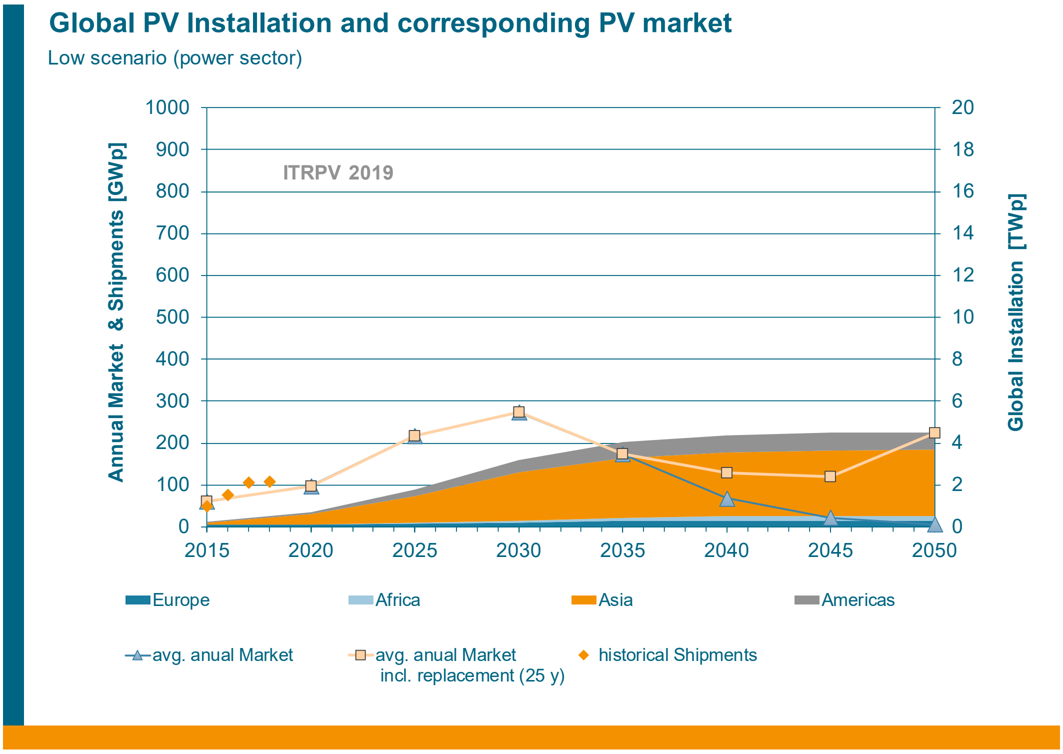

Fig. 61: Cumulative installed PV module power and 5-year average annual market calculated with a logistic growth approximation for the scenario, assuming 4.5 TWp installed PV module power in 2050.

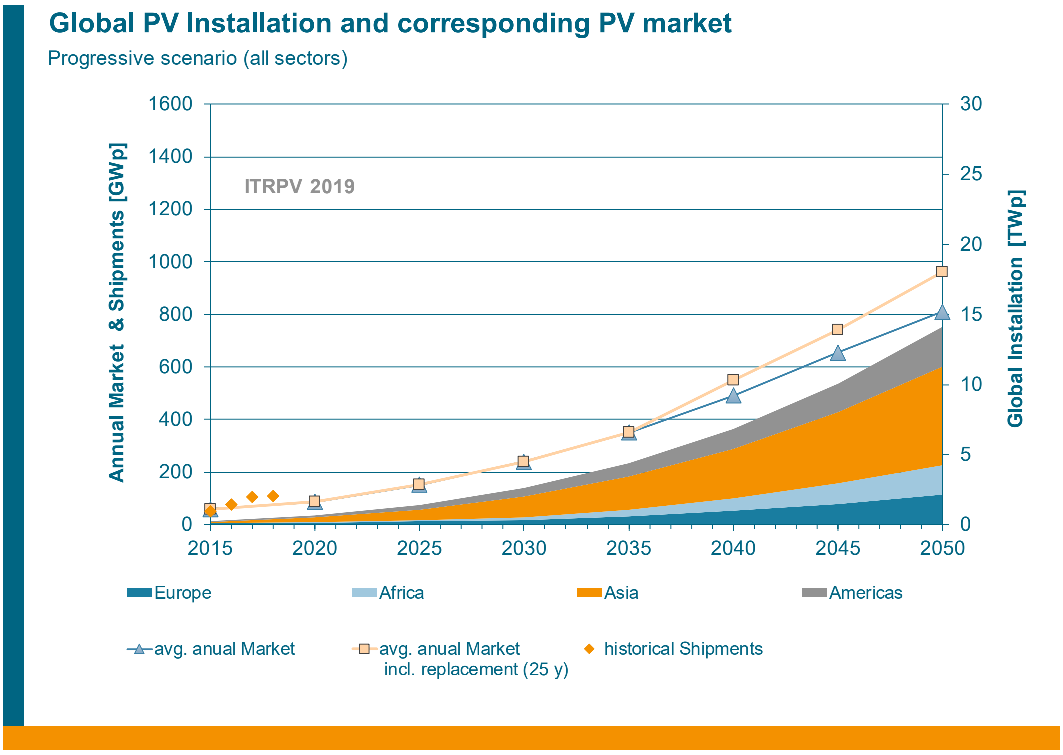

Fig. 62: Cumulative installed PV module power and 5-year average annual market for global PV module installation of 31 TWp in 2070 and 14 TWp in 2050 respectively (see Table 4 and [29]).

Scenario 2 is shown in Fig. 62. In this scenario we assume 14 TWp installed PV modules in 2050.

Energy yield in this scenario is 1.3 kWh/kWp. We did not use the logistic growth approach and therefore the annual market assumption shows continued growth. Assuming a replacement cycle of 25 years results in a steeper growth from 2035 onwards. The assumed average market size until 2018 is well below current shipments.

Scenario 3 and 4 consider as well as need a net zero greenhouse gas emission energy system no later than 2050. As PV is a key technology to reach this goal. To reach a 100% renewable energy and greenhouse gas emission free energy economy by 2050, considering the three main energy consumption field of power & heat, transportation, and desalination for 9 major global regions as summarized in Tab. 2, a model presented in [26, 30] is used.

The Electricity scenario is shown in Fig. 63 and considers the contribution of PV in a 100% renewable energy-based power sector [28]. The 22.0 TWp will generate approximately 38.1 PWh in 2050.

Fig. 64 shows the required PV installation trend to reach the Broad electrification scenario 4. This will be the path towards a zero-greenhouse gas emission economy in 2050

Scenario 3 and 4 consider an average system energy yield of approximately 1730 kWh/kWp and 1650 kWh/kWp respectively realized by power plant installations in higher insolation regions, also taking single-axis tracking with higher yields into account.

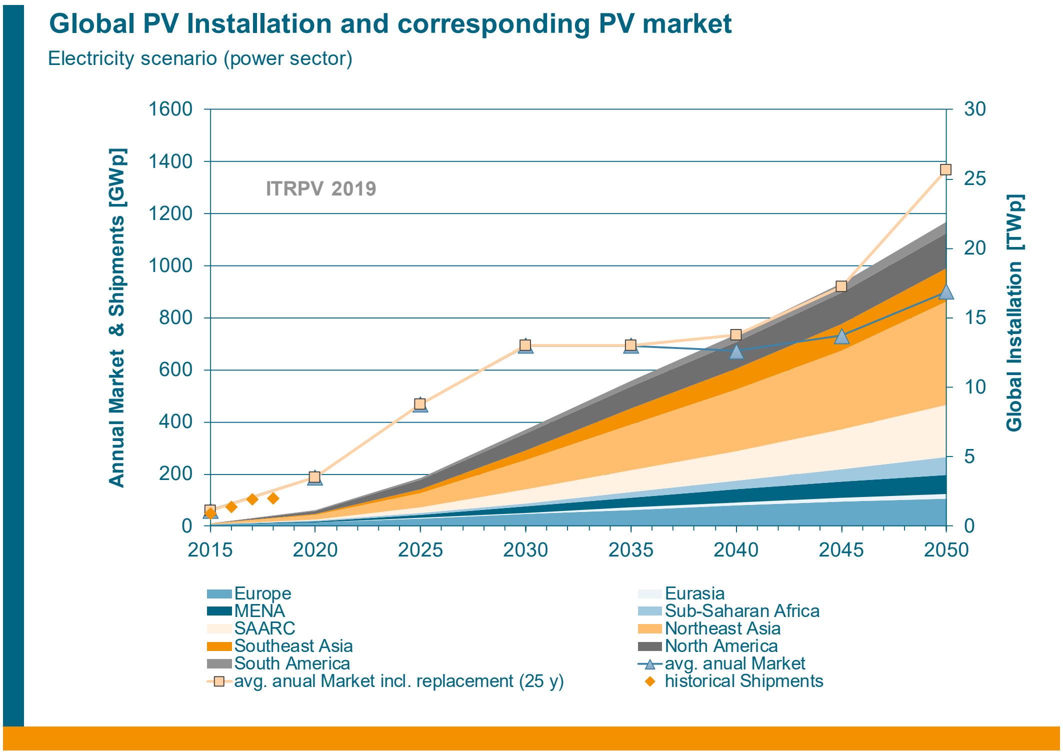

Fig. 63: Cumulative installed PV module power and 5-year average annual market for global PV module installation of 22.0 TWp in 2050 (see Table 4 and [26]).

It is remarkable that the historic shipments are nearly in-line with the required shipments in scenario 3 and 4.

All four scenarios show that there will be a considerable module market in the future – we may consider also higher growth scenarios as manageable. Nevertheless, there is a risk of overheated market present especially as production capacity is currently exceeding the shipments by about 50% as discussed in Section 1. A very high PV module demand is finally driven by the fact that PV electricity is the least cost source of electricity globally and very low-cost PV electricity drives power-to-X demand so that other energy sectors can also benefit from very low cost PV. Scenario 4 assumes a broad electrification for fulfilling the targets of the Paris Agreement for a least cost energy system.

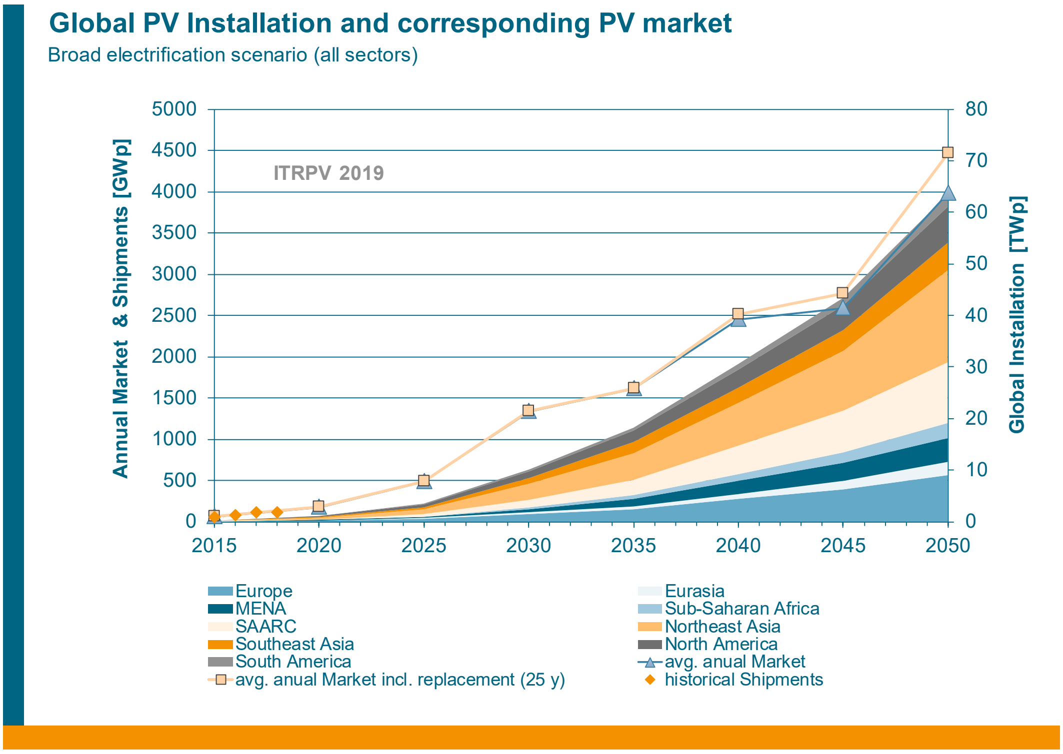

Fig. 64: Cumulative installed PV module power and 5-year average annual market for global PV module installation of 63.4 TWp in 2050 in a zero greenhouse gas emission economy - broad electrification (see Table 4 and [30]).

The scenarios 1 and 2 will be no challenge at all for the PV industry. Production capacities of up to 1 TWp seam manageable also with the current mainstream technologies. Production capacities beyond 1 TWp appear more challenging.

Beside the expected increase of PV installation and production, recycling needs will become more important in the future – both as business opportunity and as challenge [34].

Progressive tool concepts in cell manufacturing for production lines with matched throughput between front and backend, as discussed in Section 5, will support future production capacity increase. Anyhow, a further increase of production beyond the 1 TWp level will require new and lower cost production technologies.

PV equipment suppliers have currently to support upgrades of existing production capacities for new technologies such as PERC and the installation of new production capacities. New c-Si capacities will be implemented mostly for the maturing PERC concepts but also for n-type HJT technologies.

The continued support of depreciated production lines, the replacement of worn-out equipment and the support of upcoming capacity expansions will constitute a considerable business segment in the future. All of this continues the positive outlook for the whole c-Si PV industry.

All activities for increasing module power and cell efficiency, ensuring more efficient wafering and poly-Si usage, and achieving a higher utilization of production capacities as discussed in the current ITRPV edition will help manufacturers in their efforts to supply the market with highly competitive and reliable c-Si PV power generation products in the years to come.

7.3. Accuracy of roadmap projections

ITRPV has been publishing reports since 2010. Since the first edition, the investigated parameters have been reported as median values of the past year as well as predictions for the current year and the next 10 years to come. The data of the first reported year are therefore state of the art values of technical parameters and status quo values for others. In [38] we reviewed for the first time the forecast quality of several technical parameters like the amount of remaining silver of a c-Si cell and the as-cut wafer thickness of c-Si wafers.

Saving Silver in cell manufacturing is important it is the costliest non-silicon material in the c-Si PV value chain and a resource used not only by PV but also by other industries. The dependency on the world market requires continues reduction of silver consumption. Reduced usage of Silver will be mandatory to stay competitive.

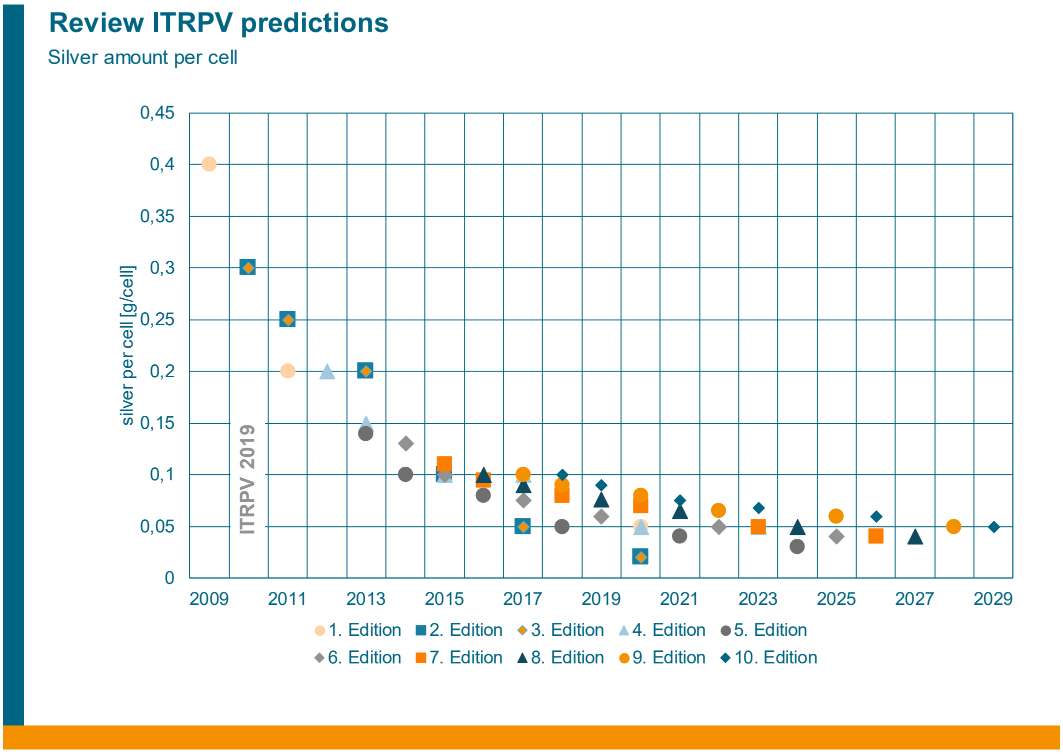

Fig. 65: Predicted trend of remaining Silver per cell – predictions of ITRPV editions.

Fig. 65 shows that Silver reduction – including the data of the 10th edition – has been predicted quite well since the first edition despite that the reduction to below 100mg remaining Silver per cell is currently slower as expected.

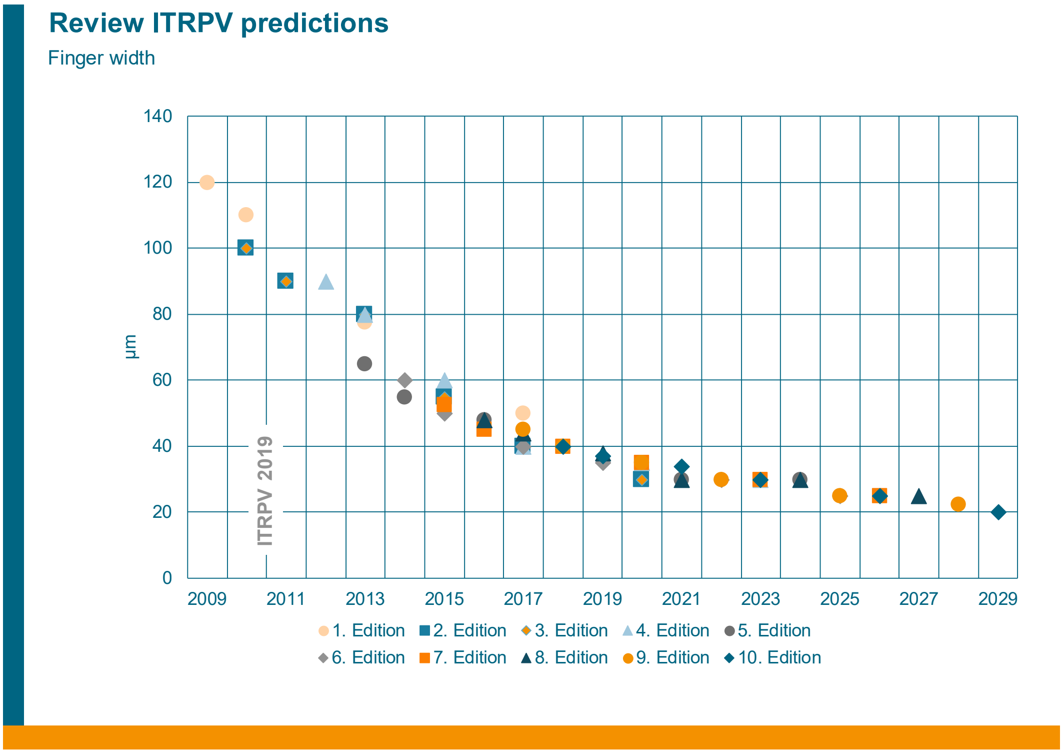

Fig. 66: Predicted trend of finger width at front side print – predictions of ITRPV editions.

The reduction of finger width at the cell front side is following the predictions quite precise as shown in Fig. 66.

Both trends emphasize that cost saving activities have been consistently continued since the first edition in 2009. The improvement of c-Si bulk is key to improve cell efficiency as discussed in 5.2.2. Fig. 67 shows that the ITRPV prediction improvements in J0bulk of p-type mc-Si material were also predicted well.

Fig. 68 and 69 visualize the prediction quality regarding reduction of wafer thickness for mc-Si and mono-Si wafers. The expected optimistic predictions of the past could not be met. In contrast to Silver, Si is a material mainly produced and used in PV (beside in microelectronics).

Capacity increases and corresponding price reductions for poly-Si slowed down ambitious activities for material reduction. With continued cost pressure, thickness reduction will materialize – for mono-Si we see a first indication that thickness reductions will come.

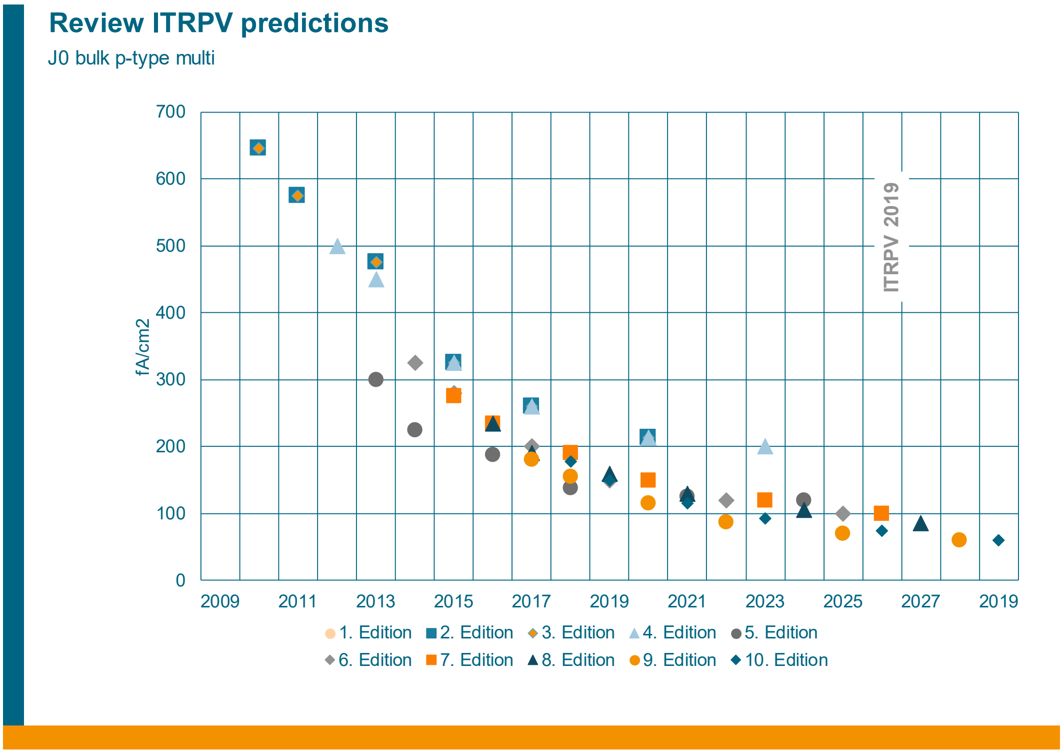

Fig. 67: Predicted trend of J0 bulk for p-type mc-Si material – predictions of ITRPV editions.

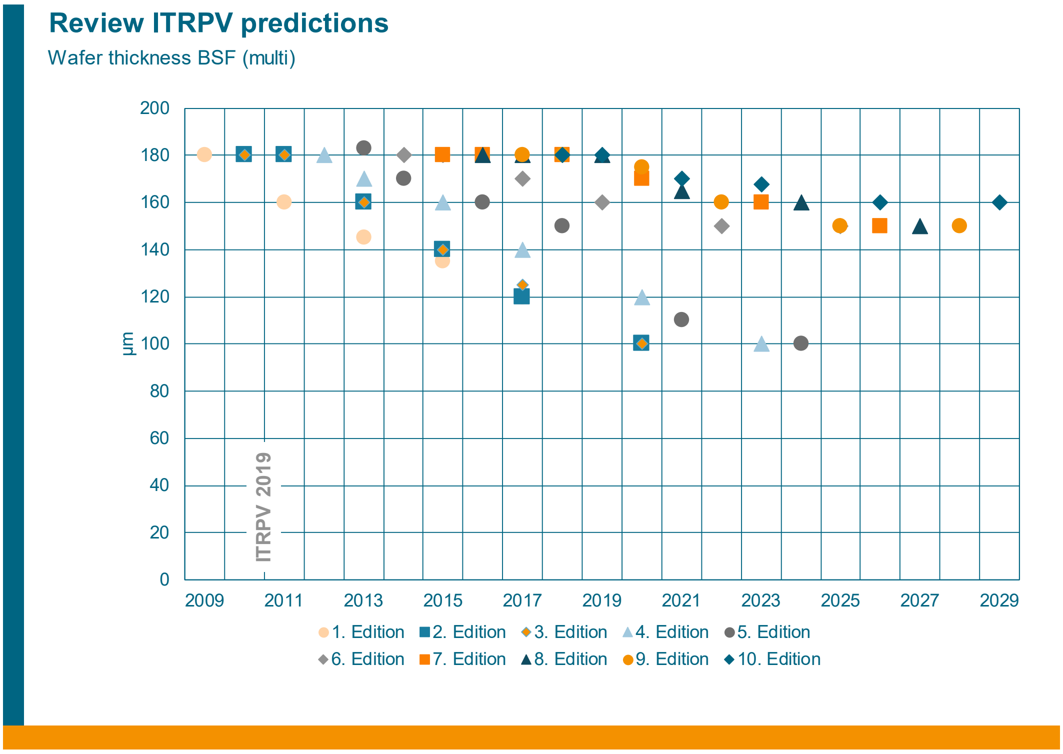

Fig. 68: Predicted trend of minimum as-cut mc-Si wafer thickness for mc-Si solar cells - predictions of ITRPV editions.

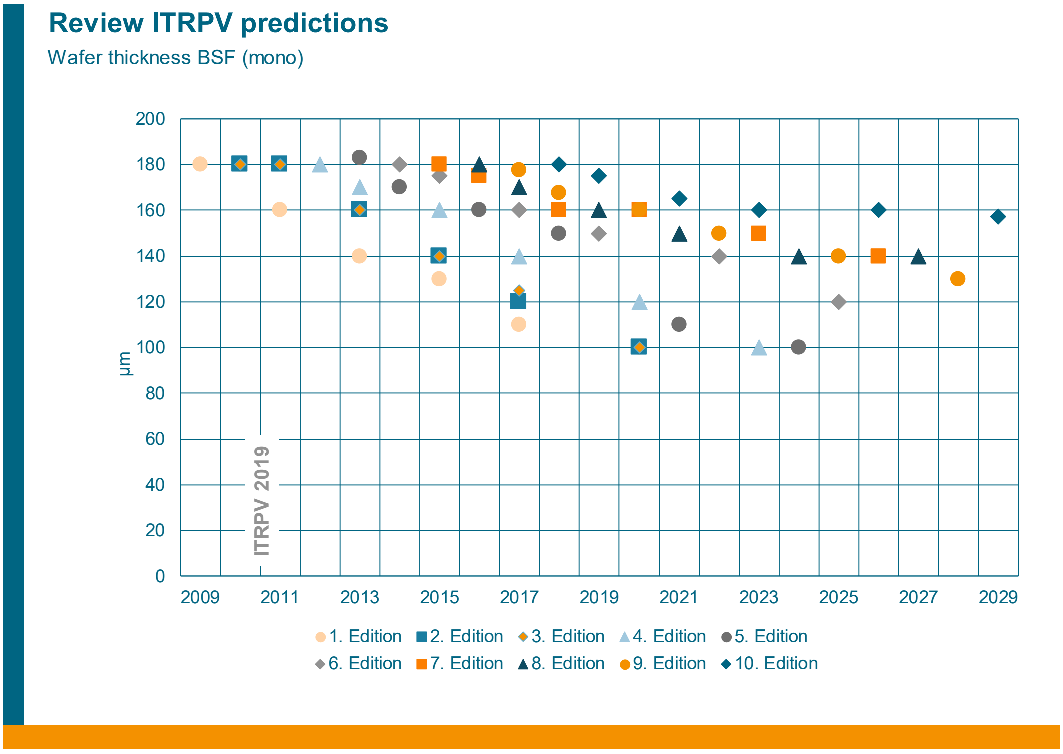

Fig. 69: Predicted trend of minimum as-cut mono-Si wafer thickness for mono-Si solar cells - predictions of ITRPV editions

7.4. Final remarks

We collected all data presented in this roadmap at the end of 2018 from leading companies along the c-Si value chain, international PV manufacturers, PV equipment and material suppliers, PV institutes as well as PV service providers, listed in the Acknowledgment. Plans call for this information to be updated annually. The topics discussed require cooperation between tool and material suppliers, manufacturers, and other companies along the value chain. A version of this document for download, as well as information on how to get involved in roadmap activities, can be found at the following website: itrpv.vdma.org.

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