Enhanced nFinFET ESD Performance

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Abstract – A very simple and useful scheme to enhance the ESD performance of the nFinFET is proposed. By incorporating the N-Well (NW) with the nFinFET, it becomes a low holding-voltage SCR if the NW contact is ohmic and becomes a high holding-voltage SCR if the NW contact is a Schottky contact.

I. Introduction

The NMOS transistor is one of the most important ESD protection devices in CMOS due to the parasitic npn for positive ESD event and drain-body diode for negative ESD event (w.r.t GND) (Fig. 1). Often the NMOS devices are self-protecting in many applications. The scheme commonly used to enhance the ESD performance of NMOS in planar technology is to build a ballast resistor in series with the drain. Although this scheme is also valid for FinFET technology, it cannot prevent the oxide reliability degradation of the nFinFET after an ESD event. Devices with the minimum channel length are also not useful since the nFinFET snapback voltage is still greater than the oxide breakdown voltage. Moreover, the ESD event is a high current stress event. With the large snapback voltage and high current, a large amount of hot carriers are generated near drain and gain enough energy to tunnel through the oxide, resulting in charges being trapped in the oxide.

Unlike the current flow due to snapback nFinEFT being confined within the FIN, the current of SCR can flow deep into the p-substrate. Once it is incorporated within the nFinFET, most ESD current can be pushed away from the channel to prevent the oxide degradation. In this paper, a SCR is developed to enhance the ESD performance as well as prevent ESD from inducing the oxide degradation of the nFinFET. One drawback of the SCR device is smaller holding voltage, which is close to 1.0V. So, it only can be used for the thin oxide nFinFET (1.0V), but cannot be used for the thick oxide NMOSFET (1.8V and above). Developing the SCR based device with high-holding voltage is a big challenge for FinFET technology. In this paper, a new kind of SCR is developed successfully to achieve the high-holding voltage necessary for the ESD enhancement of the thick gate nFinFET (1.8V up to 5V) without increasing any dimension of the SCR based device.

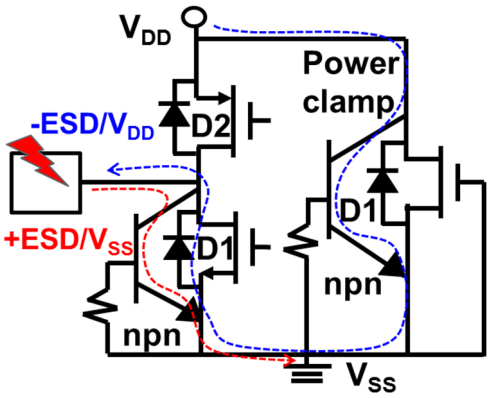

Figure 1: Current paths of an I/O under positive ESD to Vss and negative ESD to V_{DD}.

II. Experiment

14nm FinFET technology process has been used to develop the devices in this work. The devices used for the ESD study include the grounded-gate nFinFET (GGNMOS) [1], embedded SCR (EM-SCR) Fig. 3 [2], and embedded Schottky-SCR (EMS-SCR) [3] as shown in Fig. 2-Fig.4. The only layout difference between EM-SCR and EMS-SCR is the P+ implant in the N-Well (NW). The EM-SCR uses the P+ implant to form the ohmic contact for NW, while the EMS-SCR does not have the N+ or P+ implant to form the ohmic contact for NW. Without the heavily doped contact implant, the contact and NW of the EMS-SCR becomes a Schottky diode (DS in Fig. 4). Although

the Schottky diode is a high-leakage current device [3], [4] due to the imperfect interface between the contact and silicon [5], the EMS-SCR is a low-leakage device [3] since the current is limited by the series NW to PW diode (D1 in Fig. 4). All the three devices were developed with both thin (1.0V) and thick (1.8V) gate options. Device characterization was done using standard 100ns TLP (with rise time 2ns) and Very Fast TLP (pulse width 1ns and rise time 0.2ns) testers.

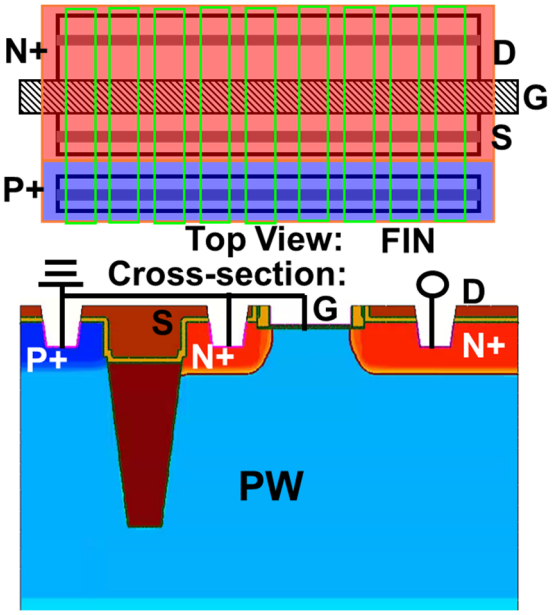

Figure 2: Top view and simulated net-doping for GGNMOS.

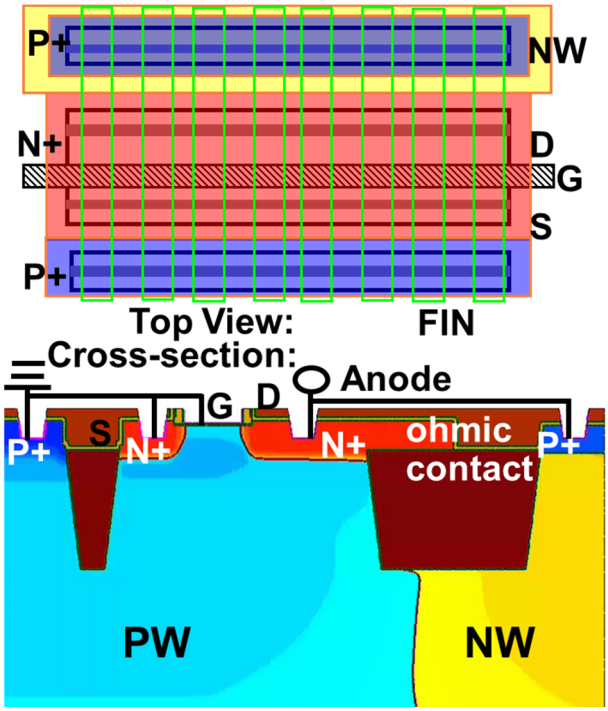

Figure 3: Top view and simulated net-doping for EM-SCR.

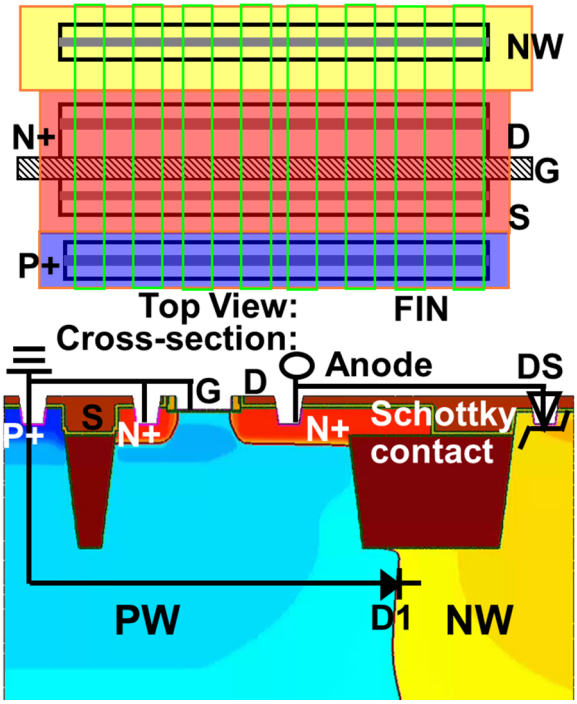

Figure 4: Top view and simulated net-doping for EMS-SCR.

A. 100ns TLP IV Characteristics

Fig. 5-Fig. 7 show the 100ns TLP IV characteristics of the 1.0V GGNMOS, EM-SCR and EMS-SCR for the cross sections shown in Fig. 2-Fig. 4. Except for the trigger voltage Vt1, the IV characteristics of three devices are different from each other. The GGNMOS has the smallest It2 (0.45A) and larger snapback holding voltage (3.6V). The EM-SCR has the largest It2 (2.1A) and smallest snapback holding voltage (1.8V). The It2 of the EMS-SCR (1.5A) is in between, but it does not have the snapback phenomenon. Moreover, the leakage currents of the three devices after the TLP stress events are also different from each other. This stress leads to the leakage current decrease for the GGNMOS after each TLP, while it induces a leakage current increase for the 1.0V EMS-SCR after each TLP. However, the stress does not result in any leakage current change to the EM-SCR until damage. From the waveforms in Fig. 8, the discharge behavior of the EMS-SCR during the ESD event is different from that of the EM-SCR. The voltage of the EM-SCR under a 1A TLP stress is initially clamped at 4.1V due to the GGNMOS component turning on and then drops down to 2.1V within 15ns due to the SCR component turning on. In series with a Schottky diode, the voltage of the EMS-SCR during a 1A TLP is ~5.2V at the initial transient (A in Fig. 8) and then follows the current to rise to 6.5V.

Fig. 9-Fig. 11 shows the TLP characteristics of the

1.8V GGNMOS, EM-SCR and EMS-SCR for the cross sections shown in Fig. 2-Fig. 4. Although similar to 1.0V devices in construction, the three 1.8V devices have some different IV characteristics. The GGNMOS has the smallest It2 (0.5A) and a large snapback holding voltage (5.2V). The EM-SCR has the largest It2 (2.0A) and a smallest snapback holding voltage (1.3V). The It2 of the EMS-SCR (1.66A) is in between and its snapback holding voltage (5.2V) is the same as that of the GGNMOS. Similar to the 1.0V devices, the leakage current of the 1.8V GGNMOS decreases after each TLP, while it does not lead to any leakage current change for the 1.8V EM-SCR or the 1.8V EMS-SCR until damage. By comparing Fig. 8 and Fig. 12, the discharging behaviors of the 1.8V EM-SCR and EMS-SCR are different from that of the 1.0V EM-SCR and EMS-SCR. During a 1A TLP, the voltage of the 1.8V EM-SCR is clamped at 4.5V and then drops down to 2.2V within 5ns, which is shorter than the turn-on time of the 1.0V EM-SCR (15ns). Unlike the 1.0V EMS-SCR, the voltage of the 1.8V EMS-SCR during a 1A TLP is the same as that of the 1.8V EM-SCR (4.5V) at the initial transient (A in Fig. 12) and then follows the current to rise to 6.5V.

The different turn-on times for the 1.8V EM-SCR and 1.0V EM-SCR are caused by the different well doping concentrations (PW and NW). The voltage of SCR is given by [6], [7]

$$V_H = V_P + V_N + \int \frac{J}{q(n\mu_n + p\mu_p)} dx + \iint \frac{q}{\epsilon}(p - n + N_D^+ - N_A^-)dxdy \quad (1)$$

where V_P is the P+/NW junction potential, V_N is the N+/PW junction potential, J is the current density, n and p are the average electron concentration and hole concentration inside the injected region.

Operating at high level injection, the concentrations of the minority carriers (electron or hole) increase with time as shown in Fig. 13-Fig. 15. This makes the fourth term in the equation decrease that results in voltage falling after the voltage peak (A in Fig. 12). In order to maintain the charge neutrality, the electron concentration is nearly equal to the hole concentrations (n=p) [8] as they increase beyond the background concentration (Fig. 15). Then, the fourth term in the right hand side of Eq. (1) is equal to zero and it becomes the summation of two pn junction potential terms and one ohmic term, corresponding to the NW and PW vanishing and becoming a heavy-conductivity (ohmic) region. This is the heavy-conductivity modulation effect [8]-[10]. The time to modulate the PW and NW to a heavy-conductivity region increases with the background concentrations. With the lower well doping concentrations, the 1.8V EM-SCR has the shorter turn-on time compared to the 1.0V EM-SCR.

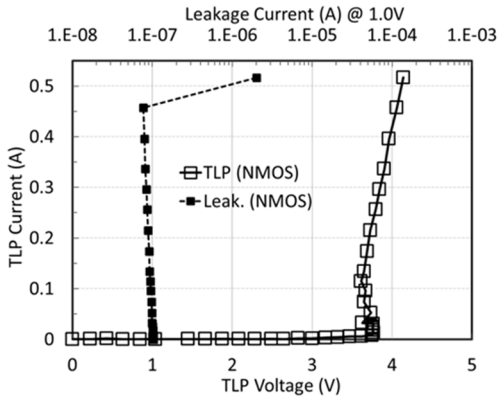

Figure 5: TLP IV Characteristics of 1.0V GGNMOS in Fig. 2.

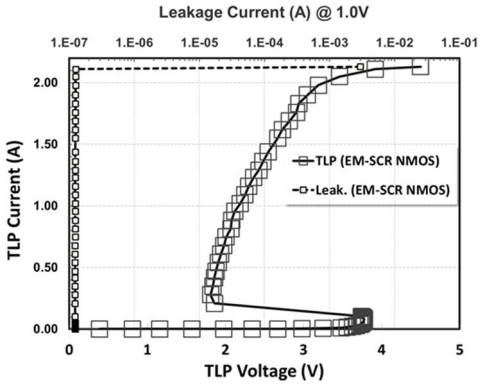

Figure 6: TLP IV Characteristics of 1.0V EM-SCR in Fig. 3.

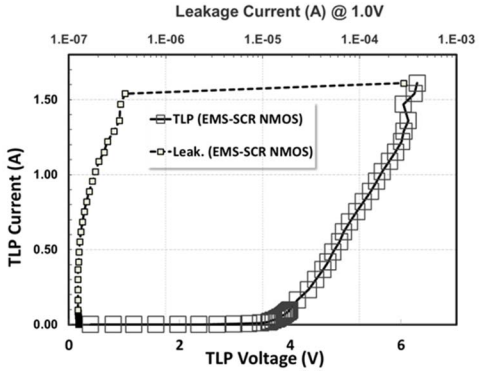

Figure 7: TLP IV Characteristics of 1.0V EMS-SCR in Fig. 4.

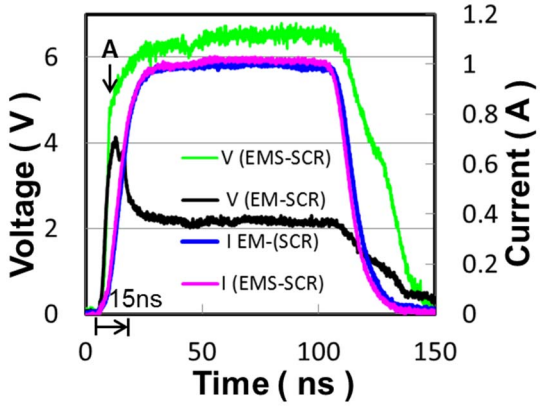

Figure 8: Voltage and current waveforms of 1.0V EM-SCR and 1.0V EMS-SCR under the 1A TLP stress events.

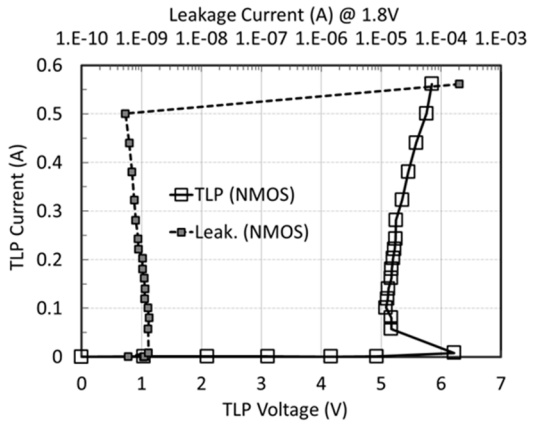

Figure 9: TLP IV Characteristics of 1.8V GGNMOS in Fig. 2.

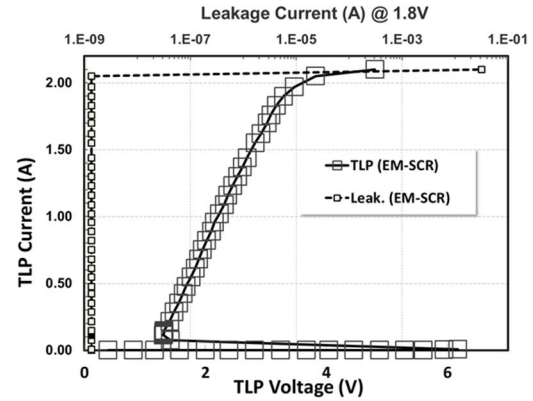

Figure 10: TLP IV Characteristics of 1.8V EM-SCR in Fig. 3.

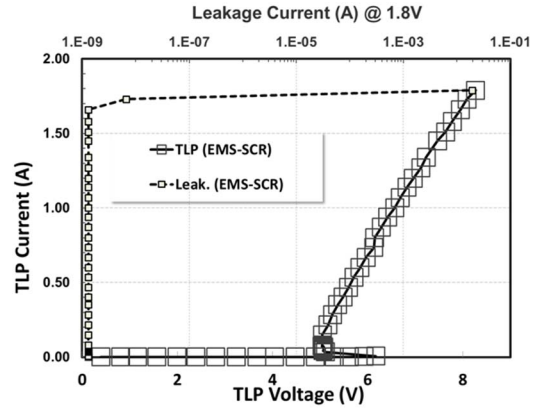

Figure 11: TLP IV Characteristics of 1.8V EMS-SCR in Fig. 4.

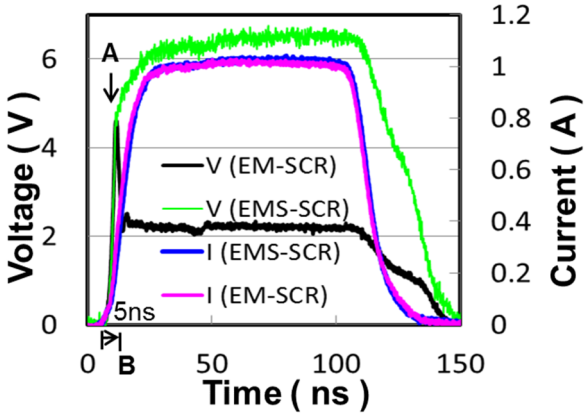

Figure 12: Voltage and current waveforms of 1.8V EM-SCR and 1.8V EMS-SCR under the 1A TLP stress events.

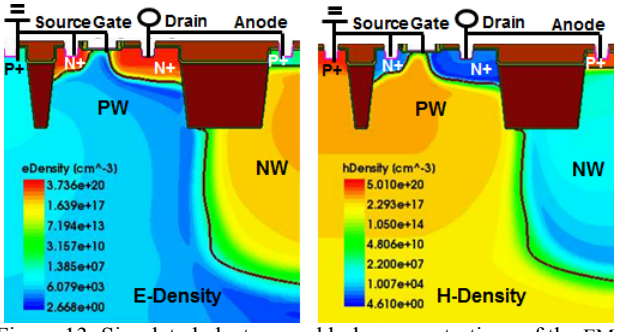

Figure 13: Simulated electron and hole concentrations of the EM-SCR at the initial transient (0 in Fig. 12).

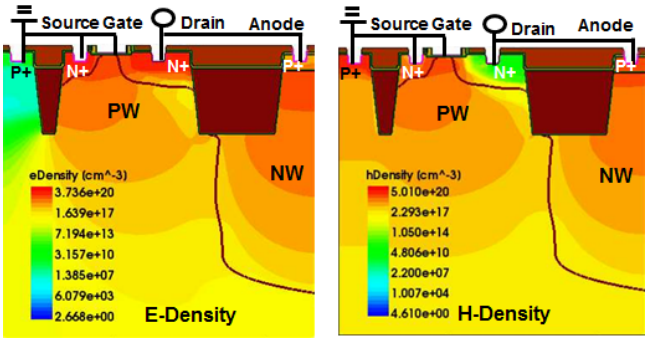

Figure 14: Simulated electron and hole concentrations of the EM-SCR at the voltage peak transient (A in Fig. 12).

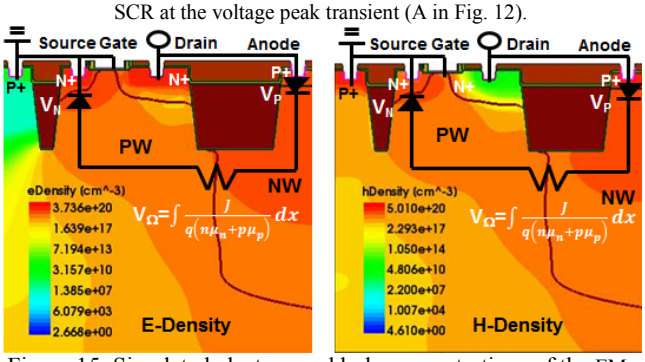

Figure 15: Simulated electron and hole concentrations of the EM-SCR at the snapback region (B in Fig. 12).

B. 1ns TLP IV Characteristics

Fig. 16-Fig. 18 show the 1ns very fast TLP IV characteristics of the 1.0V GGNMOS, EM-SCR and EMS-SCR for the cross sections shown in Fig. 2-Fig. 4. The three devices have the similar IV characteristics below the 1A TLP stress, in which the voltage increases with current. This implies that the npn bipolar dominates the ESD event in this region. As the stress current goes beyond 1.1A, it leads to the 1.0V GGNMOS damage and the leakage current increases in the EM-SCR and EMS-SCR after each TLP. Although the EM-SCR and EMS-SCR can clamp the voltages at 7V and 7.8V for the TLP current below 2.7A, the voltages are still too high for the gate oxide of the 1.0V GGNMOS. From the waveforms in Fig. 19, it can be seen that the voltages of the two devices decrease with time after rising to the peak

voltages, which are from 7V to 6V and from 7.9V to 7.1V for the EM-SCR and EMS-SCR, respectively. This can be attributed to that the electron and hole concentrations increase with time (Fig. 13 and Fig. 15) from Eq. (1).

Fig. 20-Fig. 22 show the 1ns TLP IV characteristics of the 1.8V GGNMOS, EM-SCR and EMS. Unlike the 1.0V devices, the three 1.8V devices all have the snapback phenomena. The snapback holding voltages of the two SCR devices are all smaller than that of the GGNMOS (6.4V), which are 4.3V and 5.1V for the EM-SCR and EMS-SCR, respectively. It implies that the SCR conduction dominates the 1ns ESD event and this is why the leakage currents of the two SCR's do not increase after TLP stresses. From the waveforms in Fig. 23, it can be seen that the voltage of the 1.8V EM-SCR decreases to 3.2V from 7.3V (A to B), while that of the 1.8V EMS-SCR only drops from 7.5V to 6.8V (C to D) after rising to the peak voltages. This difference is caused by the interface-sate density of the Schottky diode being much lower than the doping concentration of the P+ implant. Without the high concentration of holes, the NW and PW of the EMS-SCR cannot be modulated to the heavy-conductivity region since the electron and hole concentrations are still not higher than the background concentrations from the simulation results in Fig. 24 and Fig. 25.

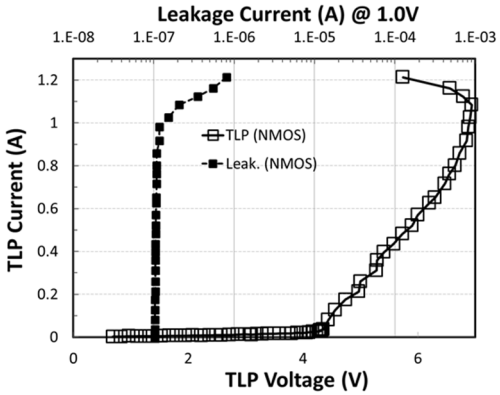

Figure 16: 1ns TLP IV Characteristics of 1.0V GGNMOS in Fig. 2.

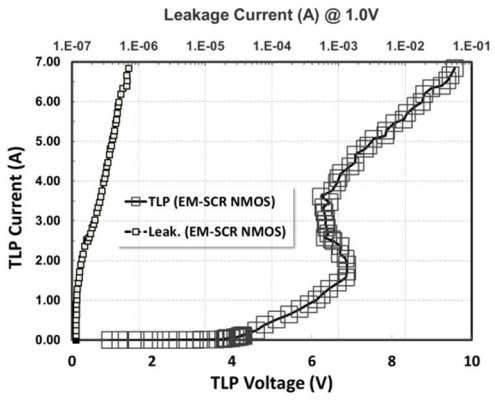

Figure 17: 1ns TLP IV Characteristics of 1.0V EM-SCR in Fig. 3.

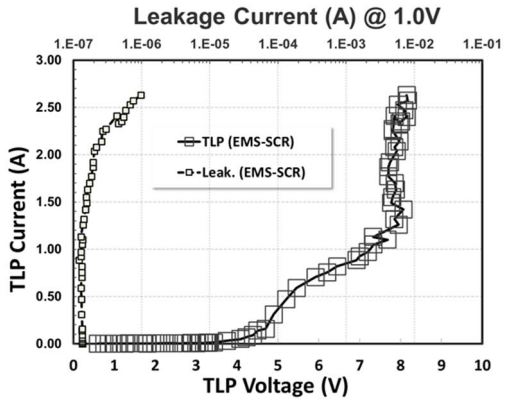

Figure 18: 1ns TLP IV Characteristics of 1.0V EMS-SCR in Fig. 4.

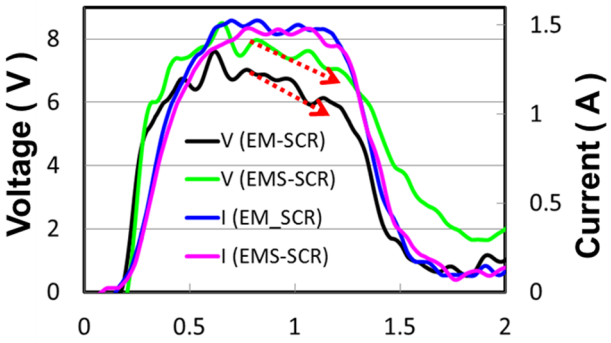

Figure 19: Voltage and current waveforms of 1.0V EM-SCR and 1.0V EMS-SCR under the 1A TLP stress events (1ns).

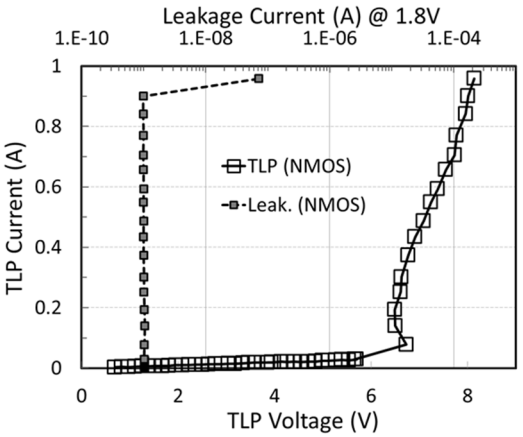

Figure 20: 1ns TLP IV Characteristics of 1.8V GGNMOS in Fig. 2.

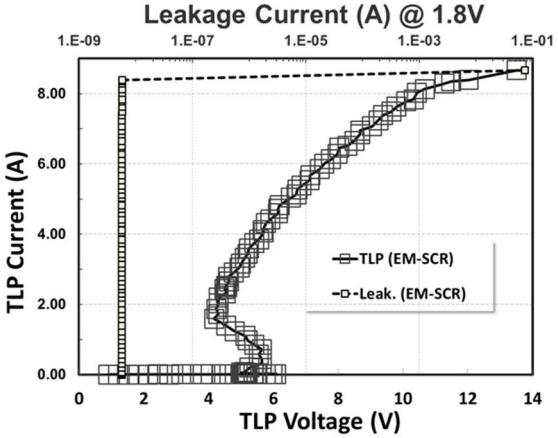

Figure 21: 1ns TLP IV Characteristics of 1.8V EM-SCR in Fig. 3.

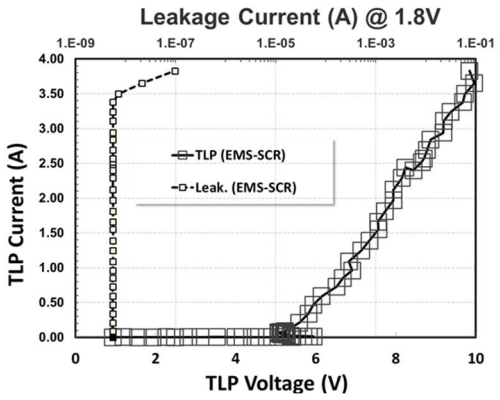

Figure 22: 1ns TLP IV Characteristics of 1.8V EMS-SCR in Fig. 4.

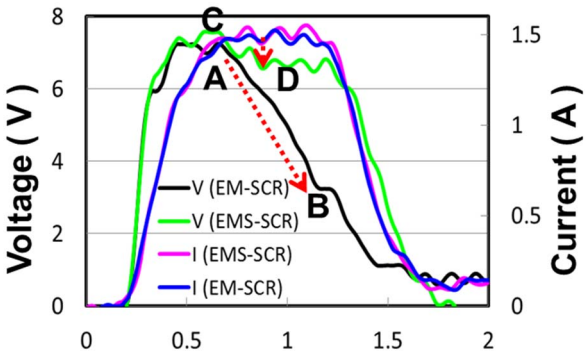

Figure 23: Voltage and current waveforms of 1.8V EM-SCR and 1.8V EMS-SCR under the 1A TLP stress events (1ns).

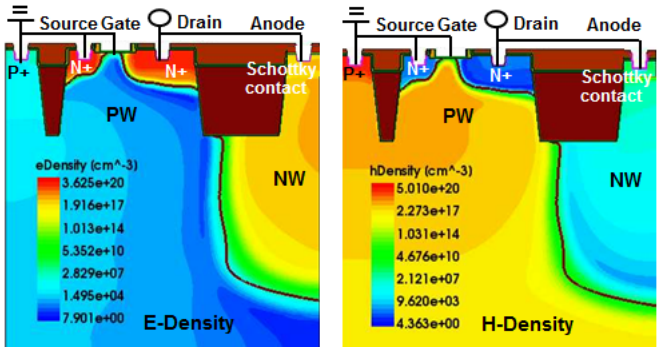

Figure 24: Simulated electron and hole concentrations of the EMS-SCR at the initial transient (0 in Fig. 23).

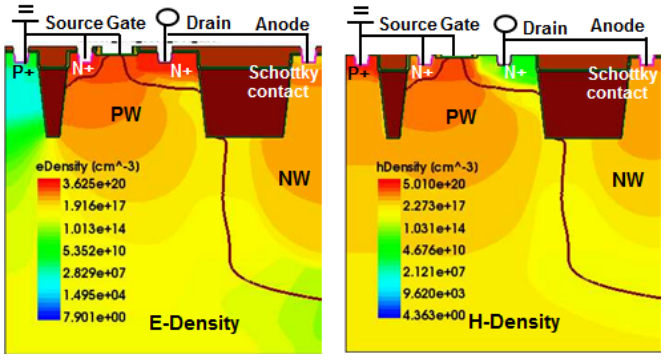

Figure 25: Simulated electron and hole concentrations of the EMS-SCR at the time 1ns (D in Fig. 23).

C. DC IV Characteristics

Fig. 26 and Fig. 27 show the DC leakage currents of the EM-SCR's and EMS-SCR's at 25°C and 125°C. Regardless of being 1.0V devices or 1.8V devices, the IV curves of the EMS-SCR and EM-SCR overlap together and cannot be distinguished. This demonstrates that the Schottky diode does not lead to a leakage increase in the EMS-SCR although the Schottky diode is a high leakage current device [3], [4]. The main reason is that the Schottky diode is in series with a pn diode D1 from Fig. 4. Biased at the reverse voltage, the diode D1 limits the current from the NW to the grounded PW. Since the breakdown voltage (V_{BR}) of the GGNMOS is much smaller than that of NW, the currents of the EM-SCR and EMS-SCR from the GGNMOS should be much higher than from the NW as the applied voltage approaches or goes beyond the GGNMOS V_{BR}.

Fig. 28-Fig. 29 show the DC snapback characteristics of the 1.0V EM-SCR and EMS-SCR at high temperature (125°C). The holding voltage of the 1.0V EM-SCR is 1.5V, which is higher than 1.0V. This implies that the 1.0V EM-SCR can be operated at 1.0V without suffering the latch-up problem. Similar to the TLP IV characteristic, the 1.0V EMS-SCR does not have the snapback phenomenon but it can clamp the voltage at ~4.0V for current below 0.1A.

Fig. 30 and Fig. 31 show the DC snapback characteristics of the 1.8V EM-SCR and EMS-SCR at the high temperature (125°C). The holding voltage of 1.8V EM-SCR NMOS is only 1.1V. Because it is smaller than 1.8V, the 1.8V EM-SCR cannot be used for 1.8V application without suffering a latch-up problem. Different from the 1.0V EMS-SCR, the 1.8V EMS-SCR has the snapback phenomenon and its holding voltage is 5.4V, which is much higher than 1.8V. So, it can be used for applications below 5V without any latchup risk.

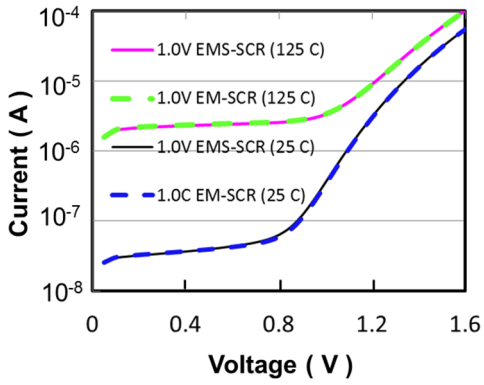

Figure 26: DC Leakage current of 1.0V EM-SCR and EMS-SCR.

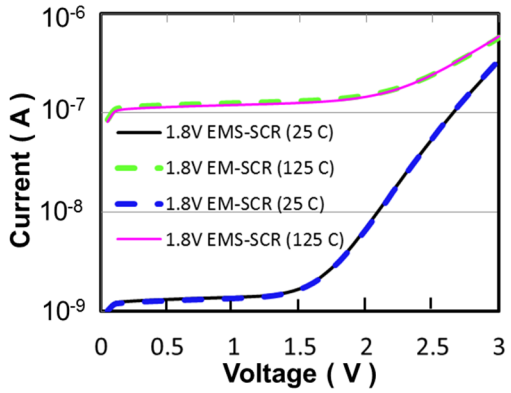

Figure 27: DC leakage current of 1.8V EM-SCR and EMS-SCR.

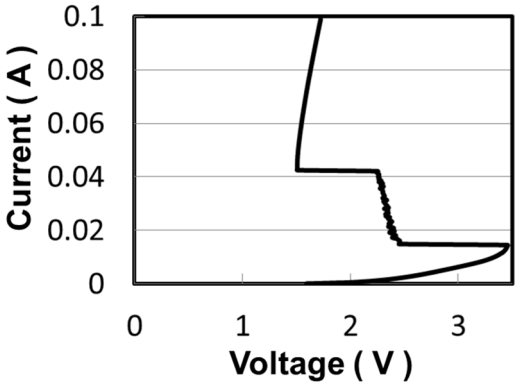

Figure 28: DC IV characteristics of 1.0V EM-SCR in Fig. 4 at 125°C.

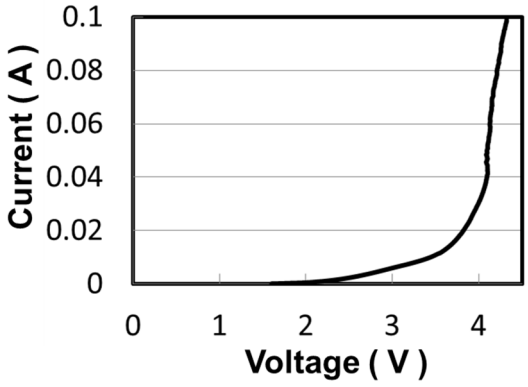

Figure 29: DC IV characteristics of 1.0V EMS-SCR in Fig. 4 at 125°C.

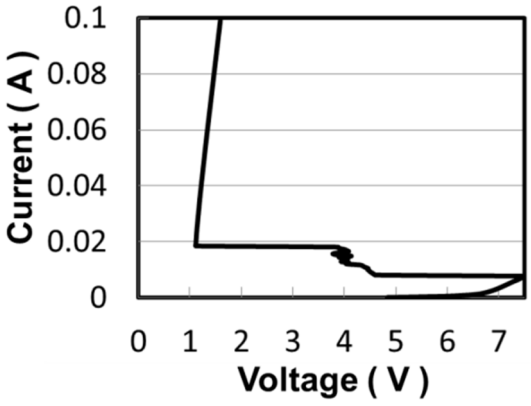

Figure 30: DC IV characteristics of 1.8V EM-SCR in Fig. 3 at 125°C.

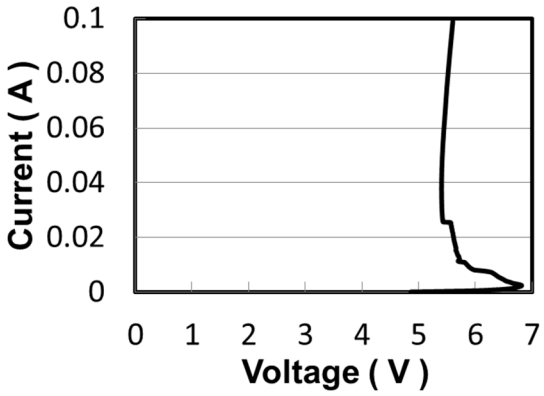

Figure 31: DC IV characteristics of 1.8V EMS-SCR in Fig. 4 at 125°C.

III Discussion

A. Current and Thermal Behavior

Fig. 32-Fig. 34 show the simulated current densities of the GGNMOS, EM-SCR and EMS-SCR under the 100ns TLP stresses. Since the GGNMOS only has the parasitic npn bipolar transistor, the TLP current only flows from the drain through the region below the gate into the source (Fig. 32). For the EM-SCR, there are two npn bipolar transistors and one pnp bipolar transistor. Once the npn2 bipolar and pnp bipolar both turn on, the device goes into the latchup state [10], corresponding to the SCR turning on. Owing to the SCR, most current flows from the P+ diffusion in the NW through the NW and PW into the source and only a small current can flow from the drain into the source (Fig. 33). Similar to the EM-SCR, the Schottky diode of the EMS-SCR is equivalent to a pnp bipolar. Hence, the EMS-SCR also has the two discharge current paths as shown in Fig. 34. Because of the Schottky SCR, most current flows from the Schottky contact through the NW and PW into the source and part of current flows from the drain into the source. Moreover, the currents caused by the npn1 bipolar transistors of the EM-SCR and EMS-SCR are all away from the surface channels. Without the high current flowing through the channel, the oxide trapped charges caused by the hot carrier generation on the high field drain are reduced significantly. This is why the leakage currents of the 1.0V and 1.8V EM-SCR's (Fig. 6 and Fig. 10) and 1.8V EMS-SCR (Fig. 11) do not increase after each TLP. On the contrary, it leads to the leakage current decreasing to the 1.0V and 1.8V GGNMOS's value after each TLP (Fig. 5 and Fig. 9) caused by electrons trapped in the oxide [11] due to the high current flowing through the channel.

Fig. 35-Fig. 37 show the simulated potentials of the GGNMOS, EM-SCR and EMS-SCR under the 100ns

TLP stress events. Similar to the 100ns TLP test results (Fig. 5-Fig. 7 and Fig. 9-Fig. 11), the potential of the EMS-SCR is close to that of the GGNMOS, but larger than that that of the EM-SCR. Moreover, it can be seen that a depletion region exists at the NW/PW junction for the EMS-SCR (Fig. 37), while there is no depletion region at the NW/PW junction of the EM-SCR (Fig. 36) due to the heavy-conductivity modulation effect. With a depletion region to separate the NW from the grounded PW, the NW potential of the EMS-SCR is the same as the drain potential (Fig. 37) since they are tied together. This is why the EMS-SCR has a high holding voltage. Without the depletion region as the potential barrier to separate the NW and PW, the NW potential of the EM-SCR is pulled down by the grounded PW, which is almost the same as the PW potential (Fig. 36). Because of this, the snapback voltage of the EM-SCR is smaller than that of the two other devices.

Fig. 38-Fig. 40 show the simulated temperatures of the GGNMOS, EM-SCR and EMS-SCR under the 100ns TLP stress events. Unlike the GGNMOS, the hottest region of the EM-SCR or EMS-SCR is at the NW junction below the trench since most current flows through this region from Fig. 33 and Fig. 34. With the low holding voltage and low current density due to the SCR turn-on, the temperature of the EM-SCR caused by Joule-heating is lower than that of two other devices. Regardless of being 1.0V devices or 1.8V devices, the EM-SCR always has the largest It2. With the low current density and high holding voltage due to the Schottky SCR turn-on, the temperature of the EMS-SCR caused by Joule-heating is lower than that of the GGNMOS, but higher than that of the EM-SCR. So, the It2 of the EMS-SCR is higher than that of the GGNMOS, but smaller than that of the EM-SCR irrespective of gate oxide option.

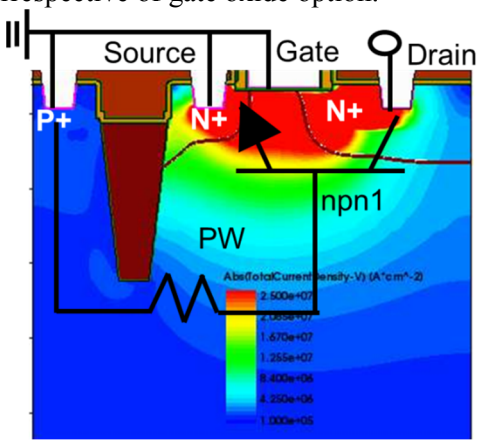

Figure 32: Simulated current density and equivalent circuits of GGNMOS under a 100ns TLP.

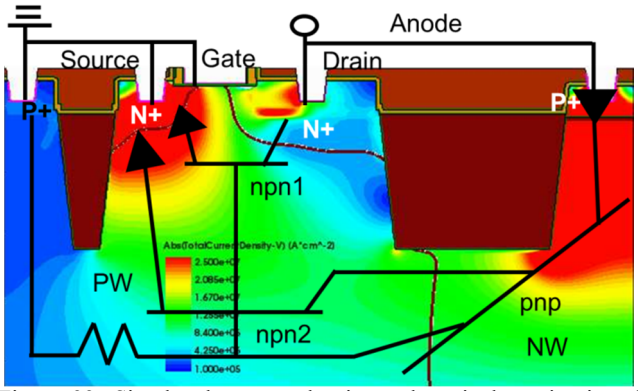

Figure 33: Simulated current density and equivalent circuits of EM-SCR under the 100ns TLP.

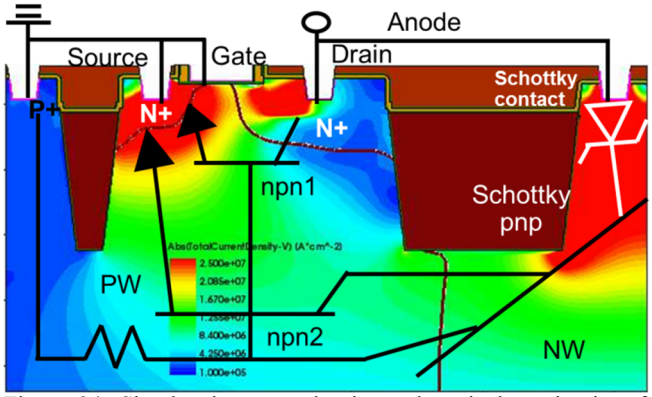

Figure 34: Simulated current density and equivalent circuits of EMS-SCR under the 100ns TLP.

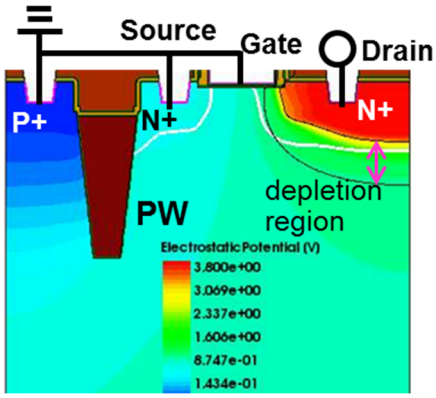

Figure 35: Simulated electric potential of GGNMOS under the 100ns TLP.

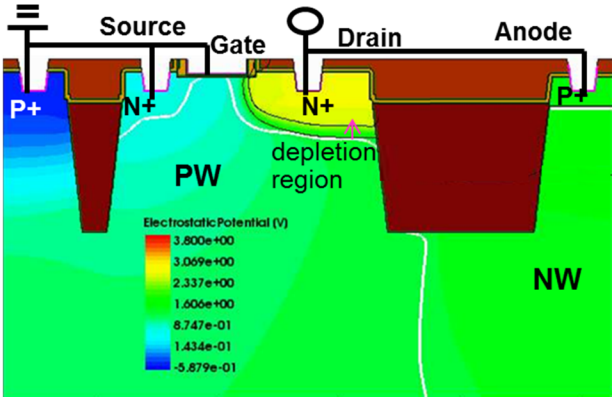

Figure 36: Simulated electric potential of EM-SCR under the 100ns TLP.

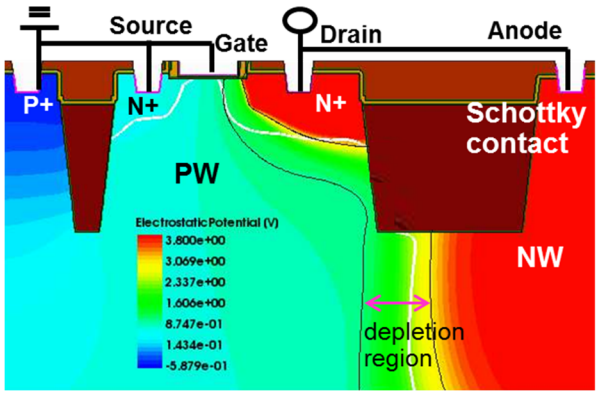

Figure 37: Simulated electric potential of EMS-SCR under the 100ns TLP.

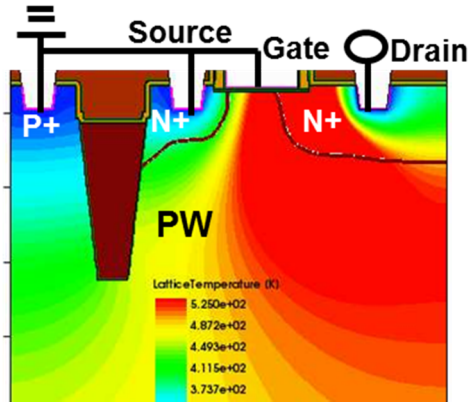

Figure 38: Simulated temperature of GGNMOS under the 100ns TLP.

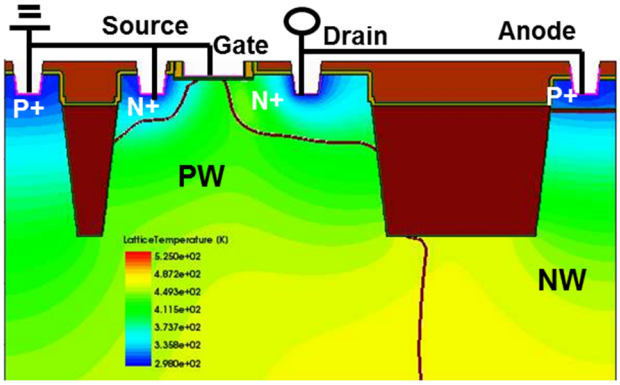

Figure 39: Simulated temperature of EM-SCR under the 100ns TLP.

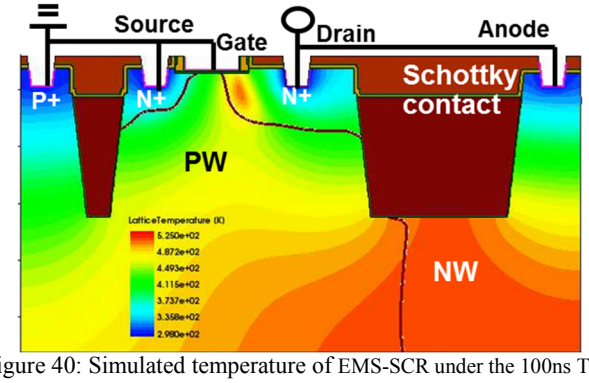

Figure 40: Simulated temperature of EMS-SCR under the 100ns TLP.

IV Conclusion

Although the EM-SCR NMOS has the very robust ESD performance, it is a low-holding voltage device and only can be used for 1.0V application. Changing the SCR of EM-SCR NMOS to a Schottky SCR will slightly degrade the device ESD performance, it will allow the device to be used in higher voltage application through its higher holding voltage.

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