内部资料

集微技术信息简报

Vol.3 No.4
2016 年 8 月
（总第十四期）

国家科技图书文献中心
中国科学院文献情报中心

本期目录

专题分析

政策计划

前沿研究

应用实施

专题分析

多重图形技术专利态势分析

研究背景

光刻技术是半导体及相关产业发展和进步的关键技术，传统的光刻技术有紫外光刻、电子束光刻技术等。在过去的几十年中，传统光刻技术一方面发挥了重大作用；另一方面，这些传统技术存在不同的缺点，如结构复杂，依赖于光学系统进行成像，分辨率受限于衍射极限等。随着传统光刻技术在应用中问题的增多、用户对应用本身需求的提高，寻找解决技术障碍的新方案、找到下一代可行的技术路径，去支持产业的进步显得非常紧迫，各国将大量的研究和开发资金投入到这场技术竞赛中。极紫外光刻技术、DSA（定向自组装光刻）技术、无掩模光刻技术、原子光刻技术、电子束光刻技术、多重图形技术等技术作为解决方案进入下一代光刻技术角逐场。

多重图形技术（Multiple-pattern lithography，Multiple patterning technology）原理是将一套高密度的电路图形分解成多套分立的、密度低一些的图形，然后将它们印制到目标圆晶上。多重图形被当作是一种能够使本已很难再降低的 k1 因子（表征光刻工艺复杂度的参数）得以继续减小的主流方案。多重图形技术技术目前主要有双重、三重、四重和八重等，其中双重图形技术是研究最多和使用最广泛的。

早在 1997 年，R.J.B. Steven 就提出了双重图形技术，由于其能够有效地降低制作小尺寸图形的难度，获得了工业界的广泛认同。Intel 公司在其 22nm 三栅工艺中采用了双重图形技术，成功实现了 60nm 间距的鳍。双重图形技术将在较长的时间内，成为 EUV 成熟之前的光刻技术桥梁。

双重图形技术可分为间距分离（pitch split）技术和间距分割（pitch division）技术。前者的典型工艺为光刻－蚀刻－光刻－蚀刻（litho-etch-litho-etch, LELE）工艺，而后者的典型工艺则为侧墙图案转移（sidewall image transfer, SIT）工艺，其又被称为自对准双重图形（self-aligned double patterning, SADP）技术。

但是浸入式 193nm 光刻工艺即使结合双重图形技术，依然难以满足间距在 40nm 以下的光刻要求。因此，在 10nm 技术代，三重以上的多重图形技术成为一项不可或缺的图形技术，跟踪和关注其最新的多重图形技术显得尤为重要[1]。

研究内容

本研究从多重图形技术专利入手，力求呈现当前该专利技术态势及专利活动特点。

多重图形技术专利分析内容共包括：专利数申请时间趋势分析、技术构成分析、国家/地区分析、申请人等四大项专利分析模块。

数据来源

数据来源：美国汤森路透科技（Thomson Reuters Scientific）公司 ThomsonInnovation 全球专利数据库（检索日期 2016 年 8 月 23 日），分析过程中采用了该公司的 TDA（Thomson Data Analyzer）分析工具。

1 专利申请时间趋势

1.1 专利申请时间走势

截至检索日期，共检索到多重图形技术相关的专利家族 2268 个，专利家族最早优先权年时间跨度为 1966-2016 共 50 年，考虑到专利一般从申请到公开需要最长达 30 个月（12 个月优先权期限+18 个月公开期限）的时间，再考虑到数据库录入的时间延迟，近两年的专利申请量会出现失真。

分析多重图形技术的专利数量随时间的变化趋势，可以作为预测多重图形技术发展趋势的重要参考指标。图 1.1 揭示了多重图形技术专利数量的年度统计情况，可以看出多重图形技术的专利家族数量整体呈现递增趋势。

第一个多重图形技术的专利是科宁玻璃厂在 1966 年（CORNING GLASS WORKS）申请的，专利号为 US3507654A（Production of precision silk screens by indirect double exposure method）。该专利中显示该方法可以用于印刷微型电路、装饰艺术品、普通印刷物等。

[1]洪中山,吴汉明. 多重图形技术的研究进展[J].微纳电子技术.2013(10)

此后该技术发展缓慢，每年只有少量专利产出。直到 1980 年以后，专利申请量开始逐渐上升，年均申请量突破 10 件以上。在 1994 年左右出现一个小的申请高峰。

1997 年，R.J.B. Steven 提出将双重图形技术应用在光刻技术中，使其能够有效地降低制作小尺寸图形的难度。从这一年开始，该技术进入快速发展期。尤其是在 2005 年后专利申请量大幅提高，在 2008 年达到申请高峰。此后稍有缓和，但年均申请量都在 130 项以上，又在 2014 年达到新的申请量高峰。

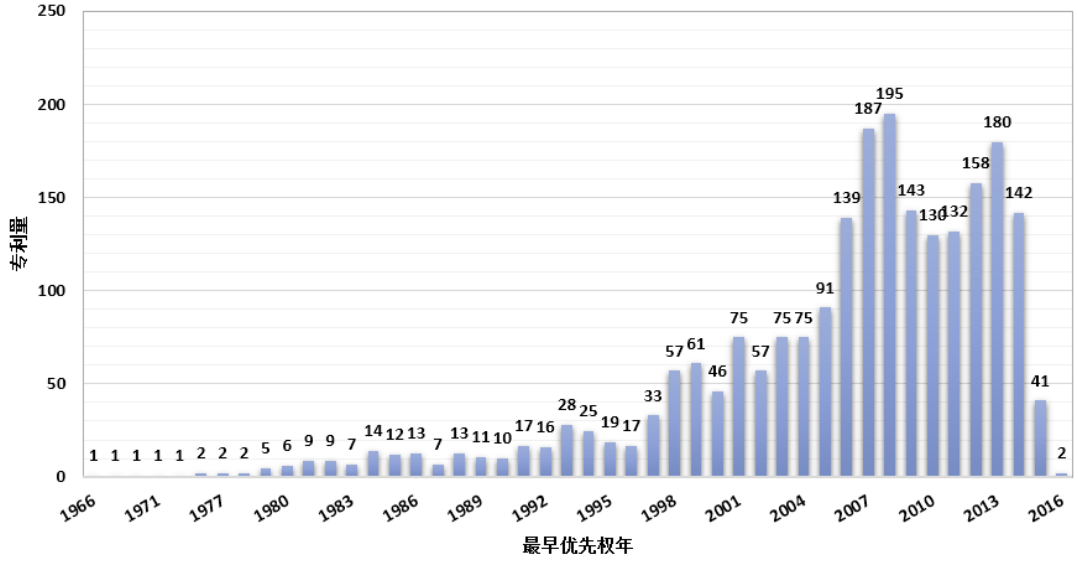


图 1.1 多重图形技术专利申请时间趋势(单位：项)

1.2 专利技术生命周期

专利技术生命周期是指在专利技术发展的不同阶段中，专利申请量与专利申请人数量的一般性的周期性的规律。一个比较完整的技术生命周期示意图是利用某段时间内与某项技术相关的专利申请数量和相应的专利申请人数量的变化情况绘制而成的，以年度申请人量为横坐标，年度申请数量为纵坐标，绘制出曲线对技术发展的各个阶段进行分析，预测技术的发展速度及前景。专利技术生命周期常用 4 段论，即萌芽期、发展期、成熟期、衰退期。

对多重图形技术领域的专利分析发现，多重图形技术整体上处于技术成长期。

（1）萌芽期：从 1966 年到 1997 年，多重图形技术领域发明的数量和专利申请人较少，但是呈现缓慢上升趋势。

（2）发展期：

1997 年到 2008 年，多重图形技术领域的相关专利技术数量和申请人数量明显增加，进入快速发展期，该技术的研发投入逐渐增多。

（3）瓶颈期：

近年来该技术领域专利申请数量和申请人数处于波动状态，2008 年到 2011 年专利申请人数量及专利数量都有大幅度下，2011 专利申请量回升，2012 年专利申请人数量有所回升。

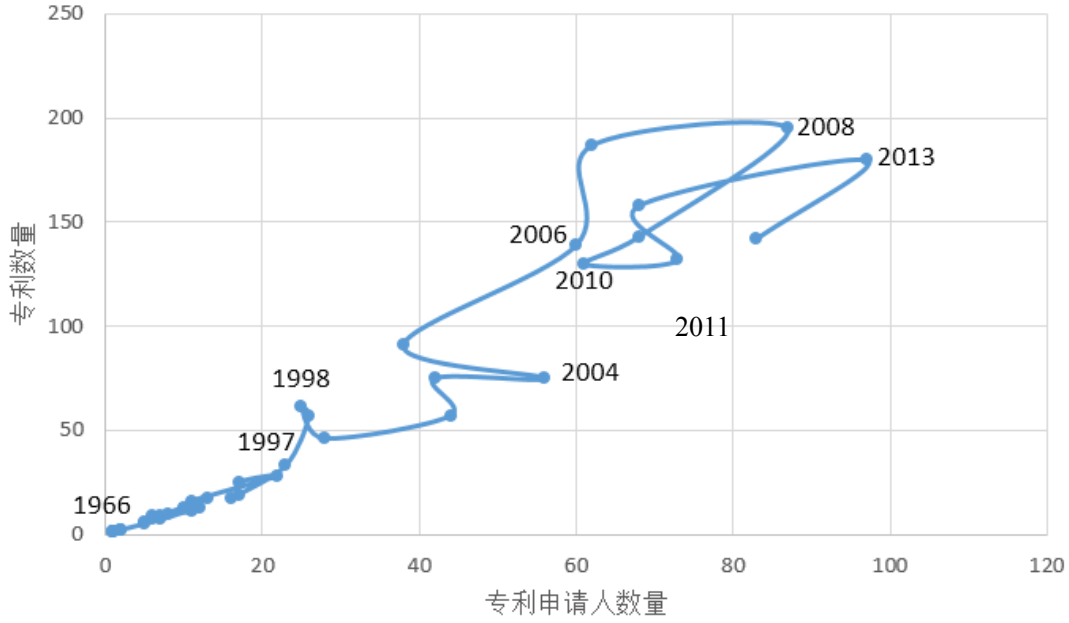


图 1.2 多重图形技术专利技术生命周期

2 专利申请技术构成分析

2.1 主题聚类分析

为了方便直观形象的了解多重图形技术的研究点，对该技术专利相关关键词进行处理并绘制专利技术主题聚类图，从而更深入的探索专利技术的发明内容与创新性。

图 2.1 多重图形技术专利技术主题分布

分析多重图形技术主题聚类图，发现多重图形技术主题聚焦于掩膜层、双重图形、半导体器件、多图案、多重曝光、光刻胶层、目标模式、光掩膜、相移等，具体研究热点见表 2.1。

表 2.1 研究主题及热点

序号	研究主题	研究热点	序号	研究主题	研究热点
1	掩膜层	Hard Mask Layer Photoresist Pattern Fine Pattern Contact Hole Double Exposure Self Aligned Contacts Sacrificial Layer Dielectric Layer Side Wall Active Area Thin Film Pixel Defining Layer Mask Data Pattern Photosensitive Film	6	光刻胶层	Hard Mask Layer Spacer Pattern Exposure Process Underlying Layer Double Exposure Self Aligned Contacts Positive Photoresist Amorphous Carbon Line Width Critical Dimension Exposure Region Negative Photoresist Layer Silicon Nitride Side Wall
2	双重图形	Photoresist Pattern Material Layer Double Patterning Technology Spacer Pattern Hard Mask Layer Fine Pattern Self-aligned Double Patterning Line Width Phase Shift Mask Contact Hole Alignment Mark Heat Treatment Thin Film Sacrificial Layer	7	目标模式	Etching Target Layer Imaging Performance Double Patterning Process Projection Beam Hard Mask Layer Pattern Decomposition Vertical Mask Material Layer Sacrificial Layer Critical Features Multiple Patterning Lithography Pattern Element Contact Hole Side Wall
3	半导体器	Spacer Pattern	8	光掩膜	Double Exposure

	件	Hard Mask Layer Photoresist Pattern Fine Pattern Insulation Layer Line Pattern Self Aligned Contacts Contact Hole Sacrificial Layer Gate Electrode Active Region Side Wall Memory Cells Thin Film			Circuit Pattern Phase Shift Mask Photolithography Process Photosensitive Substrate Photosensitive Film Photoresist Film Critical Dimension Hole Pattern Dielectric Layer Position Accuracy Latent Image Conductive Layer Base Plate
4	多图案	Exposure Process Circuit Pattern Manufacturing Methods Lithographic Process Exposure Region Design Layout Semiconductor Substrate Mask Data Exposure Tool Light Beam Hard Mask Layer Drawing Data Mask Stage Word Line	9	相移	Light Shielding Phase Difference Line Width Trim Mask Critical Features Layer Forming Semiconductor Wafer Photoresist Pattern Reticle Stage Transparent Substrate Fabrication Process Contact Hole
5	多重曝光	Exposure Step Manufacturing Methods Exposure Region Exposure Tool Vertical Mask Semiconductor Substrate Line Pattern Light Beam Mask Data Exposure Dose Drawing Data Latent Image Hard Mask Layer Light Shielding	10	其他	光源 碱显影液 液晶显示器 激光束 带电粒子束 大面积 支持层 光学元件 光学特性 光罩布局 电路板 金属布线

2.2 技术时间走势分析

技术时间走势分析主要是分析多重图形技术的技术手段随时间发展的变化情况，揭示出多重图形技术的发展过程以及最新的技术情况。本文使用德温特手工代码来体现技术分类。

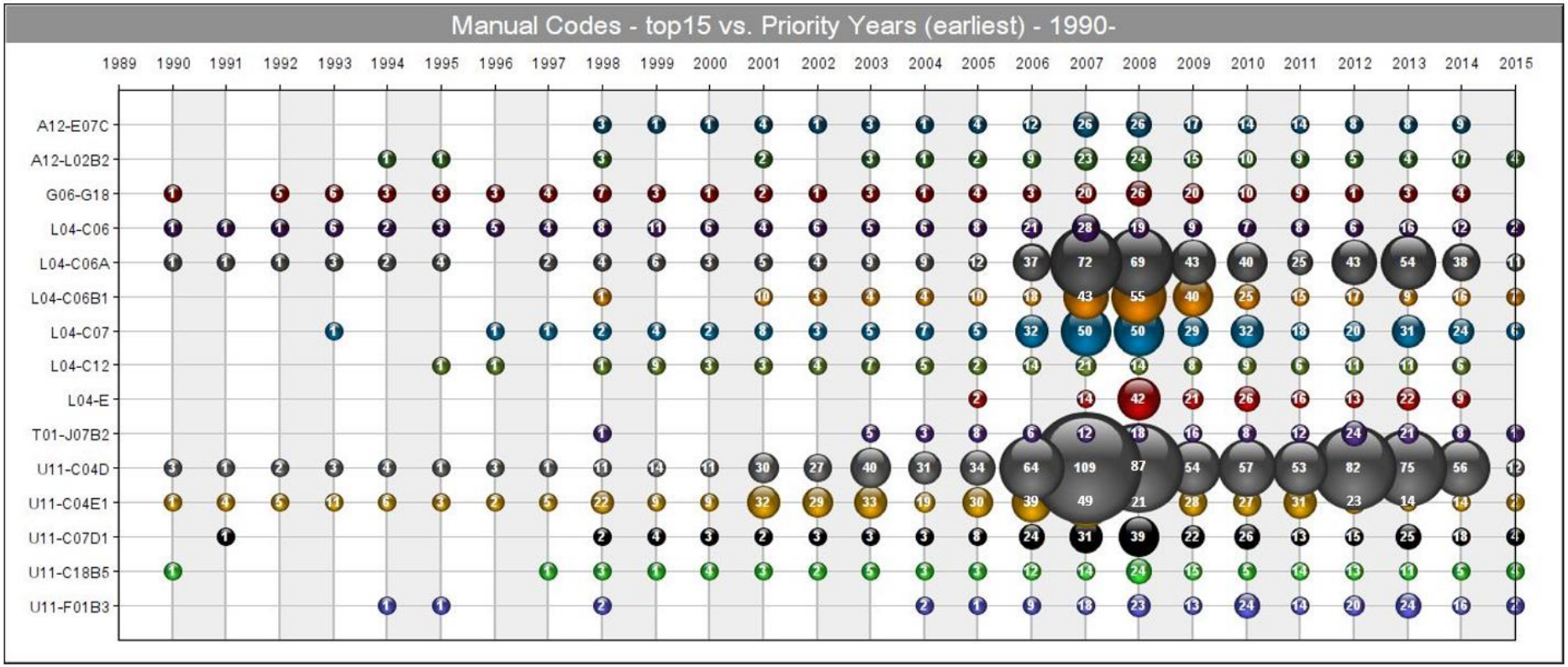
由于 1990 年以前专利申请数量非常少，指导意义不大，所以本文只研究 1990 年以来专利的技术走势情况。下图显示多重图形技术在 1990 年以来排名前 15 的德温特手工代码随时间的变化情况。

从图中看出，1997 之前，该技术处于缓慢发展期，涉及的技术点比较少，

U11-C04F1（半导体和电子电路 - >半导体材料和加工 - >半导体装置制造基板处理 - >光刻（光电，波束等），掩膜，技术，曝光和对准 - >多重图形技术半导体制造 - >多重图形技术的装置和方法）是最早涉及最多的技术点。

1997 年后相关研究涉及的技术点更加全面，每个技术分支的专利数量呈现持续增长势头，其中 U11-C04D（半导体和电子电路 - >半导体材料和加工 - >半导体装置制造基板处理 - >光刻（光电，波束等），掩膜，技术，曝光和对准 - >掩蔽技术微光刻）是涉及最多的技术点，并在 2001 年后快速增长。

2005 年后，L04-C06（耐火材料，玻璃，陶瓷 - >半导体[常规] - >半导体加工[常规] - >半导体加工 - 图形化技术[普通]）、L04-C07（耐火材料，玻璃，陶瓷 - >半导体[常规] - >半导体加工[常规] - >半导体加工 - 蚀刻工艺[普通]）和 L04-C06B1（耐火材料，玻璃，陶瓷 - >半导体[常规] - >半导体加工[常规] - >半导体加工 - 图形化技术[常规] - >半导体加工 - 抵抗 - >抗蚀图案）这三个技术点发展迅速，在 2009 年后申请量稍有下滑后在 2012 年后上升。



2.2 多重图形技术时间走势分析

表 2.1 德温特手工代码具体内容

序号	手工代码	手工代码含义	专利数量
1	U11-C04D	Semiconductors And Electronic Circuitry -> Semiconductor materials and processing -> Substrate processing for semiconductor device manufacture -> Lithography (photo-, beam-, etc.), masks, techniques, exposure and alignment -> Masking techniques for microlithography	879
2	L04-C06A	Refractories, Glass, Ceramics -> Semiconductors [general] -> Semiconductor processing [general] -> Semiconductor processing - patterning techniques [general] -> Semiconductor processing - mask design and manufacture	500
3	U11-C04E1	Semiconductors And Electronic Circuitry -> Semiconductor materials and processing -> Substrate processing for semiconductor device manufacture -> Lithography (photo-, beam-, etc.), masks, techniques, exposure and alignment -> Photolithography for semiconductor mfr. -> Apparatus and method for photolithography	469
4	L04-C07	Refractories, Glass, Ceramics -> Semiconductors [general] -> Semiconductor processing [general] -> Semiconductor processing - etching processes [general]	331
5	L04-C06B1	Refractories, Glass, Ceramics -> Semiconductors [general] -> Semiconductor processing [general] -> Semiconductor processing - patterning techniques [general] -> Semiconductor processing - resists -> Patterning of resists	277
6	U11-C07D1	Semiconductors And Electronic Circuitry -> Semiconductor materials and processing -> Substrate processing for semiconductor device manufacture -> Etching; chemical treatment for semiconductor manufacture -> Etching techniques -> Etching to produce finer details	246
7	L04-C06	Refractories, Glass, Ceramics -> Semiconductors [general] -> Semiconductor processing [general] -> Semiconductor processing - patterning techniques [general]	210
8	U11-F01B3	Semiconductors And Electronic Circuitry -> Semiconductor materials and processing -> Measuring; positioning for semiconductor technology -> Measuring; testing (including sorting) for semiconductor technology -> Film parameter measurement for semiconductor processing -> Measuring using image recognition	173
9	L04-E	Refractories, Glass, Ceramics -> Semiconductors [general] -> Semiconductor devices	165
10	A12-E07C	Polymers, Plastics -> Polymer applications -> Electrical engineering [others] -> Circuit components -> Semiconductor devices, integrated circuits; resistors	153
11	G06-G18	Printing, Coating, Photographic -> Photographic materials and processes -> Photographic processing agents and steps [others] -> Image formation by exposure to ionising radiation, light etc.	150
12	T01-J07B2	Computing And Control -> Digital computers -> Data processing systems -> For industrial process control -> Computer control of manufacturing/industrial machines and Quality Control (QC) -> Semiconductor manufacture control	143
13	U11-C18B5	Semiconductors And Electronic Circuitry -> Semiconductor materials and processing -> Substrate processing for semiconductor device manufacture -> Multistep processes for semiconductor device mfr. -> Multistep processes for manufacture of electronic devices other than transistors per se -> Complete manufacture of memory	143
14	A12-L02B2	Polymers, Plastics -> Polymer applications -> (Electro)photography, laboratory, optical [other] -> Other photographic materials, processes [exc. (film) support; binders] -> Compositions for making printing plates or electrical devices* -> Compositions for making electrical devices	137
15	L04-C12	Refractories, Glass, Ceramics -> Semiconductors [general] -> Semiconductor processing [general] -> Semiconductor processing - insulating and passivating layers [general]	136

3.专利申请国家/地区分布

专利最早优先权国家/地区在一定程度上反应技术的来源地，美国是多重图形技术专利产出最多的国家，占比 35%；其次日本、韩国也是该领域技术产出较多的国家，分别占 27%和 24%；中国专利产出排名第四。

专利公开国家/地区在一定程度上反映的是技术的市场保护分布情况，从图 3.1 可以看出美国是全球多重图形技术方面的专利申请人最重视的；日本、韩国分别排名第二、第三，分别占 19%和 16%；国际申请排名第五，这在一定程度上反映专利的国际布局程度；中国、欧洲专利、台湾、德国也具有相对比重的市场份额。

通过专利最终优先地和受理地的对比发现，美国在最早优先权国家/地区的比例图中占比 35%，而在公开国家/地区的比例图中占比 45%，比例上升，说明在美国多重图形技术流入多于技术产出。说明美国在国际市场的受重视程度很大。而日本和韩国刚好相反，这两个国家的技术流入少于技术产出。注意的是“研究成果披露”的专利也占 1%。在该技术领域一些公司选择披露来进行防御性保护。

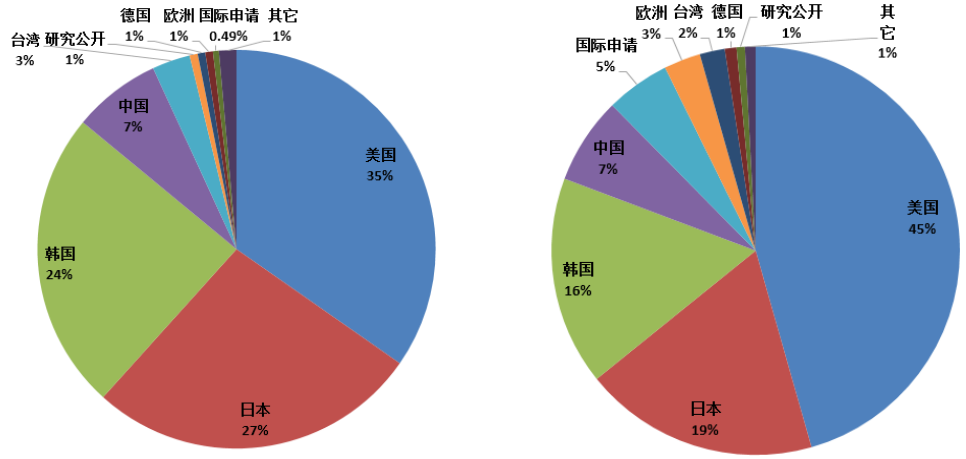


图 3.1 多重图形技术专利最早优先国家/地区、公开国家/地区对比

4 专利申请人分析

4.1 主要申请人专利数分析

主要申请人分析主要是分析多重图形技术领域专利申请人的专利产出数量，从而遴选出主要申请人，作为后续多维组合分析、评价的基础，通过对清洗后的专利家族的专利申请人分析，可以了解在多重图形技术领域的主要研发机构。

按照专利家族数量进行统计分析，得出该领域排名前 15 名的机构如图 4.1 所示。

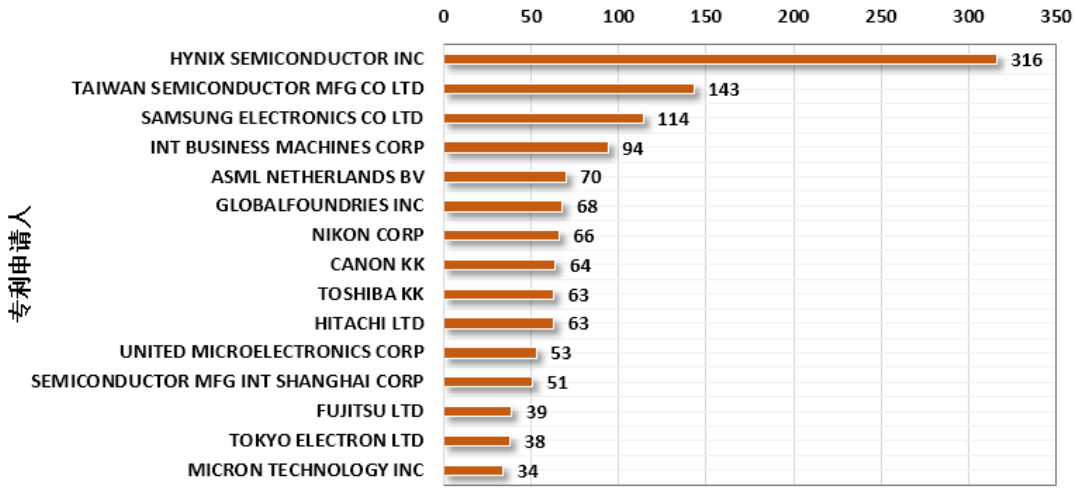


图 4.1 多重图形技术专利主要申请人

海力士半导体公司（HYNIX SEMICONDUCTOR INC）拥有专利技术 316 个位列第一，占总量的 13.9%。专利数量排名第二的台湾半导体制造公司（TAIWAN SEMICONDUCTOR MFG CO LTD）拥有专利技术 143 个，占总量的 6.3%。排名第三的三星电子（SAMSUNG ELECTRONICS CO LTD）拥有专利技术 114 个，占总量的 5.0%。排名前 15 的研究机构共有专利 1276 个，占总量的 56.3%。以上数据显示该技术没有集中在几个大的公司或机构，说明其集中性不是很强。

4.2 主要申请人时间趋势

分析多重图形技术主要申请人的历年专利数量的趋势，从而了解主要申请人投入多重图形技术的动态，深入了解申请人各年间的专利布局态势，观察多重图形技术的新秀或是退出等信息。

图 4.2 显示了多重图形技术的前 15 名专利权人历年专利的增长趋势对比图。通过该图我们可以看出，富士通（FUJITSU）、IBM、日立（HITACHI）、佳能（CANON）都属于在该领域研究比较早的机构。

该技术专利申请最多的海力士半导体公司（HYNIX SEMICONDUCTOR INC）从 1995 年才开始申请专利，在 2006 年起进入大量专利申请期，异军突起，在 2008 年达到申请高峰后，专利申请量开始递减。

GLOBAL FOUNDRIES 在 2009 年才开始申请该技术方向的专利，在 2012 年申请量达到 24，是当年申请量最多的公司。

台湾半导体制造公司（TAIWAN SEMICONDUCTOR MFG CO LTD）从早期 1993 年开始申请相关专利，此后一直以每年个位数的申请量维持该技术的先进性，在 2009 年开始申请量上升，在 2013 年达到最高，也是该年申请量最多的公司。

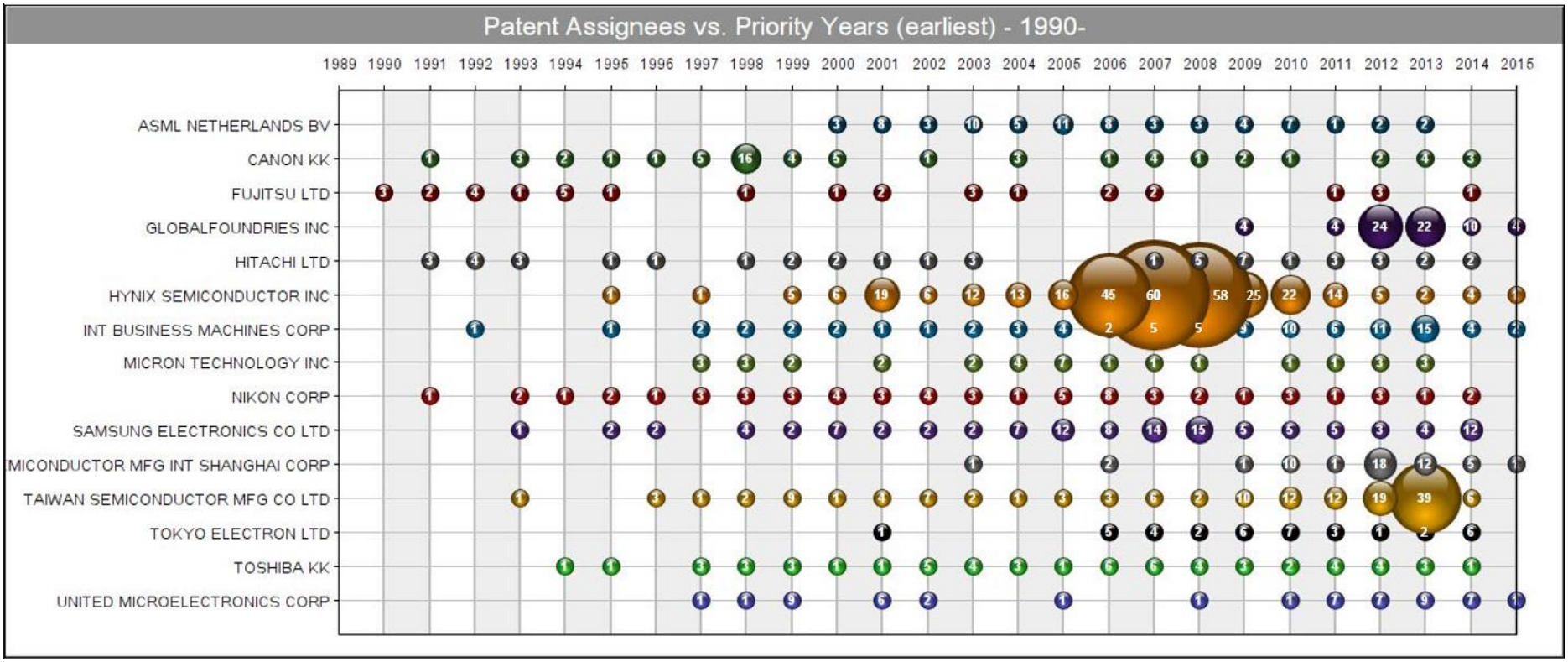


图 4.2 多重图形技术专利主要申请人申请时间趋势

4.3 主要申请人技术对比

主要申请人技术对比分析是对主要申请人投资技术领域进行对比分析，透析各申请人的技术布局，从而分析各申请人的技术发展策略。图 4.3 显示了多重图形技术的前 15 名专利权人主要技术对比图。

技术大头海力士半导体公司（HYNIX SEMICONDUCTOR INC）研究最多的是 U11-C04D（半导体和电子电路 - >半导体材料和加工 - >半导体装置制造基板处理 - >光刻（光电，波束等），掩膜，技术，曝光和对准 - >掩蔽技术微光刻）、L04-C06A（耐火材料，玻璃，陶瓷 - >半导体[常规] - >半导体加工[常规] - >半导体加工 - 图形化技术[常规] - >半导体加工 – 掩膜设计和制造）和 L04-C07（耐火材料，玻璃，陶瓷 - >半导体[常规] - >半导体加工[常规] - >半导体加工 - 蚀刻工艺[普通]）。其中前两个技术 U11-C04D、L04-C06A 也是其他机构都研究比较多的技术。

此外，U11-C04E1（半导体和电子电路 - >半导体材料和加工 - >半导体装置制造基板处理 - >光刻（光电，波束等），掩膜，技术，曝光和对准 - 半导体制造>光刻 - >仪器和方法 光刻）是各个机构研究最多的技术之一。

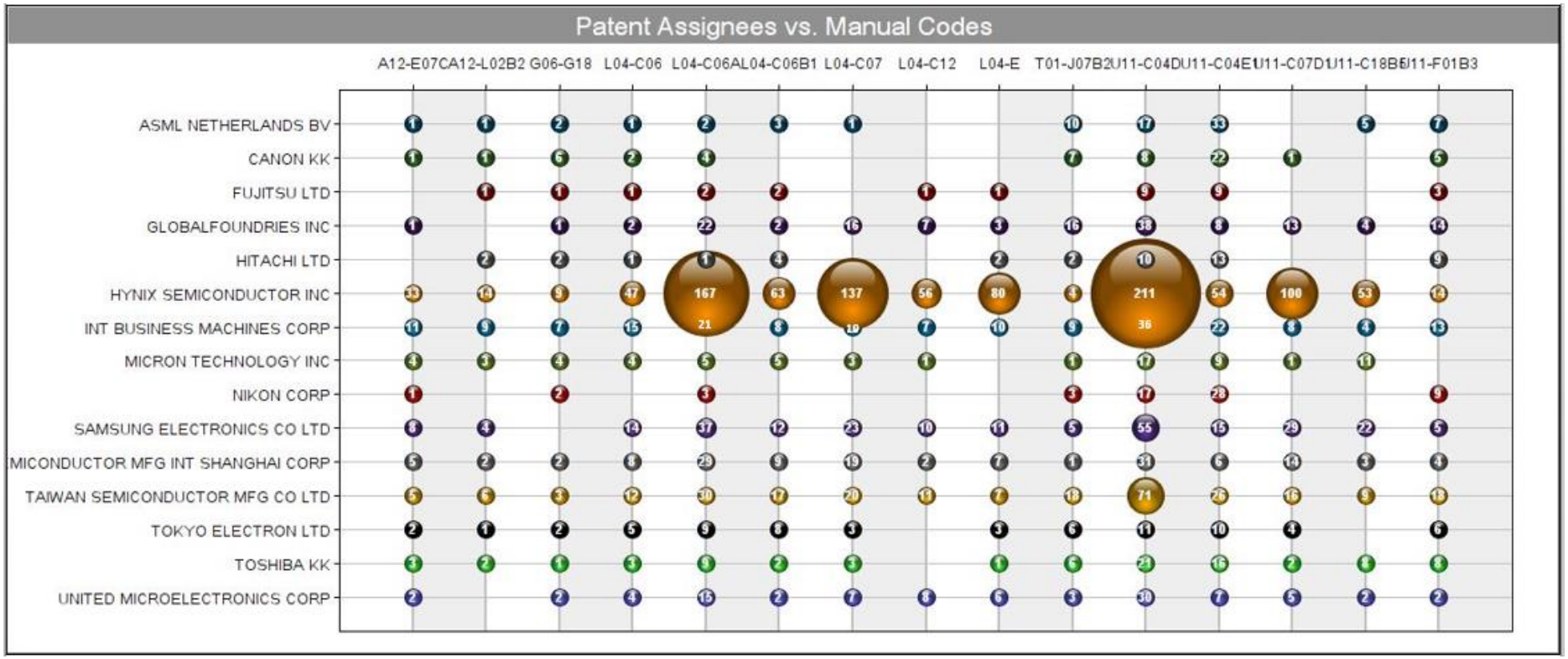


图 4.3 多重图形技术专利主要申请人技术对比

4.4 主要申请人合作分析

申请人合作分析是对申请人合作申请专利的情况进行对比分析，借以发现申请人的知识产权共享模式、创新能力、被支持力度和技术流动信息等，如图4.4是排名前50的（拥有7个以上）技术申请人的合作网络图。

从图中看到，该技术的合作性相对不多。只有两个相对大的合作圈和 4 个小的合作伙伴关系。有36个机构是独立产出专利。

第一个大的合作圈中，瑞萨电子（RENESAS ELECTRONICS）作为合作核心分别与日立（HITACHI）、NEC、和三菱电子（MITSUBISHI ELECTORIC）有专利合作产出。

第二个大的合作圈中，IBM 是重要的合作核心，分别与英飞凌（INFINEON TECHNOLOGIE）和 GLOBAL FOUNDRIES 合作。而 GLOBAL FOUNDRIES 又与 AMD 有合作。

此外，台湾半导体制造公司（TAIWAN SEMICONDUCTOR MFG CO LTD）、三星（SAMSUNG）、INTEL 等公司的专利都是独立申请的，与其他机构没有合作。

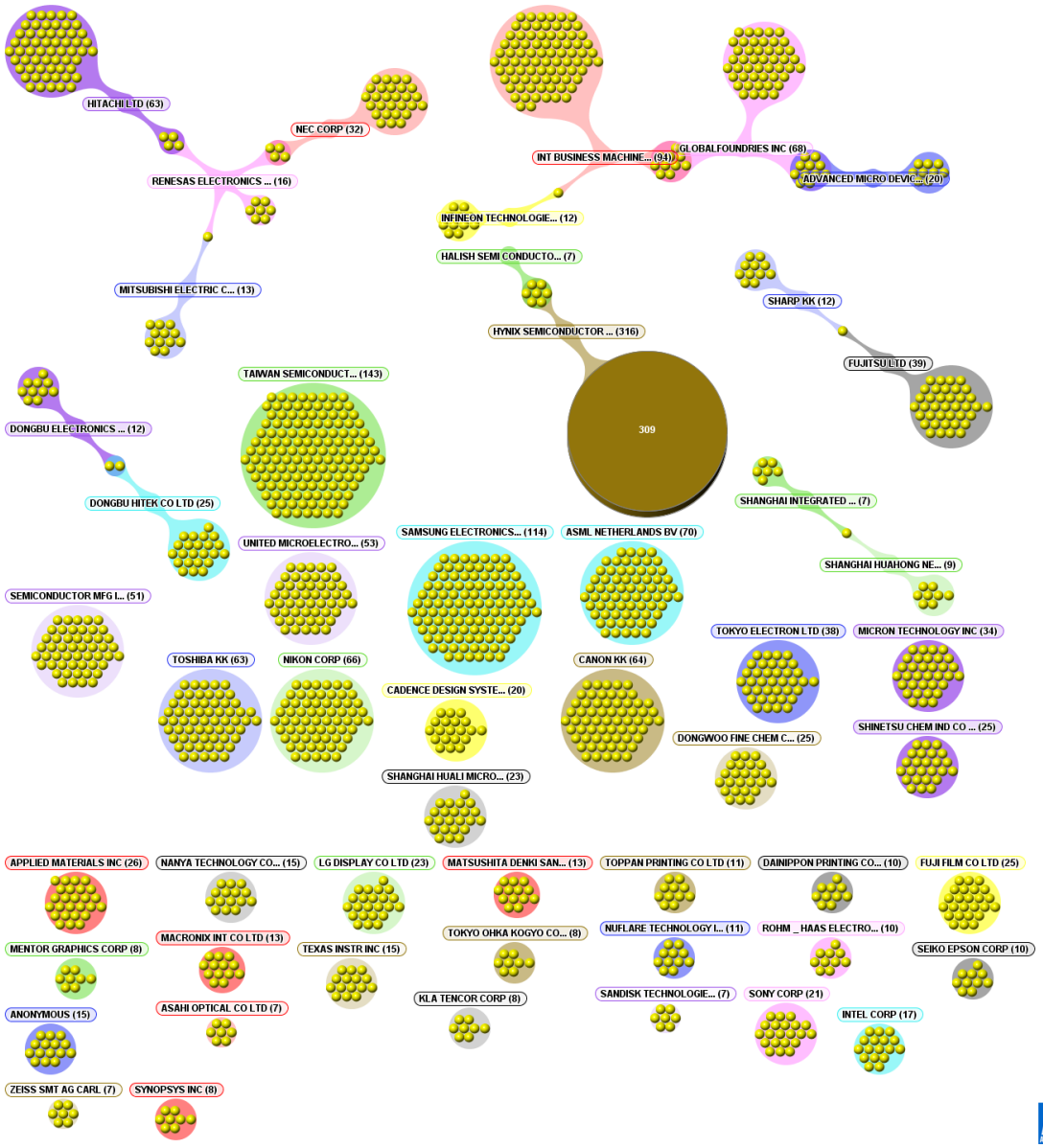


图 4.4 多重图形技术专利主要申请人合作

4.5 主要申请人技术关联分析

基于技术分类等对申请人潜在关系进行分析，借以发现申请人的技术关联、潜在合作或竞争关系等，如图 4.5 所示的多重图形技术专利主要申请人技术关联图，该图排名前 50 的（拥有 7 个以上）多重图形技术申请人的合作网络图。可以看到存在技术切合度非常高机构，这些申请人之间存在可能的激烈竞争或密切的合作，而独立的点代表该机构技术的相对独立性。

从图中看出，该技术的合作网络存在小范围性。

海力士半导体公司（HYNIX SEMICONDUCTOR INC）、台湾半导体制造公司（TAIWAN SEMICONDUCTOR MFG CO LTD）、尼康（NIKON）和联华电子（UNITED MICROELECTRONICS）是其中的几个技术核心。与它们的技术相似的公司最多，有 5 个以上。说明他们研究的技术范围最广。

海力士半导体公司（HYNIX SEMICONDUCTOR INC）在 U11-C07D（半导体和电子电路 - >半导体材料和加工 - >半导体器件制造的基板加工 - >蚀刻;化学处理半导体制造 - >蚀刻技术）上与其他公司技术相似性较大，研究最多。

台湾半导体制造公司（TAIWAN SEMICONDUCTOR MFG CO LTD）在 T01-J15A（计算与控制 - >数码电脑 - >数据处理系统 - >计算机辅助设计（CAD）和模拟 - >设计和电路和硬件的模拟）上与其他公司技术相似性较大。

尼康（NIKON）在 U11-C04E（半导体和电子电路 - >半导体材料和加工 - >半导体装置制造基板处理 - >光刻（光电，波束等），掩膜，技术，曝光和对准 - 半导体制造>光刻）与其他公司技术相似性较大。

联华电子（UNITED MICROELECTRONICS）则是在 L04-C06A（耐火材料，玻璃，陶瓷 - >半导体[常规] - >半导体加工[常规] - >半导体加工 - 图形化技术[常规] - >半导体加工 - 面膜设计和制造）与其他公司技术相似性最大。

此外，INTEL 等公司的技术相对独立。

图中显示，各个公司技术上的相似性不集中，比较分散，说明该技术的多个技术分支方向上都有不同的公司在研究，并掌握相应的核心技术，展开相应的技术合作。

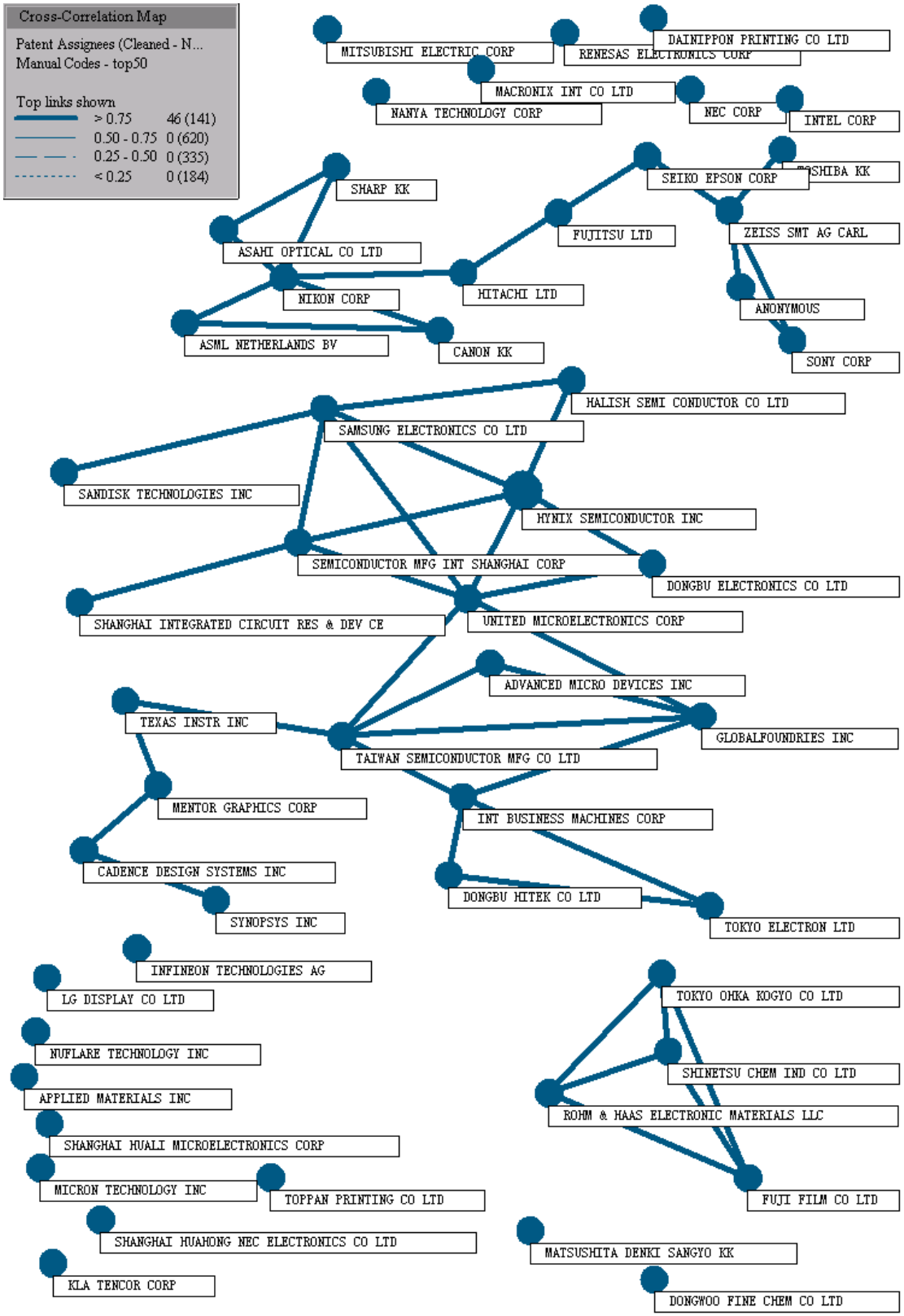


图 4.5 多重图形技术专利主要申请人技术关联

检索分析：赵慧敏、王丽

多重图形技术重点专利

说明：

将此前专利分析所用的数据集导入 Innography 专利数据库分析“多重图形技术”专利，抽取专利结果中专利强度≥91 分（专利强度范围是 1-100 分，其中 80-100 分的专利代表核心专利），最早优先权年在 2008 年以后的，33 件专利作为重点专利进行推荐。

1. 专利号：JP05886804B2

专利名称：Producing resist composition used for producing semiconductor apparatus, involves cleaning apparatus for producing resist composition with cleaning liquid, and applying cleaning liquid on evaluation substrate by spin-coating

专利发明人：BIYAJIMA Y; IWABUCHI M; OGIHARA T; OGIWARA T

专利权人：SHINETSU CHEM CO LTD; SHINETSU CHEM IND CO LTD; BIYAJIMA Y; IWABUCHI M; OGIHARA T

申请日： 2013-09-02

摘要：NOVELTY - Resist composition used in a process for producing a semiconductor apparatus, is produced which involves cleaning an apparatus for producing the resist composition with a cleaning liquid; applying the cleaning liquid on an evaluation substrate by spin-coating after removing the cleaning liquid from the apparatus for producing the resist composition; repeating the step of cleaning and the step of applying until the change in the density of defects having a size of 100nm or more on the evaluation substrate; and producing the resist composition.

USE - The method is useful for producing resist composition used in process for producing semiconductor apparatus (claimed).

ADVANTAGE - The method can produce resist composition stably capable of producing resist composition whose coating defects are reduced. Additionally, the method for producing resist composition can more accurately measure the degree of cleanliness in an apparatus for producing a resist composition than a conventional method. A residue generated in the previous production process in the apparatus for producing a resist composition can be cleaned and removed until the change in the density of defects becomes a predetermined value by using a defect detecting apparatus. Since coating defects of the resist composition obtained are reduced, the resist composition can preferably be used for liquid immersion exposure, double patterning and organic solvent development, and the yield of semiconductor apparatuses produced can be improved.

2. 专利号：JP05913191B2

专利名称：Forming resist under layer film used in lithography process, involves applying composition including organic compound having aromatic unit on substrate and heat-treating resist under layer film in atmosphere having specified oxygen content

专利发明人：FUJII T; KOORI D; KORI D; NONAKA S; OGIHARA T; OGIWARA T; TACHIBANA S

专利权人：SHINETSU CHEM CO LTD; SHINETSU CHEM IND CO LTD

申请日：2013-05-08

摘要：NOVELTY - Forming a resist under layer film comprises: applying a composition, for forming a resist under layer film containing an organic compound having an aromatic unit, on a substrate; and heat-treating the resist under layer film applied in an atmosphere whose oxygen concentration is ≥ 10% at 150-600° C for 10-600 seconds after heat-treating the same in an atmosphere whose oxygen concentration is less than 10% at 50-350° C.

USE - The method is useful for forming a resist under layer film used in a lithography process, which is useful for forming a pattern on a substrate such as a semiconductor substrate (all claimed).

ADVANTAGE - The resist under layer film has excellent filling/flattening properties, high durability and etching resistance so that unevenness on the substrate can be flattened even in complex processes such as multilayer resist method and double patterning method, and forms the fine pattern on the substrate to be processed with high precision.

3. 专利号：US9093457B2

专利名称：Method for fabricating stacked microelectronic packages for multiple microelectronic devices, involves removing selected portions of unpatterned paste layers between neighboring sidewall conductors on each package during patterning

专利发明人：GONG Z; GONG Z T; HAYES S M; VINCENT M B; WRIGHT J R

专利权人：FREESCALE SEMICONDUCTOR INC

申请日：2012-08-22

摘要：NOVELTY - The method involves separating the panel stack into partially-completed stacked microelectronic packages and patterning the unpatterned paste layers to form multiple patterned sidewall conductors interconnecting the microelectronic devices (38) included within the stacked microelectronic packages. The selected portions of the unpatterned paste layers between neighboring sidewall conductors on each stacked microelectronic package are removed during patterning.

USE - Method for fabricating stacked microelectronic packages for multiple microelectronic devices, for semiconductor die carrying integrated circuits, micro electromechanical systems (MEMS), optical devices and passive electronic components.

ADVANTAGE - Mechanical sawing can be performed in a highly efficient manner, and the trenches are formed as a linear cuts extending entirely across the case of panel stack such that fabrication can be performed easily and effectively. The microelectronic device panels are bonded

together using double-sided adhesive tape such that the relative positioning of the microelectronic devices which are embedded within panels can be maintained during processing and after singulation into discrete stacked microelectronic packages.

4. 专利号：US8782570B1

专利名称：Method for implementing physical electronic circuit design with multiple-patterning techniques, involves coloring fixed objects in electronic design with color based on result of coloring routing tracks colors with primary number of colors

专利发明人：ARIFIN T; CHEN D; CHEN J; GEROUSIS V; HUANG Y; KIM S A; LI J; ZHANG S; ZHAO G

专利权人：CADENCE DESIGN SYSTEMS INC

申请日：2012-05-07

摘要：NOVELTY - The method involves using a processor or processor core to identify (102) a constraint for multiple mask designs of a multiple-patterning lithography process for manufacturing an electronic design. Multiple routing tracks are colored (104) in the electronic design with primary number of colors. The fixed objects in the electronic design are colored (106) with a color based on the result of coloring routing tracks with primary number of colors. A color conflict is improved in the electronic design based on a characteristic of an object that exhibits the color conflict with another object.

USE - Computer implemented method for implementing a physical electronic circuit design of an electronic circuit with multiple-patterning techniques.

ADVANTAGE - The fixed objects in the electronic design are colored with a color based on the result of coloring routing tacks with primary number of colors, which enables to minimize color conflicts and reduce design rule violations, and thus ensures a multiple-patterning clean layout, such that the electronic circuit design satisfies applicable multiple-patterning constraints on creation in a simple, economical and time-effective manner.

5. 专利号：US8772102B2

专利名称：Forming self-aligned contacts on e.g. semiconductor device that is used in fabrication of e.g. CPUs, by forming sacrificial gate structures for transistors above substrate, and forming etch stop layer above substrate and gate structures

专利发明人：CHI M

专利权人：GLOBALFOUNDRIES INC

申请日：2012-04-25

摘要：NOVELTY - The method comprises: forming sacrificial gate structures (30) for spaced-apart transistors (33) above a semiconducting substrate (101); forming an etch stop layer above the substrate and the sacrificial gate structures; performing an angled ion implant process to implant an etch-inhibiting species into less than an entirety of the etch stop layer; forming a layer of insulating

material above the etch stop layer after performing the angled ion implant process; and performing a chemical mechanical polishing process to expose a portion of each of the sacrificial gate structures.

USE - The method is useful for forming self-aligned contacts on a semiconductor device such as transistor including p-type FET and n-type FET, a planar FET device and a non-planar device such as FinFET, that is used in the fabrication of advanced integrated circuits such as CPUs, memory devices and application specific integrated circuits.

ADVANTAGE - The method is capable of improving the accuracy and reliability of the self-aligned contacts formation on the semiconductor device in a simple and cost-effective manner.

6. 专利号：VN40733A

专利名称：Method for forming semiconductor structure, involves performing negative-tone development process so as to remove portions of negative photoresist layer to form double patterned negative photoresist layer

专利发明人：CHEN P; GU Y; HU D; HU H; WU K; WU Q

专 利 权 人：SEMICONDUCTOR MFG INT CORP; SEMICONDUCTOR MFG INT SHANGHAI CORP; TENCENT TECHNOLOGY SHENZHEN CO LTD

申请日：2012-03-12

摘要：NOVELTY - The method involves performing (S203) exposure process to form first and second exposure regions in respective positive and negative photoresist layers. A positive-tone development process is performed (S204) to remove first exposure region to form first opening. The second exposure region is etched (S205) along first openings to form second openings through photoresist layers. A negative-tone development process is performed (S206) so as to remove portions of negative photoresist layer to form double patterned negative photoresist layer.

USE - Method for forming semiconductor structure (claimed).

ADVANTAGE - The single exposure process and single photo mask are used to form double patterned structure in the negative photoresist layer, by forming first and second exposure regions on respective positive and negative photoresist layers and transferring the pattern of positive photoresist layer to the negative photoresist layer, thus the process is simple with high accuracy. Hence the manufacturing cost is reduced effectively. The development processes are performed on respective negative and positive photoresist layer so that there is no interaction between the development processes, thus the processes can be easily controlled with good topography.

7. 专利号：CN103227152B

专利名称：Method of forming static RAM (SRAM) device using sidewall image transfer techniques involves performing etching process on hard mask layer through patterned hard mask layer to define first, second and third fins in semiconductor substrate

专利发明人：LICAUSI N V; RIKOS N V

专 利 权 人：ADVANCED MICRO DEVICES INC; GLOBAL FOUNDRIES INC;

GLOBALFOUNDRIES INC; GLOBALFOUNDRIES US INC

申请日：2012-01-26

摘要：NOVELTY - The manufacturing method involves forming a patterned spacer mask layer above a hard mask layer that is formed above a semiconductor substrate (220). The patterned spacer mask layer is comprised of first spacers, second spacers and third spacers. A first etching process is performed on the hard mask layer through the patterned spacer mask layer to define a patterned hard mask layer. A second etching process is performed on the hard mask layer through the patterned hard mask layer (222A) to define first, second and third fins (202,204,206,208,210,212) in the substrate.

USE - Method of forming SRAM device using sidewall image transfer techniques.

ADVANTAGE - Enables device designers to finely tune the design of SRAM devices if desired. The fin width of the P-FinFET devices and N-FinFET devices can be varied to tailor threshold voltage values for such devices on individual basis, leading to better threshold voltage matching. Provides for precise control of spacing between transistor banks on the SRAM device.

8. 专利号：TWI509669B

专利名称：Method for patterning features e.g. trenches in material layer utilized during formation of e.g. storage devices, involves performing etching process through etch mask on structure to define features in structure

专利发明人：LICAUSI N V; RICOSE N V

专 利 权 人 ：ADVANCED MICRO DEVICES INC; GLOBALFOUNDRIES INC; GLOBALFOUNDRIES US INC

申请日：2011-11-28

摘要：NOVELTY - The method involves forming a first set of spacers (114A) adjacent to a mandrel (112), and a second set of spacers (118A) adjacent to other set of mandrels (116A). An etching process is performed to selectively remove the mandrels such that an etch mask is defined. Another etching process is performed through the etch mask on a structure (110) to define a set of features in the structure, where each spacer of the first set has a width same as a width (118AW) of each spacer of the second set. The structure is designed as a semiconducting substrate or a material layer.

USE - Method for patterning features e.g. fins, lines or trenches, in a structure i.e. material layer, utilized during formation of integrated circuit devices e.g. CPUs, storage devices and application specific integrated circuit (ASIC) device, or in a semiconducting substrate of a FinFET device (all claimed) using a multiple sidewall image transfer technique.

ADVANTAGE - The method enables performing the etching process through the etch mask on the structure to define the features in the structure such that the features can be patterned in the substrate in a simple manner.

9. 专利号：US8560998B1

专利名称：Computer implemented method for routing electronic circuit design for double pattern lithography, involves using processor to perform C-routing for electronic design using high-level routing generated from global routing

专利发明人：RAJ S S; SALOWE J S

专利权人：CADENCE DESIGN SYSTEMS INC

申请日：2010-12-29

摘要：NOVELTY - The method involves performing global routing for an electronic design to generate a high-level routing for the electronic design. A processor is used to perform C-routing for the electronic design using the high-level routing generated from the global routing, where the C-routing provides color seeding for space tiles in conduits using a marking including a first color and a second color in which a space tile comprises a region that provides an allowable area for introducing routing path. Detail routing is performed based upon the color-seeded space tiles from the C-routing.

USE - Computer implemented method for routing an electronic circuit design for double pattern lithography.

ADVANTAGE - The method implements the track assignment spacings to match any required distances, which are not dependent and/or constrained by grid-based distance requirements, thus allowing the tracks to be assigned with spacing distances that are specific to the current routing and process requirements instead of being locked into a fixed grid having grid parameters.

10. 专利号：US8671368B1

专利名称：Computer implemented method for routing electronic circuit design, involves routing electronic design by identifying probes, and processing probes by checking whether probe reaches intended destination with appropriate color

专利发明人：RAJ S S; SALOWE J S

专利权人：CADENCE DESIGN SYSTEMS INC

申请日：2010-12-29

摘要：NOVELTY - The computer implemented method involves receiving a color-seeded layout for an electronic design with first color and second color to color several routing tracks. A processor is used to route the electronic design by identifying probes through space-tiles which identifies an area available for routing in the electronic design. The probes have sub-divisions of the space-tiles, and are associated with several colors. The probes are processed by checking whether the probe reaches the intended destination with appropriate color.

USE - Computer implemented method for routing electronic circuit design.

ADVANTAGE - The efficient routing of the electronic circuit design is achieved for double-patterning lithography without the occurrence of any error in the layout decomposition. Efficient routing of electronic circuit is achieved under low cost.

11. 专利号：TWI496192B

专利名称：Method for patterning e.g. material portion or structure of semiconductor device, involves removing pattern using etching process to leave final pattern comprising remaining portion of material layer that remains on sidewalls of pattern

专利发明人：DUNN S W; HETZER D

专利权人：TOKYO ELECTRON AMERICA INC; TOKYO ELECTRON LTD

申请日：2010-11-23

摘要：NOVELTY - The method involves preparing a pattern (122) in a layer of radiation-sensitive material (120') using lithographic process. Critical dimension (CD) slimming process is performed to reduce CD to reduced CD. A material layer (160) is conformally deposited over the pattern with the reduced CD. The material layer is partially removed using etching process to expose a top surface of the pattern. The pattern is removed using the etching process to leave a final pattern comprising a remaining portion of the material layer that remains on the sidewalls of the pattern.

USE - Method for patterning a substrate e.g. material portion and structure of a device e.g. semiconductor and electronics device, base substrate structure such as semiconductor wafer, and layer on or overlying base substrate structure such as thin film.

ADVANTAGE - The method enables increasing normality in excess of 0.26 to provide increase in substrate throughput for double patterning process and decrease in substrate defectivity, which affects device yield. The method enables providing freeze process to create a protective layer extending partly or wholly through the pattern, thus protecting the pattern in the layer of radiation-sensitive material from subsequent lithographic processes such as coating, exposing, developing and slimming processes, thus freezing the layer of radiation-sensitive material to form a frozen layer of radiation-sensitive material characterized by the reduced CD. The method enables reducing ultimate feature size that is printable on the substrate in an effective manner.

12. 专利号：TWI443448B

专利名称：Method for composing polygons of mask levels into target pattern of polygons to be formed on substrate, involves generating plug pattern to be printed on substrate as specific mask level to remove enabling pattern from substrate

专利发明人：ATKAR P N; BAIDYA B; BENKATESAN R; HOOKER K J; HU B; JEONG S; KIM S; OGADHOH S; SINGH V; VENKATESAN R

专利权人：INTEL CORP; ATKAR P N; BAIDYA B; HOOKER K J; HU B; JEONG S; KIM S; OGADHOH S; SINGH V; VENKATESAN R

申请日：2010-06-25

摘要：NOVELTY - The method involves receiving a design layout defining a target pattern. A sacrificial enabling pattern increasing regularity of edges to approximate diffraction grating is synthesized based on target pattern. A grating pattern to be printed on the substrate with exposure

wavelength is generated as specific mask level. A plug pattern to be printed on substrate with exposure wavelength is generated as another mask level, such that sacrificial enabling pattern are removed from the substrate while retaining the target pattern on the substrate.

USE - Method for composing polygons of mask levels into target pattern of polygons to be formed on substrate.

ADVANTAGE - Since the plug pattern to be printed on substrate is generated as specific mask level to remove enabling pattern from substrate, the improved double-patterning process can be achieved while reducing the number of false violations.

13. 专利号：US8455364B2

专利名称：Sidewall image transfer method for fabrication of semiconductors and integrated circuit chips, involves forming sacrificial mandrel by patterning portion of lithographic layer consisting of planarization layer

专利发明人：KANAKASABAPATHY S K

专利权人：INT BUSINESS MACHINES CORP

申请日：2009-11-06

摘要：NOVELTY - A lithographic layer consisting of silicon containing antireflective coating and a planarization layer overlying the antireflective coating is formed on a substrate. A sacrificial mandrel consisting of a portion of lithographic layer is formed by patterning a portion of lithographic layer using photolithographic process. A microstructure is produced by using the sacrificial mandrel in a sidewall image transfer process.

USE - Sidewall image transfer method for fabrication of semiconductors and integrated circuit (IC) chips.

ADVANTAGE - The litho stack is used to define and form the sacrificial mandrel for avoiding the necessary high temperature processes and enabling usage of very low temperatures for the spacer deposition process. The lower temperature atomic layer control and conformality enables usage of atomic layer deposition (ALD) or multilayer deposition (MLD).

14. 专利号：KR1603346B1

专利名称：Multiple pattern-forming process, comprises coating a first positive resist composition, applying a resist-modifying composition, and coating a second positive resist composition

专利发明人：IIO M; NISHI T; WATANABE T

专利权人：SHINETSU CHEM CO LTD; SHINETSU CHEM IND CO LTD

申请日：2009-08-05

摘要：NOVELTY - A multiple pattern-forming process comprising: (a) coating a first positive resist composition comprising as a base resin a polymer comprising recurring units adapted to increase alkali solubility under the action of acid and recurring units having lactone structure onto

a substrate and baking to form a first resist film; (b) applying a resist-modifying composition comprising a basic nitrogen-containing compound; and (c) coating a second positive resist composition on it and baking to form a second resist film.

USE - The process is useful for forming multiple pattern (claimed).

ADVANTAGE - The process forms a fine size pattern.

15. 专利号：KR1442876B1

专利名称：Forming pattern comprises coating a composition comprising copolymer having lactone-, acid- and carbamate repeating units onto substrate, exposing film to radiation, baking, developing, heating, and coating a composition comprising solvent

专利发明人：HATAKEYAMA; HATAKEYAMA J; KATAYAMA K; OHASHI M; OHSAWA Y; OSAWA Y

专利权人：SHINETSU CHEM CO LTD; SHINETSU CHEM IND CO LTD

申请日：2009-08-04

摘要：NOVELTY - Forming a pattern, comprises: coating a first positive resist composition comprising a copolymer comprising recurring units having lactone, an acid labile group and a carbamate structure and a photoacid generator onto a substrate (10) to form a first resist film (30), exposing the film to high-energy radiation, post-exposure baking, developing, heating, coating a second positive resist composition comprising a solvent containing alcohol and an optional ether onto the first resist pattern-bearing substrate to form a second resist film, exposing, post-exposure baking, and dveloping.

USE - The process useful for forming pattern.

ADVANTAGE - The process: provides pattern, without deformation of the first resist pattern; does not narrow or widen the size of pattern; and reduces the pitch between pattern features to one half. The substrate can be processed by a single dry etching.

16. 专利号：TWI509442B

专利名称：Method for routing interconnection of integrated circuit using double patterning, involves assigning alternate lines from array of routing tracks to be placed on photomasks such that adjacent tracks are associated with different photomasks

专利发明人：GEROUSIS V; NOICE D C; SEZGINER A; SWEIS J; YAO S

专利权人：CADENCE DESIGN SYSTEMS INC

申请日：2009-07-16

摘 要：NOVELTY - The method involves determining an array of routing tracks corresponding to metal lines oriented along a preferred direction. The alternating lines are assigned from the array of routing tracks to be placed on photomasks such that the adjacent tracks are associated with different photomasks. The wires are routed for integration circuit along the tracks and results are output by storing the results in computer readable medium or displaying the results

on a display device.

USE - Method for routing interconnections of integrated circuit (IC).

ADVANTAGE - The interconnections of integrated circuit are routed using routing algorithm which minimizes cost function. The router does not allow routing configuration in the layout that cannot be successively manufactured with double patterning.

17. 专利号：JP05573356B2

专利名称：Forming pattern comprises coating a composition comprising e.g. copolymer having e.g. lactone unit and base generator onto substrate, exposing the film to radiation, baking, developing, heating and coating a composition comprising solvent

专利发明人：GATTAYAMA G; HATAKEYAMA; HATAKEYAMA J; KATAYAMA K; OHASHI M; OHSAWA Y; OSAWA Y

专利权人：SHINETSU CHEM CO LTD; SHINETSU CHEM IND CO LTD

申请日：2009-05-26

摘要：NOVELTY - Forming a pattern, comprises: coating a first positive resist composition comprising a copolymer comprising recurring units having lactone as an adhesive group and an acid labile group, a photoacid generator, and a base generator onto a substrate (10) to form a first resist film (30a), exposing to high-energy radiation, post-exposure baking and developing; heating the first resist pattern; and coating a second positive resist composition comprising solvent onto the first resist pattern-bearing substrate to form a second resist film (50), exposing, post-exposure baking and developing.

USE - The process is useful for forming pattern.

ADVANTAGE - The process enables a double patterning process of processing a substrate by a single dry etching, leading to improved throughputs and avoiding the problem of misregistration due to stress relaxation of the hard mask during etching.

18. 专利号：JP05353816B2

专利名称：Pattern forming, comprises coating first positive resist composition onto substrate to form first resist pattern, applying resist-modifying composition to first pattern, or coating second resist composition to form second resist pattern

专利发明人：GATTAYAMA G; HATAKEYAMA J; IIO M; KANAO G; KANO T; KATAYAMA K; KINSHO T; LIO M; NISHI T; WATANABE T

专利权人：SHINETSU CHEM CO LTD; SHINETSU CHEM IND CO LTD

申请日：2009-05-25

摘要：NOVELTY - Pattern forming process, comprises at least: coating first positive resist composition onto substrate and baking to form first resist film, exposing to high-energy radiation, post-exposure baking and developing with alkaline developer to form first resist pattern; applying resist-modifying composition to first resist pattern and heating to modify resist pattern; or coating

second positive resist composition on it and baking to form second resist film, exposing to high-energy radiation, post-exposure baking and developing with alkaline developer to form second resist pattern.

USE - The process is useful in pattern forming (claimed).

ADVANTAGE - The process: maintains and retains the first resist pattern satisfactory even after the pattern modifying treatment and second pattern formation; ensures double patterning process of processing a substrate through two exposures and a single dry etching; and provides desired hole pattern and fine feature pattern.

19. 专利号：US8024676B2

专利名称：Substrate e.g. workpiece, processing method for de-convolving lithographic process parameters during e.g. single-patterning procedure, involves performing corrective actions when confidence data is not greater than confidence threshold

专利发明人：CARCASI M A; DIXON D

专利权人：TOKYO ELECTRON LTD

申请日：2009-02-13

摘 要：NOVELTY - The method involves creating a mask including a multi-pitch scatterometry target (M-PST) masking pattern, where the M-PST masking pattern is aligned in a direction. Confidence data is determined using a neural network model, output parameters and/or input parameters. The confidence data is compared to a confidence threshold. The developed M-PST pattern is identified as a verified pattern when the confidence data is greater than the confidence threshold. Multiple corrective actions are performed when the confidence data is not greater than the confidence threshold.

USE - Method for processing a substrate e.g. semiconductor substrate, workpiece and LCD, using multi-pitch scatterometry targets (M-PSTs) for de-convolving lithographic process parameters during single-patterning (S-P) procedure, double-patterning (D-P) procedure and double-exposure (D-E) procedure that are utilized to control a transistor structure.

ADVANTAGE - The method enables processing the substrate in an effective manner using multi-pitch scatterometry targets (M-PST) that have critical dimension (CD) and sidewall angle (SWA) sensitivity to exposure focus variations, exposure dose variations and post exposure bake (PEE) temperature variations. The variations can be de-convolved, so that the individual measurement process variable contributor can be identified. The M-PSTs can be used during double-patterning (D-P) procedure, double-exposure (D-E) procedure and single-patterning (S-P) procedure, so as to control transistor structures in an effective manner.

20. 专利号：JP2012514762A

专利名称：Formation of microelectronic structure involves applying shrinkable composition to patterned surface, heating composition to form conformal layer of the composition on patterned

surface and over the feature, and removing of conformal layer

专利发明人：CLAYPOOL J; GUERRERO D; GUERRERO D J; LIN Q; PULIGADDA R; SMITH B

专利权人：BREWER SCI INC

申请日：2009-01-07

摘要：NOVELTY - A microelectronic structure is formed by providing a precursor structure (10) having a patterned surface including raised feature(s) having two sidewalls and an upper surface; applying a shrinkable composition to the patterned surface, where the composition covers the feature sidewalls and upper surface; heating the shrinkable composition to form a conformal layer of the composition on the patterned surface and over the feature; and removing some of the conformal layer to yield a pre-spacer structure comprising the feature and remnants of the conformal layer against the feature sidewalls.

USE - Method of forming a microelectronic structure.

21. 专利号：US7846756B2

专利名称：Semiconductor device i.e. non-volatile memory array, manufacturing method, involves etching hard mask features to form other hard mask features, and etching underlying layer of substrate using latter features as mask

专利发明人：CHEN Y; MAXWELL S; WANG C; YEN B K

专利权人：SANDISK 3D LLC

申请日：2008-12-31

摘要：NOVELTY - The method involves forming a hard mask layer i.e. silicon layer, and an imprint resist layer over an underlying layer of a substrate (100) in an order, forming features over hard mask features, and forming a spacer layer over the features. The spacer layer is etched to form a spacer pattern and expose top of the features. The features are removed. The hard mask features are etched using the spacer pattern as a mask to form other hard mask features. A part of the underlying layer is etched using the latter hard mask features as a mask to form a set of lines in communication with a memory cell.

USE - Method for manufacturing a semiconductor device i.e. non-volatile memory array.

ADVANTAGE - The method allows forming the features on the hard mask layer at a sufficiently low temperature using nano-imprint lithography, thus avoiding damages to the resist features. The method enables avoiding the need for forming and subsequent etching a bottom anti-refection coating (BARC) layer, thus simplifying processing during manufacturing the semiconductor device while avoiding uneven erosion of patterned features during the BARC etching.

22. 专利号：US8080443B2

专利名称：Semiconductor device i.e. nonvolatile memory array, making method, involves etching mask feature using spacer pattern as mask to form another mask feature, and etching

underlying layer as mask using latter mask feature

专利发明人：CHEN Y; RADIGAN S J; WANG C

专利权人：SANDISK 3D LLC

申请日：2008-10-27

摘要：NOVELTY - The method involves forming hard mask layers (300, 230) i.e. dielectric anti-reflective coating (DARC) layer, and patterning a hard mask using a spacer pattern (502) to form a hard mask feature. Features (402) are formed over the mask feature. Spacer layers are formed over the features. The spacer layers are etched to form the spacer pattern and expose top of the features. The features are removed. The mask feature is etched using the spacer pattern as a mask to form another hard mask feature. An underlying layer (200) is etched as a mask using the latter mask feature.

USE - Method for making a semiconductor device i.e. nonvolatile memory array.

ADVANTAGE - The method enables depositing a spacer layer at a sufficiently low temperature to avoid damaging of resist features. The method enables forming a bottom anti-reflection coating (BARC) material by performing a liquid phase deposition over and between the hard mask features to make a semiconductor device in an effective manner.

23. 专利号：US8209656B1

专利名称：Method for decomposing hierarchical design layout region of semiconductor device into two mask layouts, involves selecting decomposition solution to reduce number of split, where split occurs when geometry is divided into segment

专利发明人：HUCKABAY J; QIU Y; UPPALURI P; WANG X; ZHANG T

专利权人：CADENCE DESIGN SYSTEMS INC

申请日：2008-10-14

摘要：NOVELTY - The method involves iteratively examining different decomposition solutions for a design layout region to assign sets of geometry segments to a set of mask layouts, where the geometry segment is in conflict with another geometry segment according to a design rule such that the two geometry segments are assigned to different mask layouts at a computing device. The decomposition solution is selected to reduce a number of a split, where the split occurs when geometry is divided into two different segments that are assigned to the different mask layouts.

USE - Method for decomposing a design layout region i.e. hierarchical design layout region, of an integrated circuit e.g. semiconductor device and electronic system, into two mask layouts to fabricate a routing layer e.g. polysilicon layer and metal layer (all claimed) in multiple lithographic exposures.

ADVANTAGE - The method enables searching for conflicts to performs a determination of whether a valid solution exists for decomposition problem for the design layout region such that the design layout region does not decomposed within manufacturing constraints if conflicts detected, thus optimizing objective function in an efficient manner. The method enables assigning the

geometries in a group of collectively-assigned sets to different mask layouts so as to minimize the number of splits in the geometries of another group in an efficient manner.

24. 专利号：KR1523951B1

专利名称：Forming fine patterns of semiconductor device involves forming first patterns separated by space/forming capping films of material with first solubility in solvent/forming second layer with solubility less than first/forming second patterns

专利发明人：CHOE S; CHOE S U; CHOI S; CHOI S W; GANG Y; KANG R; KANG Y; KIM H; KIM H H; YOON J; YOON J Y; YUN J; YUN J Y

专利权人：SAMSUNG ELECTRONICS CO LTD; CHOI S; KANG Y; KIM H; YOON J

申请日：2008-10-09

摘要：NOVELTY - Forming fine patterns of semiconductor device involves forming first mask patterns (120) on substrate (100) such that patterns are separated from one another by a space, in direction parallel to main surface of substrate; forming capping films (130) formed of first material having first solubility in a solvent on sidewalls and top surface of patterns; forming second mask layer (140) formed of second material having second solubility which is less than first, so as to fill space located between patterns; and forming second mask patterns corresponding to residual portions of second layer.

USE - For forming fine patterns of a semiconductor device (claimed) used in the manufacturing of highly integrated semiconductor devices.

ADVANTAGE - The method repeatedly forms fine patterns at intervals of a fine pitch by using a double patterning process, thereby overcoming a resolution limit of existing exposure equipment. The method forms fine patterns of semiconductor device without using expensive deposition equipment. The method forms fine patterns of a semiconductor device using a double patterning process, by which etch mask patterns are formed with a doubled density within a predetermined area by using a chemical reaction without using expensive deposition equipment. The manufacturing method is simple and cost-effective.

25. 专利号：CN102656515B

专利名称：Method for processing image data in lithography manufacturing process, involves performing multiple exposures to image objects in area of substrate by controlling several SLM to write several partitioned mask data pattern in parallel

专利发明人：LAIDIG T

专利权人：PINEBROOK IMAGING SYSTEMS CORP; PINEBROOK IMAGING TECHNOLOGY LTD

申请日：2009-12-14

摘要：NOVELTY - The method involves processing a mask data pattern to form several partitioned mask data patterns corresponding to different areas of a substrate. One or more image

objects (3301,3303) are identified in an area of substrate to be imaged by corresponding spatial light modulator (SLM). A parallel imaging writer system is configured to image objects using evaluations points which are selected along edges of objects. Multiple exposures are performed to image objects in area of substrate by controlling several SLM to write several partitioned mask data patterns in parallel.

USE - Method for processing image data in lithography manufacturing process of integrated circuit (IC), computer generated hologram (CGH), printed circuit board (PCB) and for large imaging display application such as flat panel displays. Can also be used in manufacturing of active matrix liquid crystal display (AMLCD) TV and computer monitor displays.

ADVANTAGE - The lithography manufacturing process is performed without using mask, so that the mask cost and associated issues are eliminated. The exposure tools are enabled for mask-less exposure that exceeds the throughput requirements. The improved process window ensures better lithography yield. The accumulation and use of the exposure dosages from each exposure provides a feedback mechanism to allow the imaging writer system to adaptively adjust imaging profile at the boundaries of the object being imaged and at the same time ensures that the total target exposure dosage is maintained. The creation of the stitching path allows to create an image with reduced amount of artifacts. The compact SLM imaging units can be optimized locally for better illumination and focus corresponding to its own exposure area, so that a better process window is ensured in each exposure area of the SLM imaging unit. The entire process window is improved globally using optimized contributions from the SLM imaging units. In order to achieve the intended alignment accuracy and precision for the array parallel imaging system, the method decomposes the alignment scheme into several accuracy precision levels in cascade. The desired accuracy precision level is achieved.

26. 专利号：CN102656514B

专利名称：Method for processing image data in lithography manufacturing process, involves performing multiple exposures to image objects in area of substrate by controlling several SLM to write several partitioned mask data pattern in parallel

专利发明人：LAIDIG T

专利权人：APPLIED MATERIALS INC; PINEBROOK IMAGING SYSTEMS CORP; PINEBROOK IMAGING TECHNOLOGY LTD

申请日：2009-12-14

摘要：NOVELTY - The method involves providing a parallel imaging writer system with several spatial light modulator (SLM) imaging units. A mask data pattern to be written to a substrate is received and is processed to form several partitioned mask data patterns corresponding to different areas of substrate. One or more objects (3301,3303) are identified in an area of substrate to be imaged by corresponding SLM. Multiple exposures are performed to image objects in area of substrate by controlling several SLM to write several partitioned mask data patterns in parallel.

USE - Method for processing image data in lithography manufacturing process of integrated circuit (IC), computer generated hologram (CGH), printed circuit board (PCB) and for large imaging display application such as flat panel displays. Can also be used in manufacturing of active matrix liquid crystal display (AMLCD) TV and computer monitor displays.

ADVANTAGE - The lithography manufacturing process can be performed without using mask, so that the mask cost and associated issues of concern are eliminated. The exposure tools are enabled for mask-less exposure that exceeds the throughput requirements. The improved process window, ensures better lithography yield. Moreover, the accumulation and use of the exposure dosages from each exposure provides a feedback mechanism to allow the imaging writer system to adaptively adjust imaging profile at the boundaries of the object being imaged and at the same time ensures that the total target exposure dosage is maintained. The creation of the stitching path allows to create an image with reduced amount of artifacts. The compact SLM imaging units can be optimized locally for better illumination and focus corresponding to its own exposure area, so that a better process window is ensured in each exposure area of the SLM imaging unit. The entire process window is improved globally using optimized contributions from the SLM imaging units. In order to achieve the intended alignment accuracy and precision for the array parallel imaging system, the method decomposes the alignment scheme into several accuracy precision levels in cascade. The desired accuracy precision level is achieved.

27. 专利号：TWI416263B

专利名称：Double pattern forming process comprises coating first positive resist composition onto substrate, exposing resist film to radiation, rendering first positive resist pattern and coating second resist composition on first resist pattern

专利发明人：HATAKEYAMA; HATAKEYAMA J; KANAO G; KINSHO T; NISHI T; OHASHI M; TAKEMURA K

专利权人：SHINETSU CHEM CO LTD; SHINETSU CHEM IND CO LTD

申请日：2008-09-05

摘要：NOVELTY - Double pattern forming process comprises: coating a first chemically amplified positive resist composition onto a processable substrate; exposing the first resist film to high-energy radiation; rendering the first positive resist pattern to be applied upon subsequent patterning of the second resist composition; and coating a second chemically amplified resist composition on the first resist pattern, prebaking the second resist composition to remove the unnecessary solvent and form a second resist film, and exposing the second resist film to high energy radiation in a second pattern.

USE - The process is useful for forming a first positive resist pattern and a second resist pattern. The double pattern is useful as a bilayer resist and a mask.

ADVANTAGE - The process, combined with the immersion lithography, is able to process a finer size pattern in a simple manner. The double pattern forming process is simple process

management without complex steps as the technology of processing patterns to very fine rules as required in the manufacture of latent semantic indexing featuring higher integration and faster operation.

28. 专利号：US9070448B2

专利名称：Method for pattern formation in e.g. NOT-AND (NAND) flash memory element, involves etching substrate regions, simultaneously, using spacers that cover sidewalls of mask pattern formed in substrate regions as etching mask

专利发明人：KIM B; KIM B S; KIM D; KIM D C; KIM M; KIM M C; KIM P; KIM P S; KIM T; KIM T C; KIN M; KWON O; KWON O I; MIN J; MIN J H

专利权人：SAMSUNG ELECTRONICS CO LTD; KIM B; KIM D; KIM M; KWON O; MIN J

申请日：2008-08-11

摘 要：NOVELTY - The method involves forming spacers (350A,350B) for covering sidewalls of respective mask patterns (320A,320B) formed in respective regions (A,B) of substrate (300), simultaneously. The mask pattern (320A) formed in substrate region (A) is removed. The substrate regions (A,B) are then etched using respective spacers (350A,350B) as etching mask, simultaneously.

USE - Method for pattern formation in semiconductor element (claimed) such as NOT-AND (NAND) flash memory element.

ADVANTAGE - Patterns of various widths can be formed easily using the double patterning process at reduced cost and productivity can be improved.

29. 专利号：US7915171B2

专利名称：Double-patterning method for forming integrated circuit structure of e.g. transistor region in electronic device, involves forming pattern in photoresist, where pattern has structures that are close to trench structures of another pattern

专利发明人：SIVAKUMAR S; TINGEY M; WALLACE C H

专利权人：INTEL CORP; SIVAKUMAR S; TINGEY M; WALLACE C H

申请日：2008-04-29

摘 要：NOVELTY - The method involves depositing a photoresist (206) e.g. positive photoresist, to a semiconductor substrate (204), and forming an integrated circuit (IC) pattern (208-1) in the photoresist. The pattern is protected from actions that form another IC pattern (208-2) in another photoresist (215). The latter photoresist is deposited to the former pattern. The latter pattern is formed in the latter photoresist, where the latter pattern has structures that are close to trench structures (212-1-212-n) of the former pattern to cause scumming of the latter photoresist in the trench structures.

USE - Double-patterning method for forming an integrated circuit (IC) structure of a transistor

region and an interconnect region in an electronic device.

ADVANTAGE - The pattern is formed in the photoresist, where the pattern has the structures that are close to the trench structures of another pattern to cause scumming of the photoresist in the trench structures, thus exploiting the contrast and dissolution properties of common photoresists to increase the resolution capabilities of current patterning equipment used to form the patterns.

30. 专利号：US8082524B2

专利名称：Computer-implemented mask patterns determining method for manufacturing e.g. semiconductor wafer, involves utilizing photo-masks to print one wafer pattern corresponding to target pattern during multiple-exposure photolithographic process

专利发明人：GLEASON R P; LIN T; MOORE A J; OLSON B W; RISSMAN P

专利权人：GLEASON R P; LIN T; LUMINESCENT TECHNOLOGIES INC; MOORE A J; OLSON B W; RISSMAN P

申请日：2008-04-15

摘要：NOVELTY - The method involves arranging an initial photo-mask corresponding to an initial mask pattern to print a wafer pattern corresponding to a target pattern during a single-exposure photolithographic process. Two mask patterns are determined based on the initial mask and target patterns, where the patterns include features, which are overlapped together proximate to a critical region in the initial mask pattern. The photo-masks are utilized to print another wafer pattern during multiple-exposure photolithographic process.

USE - Computer-implemented method for determining mask patterns to be used on photo-masks in a multiple-exposure photolithographic process for manufacturing a semiconductor wafer and an integrated circuit. Can also be used for manufacturing a micro-electro-mechanical system and nanoelectro-mechanical system.

ADVANTAGE - The method decomposes the initial mask pattern to facilitate lithographic processes with increased resolution or decreased critical dimension for specific wavelength of light and optical path and improved process control, thus increasing manufacturing yield of the semiconductor-wafer and reducing cost of the semiconductor- wafer.

31. 专利号：US7713818B2

专利名称：Preparing semiconductor device e.g. diode involves forming first photoresist layer on underlying layer followed by patterning and rendering the pattern insoluble to solvent; patterning second photoresist layer; and etching underlying layer

专利发明人：CHAN M

专利权人：SANDISK 3D LLC

申请日：2008-04-11

摘要：NOVELTY - Preparation of semiconductor device involves forming a first photoresist layer over an underlying layer; patterning the first photoresist layer to form a first photoresist pattern

(111); rendering the first photoresist pattern insoluble to a solvent; forming a second photoresist layer over the first photoresist pattern; patterning the second photoresist layer to form a second photoresist pattern (211) over the device layer; and etching the underlying layer using both the first and the second photoresist patterns as a mask.

USE - For preparing semiconductor device (claimed) e.g. diode containing nonvolatile memory array.

ADVANTAGE - The bottom anti-refection coating layer has a thickness of 15-30 nm which improves the performance of the photoresist by forming a sharper resist contrast after double patterning.

32. 专利号：TWI427428B

专利名称：Forming pattern, comprises applying positive resist composition on substrate, heat treating obtained resist film and exposing to radiation, heat treating exposed resist film, and then causing to crosslink and cure with heat/acid and heat

专利发明人：HATAKEYAMA; HATAKEYAMA J; KANAO G; KATAYAMA K; KINSHO T; OHASHI M

专利权人：SHINETSU CHEM CO LTD; SHINETSU CHEM IND CO LTD

申请日：2008-03-05

摘要：NOVELTY - Process for forming a pattern, comprises: applying a positive resist composition onto a substrate to form a resist film; heat treating the resist film and exposing it to high-energy radiation; heat treating the exposed resist film and developing it with a developer; and then causing the resist film to crosslink and cure with the aid of heat or of acid and heat, where the resist composition comprises a polymer comprising recurring units derived from optionally substituted hydroxyalkylnaphthalene and recurring units which become alkali soluble under the action of an acid.

USE - The process is useful for forming a pattern.

ADVANTAGE - The process: provides half-pitch fine-feature pattern through double exposures and a single dry etching; and reduces the pitch between patterns to one half.

33. 专利号：US8208121B2

专利名称：Alignment mark for use in optical lithography, has pair of areas overlapping on each other and comprising set of periodic structures formed by mark lines extending in set of directions, where directions are formed at pair of angles

专利发明人：BIJNEN F G C; TENNER M G; VAN K M; VAN KEMENADE M; WARNAAR P

专利权人：ASML NETHERLANDS BV

申请日：2008-02-01

摘要：NOVELTY - The mark (AM) has a pair of areas overlapping on each other and

comprising a set of periodic structures formed by mark lines (ML) extending in a set of directions, where the directions are formed at a pair of angles (alpha, beta) with respect to a scribe lane direction, which is parallel or perpendicular to a scanning direction, and a range of one of the angels is 0 degree to 90 degrees and other angle is from minus 90 to zero degree. The mark lines are formed by multiple sub-segment lines extending parallel or perpendicular to the scribe lane direction.

USE - Alignment mark for being formed in a scribe lane of a substrate (claimed), in optical lithography during manufacturing of an integrated circuit. Can also be used in imprint lithography.

ADVANTAGE - The mark enables better reproduction of alignment on the substrate to allow better overlay for double patterning and exposure.

政策计划

“十三五”国家科技创新新规划

“十三五”国家科技创新规划，依据《中华人民共和国国民经济和社会发展第十三个五年规划纲要》、《国家创新驱动发展战略纲要》和《国家中长期科学和技术发展规划纲要（2006—2020 年）》编制，主要明确“十三五”时期科技创新的总体思路、发展目标、主要任务和重大举措，是国家在科技创新领域的重点专项规划，是我国迈进创新型国家行列的行动指南。

8 月 8 日，国务院正式印发《“十三五”国家科技创新规划》（下称“规划”）。该规划是国务院确定的 22 个国家重点专项规划之一，对我国未来 5 年科技创新做了系统谋划和前瞻布局，是国家“十三五”规划纲要和《国家创新驱动发展战略纲要》的细化落实。

规划共分 8 篇 27 章，从创新主体、创新基地、创新空间、创新网络、创新治理、创新生态六个方面提出建设国家创新体系的要求，并从构筑国家先发优势、增强原始创新能力、拓展创新发展空间、推进大众创业万众创新、全面深化科技体制改革、加强科普和创新文化建设等六个方面进行了系统部署。

跟着权威人士画重点，《“十三五”国家科技创新规划》的全景图解版，希望能帮助大家更全面、直观地了解规划全文。


发展目标
{总目标：迈进创新型国家行列}
自主创新能力全面提升
科技创新支撑引领作用显著增强
创新创业生态更加优化
有利于创新的体制机制更加成熟定型
创新型人才规模质量同步提升
指标
2015年指标值
2016年目标值
国家综合创新能力世界排名（位） 18 15
科技进步贡献率（%） 55.3 60
研究与试验发展经费投入强度（%） 2.1 2.5
每万名就业人员中研发人员（人年） 48.5 60
高新技术企业营业收入（万亿元） 22.2 34
全国技术合同成交金额（亿元） 9835 20000


总体部署
1 围绕构筑国家先发优势，加强兼顾当前和长远的重大战略布局。
2 围绕增强原始创新能力，培育重要战略创新力量。
3 围绕拓展创新发展空间，统筹国内国际两个大局。
4 围绕推进大众创业万众创新，构建良好创新创业生态。
5 围绕破除束缚创新和成果转化的制度障碍，全面深化科技体制改革。
6 围绕夯实创新的群众和社会基础，加强科普和创新文化建设。
重大科技项目和重大专项远近结合梯次接续
国家科技重大专项
核心电子器件 高端通用芯片 基础软件产品
极大规模集成电路制造装备及成套工艺
新一代无线宽带移动通信网
电子信息领域
科技创新2030重大项目
量子通信和量子计算机
国家网络空间安全
天地一体化信息网络
大数据


高档数控机床和基础制造装备
大型飞机
先进制造领域
航空发动机及燃气轮机
智能制造和机器人
重点新材料研发及应用
大型油田及煤层气开发
水体污染的控制与治理
大型先进压水堆和高温气冷堆核电站
能源环境领域
智能电网
煤炭清洁高效利用
京津冀环境综合治理
转基因生物新品种培育
农业领域
种业自主创新
重大新药创制
艾滋病和病毒性肝炎等重大传染病防治
生物健康领域
健康保障
脑科学与类脑研究


高分辨率对地观测系统
载人航天与探月工程
太空海洋开发利用领域
深海空间站
深空探测及空间飞行器在轨服务与维护系统
十大现代产业技术
高效安全生态的现代农业技术
新一代信息技术
智能绿色服务制造技术
新材料技术
清洁高效能源技术
现代交通技术与装备
先进高效生物技术
现代食品制造技术
支撑商业模式创新的现代服务技术
引领产业变革的颠覆性技术

滕飞 选摘自
http://www.scio.gov.cn/32344/32345/33969/34872/xgzc34878/Document/1486317/1486317_1.htm

中共中央办公厅 国务院办公厅印发《国家信息化发展战略纲要》

当今世界，信息技术创新日新月异，以数字化、网络化、智能化为特征的信息化浪潮蓬勃兴起。没有信息化就没有现代化，适应和引领经济发展新常态，增强发展新动力，需要将信息化贯穿我国现代化进程始终，加快释放信息化发展的巨大潜能。以信息化驱动现代化，建设网络强国，是落实“四个全面”战略布局的重要举措，是实现“两个一百年”奋斗目标和中华民族伟大复兴中国梦的必然选择。

2016 年 7 月 27 号，国务院办公室根据新形势对《2006－2020 年国家信息化发展战略》进行调整和发展，它是规范和指导未来 10 年国家信息化发展的纲

领性文件，是国家战略体系的重要组成部分，是信息化领域规划、政策制定的重要依据。

该发展战略从国家信息化发展的基本形势；指导思想、战略目标和基本方针；大力增强信息化发展能力；着力提升经济社会信息化水平；不断优化信息化发展环境；体制保障和组织实施六大方面进行阐述，其中在大力增强信息化发展能力方面要发展核心技术，做强信息产业。其具体规划如下所述。

信息技术和产业发展程度决定着信息化发展水平。我国正处于从跟跑并跑向并跑领跑转变的关键时期，要抓住自主创新的牛鼻子，构建安全可控的信息技术体系，培育形成具有国际竞争力的产业生态，把发展主动权牢牢掌握在自己手里。

1． 构建先进技术体系。制定国家信息领域核心技术设备发展战略纲要，以体系化思维弥补单点弱势，打造国际先进、安全可控的核心技术体系，带动集成电路、基础软件、核心元器件等薄弱环节实现根本性突破。积极争取并巩固新一代移动通信、下一代互联网等领域全球领先地位，着力构筑移动互联网、云计算、大数据、物联网 等领域比较优势。

2． 加强前沿和基础研究。加快完善基础研究体制机制，强化企业创新主体地位和主导作用，面向信息通信技术领域的基础前沿技术、共性关键技术，加大科技攻关。遵循创新规律，着眼长远发展，超前规划布局，加大投资保障力度，为前沿探索提供长期支持。实施新一代信息技术创新国际交流项目。

3．打造协同发展的产业生态。统筹基础研究、技术创新、产业发展与应用部署，加强产业链各环节协调互动。提高产品服务附加值，加速产业向价值链高端迁移。加强专利与标准前瞻性布局，完善覆盖知识产权、技术标准、成果转化、测试验证和产业化投资评估等环节的公共服务体系。

4． 培育壮大龙头企业。支持龙头企业发挥引领带动作用，联合高校和科研机构打造研发中心、技术产业联盟，探索成立核心技术研发投资公司，打通技术产业化的高效转化通道。深化上市发审制度改革，支持创新型企业在国内上市。支持企业在海外设立研发机构和开拓市场，有效利用全球资源，提升国

际化发展水平。

5．支持中小微企业创新。加大对科技型创新企业研发支持力度，落实企业研发费用加计扣除政策，适当扩大政策适用范围。完善技术交易和企业孵化机制，构建普惠性创新支持政策体系。完善公共服务平台，提高科技型中小微企业自主创新和可持续发展能力。

滕飞 选摘自

http://www.miit.gov.cn/n1146290/n1146392/c5168620/content.html

国际半导体科技蓝图未来将不再推出

近 20 年的国际半导体科技蓝图(International Technology Roadmap for Semiconductors；ITRS)在 2016 年 7 月份将停止发布，最新的报告也截止到 2015 年 7 月，且代表英特尔、IBM 等业者利益的贸易团体美国半导体产业协会(Semiconductor Industry Association；SEA)，也将脱离 ITRS 赞助参与圈，未来将与半导体研究公司(Semiconductor Research Corporation；SEC)合作，为政府确定研究的优先顺序以及产业资助的计划。至于其他 ITRS 参与业者，未来仍将持续发布新的蓝图报告，只不过将不再以 ITRS 名义发布，将改以新名称发布。

根据 2015 年的这份蓝图，显示半导体产业的电晶体(Transistor)体积缩减进程到了 2021 年将会停止，主要与 2021 年后持续缩减微处理器的电晶体体积，可能不再符合业者经济效益有关。

根据电机电子工程师学会(IEEE)指出，在 2021 年后预估电晶体体积将不再缩减下，全球主要芯片制造商将采取其他方式来提升电晶体密度，即透过将电晶体从水平几何改为垂直几何，以及打造多层电路系统等方式着手提升密度。

对于这样的改变，部分人士可能认为，这又会是另一种摩尔定律(Moore's Law)结束的丧钟。另外，虽然部分人士认为此蓝图的改变可能只是微不足道的行政作业上的改变，不过却有市场分析师认为，这样的改变是对业界形成主要的破坏，甚至可说是一场地震。

美国半导体业者在 1990 年代早期时，曾有共同合作及确认共同需求的理由，

而后于 1998 年首度推出上述的 ITRS 蓝图，不过如 VLSI Research 分析师 Dan Hutcheson 所言，供应商不易确认半导体业者的需求；对芯片业者来说，共同设立优先顺序充分运用有限的研发资金，符合其发展上的需求。

不过，在维持摩尔定律领先优势面临的困难度及成本支出下，因而导致后来产业的整合，从 2001 年仍有 19 家开发及制造具优势技术电晶体逻辑芯片的业者规模，到如今仅剩台积电、英特尔(Intel)、三星集团(Samsung Group)以及 GlobalFoundries 等 4 家业者仍存在，即可见一斑。

这 4 家业者如今各自拥有自己的产品规划蓝图，并能够直接与其设备及材料供应商沟通，而且 Hutcheson 表示，这 4 家业者彼此高度竞争，不会希望好好坐下来讨论彼此的需求为何。

滕飞 选摘自

http://www.cedachina.org/index.php?a=shows&catid=26&id=601

美国国会智库分析美国半导体制造业

2016 年 6 月底，美国国会研究服务局（CRS）发布报告《美国半导体制造：行业趋势、国际竞争与联邦政策》，阐述了美国半导体制造业的发展现状、全球竞争态势，以及政府在该行业所起的作用。

1. 美国半导体制造业的重要地位

2013 年美国国内约有 820 家公司涉足半导体或相关的设备制造行业，其对美国经济的价值贡献到 2014 年已达到 272 亿美元，约占美国制造业总产值的 1%。2015 年，总部位于美国的半导体公司的海外市场销售额为 418 亿美元（占总销售额的 83%），半导体产业已经成为美国高科技出口产业的代表。在知识产权方面，美国高通、英特尔和博通等主要半导体制造商是专利大户。根据美国劳工统计局数据，2015 年半导体及相关设备制造业的员工数量为 18.07 万人（较 2001 年下降了 38%），该行业员工数量占制造业总员工数量的 1.5%，平均工资约为 13.81 万美元，是美国制造业员工平均工资的两倍以上。

2. 全球竞争格局

到 2015 年年底，全球共有 94 家先进的晶圆制造厂商，其中 17 家在美国，71 家在亚洲（其中中国有 9 家），6 家在欧洲。日本在上世纪 80 年代处于领先地位，但自 90 年代开始其全球半导体市场份额显著下降，至 2015 年仅有 3 家日本芯片制造商位列全球排名前 20—东芝、瑞萨电子和索尼。而与此同时，东亚其他国家已成为动态随机存取存储器市场的主要公司。韩国三星电子和海士力目前是世界第二和第三大半导体公司。

3. 美国联邦政府扶植政策

2015 年，国会完善了研发税收抵免制度。同年 7 月，美国颁布行政命令设立“国家战略计算计划”，其中一个关键目标就是在未来 15 年里，在目前半导体技术受到限制的情况下，开创一条通往未来高性能计算系统的可行道路。美国联邦政府其他的支持工作还包括：半导体技术先进研究网络，安全与可靠的网络空间计划中的“安全、可信、保障和弹性的半导体系统”项目，2020 及未来纳米电子器件发展计划，以及节能计算：从设备到架构计划。

滕飞 选摘自

http://www.clas.ac.cn/xwzx2016/kxxw2016/xxjsdt2016/201607/t20160723_4644703.html

前沿研究

考虑复杂着色规则的多图案布局分解

对于提高常规光学光刻术分辨率极限来说，多重图形化光刻是除了超紫外线光刻技术、直接自组装、纳米压印光刻、电子束光刻之外，被公认为的最有前途的解决方案之一。多图案布局分解（MPLD）因为复杂着色规则的引入变为了更具挑战性的先进技术。现有的工程模型把 MPLD 看作一个图形着色问题，尽管如此，当考虑到复杂的着色规则时，布局分解不再能由图形着色准确地建模。因此，研究人员通过捕捉复杂着色规则的布局分解精髓，把 MPLD 问题作为一个精确覆盖问题建模。然后，研究人员基于增强舞蹈链提出了一个快速、准确的 MPLD 框架。研究人员的方法是灵活、一般的：它可以同时考虑基本和复杂的着色规则，并且它可以处理四倍及以上的图案。实验结果表明，该方法优于已报道的其他方法，并有望用于处理复杂的着色规则。

研究成果发表于 Design Automation Conference (DAC), 2016 53nd ACM/EDAC/IEEE（5-9 June 2016）。

张迪 摘译自

http://ieeexplore.ieee.org/document/7544283/

原文标题

Multiple patterning layout decomposition considering complex coloring rules

14nm 节点多图案光刻技术的有效解决方案

当我们在向更先进的技术节点努力的时候，多图案光刻（MPL）有助于实现缩小的目标，但仍然会因为 14nm 尺度逻辑设计的多尺寸和取向等性能使光刻遇到大的挑战。通过对源掩模优化（SMO）的点中心位移问题进行分析和解决，重叠工艺窗口（PW）得到了扩大。研究人员根据模拟结果，调谐分解规则，以提高打印的图像性能。同时，研究人员研究了插入针的影响以及 DPL 和 TPL 之间的比较。结果表明，不同的方法面临着不同的图案时，都有自己的优点和缺点。

研究成果发表于 Semiconductor Technology International Conference (CSTIC), 2016 China （13-14 March 2016） 。

张迪 摘译自

http://ieeexplore.ieee.org/document/7463989/

原文标题

Effective solution for the 14nm node multiple patterning lithography

自对准双倍和四倍图案感知网格进程方法

虽然自对准双倍和四倍图案（SADP，SAQP）对亚 20 纳米及更高的节点先进技术来说，拥有理想的过程，然而不是所有的布局都与其兼容。在先进技术中，可以通过利用晶圆图案被选择的心轴模式确定的 SADP 和 SAQP 来有效产生可行晶圆图案。然而，预测心轴图案是不容易的，因为它与晶片图案（或目标图案）是不同的。研究人员于是提出了一种新的进程方法，间隔是电介质（spacer-is-dielectric，SID）型的 SADP 和 SAQP，以及间隔是金属（spacer-is-metal，SIM）型 SADP，来生成满足连接要求一个可行的布局。进程算法包括简单的连接和切割规则，执行在新的网格结构上，其中两个（SID 型 SADP）或三种颜色（SID 型 SAQP 和 SIM 型 SADP）交替分配在网格节点上。然后，无需复杂的着色或分解的方法，心轴图案就可以被选择。此外，研究人员试图通过 SID 型 SADP 的伪图案翻转来减少热点（可能存在缺陷的区域）。实验结果表明，满足连接需求的可行布局可以产生，有效性也被确认。

研究成果发表于 IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (Volume: 34, Issue: 5, May 2015) Page(s): 753 - 765 （19 February 2015）。

张迪 摘译自

http://ieeexplore.ieee.org/document/7045535/

原文标题

Self-Aligned Double and Quadruple Patterning Aware Grid Routing Methods

利用多图案等离激元纳米结构提升有机光电器件的性能

多图案的纳米结构可以通过协同嵌段共聚物光刻和纳米压印光刻组合制备，该结构也已被用作反向反射器，从而增强有机光电子器件的光吸收性能。多图案化的电极可以显著提升有机光伏和光电晶体管的性能，这些归因于高效光散射性能和等离子体效应，从而延长了它们的实际应用范围。

相关研究发表在 ADVANCED MATERIALS 卷: 28 期: 25 页: 4976-4982 出版年: JUL 6 2016 。

张迪 摘译自

http://apps.webofknowledge.com/full_record.do?product=WOS&search_mode=GeneralSearch&qid=1&SID=N28H5hDNLnkq8Gw9VS4&page=1&doc=1

原文标题

Boosting the Performance of Organic Optoelectronic Devices Using Multiple-Patterned Plasmonic Nanostructures

多图案光刻标准单元 middle-of-line 稳健性评价的系统架构

对于坚稳标准单元设计，设计人员需要改善单元和单元展示位置之间的兼容性。多图案光刻着色检查打破了传统规则检查的局部性，为了验证跨单元边界布局相互作用的着色效果，N-wise 的检查是强烈需要的。研究人员提出了一个系统的框架，从两个角度评价多图案光刻的库级稳健性，包括两排组合单元的完整检查和长程相互作用评估。对于两排组合单元的完整检查来说，在垂直和水平边界检查探索预测了非法单元组合。对于长程相互作用，研究人员对单元位移产生的随机基准进行了测试，从而评估对制备 middle-of-line (MOL)层来说，从四倍图案光刻制造降低到三倍图形光刻制造的复杂性。研究人员从框架上对 MOL 层进行测试，但也容易地适用于多图案光刻的其他重要的层。

相关研究发表于 JOURNAL OF MICRO-NANOLITHOGRAPHY MEMS AND MOEMS 卷: 15 期: 2 出版年: APR 2016 。

张迪 摘译自

http://apps.webofknowledge.com/full_record.do?product=WOS&search_mode=GeneralSearch&qid=1&SID=N28H5hDNLnkq8Gw9VS4&page=1&doc=4

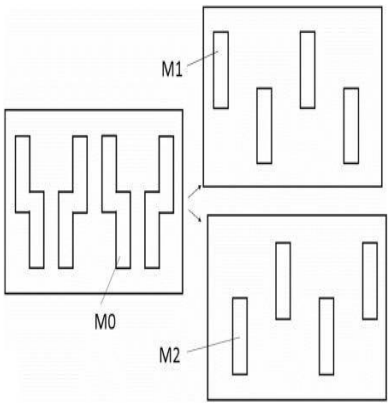
原文标题

Systematic framework for evaluating standard cell robustness for multiple patterning lithography

应用实施

基于多重曝光的图形制作方法

上海华力微电子有限公司发明了一种基于多重曝光的图形制作方法，它包括：将期望形成的密集初始图形分割成较为第一图形和第二图形，在掩模板上的不同区域分别形成第一图形和第二图形；在衬底硅片上沉积硅薄膜，然后涂敷光刻胶层，对光刻胶层进行加热固胶；以第一照明条件对光刻胶层执行第一次曝光，曝光图形为第一图形；以第二照明条件对光刻胶层执行第二次曝光，曝光图形为第二图形，使得第一图形与第二图形在光刻胶层上同时存在以组成密集初始图形；将晶圆转运入自动化光阻涂布及显影系统进行曝光后烘焙，两次曝光作业中被光照的光刻胶部分发生光酸反应；将晶圆执行显影，从而光刻胶保留部分形成密集初始图形；将晶圆执行蚀刻，从而在硅薄膜上形成了密集初始图形。



滕飞 选摘自
http://www.pss-system.gov.cn/sipopublicsearch/patentsearch/searchHomeIndex-searchHomeIndex.shtml

32nm 螺距的抗蚀剂中集成应用间隔节距分裂的自对准四重图形化技术

193nm 光刻间距分辨率的多图案技术集成在追求降低成本和实现所需关键尺寸时变得越来越有创意。实施这些计划到生产可以是一个挑战。为了降低

10nm 节点及之下多重图形化的技术成本，提出自对准四重图形化的策略。其采用 193nm 沉浸式光刻胶图案作为第一芯轴和间隔件的组合实现 30nm 的螺距。此选项可以实现前端或后端关键层如 FIN 和 M_X。通过对低温的 ALD 薄膜如 TiO 的调查，Al_2O_3 和 SiO_2 满足其 LER/LWR 和 CDs 等需求，将作为最佳的候选材料。

使用间隔节距分裂的自对准四重图形化技术面临着挑战，如第一个间隔件的形状影响第二间隔的沉积剖面和最终的蚀刻配置文件，以及间距行走控制。在文章中，作者总结优化模式、蚀刻化学、工艺步骤，以及其他传统的多图形化技术提供一个可行的替代方案。将新的方案与先前的方案进行比较，依据 LER / LWR 性能， CDs 目标，蚀刻轮廓和成本效益判断 SAQP 流程的优缺点。

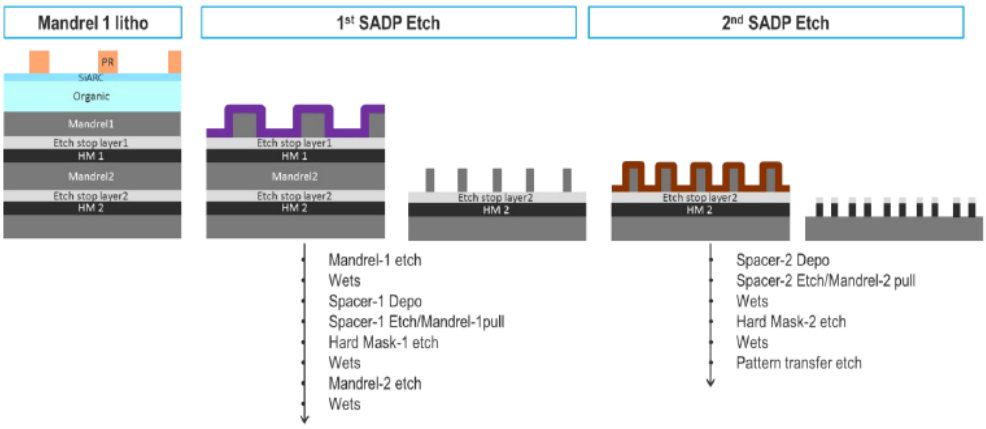


图 1 标准 SAQP 层和步骤

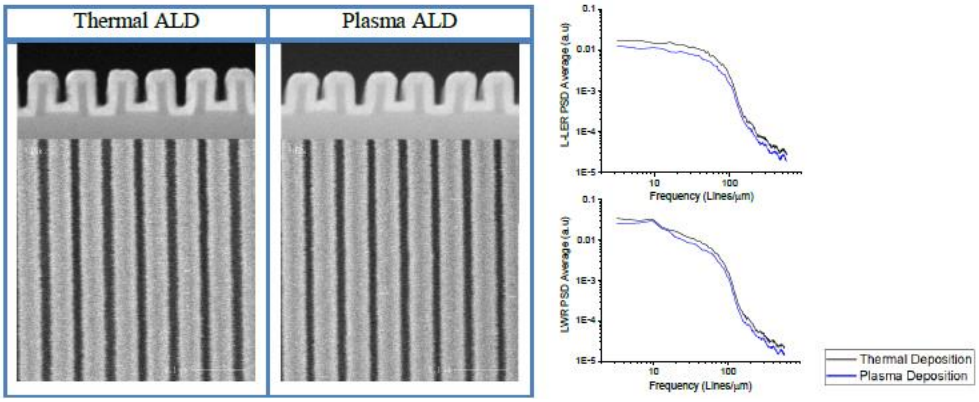


图 2 TiO 沉积法比较--横截面、自上而下和 PSD 粗糙度

滕飞 编译自

Proc. SPIE 9782, Advanced Etch Technology for Nanopatterning V, 97820F (April 1, 2016);

doi:10.1117/12.2219321

原文标题

Self-aligned quadruple patterning integration using spacer on spacer pitch splitting at the resist level for sub-32nm pitch applications

多重图形技术中应用 CD 偏差控制孔形状

网格设计规则是 193nm 沉浸式光刻胶图案过程配置逻辑电路的主要过程。在网格图形的规模中，用多图形化技术（如自对准多个图形模式（SAMP）和光刻刻蚀（LELE））制作 10nm 的订单线与空间模式。另一方面，线切割过程中有一些误差参数，如模式缺陷、位置误差、表面粗糙度和 X-Y CD 偏差等，特别是表面粗糙度和 X-Y CD 的偏差能够减少错误和缺陷的出现。在这种情况下，采用一些平滑处理孔的粗糙度，每一个平滑过程显示 X-Y CD 偏差的效果。将多图形化模式下的沟槽和可逆块进行可控性比较，包括 X-Y CD 偏差、粗糙度和加工工艺性。此外，还讨论了针对 X-Y CD 偏差的最佳方法。

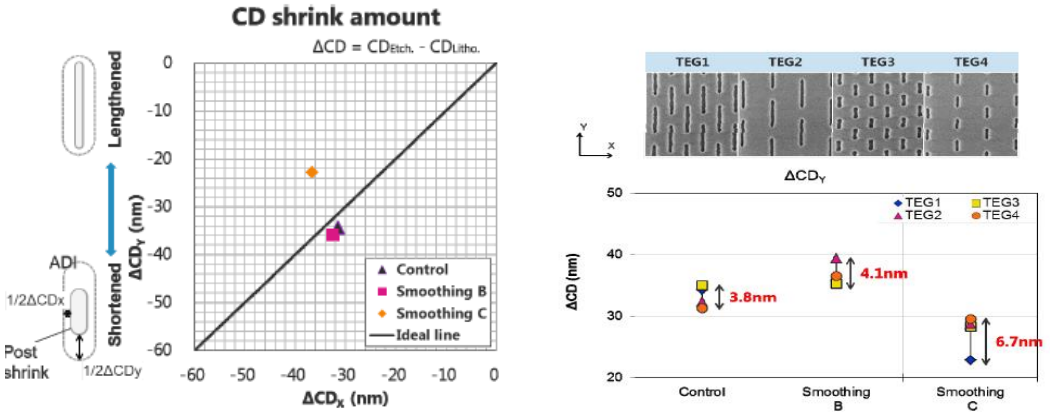


图 3 X-Y CD 偏差

滕飞 编译自

Proc. SPIE. 9779, Advances in Patterning Materials and Processes XXXIII, 97790V. (March 25, 2016) doi: 10.1117/12.2218961

原文标题

CD bias control on hole pattern

多重图形化中应用 10 nm 和 7nm 节点的整体覆盖控制技术

多图形光刻技术在 10 nm 和 7nm 节点驱动下允许覆盖误差降到极低值，但是需要先进的高阶覆盖校正方案来控制过程的变化。

分裂层数目的增加导致总的覆盖和对齐树的计量复杂度指数增加。同时，该过程包括更多的硬掩模步骤，覆盖计量配方的设置和验证变得更加关键。上述过程解决了总覆盖优化设计过程中的设置和控制量的制造，解决方案空间将会急剧增加，以满足对产品的覆盖目标。

在解决方案中空间的增加可以看出，在扫描仪仅覆盖控制上每个晶片每个字段可以有 20 个不同的参数。在计量选择时必须对目标设计，目标选择，测量配方进行设置，但面临的一个重大问题是：在这个巨大的解决方案空间，每层有成千上万个可能的设置，如何找到最佳组合？哪些计量目标可以捕获所有的相关信息？需要什么样的采样计划，准确地捕捉到一个扭曲晶片的形状？图 4 和图 5 分别为 10 nm 和 7nm 节点提出整体覆盖控制流设计和修正两步法，指出可达到最终覆盖性能逻辑和内存使用情况。

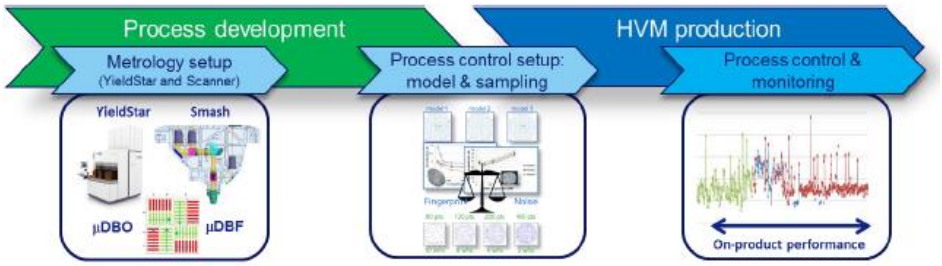


图 4 整体覆盖的设计、开发和产品的过程

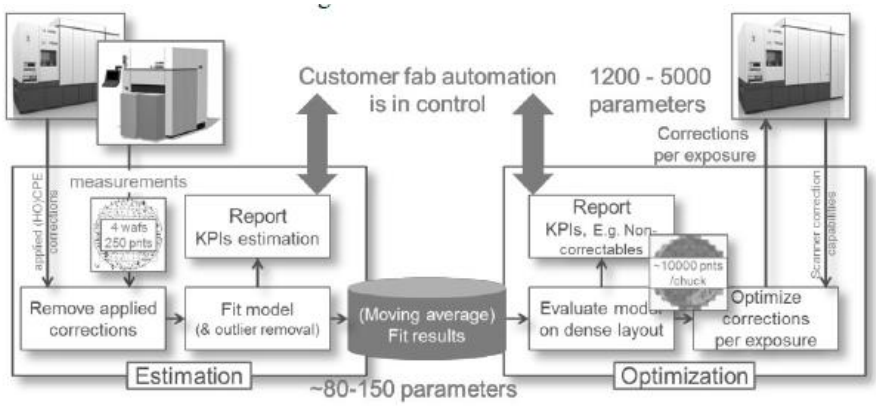


图 5 最佳 OV 修正两步法

滕飞 编译自

Proc. SPIE. 9778, Metrology, Inspection, and Process Control for Microlithography XXX,

97781Y. (March 25, 2016) doi: 10.1117/12.2230390

原文标题

Holistic Overlay Control for Multi-Patterning Process layers at the 10-nm and 7-nm nodes

《集微技术信息简报》

《集微技术信息简报》是由中国科学院文献情报中心学科咨询服务部承担编辑的集成电路、微电子相关领域科技信息综合报道及专题分析简报（双月报），于2014年3月正式启动，2014年为季度发行的《光刻技术信息简报》，2015年3月改版为《集微技术信息简报》双月发行（2015年12月起改为双月月底发布）。按照“统筹规划、系统布局、分工负责、整体集成、长期积累、深度分析、协同服务、支撑科研”的发展思路，规划和部署《集微技术信息简报》。《集微技术信息简报》服务对象，一是“02专项”的相关领导、科技战略研究专家和科研一线工作者；二是集成电路、微电子领域科技战略研究专家和科研一线工作者。《集微技术信息简报》内容力图兼顾科技决策和管理者、科技战略专家和领域科学家的信息需求，报道集成电路、微电子领域的国际科技战略与规划、科技计划与预算、科技进展与动态、科技前沿与热点、重大科技研发与应用、重要科技政策与管理等方面的最新进展与发展动态，每期提供一个集成电路、微电子领域热点方向的专题分析。《集微技术信息简报》是内部资料，不公开出版发行；除了其所报道的专题分析报告代表相应作者的观点外，其所刊载报道的中文翻译信息并不代表译者及其所在单位的观点。

更多及时信息请关注集成电路研发竞争情报公众服务号！

扫一扫关注我们

主编：吴鸣（中国科学院文献情报中心学科咨询部主任）

常务副主编：王丽（中国科学院文献情报中心学科咨询部学科馆员）

编辑部：中国科学院文献情报中心学科咨询部

编辑： 赵慧敏 张迪 腾飞

电话：010—82629002

本期责任编辑：王丽

承办单位：中国科学院文献情报中心

联系地址：北京市海淀区北四环西路 33 号（100190）

网址：www.las.ac.cn

联系人：王丽

电话：010-82629002，010-82626611-6168

电子邮件：wangli@mail.las.ac.cn