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研究背景

光刻技术是半导体及相关产业发展和进步的关键技术，传统的光刻技术有紫外光刻、电子束光刻等。在过去的几十年中，传统光刻技术一方面发挥了重大作用；另一方面，这些传统技术存在不同的缺点，如结构复杂，依赖于光学系统进行成像，分辨率受限于衍射极限等。随着传统光刻技术在应用中问题的增多、用户对应用本身需求的提高，寻找解决技术障碍的新方案、找到下一代可行的技术路径，去支持产业的进步显得非常紧迫，各国将大量的研究和开发资金投入到这场技术竞赛中。极紫外光刻技术、DSA（定向自组装光刻）技术、无掩模光刻技术、原子光刻技术、电子束光刻技术等技术作为解决方案进入下一代光刻技术角逐场。

DSA（Directed Self-assembling 嵌段共聚物自组装）技术是近年发展起来的一种自下而上构造纳米结构新方法。嵌段共聚物(BlockCopolymers)，是由不同结构单元组成的均聚链段，通过共价键相互结合成主链的共聚物。不同的均聚链段可以为两种或两种以上，每链段只含一种结构单元，各链段的长短没有严格的限制。因为嵌段共聚物由热力学上互不相容的链段通过化学键连接而成，这种结构特点导致嵌段共聚物不具有共混物的宏观相分离行为，只能发生微观相分离，在介观尺度上形成丰富多彩的有序相形态。这些微观有序相形态具有良好的可调控性及相对容易的制备方法，通过改变嵌段共聚物的组成、链长、施加外场或改变制备方法等可以使嵌段共聚物通过自组装产生各种高度有序的介观图案。DSA 工艺开始于在晶圆上先形成一个“尺寸宽松”的引导结构图形，然后根据嵌段共聚物中聚合物的长度，来将引导结构中的间隔复制成为多条线段和间隔。聚合物顶部层具有硬质掩膜的特性，具有足够的抵抗力和承受能力。

DSA 技术一直以来多在实验室发展，如今逐渐受到重视，被认为是纳米级制造中最有希望的高产出效益方法。这得益于嵌段共聚高分子自组装(Block

Copolymer Self-assembly)具有的高度结构规则性、可操控性及材料变化性。

DSA 在 2007 年首次以关键层光刻领先技术之潜力解决方案的角色出现在国际半导体技术蓝图(ITRS)，该技术被认为能作为下一代光刻候选技术的补充。IMEC 认为定向自组装光刻技术的开发“非常具有前景”，主要侧重于降低缺陷率。DSA 虽不能替代 EUV 等高分辨率光刻技术，但是可与其它技术结合使用。

研究内容

本研究从 DSA 技术专利入手，力求呈现当前该专利技术态势及专利活动特点。

定向自组装光刻 DSA 技术专利分析内容共包括：专利数申请时间趋势分析、技术构成分析、国家/地区分析、申请人分析等四大项专利分析模块。

数据来源

数据来源：美国汤森路透科技（Thomson Reuters Scientific）公司 ThomsonInnovation 全球专利数据库（检索日期 2016 年 4 月 29 日），分析过程中采用了该公司的 TDA（Thomson Data Analyzer）分析工具。

1 专利申请时间趋势

1.1 专利申请时间走势

截至检索日期，共检索到 DSA 技术相关的专利家族 2083 项，专利家族最早优先权年时间跨度为 1986-2015 共 30 年，考虑到专利一般从申请到公开需要长达 30 个月（12 个月优先权期限+18 个月公开期限）的时间，再考虑到数据库录入时间的延迟，近两年的专利申请量会出现失真。

分析 DSA 技术的专利数量随时间的变化趋势，可以作为预测 DSA 技术发展趋势的重要参考指标。图 1.1 揭示了 DSA 技术专利数量的年度统计情况，可以看出该技术专利家族的数量整体呈现递增的趋势。

本数据集中，最早出现的 DSA 相关技术是 UNIV BOSTON 在 1986 年申请的专利 US4802951A “Nanometre scale multi-device mfr. has nano-structures with pattern formed by binding 2-D material array to substrate with characteristics having dimensions of 1 to 50 nanometre”。在 1986-2000 年起初的几年里，该技术缓慢发

展，研发工作尚未形成规模，只有极少数公司申请了此技术的相关专利。

随着威斯康星大学麦迪逊分校（University of Wisconsin-Madison）的 Nealey 和 de Pablo 于 1997 年开始提出利用微影法形成化学性质不同的图案来引导 PS-b-PMMA 的自组装排列，并于 2001 年申请了专利 US20030091752A 和 US20040175628A，DSA 技术逐渐被业界人士重视起来。二人于 2012 年转到芝加哥大学分子工程研究所继续该方向的研究，目前已经在该领域发表了 14 项专利，其中合作 6 件，成为 DSA 技术的先驱者。

在 2000-2008 年之间，相关的企业、高校、科研单位开始大量投入到研发工作中来，专利申请量迅速增加，进入快速发展阶段，2008 年专利家族数量为 172 项，达到顶峰；2009-2011 年专利家族数量略有下降但基本保持在 130 项左右，呈现高位窄幅波动状态，专利布局步伐略有放缓；2012 年后又出现了申请高峰。在这些专利技术的支持下，2009 年开始出现多个相对成熟的 DSA 生产线组装并运行。

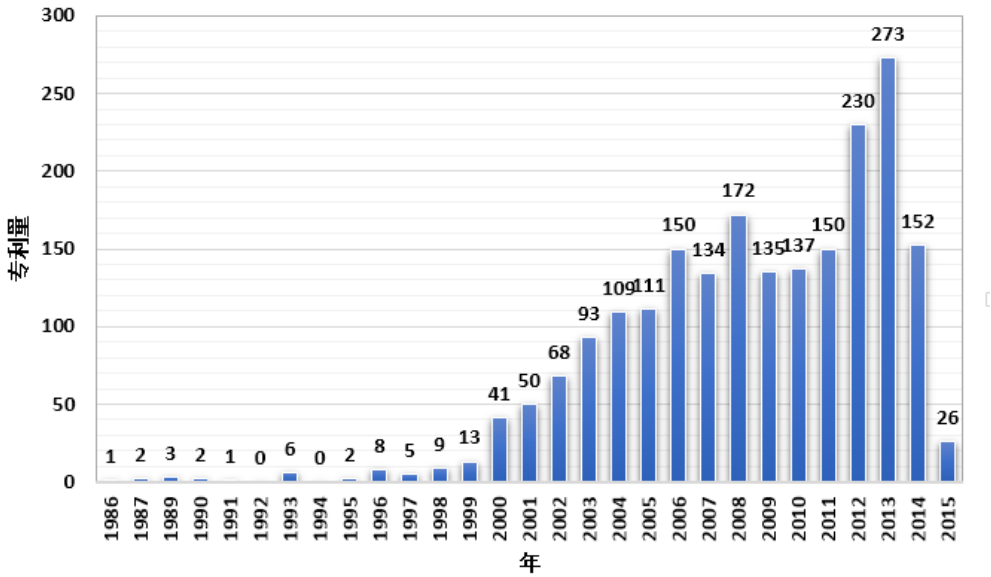


图 1.1 DSA 技术专利申请时间趋势(单位：项)

1.2 专利技术生命周期

专利技术生命周期是指在专利技术发展的不同阶段中，专利申请量与专利申请人数量的一般性的周期性的规律。一个比较完整的技术生命周期示意图是利用某段时间内与某项技术相关的专利申请数量和相应的专利申请人数量的变

化情况绘制而成的，以年度申请人量为横坐标，年度申请数量为纵坐标，绘制出曲线对技术发展的各个阶段进行分析，预测技术的发展速度及前景。专利技术生命周期常用 4 段论，即萌芽期、发展期、成熟期、衰退期。

对 DSA 技术领域的专利分析发现，DSA 技术整体上处于技术成长期。

（1）萌芽期：从 1986 年到 2000 年，DSA 技术领域发明的数量和专利申请人较少。

（2）发展期：

2001 年到 2008 年，DSA 技术领域的相关专利技术数量和申请人数量明显增加，进入快速发展期，该技术的研发投入逐渐增多。

2009 年至今，专利技术发明的数量和申请人数量略有波动，但数量仍然维持较高，整体呈现发展趋势。

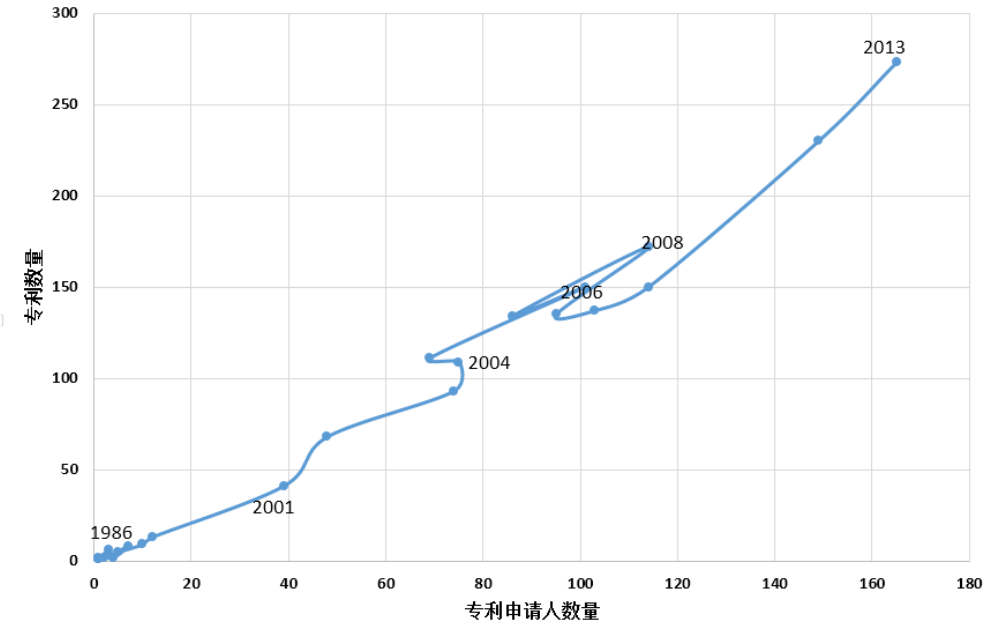


图 1.2 DSA 专利技术生命周期

2 专利申请技术构成分析

2.1 主题聚类分析

为了方便直观形象的了解 DSA 技术的研究点，对该技术专利相关关键词进行处理并绘制专利技术主题聚类图，从而更深入的探索专利技术的发明内容与创新性。

图 2.1DSA 专利技术主题分布

分析 DSA 技术主题聚类图，发现 DSA 技术主题聚焦于自组装、嵌段共聚物、薄膜、半导体器件、制备方法、电子器件、介电层、技术领域、电导率等，具体研究热点见表 2.1。

表 2.1 研究主题及热点

序号	研究主题	研究热点	序号	研究主题	研究热点
1	**自组装**	Self-assembled Block Copolymer Self Assembled Monolayer Directed Self-assembling Material Layer Nano Guiding Patterns Functional Groups Photoresist Layer Large Area Organic Solvent Organic Semiconductor Segmented Copolymer Electric Field Colloidal Crystal	**6**	**电子器件**	Self-assembled Layer Material Conductive Material Semiconductor Material Self Assembled Monolayer Organic Semiconductor SAM Nano Mask Layer Block Copolymer Layer Surface Energy Graphene Layer Multilayer Film Liquid Crystal
2	**嵌段共聚物**	Polymer Block Block Copolymer Film Directed Self-assembling Phase Separation Guiding Patterns Nanostructures BCP Diblock Copolymer Amphiphilic Block Copolymer Metal Oxide Microphase Separation Solvent Annealing Hard Mask Layer Photosensitive Layer	**7**	**介电层**	Dielectric Layer Self-assembled Metal Layer Mask Layer Gate Dielectric Material Surface Semiconductor Substrate Barrier Layer Exposed Surface Atomic Layer Deposition Conductive Material Insulator Layer Polymer Block Porous Dielectric Film 3

3	薄膜	Thin Film Transistors Material Layer Organic Semiconductor Self Assembled Monolayer Nanostructures Inorganic Thin Film Organic Solvent Printing Plate Heat Treatment Functional Groups Organic Light Surface Energy BCP Orientation Control	8	技术领域	Preparation Process Self-assembled Mesoporous Large Area Template Molecule Nanometer Structure Room Temperature Semiconductor Substrate DEG C Titanium Dioxide Silicon Dioxide Seed Crystal Liquid Crystal Main Body
4	半导体器件	Semiconductor Structure Mask Layer Self-assembly Material Organic Semiconductor Mask Pattern Insulator Layer Self Assembled Monolayer Guiding Patterns Nanostructures Diblock Copolymer Channel Region Polymer Matrix Surface Modification Base Substrate	9	电导率	Self-assembled Layer Material Electrical Contact Forming Patterns Nanostructures Electric Field Self Assembled Monolayer Polymer Film SAM Oxide Layer Line Structure Source Electrode Mask Layer Molecular Imprinting
5	制备方法	Material Layer Metal Layer Nanometer Structure Raw Material Nanostructures Template Molecule Mesoporous Material Semiconductor Substrate Silicon Dioxide Selective Solvent Liquid Crystal Colloidal Crystal Segmented Copolymer	10	其他	太阳能电池 PGT 碳纳米管 保护层 DSA 材料 图案数据 燃料电池 纳米粒子 碳原子 磁性记录层 通式 中间层 机器方向 聚合物电解质

2.2 技术时间走势分析

技术时间走势分析主要是分析 DSA 技术的技术手段随时间发展的变化情况，揭示 DSA 技术的发展过程以及最新的技术情况。本文使用德温特手工代码分析 DSA 技术方向。

下图显示DSA技术在2001年以前处于缓慢发展期，涉及的技术点非常少，之后技术分布范围逐步变大，2001 年以后相关研究涉及的技术点更加全面，每个技术分支的专利数量呈现持续增长势头，在 2006 年后开始快速增长，技术点

主要集中在 A11-B05（聚合物，塑料 - >加工聚合物，包括设备- >成型工艺 - >涂层）、A12-E07C（聚合物，塑料- >聚合物的应用 - >电气工程[其他] - >电路元件 - >半导体器件，集成电路；电阻）、A12-W14（聚合物，塑料 - >聚合物的应用 - >其他应用 - >纳米技术）、L04-C06（耐火材料，玻璃，陶瓷 - >半导体- >半导体加工- >半导体加工 -图形化技术）和 U11-C12（半导体和电子电路 - >半导体材料和加工 - >半导体器件制造的基板加工 - >自组装单层膜）。

近年来，A11-B05 和 A12-E07C 一直保持持续增长的势头，A12-W14、L04-C06 在出现微降后又开始增长；A11-C04D（聚合物，塑料 - >加工聚合物，包括设备 - >其他杂项的进程 - >表面处理 - >表面处理 - 化学处理）和 U11-C04D（半导体和电子电路 - >半导体材料和加工 - >半导体装置制造基板处理 - >光刻（光电，波束等），涂层，技术，曝光和对准 - >掩蔽技术微光刻）则迅速增长，而 U11-C12 的申请量开始下降。

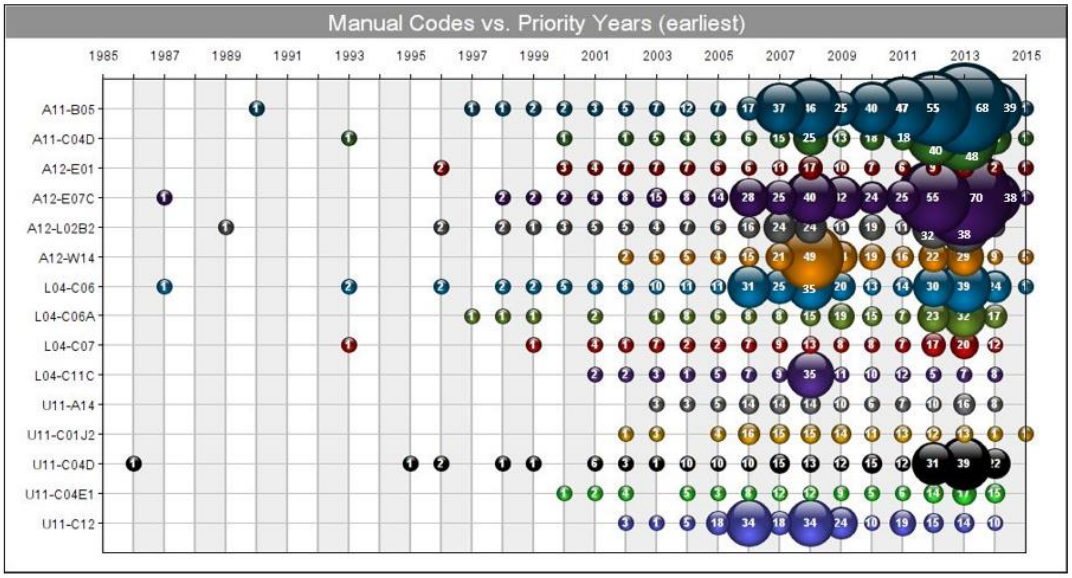


图 2.2DSA 技术时间走势分析

表 2.1 德温特手工代码具体内容

序号	手工代码	手工代码含义	专利数量
1	**A11-B05**	Polymers, Plastics -> Processing polymers including equipment -> Forming processes [others] -> Coating	**416**
2	**A12-E07C**	Polymers, Plastics -> Polymer applications -> Electrical engineering [others] -> Circuit components -> Semiconductor devices, integrated circuits; resistors	**394**
3	**L04-C06**	Refractories, Glass, Ceramics -> Semiconductors [general] -> Semiconductor processing [general] -> Semiconductor processing - patterning techniques [general]	**294**

4	**A12-L02B2**	Polymers, Plastics -> Polymer applications -> (Electro)photography, laboratory, optical [other] -> Other photographic materials, processes [exc. (film) support; binders] -> Compositions for making printing plates or electrical devices* -> Compositions for making electrical devices	**226**
5	**A12-W14**	Polymers, Plastics -> Polymer applications -> Other applications [others] -> Nanotechnology	**225**
6	**A11-C04D**	Polymers, Plastics -> Processing polymers including equipment -> Other miscellaneous processes -> Surface treatment -> Surface treatment - chemical treatment	**222**
7	**U11-C04D**	Semiconductors And Electronic Circuitry -> Semiconductor materials and processing -> Substrate processing for semiconductor device manufacture -> Lithography (photo-, beam-, etc.), masks, techniques, exposure and alignment -> Masking techniques for microlithography	**205**
8	**U11-C12**	Semiconductors And Electronic Circuitry -> Semiconductor materials and processing -> Substrate processing for semiconductor device manufacture -> Self-assembly monolayers	**205**
9	**L04-C06A**	Refractories, Glass, Ceramics -> Semiconductors [general] -> Semiconductor processing [general] -> Semiconductor processing - patterning techniques [general] -> Semiconductor processing - mask design and manufacture	**164**
10	**A12-E01**	Polymers, Plastics -> Polymer applications -> Electrical engineering [others] -> Electrical engineering [general]	**120**
11	**L04-C07**	Refractories, Glass, Ceramics -> Semiconductors [general] -> Semiconductor processing [general] -> Semiconductor processing - etching processes [general]	**119**
12	**U11-C01J2**	Semiconductors And Electronic Circuitry -> Semiconductor materials and processing -> Substrate processing for semiconductor device manufacture -> Deposition of active materials (e.g. semiconductors) -> Nature/structure/material/composition of active layers -> Semiconductor amorphous/polycrystalline film	**119**
13	**L04-C11C**	Refractories, Glass, Ceramics -> Semiconductors [general] -> Semiconductor processing [general] -> Semiconductor processing - electrodes	**117**
14	**U11-C04E1**	Semiconductors And Electronic Circuitry -> Semiconductor materials and processing -> Substrate processing for semiconductor device manufacture -> Lithography (photo-, beam-, etc.), masks, techniques, exposure and alignment -> Photolithography for semiconductor mfr. -> Apparatus and method for photolithography	**113**
15	**U11-A14**	Semiconductors And Electronic Circuitry -> Semiconductor materials and processing -> Materials -> Nano-structural materials	**110**

3.专利申请国家/地区分布

专利最早优先权国家/地区在一定程度上反应技术的来源地，美国是 DSA 技术专利产出最多的国家，占比 48%；其次韩国、中国也是该领域技术产出较多的国家；日本专利产出排名第四。

专利公开国家/地区在一定程度上反映的是技术的市场保护分布情况，从图 3.1 可以看出美国是全球 DSA 技术方面的专利申请人最重视的；国际申请排名第二，这在一定程度上反映专利的国际布局程度较高；中国、韩国分别排名第

三、第四，分别占 15%和 8%；日本、欧州、台湾、法国、英国也具有相对比重的市场份额。

通过专利最终优先地和受理地的对比发现，国际申请在最早优先权国家/地区的比例图中占比 1%，而在公开国家/地区的比例图中占比 25%，比例大幅度增长，体现了各国通过国际申请进行境外专利保护的偏爱，一定程度上说明各国重视 DSA 的全球布局；韩国、日本作为技术来源地占比较大而市场占比下降，DSA 技术产出大于技术流入；而对于中国，技术流入与技术产出基本保持平衡。

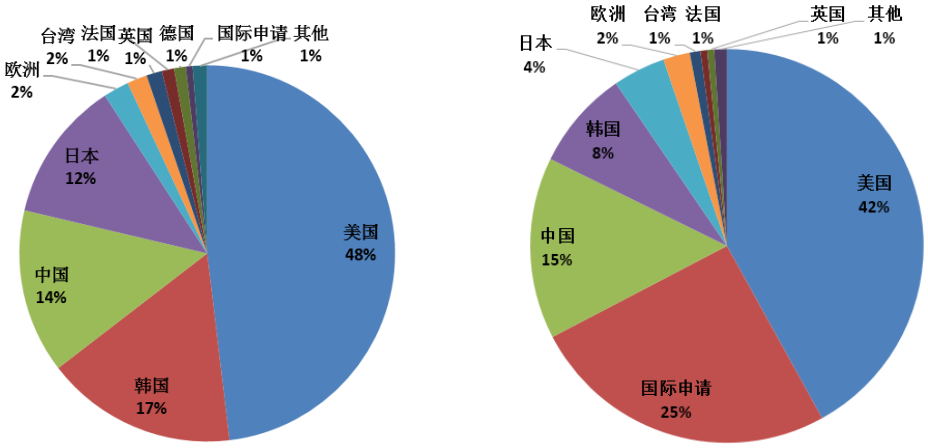


图 3.1 DSA 技术专利最早优先国家/地区、公开国家/地区对比

4 专利申请人分析

4.1 主要申请人专利数分析

主要申请人分析主要是对 DSA 技术领域专利申请人的专利产出数量进行分析，从而遴选出主要申请人，作为后续多维组合分析、评价的基础，通过对清洗后的专利家族中的专利申请人分析，可以了解在 DSA 技术领域的主要研发机构。按照专利家族数量进行统计分析，得出该领域排名前 15 名的机构如图 4.1 所示。

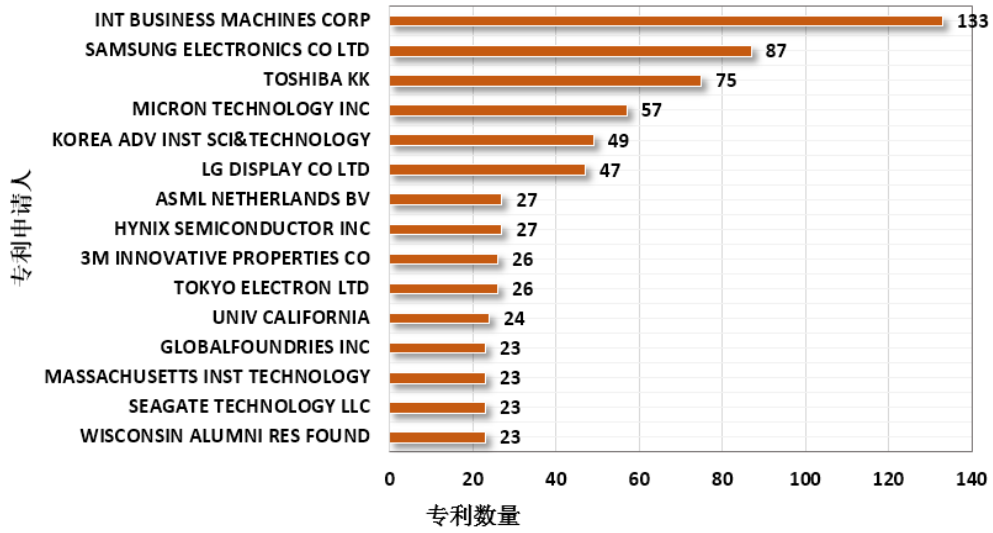


图 4.1 DSA 技术专利主要申请人

IBM 公司拥有专利技术 133 件位列第一，占总量的 4.16%。专利数量排名第二的 SAMSUNG 公司拥有专利技术 87 件，占总量的 2.72%。排名第三的 TOSHIBA 公司拥有专利技术 75 件，占总量的 2.34%。排名前 15 的研究机构共有专利 670 件，占总量的 20.94%。

目前全世界著名的 DSA 生产线联盟如表 4.1 所示，从表中看到，CEA-Leti 在 2009 年使用 Tokyo Electron 和 SOKUDO 的设备，使用 ARKEMA 等提供的材料，完成了 DSA 生产线的组装。IBM 和 IMEC 也分别在 2010 年和 2012 年完成了自己的生产线。

表 4.1 全球 DSA 生产线联盟

DSA consortiums for 300 mm-wafer scale fab-compatible DSA line

Process	Equipment	Materials	Year of consortium
CEA-Leti	Tokyo Electron Ltd., SOKUDO	ARKEMA, Laboratory of Microelectronics Technologies (LTM), Laboratoire de Chimie des Polymères Organiques (LCPO)	2009
IBM	Applied Materials	JSR Micro. Inc., AZ Electronic materials	2010
IMEC	Tokyo Electron Ltd.	AZ Electronic materials, University of Wisconsin-Madison	2012

4.2 主要申请人时间趋势

分析 DSA 技术主要申请人的历年专利数量的趋势，从而了解主要申请人投入 DSA 技术的动态，深入了解申请人各年间的专利布局态势，观察 DSA 技术的新秀或是退出等信息。

图 4.2 显示了 DSA 技术的前 15 名专利权人历年专利的增长趋势对比图。通过该图我们可以看出，MASSACHUSETTS INST TECHNOLOGY 大学、IBM、

三星、3M 和加州大学都属于在该领域研究比较早的机构。其中，IBM 和三星在 2004-2009 年之间申请专利最多，近年来有所减少，但仍然保持一定的申请量，说明他们在该方向的专利布局较早于其他机构。而威斯康星大学、3M 和加州大学一直以来都保持比较小的申请量，他们在该方向一直都有研究和产出。TOSHIBA、ASML、GLOBALFOUNDRIES 都是从 2009 年开始申请大量专利，是 DSA 领域的后起之秀。

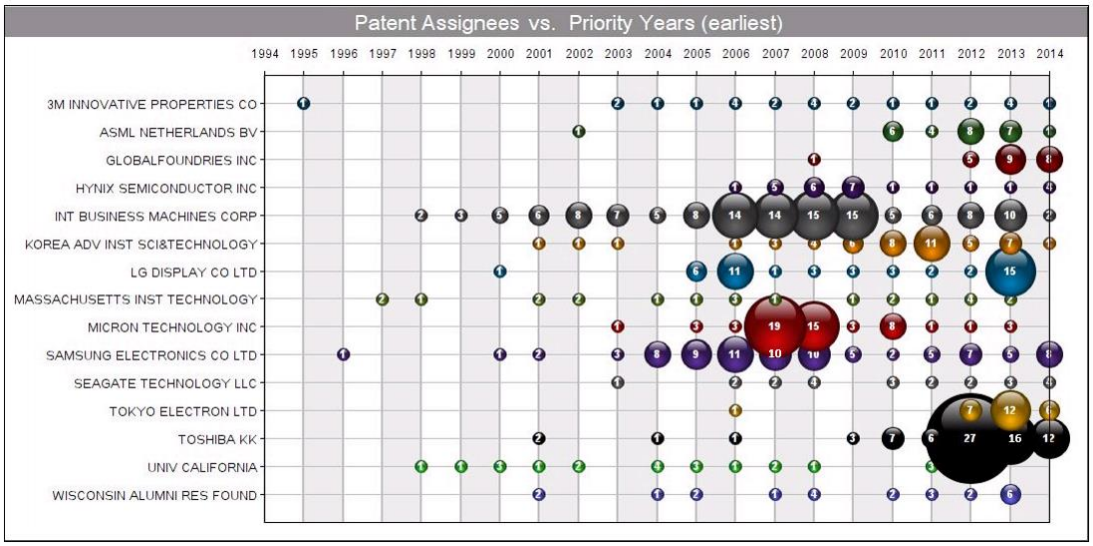


图 4.2 DSA 技术专利主要申请人申请时间趋势

4.3 主要申请人技术对比

主要申请人技术对比分析是对主要申请人的投资技术领域进行对比分析，透析各申请人的技术布局，从而分析各申请人的技术发展策略。图 4.3 显示了 DSA 技术的前 15 名专利权人主要技术对比图。

可看出 A11-B05（聚合物，塑料 - >加工聚合物，包括设备- >成型工艺 - >涂层）、A12-E07C（聚合物，塑料- >聚合物的应用 - >电气工程[其他] - >电路元件 - >半导体器件，集成电路；电阻）和 L04-C06（耐火材料，玻璃，陶瓷 - >半导体- >半导体加工- >半导体加工 -图形化技术）是各个研究机构都侧重研究的相关技术点，尤其是 IBM、MICRON、三星和 TOSHIBA。

此外，IBM 和 TOSHIBA 还侧重 A11-C04D（聚合物，塑料 - >加工聚合物，包括设备 - >其他杂项的进程 - >表面处理 - >表面处理 - 化学处理）技术的研究。

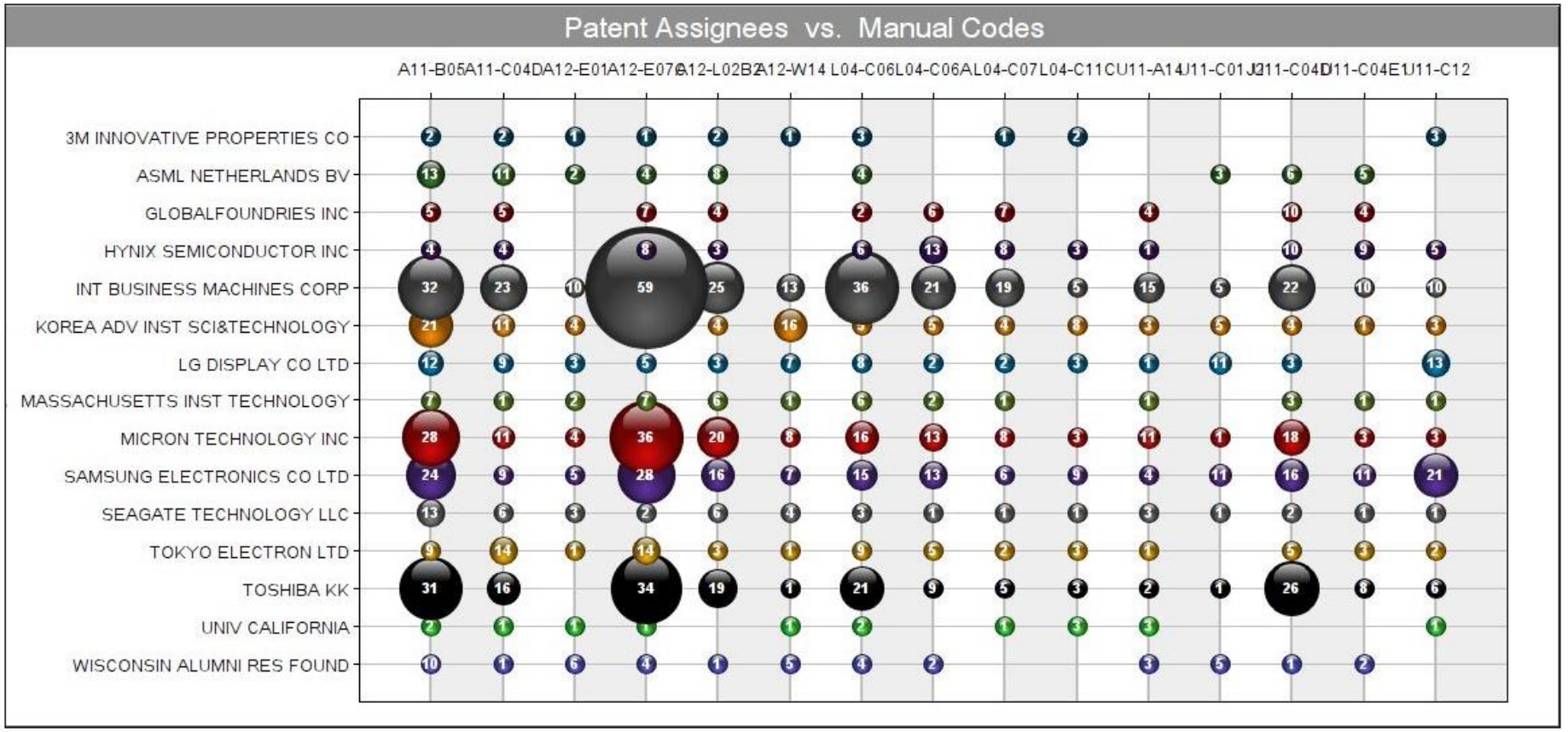


图 4.3 DSA 技术专利主要申请人技术对比

4.4 主要申请人合作分析

申请人合作分析是对申请人合作申请专利的情况进行对比分析，借以发现申请人的知识产权共享模式、创新能力、被支持力度和技术流动信息等，如图4.4是拥有专利数量大于等于8项的50个技术申请人的合作网络图。

从图上看到有两个大的专利合作圈。其中一个是IBM、GLOBALFOUNDRIES、MASSACHUSETTS INST TECHNOLOGY大学和加州大学。其中IBM是合作核心。

另一个合作圈是三星、SEAGATE、KOREA ADV INST和LG，这个合作圈是以韩国的机构为主，其中三星是合作的核心，而三星和KOREA ADV INST的专利合作最多，有4项。

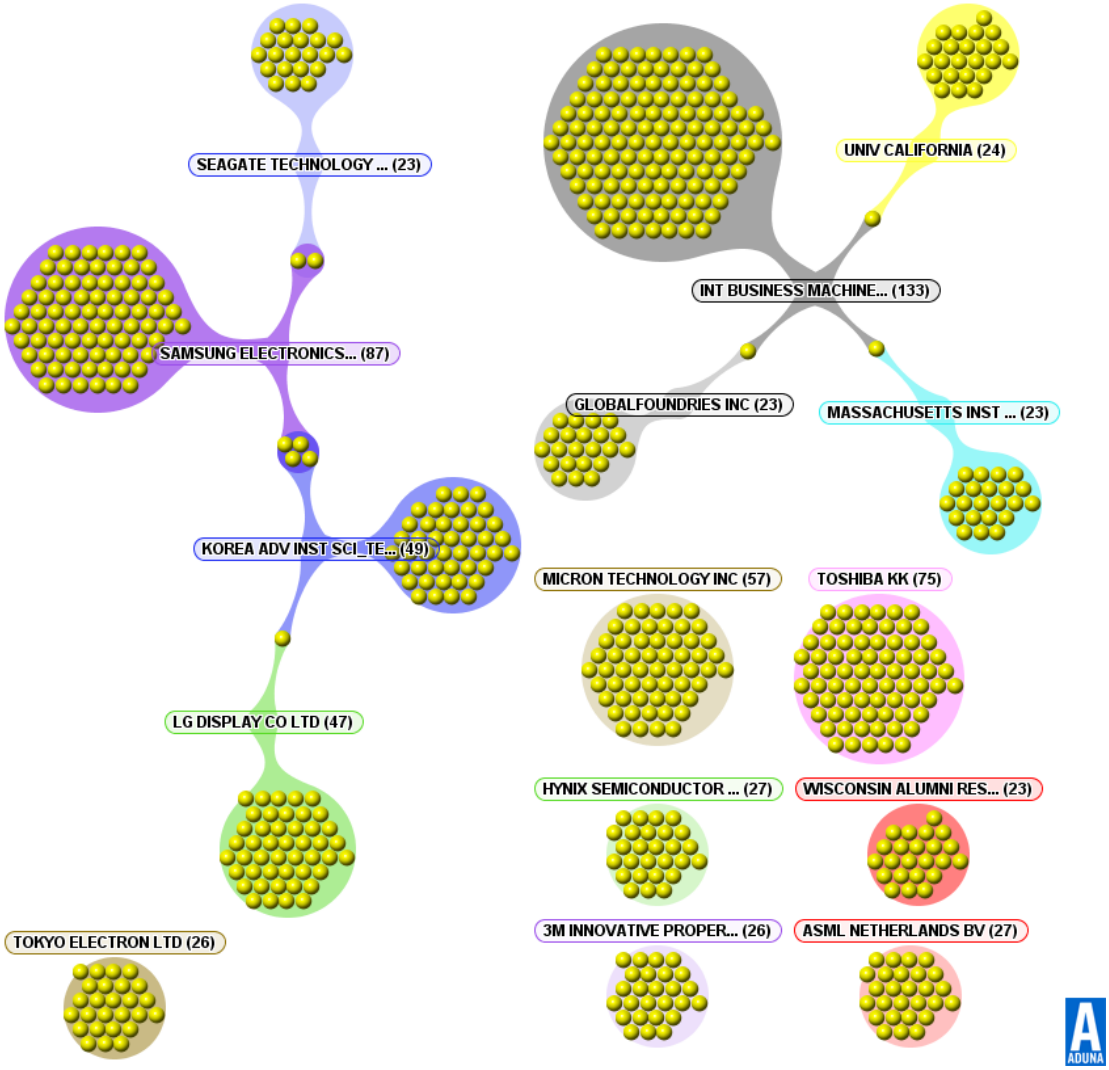


图 4.4 DSA 技术专利主要申请人合作

4.5 主要申请人技术关联分析

基于技术分类等对申请人潜在关系进行分析，借以发现申请人的技术关联、潜在合作或竞争关系等，如图 4.5 所示的 DSA 技术专利主要申请人技术关联图，可以看到这些公司之间技术契合度非常高，竞争比较激烈。

图中显示 TOSHIBA、IBM、MICRON、MASSACHUSETTS INST TECHNOLOGY 这几个机构和其他机构在研究方向上接近的最多的机构，是该行业有力的合作和竞争者，其中技术 A12-E07C（聚合物，塑料->聚合物的应用->电气工程[其他]->电路元件->半导体器件，集成电路；电阻）是他们之间最相近的研究方向。

TOSHIBA 、TOKYO ELECRON、MICRON、INTEL 和台湾半导体制造侧重于半导体工艺中的 A11-B05（聚合物，塑料->加工聚合物，包括设备->成型工艺->涂层）和 L04-C06（耐火材料，玻璃，陶瓷->半导体->半导体加工->半导体加工-图形化技术）。

此外，IMEC、WISCONSIN、3M 等机构研究的技术相对独立。其中 IMEC 主要侧重于技术 U11-C12（半导体和电子电路->半导体材料和加工->半导体器件制造的基板加工->自组装单层膜）。WISCONSIN 则主要侧重于技术 A11-C04D（聚合物，塑料->加工聚合物，包括设备->其他杂项的进程->表面处理->表面处理-化学处理）。3M 侧重于技术 L03-J（耐火材料，玻璃，陶瓷->电有机（无机）->其它用于集成电路组件和材料的制造和处理方法）

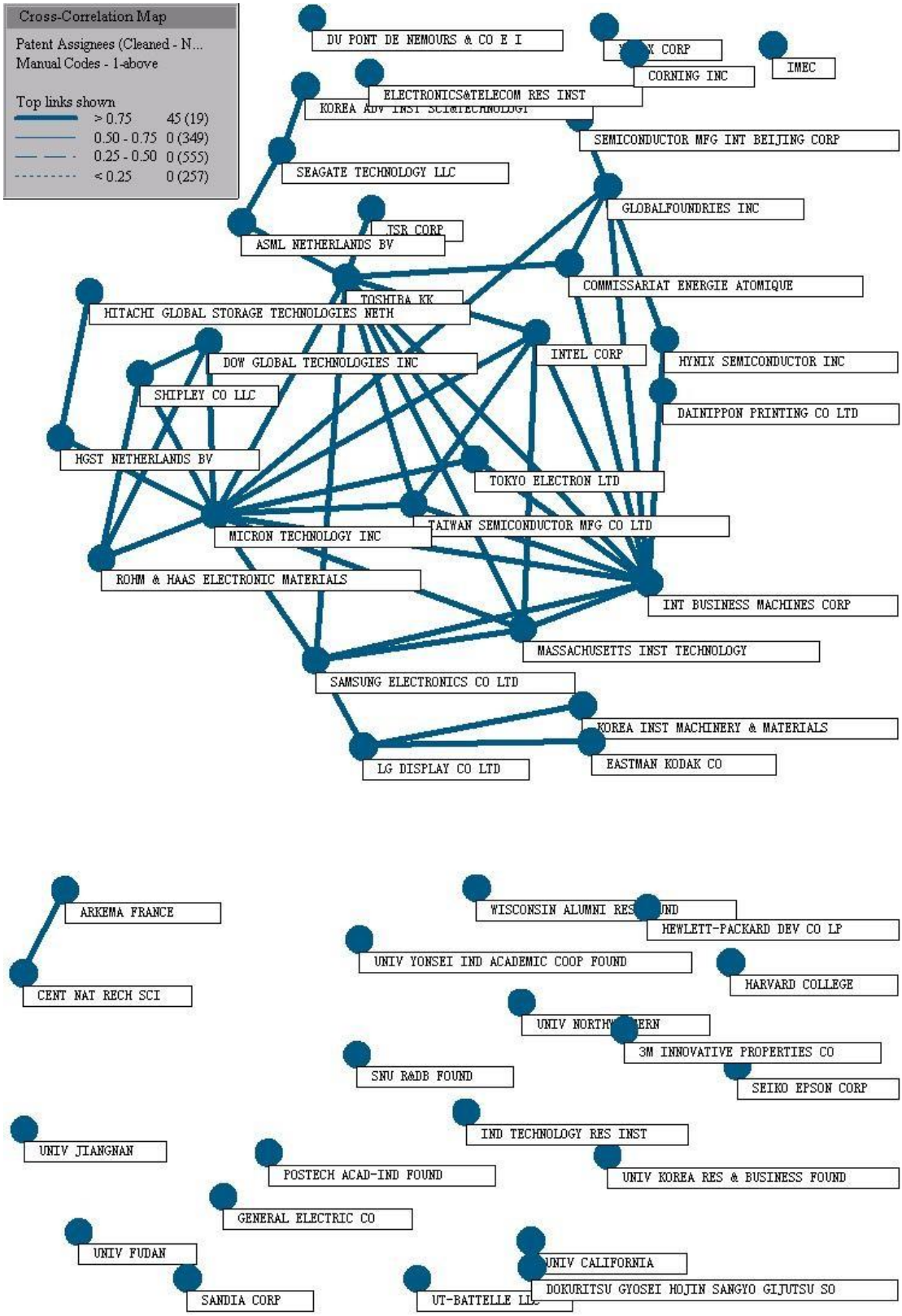


图 4.5 DSA 技术专利主要申请人技术关联

检索分析：王丽、赵慧敏

定向自组装光刻技术重点专利

说明：

将此前专利分析所用的数据集导入 **Innography** 专利数据库分析“**自组装光刻技术**”专利，抽取专利结果中专利强度≥**80** 分的 **20** 件专利作为重点专利进行推荐（专利强度范围是 **1-100** 分，其中 **80-100** 分的专利代表核心专利）。

1. **专利号**：US2009317540

专利名称：Forming non-volatile resistive oxide memory array used in computer system for storing data involves forming conductive word/bit lines over substrate, metal oxide-comprising material, and self-assembled block copolymer lines within trenches

专利发明人：SANDHU G; SMYTHE J; SRINIVASAN B

专利权人：SANDHU G (SAND-Individual); SMYTHE J (SMYT-Individual); SRINIVASAN B (SRIN-Individual); BOISE TECHNOLOGY INC (BOIS-Non-standard)

申请日: 2008/6/18

摘要： NOVELTY - Forming non-volatile resistive oxide memory array involves forming conductive word/bit lines (13, 14, 15) over substrate(10) and metal oxide containing material (12) over word/bit lines, providing series of elongated trenches (18) over word/bit lines running parallel outer major surface of substrate, trenches being angled relative to word/bit lines and having sidewalls (19), forming self-assembled block copolymer lines within trenches in registered alignment with and between sidewalls; and providing conductive word or bit lines from self-assembled block copolymer lines to form junctions.

USE - For forming non-volatile resistive oxide memory array used in computer system for storing data.

ADVANTAGE - Several non-volatile resistive oxide memory cells are fabricated

within a memory array at essentially the same time. The memory array may be fabricated such that the bit lines, word lines and or trenches serpentine relative to one another in different straight line or curved-line segments throughout the array. The materials of layer are deposited in more than one step. Non-volatile resistive oxide memory array metal having oxide-comprising material is configured to have its current leakage capabilities be selectively varied in addition to or instead of its resistive state.

2. 专利号：US2008318005

专利名称：Preparing random graft copolymer comprises reacting reaction mixture comprising p-chloromethylstyrene and styrene to form polymer chains and reacted with poly(ethylene oxide), and reacting the obtained copolymer with azide compound

专利发明人：MILLWARD D B

专利权人： MICRON TECHNOLOGY INC (MCRN-C)

申请日: 2007/6/19

摘要： NOVELTY - Process for preparing a random graft copolymer (I) comprises: reacting a reaction mixture comprising p-chloromethylstyrene and styrene to form polymer chains comprising chloromethyl moieties and repeating units derived from p-chloromethyl styrene; reacting the polymer chains with one or more oligomers or polymers of poly(ethylene oxide) to form a graft copolymer, where the poly(ethylene oxide) has only one nucleophilic end; and reacting the graft copolymer with an azide compound to displace chlorine atoms and form azidomethyl moieties on the graft copolymer.

USE - The process is useful for preparing a random graft copolymer and fabricating film, which is useful as template or mask in etching a substrate (all claimed).

ADVANTAGE - The process provides the film, which is neutral wetting to both polystyrene and polyethylene oxide. The process provides the films with self-assembled

domains, which is extend from and interface with the air and the substrate at the trench floor.

3. 专利号：US2008217292

专利名称：Nanoscale microstructure fabrication method, involves annealing portion of film overlying base layer within trench such that self-assembled lamellar domains are formed only within portion of film that has lamellar domains

专利发明人：MILLWARD D B; MARSH E P

专利权人： MICRON TECHNOLOGY INC (MICR-Non-standard)

申请日: 2007/3/6

摘要： NOVELTY - The method involves forming a base layer by annealing a film to form self-assembled polymer domains that span a specific width. Another film including a self-assembling lamellar-phase block copolymer is formed over an annealed base layer and a substrate (10). A portion of the latter film overlying the base layer is annealed within a trench (16) such that self-assembled lamellar domains are formed only within the portion of the latter film that has lamellar domains which are registered to corresponding polymer domains of the annealed base layer.

USE - Method for fabricating a nanoscale microstructure.

ADVANTAGE - The films of the linear arrays of the ordered nano structures are effectively fabricated in a cost-effective manner without defining features or utilizing self-assembling block copolymers.

4. 专利号：US6773616

专利名称：Formation of nanoscale wire for electronic and opto-electronic device, by growing nanowires with first composition on etchable layer major surface, and etching portion of etchable layer to insulating layer

专利发明人：CHEN Y; OHLBERG D A A; KAMINS T I; WILLIAMS R S

专利权人：HEWLETT-PACKARD DEV CO LP (HEWP-C)

申请日：2001/11/13

摘要： NOVELTY - Formation of nanoscale wire comprises providing etchable layer, epitaxially growing self-assembled nanowires (34), and anisotropically etching portion of the etchable layer down to the insulating layer (32). The etchable layer has second composition and buried insulating layer beneath its major surface. The nanowires have first composition on the major surface of the etchable layer to form interfacial plane between nanowires and etchable layer.

USE - For forming nanoscale wire useful in making electronic devices and opto-electronic devices.

ADVANTAGE - The invention avoids traditional lithography methods, thus minimizes environmental toxic chemical usage, simplifies manufacturing process, and allows the formation of high quality one-dimensional nanowires over large areas.

5. 专利号：US20110198736A1

专利名称：Processing self-assembled monolayer, comprises providing exposed surface, supplying organic precursor to adsorb self-assembled monolayer and supplying another organic precursor to adsorb onto reactive sites of exposed surface

专利发明人：MILLER S; MUSCAT A; SHERO E; VERGHESE M

专利权人：ASM AMERICA INC, (ASMI-C)

申请日：2011-08-18

摘 要： NOVELTY - Processing a self-assembled monolayer, comprises: providing an exposed surface; supplying a first organic precursor having a first molecular chain length to adsorb a self-assembled monolayer over the exposed surface; and supplying a second organic precursor having a second molecular chain length i.e. shorter than the first molecular chain length to adsorb onto reactive sites of the exposed surface on which a self-assembled monolayer is not adsorbed.

USE - The method is useful for processing self-assembled monolayer for forming an integrated film structure, which is useful in a semiconductor device (all claimed).

ADVANTAGE - The method effectively and rapidly inhibits the vapor deposition on selected surfaces such as reactor surfaces or selected surfaces on silicon wafer thus improving the performance and life of the semiconductor device.

6. 专利号：US20090263628A1

专利名称：Forming nano structured polymer material on substrate, useful in semiconductor manufacturing, comprises forming block copolymer material within trench in material layer on substrate, and annealing the block copolymer material

专利发明人：LLWARD D B

专利权人：MICRON TECHNOLOGY INC (MCRN-C)

申请日: 2009-10-22

摘要： NOVELTY - Forming nano structured polymer material on a substrate, comprises forming: a block copolymer material within a trench (16') in a material layer on the substrate, the trench having a floor, opposing sidewalls and ends that are preferentially wetting to a minority block of the block copolymer, and the block copolymer material having an inherent pitch value (L) and a total initial thickness within the trench such that the block copolymer material has a sufficient volume at the end of annealing to self-assemble into cylindrical domains (48'); and annealing the block copolymer material.

USE - The nano structured polymer material is useful in semiconductor manufacturing.

ADVANTAGE - The method provides: ordered and registered elements on a nanometer scale that can be prepared more inexpensively than by electron beam lithography, or conventional photolithography; and low cost, high-throughput technique for fabricating small structures. The method does not require unconventional

processes for manufacturing the required structures.

7. 专利号：US20090200646A1

专利名称：Formation of nanostructured polymer material on substrate by annealing block copolymer material so that block copolymer material self-assembles into cylindrical domains of a block of block copolymer within matrix of another block

专利发明人：MILLWARD D; MILLWARD D B; MILWOEDEU D B; SEUTYUEON K; STUEN K

专利权人：MICRON TECHNOLOGY INC (MCRN-C)

申请日：2009-08-13

摘要： NOVELTY - A nanostructured polymer material is formed on a substrate by forming a self-assembling block copolymer material within a trench in a material layer on the substrate; and annealing the block copolymer material so that the block copolymer material self-assembles into cylindrical domains of the first block of the block copolymer within a matrix of a second block of the block copolymer.

USE - Method of forming a nanostructured polymer material on a substrate (claimed).

ADVANTAGE - The method provides ordered and registered elements on a nanometer scale which can be prepared more inexpensively than by electron beam lithography, extreme UV photolithography or conventional photolithography; employs systems which can be readily employed and incorporated into existing semiconductor manufacturing process flows; is low cost; and has high-throughput efficiency.

8. 专利号：US20080299774A1

专利名称：Patterning semiconductor substrate including printing technique for integrated circuit fabrication, by providing block copolymer layer, removing block, blanket depositing spacer material on mandrels, etching spacer and transferring pattern

专利发明人：SANDEUHU G; SANDHU G

专利权人：MICRON TECHNOLOGY INC (MCRN-C)

申请日: 2008-12-04

摘要： NOVELTY - Patterning semiconductor substrate (110) comprises providing layer comprising block copolymers (162, 164) ; selectively removing one block of block copolymers to leave laterally-separated mandrels comprising other block of block copolymers; blanket (170) depositing spacer material on mandrels; etching spacer material to form spacers on sidewalls of mandrels; and transferring pattern defined by spacers to substrate. A laterally spaced apart copolymer self-assembly guides (134) are provided over the substrate.

USE - Method for patterning semiconductor substrate including printing technique for integrated circuit fabrication (claimed).

ADVANTAGE - The method allows formation of mask features smaller than that formed by block polymers alone without using newer, complex and expensive lithography techniques, and reduces burden on robustness of photoresist. A self-organizing material comprising different chemical species is allowed to organize to form domains comprising the same chemical species.

9. 专利号： US20080176767A1

专利名称：Forming nano structured polymer material on substrate, useful in semiconductor manufacturing, comprises forming block copolymer material within trench in material layer on substrate, and annealing the block copolymer material

专利发明人：MILLWARD D B

专利权人：MICRON TECHNOLOGY INC (MCRN-C)

申请日: 2008-07-24

摘要： NOVELTY - The film comprising self-assembled block copolymer is formed within trenches (14). The individual trench has width of 10-100 nm, length of

n(10-100 nm), pitch distance between adjacent trenches of 2(10-100 nm), preferential wetted sidewalls (16) and edges (20), and neutral wetted floor with edges of the trenches aligned. The copolymer film forms single array of perpendicularly oriented cylindrical domains of polymer block (A) of the block copolymer in matrix of polymer block (B) of the block copolymer within each trench. Thus, nano-scale microstructure is fabricated.

USE - Fabrication of nano-scale microstructure used for polymeric film (claimed) for semiconductor wafer and substrate.

ADVANTAGE - The method economically provides nano-scale microstructure.

10. 专利号： US20040241396A1

专利名称：Modification of a surface of a substrate useful in articles involves inkjet printing a first material comprising non-vaporizable component containing self-assembling compound onto a portion of the surface of the substrate

专利发明人：JING N; KORBA G; KORBA G A; YLITALO C; YLITALO C M

专利权人：3M INNOVATIVE PROPERTIES CO (MINN-C)

申请日: 2004-12-02

摘要： NOVELTY - Modification of a surface of a substrate comprises: inkjet printing a first material onto a portion of the surface of the substrate. The material comprises a non-vaporizable component. The non-vaporizable component comprises at least one self-assembling compound (≥ 10 wt.%).

USE - For modifying a surface of a substrate; in article (claimed); for inkjet printing methods e.g. thermal inkjet, continuous inkjet, piezo inkjet, acoustic inkjet, and hot melt inkjet printing; in the manufacture of a variety of articles (e.g. microfluidic devices (e.g. lab on a chip and drug delivery devices), analytical test strips (e.g. blood glucose test strips)).

ADVANTAGE - The method provides ability to control the wetting of a liquid on

a surface of a substrate according to a precise high-resolution pattern. The method provides high resolution pattern and is well-suited for short run applications.

11. 专利号： US20130324666A1

专 利 名 称 ：New block copolymer comprising polymer backbone groups containing wedge groups and/or polymer side chain groups used in supramolecular assembly to form structure such as templates and scaffolds for nanodots, nanowires, and optical devices

专利发明人：ATWATER H A; DAEFFLER C S; GRUBBS R H; MIYAKE G M; PIUNOVA V; SVEINBJORNSSON B R; WEITEKAMP R; XIA Y

专利权人：CALIFORNIA INSTITUTE OF TECHNOLOGY

申请日: 2013-12-05

摘要： NOVELTY - A block copolymer (C1) comprising at least 10 first repeating units, where each of the first repeating units of the copolymer comprises a first polymer backbone group covalently linked to a first wedge group or a first polymer side chain group; and at least 10 second repeating units, where each of the second repeating units of the copolymer block comprises a second polymer backbone group covalently linked to a second wedge group or a second polymer side chain group that is different than the first wedge group or the first polymer side chain group, where the first and second repeating units are directly or indirectly covalently linked along a backbone of the copolymer, and where a size (R) of the copolymer is directly proportional to molecular weight (MW) raised to power x (where x is 0.85 to less than 1), is new. An INDEPENDENT CLAIM is included for preparation of the block copolymer (C1).

USE - In supramolecular assembly to form structure (claimed) such as templates and scaffolds for nanodots, nanowires, magnetic storage media, semiconductors, optical devices, polarizers, and photonic materials.

ADVANTAGE - The block copolymers (C1) have a molecular weight of 100000 to 30000000 Da; exhibit useful physical, chemical and optical properties for a range of applications including photonics, optoelectronics, and molecular templates and scaffolding; and are capable of efficient self-assembly to generate useful periodic structures with domain lengths in the nanometer range and exhibiting optical functionality in the visible and near-infrared (NIR) regions of the electromagnetic spectrum.

12. 专利号： US20090087664A1

专利名称：Forming complex copolymer structure involves depositing copolymer material on patterned substrate, configured to drive the assembly of micro-phase separated films that exhibit the same morphology as that of the copolymer material in bulk

专利发明人：BATES F S; DE PABLO J J; NEALEY P F; PABLO J J D

专利权人：WISCONSIN ALUMNI RES FOUND (WISC-C)

申请日: 2009-04-02

摘要： NOVELTY - Forming (M1) complex copolymer structures involves: providing a substrate patterned with activated regions; depositing a layer of material comprising an n-block copolymer on the substrate; and ordering components in the copolymer material such that an ordered microphase-separated film is formed, where at least n phases are registered with the underlying substrate and the morphology of the ordered film is the bulk morphology of copolymer material.

USE - For forming complex copolymer structures useful for fabricating thin film tri-block copolymer structure on substrate (claimed); and in semiconductor processing.

ADVANTAGE - The method directs the assembly of tri-block (and higher order) copolymers of different compositions into a number of fabrication templates with complex architectures and perfect ordering over areas as large as chips, throughout

films that are thick enough to be considered three-dimensional, and precisely registered with the underlying substrate. The preferential surface interactions of blocks of the copolymer material with activated regions result overcome unfavorable blocks/substrate surface interactions, resulting in an overall minimization of the energy so that the bulk morphology is obtained. The chemically patterned substrate allows desired orientation of the structures with respect to the substrate, perfect patterning over arbitrarily large areas, and registration of the structures with the substrate.

13. 专利号： US20060108320A1

专利名称：Fabrication of semiconductor device by receiving substrate comprising dielectric material(s), and forming molecularly self-assembled layer on exposed surface of dielectric material

专利发明人：CHIANG T P; KESHAVARZ M; LAZOVSKY D E

专利权人：INTERMOLECULAR INC, (INTE-N)

申请日: 2006-05-25

摘要： NOVELTY - Fabrication of semiconductor device includes receiving a substrate comprising dielectric material(s), and forming a molecularly self-assembled layer on an exposed surface of dielectric material. The molecularly self-assembled layer comprises material(s) having molecular characteristic and/or molecular type selected according to at least one pre-specified property of self-assembled layer.

USE - For fabricating semiconductor device (claimed).

ADVANTAGE - Formation of molecularly self-assembled layer (MSAL) eliminates the need to provide a deposited barrier layer together with the MSAL between the dielectric and electrically conductive materials. Use of MSAL to seal pores provides a barrier to reactants used in an ALD process or other chemical-based process that forms a deposited barrier layer. This pore sealing MSAL seals pores formed in a porous dielectric material so that the barrier to reactant diffusion into the porous

dielectric material is the same as or better than that into a non-porous dielectric material without the MSAL. The pore sealing MSAL enables or facilitates use of porous dielectric materials with low dielectric constants. The MSAL can provide adhesion properties between the electrically conductive material and dielectric material, inhibiting delamination of electrically conductive material from dielectric material.Forming (M1) complex copolymer structures involves: providing a substrate patterned with activated regions; depositing a layer of material comprising an n-block copolymer on the substrate; and ordering components in the copolymer material such that an ordered microphase-separated film is formed, where at least n phases are registered with the underlying substrate and the morphology of the ordered film is the bulk morphology of copolymer material.

14. 专利号： US8667428B1

专利名称：Method for fabricating integrated circuit, involves applying directed self-assembly model to directed self-assembly directing pattern to generate updated DSA directing pattern by using computing system

专利发明人：CHIANG T P; KESHAVARZ M; LAZOVSKY D E

专利权人：ADVANCED MICRO DEVICES INC (ADMI-C);

GLOBALFOUNDRIES INC(MUBA-C)

申请日: 2014-03-04

摘要： NOVELTY - The method involves applying a directed self-assembly (DSA) model to a DSA target pattern to generate a first DSA directing pattern by using a computing system (100). A residual value between the DSA target pattern and the DSA directing pattern is calculated by using the computing system. A cost function of the residual value between the DSA target pattern and the DSA directing pattern is computed by using the computing system. The DSA model is applied to the first DSA directing pattern to generate an updated DSA directing pattern by using the computing

system.

USE - Method for fabricating an integrated circuit.

ADVANTAGE - The method enables achieving directed self-assembly process/proximity correction in integrated circuits in a cost effective manner.

15. 专利号： US7790045B1

专利名称：Formation of face-centered cubic system sphere array of close-packed spheres within V-shaped groove by applying self-assembling block copolymer in V-shaped groove, where angle of walls for groove and block copolymer is purposely selected

专利发明人：CHUANG P; ROSS C A

专利权人：MASSACHUSETTS INST TECHNOLOGY (MASI-C)

申请日: 2010-09-07

摘要： NOVELTY - Method comprises providing a substrate having V-shaped groove(s) (V) formed in part(s) by 2 angled side walls; and applying a self-assembling block copolymer in the V-shaped groove, where an angle of the walls for the V-shaped groove and the block copolymer is selected such that the block copolymer forms a face-centered cubic (fcc) system sphere array (A) of close-packed spheres within the V-shaped groove.

USE – The method is for forming fcc system sphere array of close-packed spheres within V-shaped groove (claimed), useful for lithography applications for forming arrays of discrete metal dots or like shapes in various semiconductor processing applications. The square symmetry of the top layer of the fcc block copolymer sphere array may provide a useful template for making square arrays of nanostructures.

ADVANTAGE - The V-shaped grooves promote the formation of fcc sphere array that is well ordered. The block copolymer confined within V-shaped groove does not adjust its interlayer spacing to within the bulk of the V-shaped groove; and

incommensurabilities are instead accommodated by changes in packing, or changes in sphere diameter, which are restricted to the top layer of spheres. Thus, the top layer of spheres may show a hexagonal arrangement or a square arrangement. The groove geometry promotes an fcc sphere array even for relatively thick films, despite the bulk morphology being body-centered cubic system. The local density of the block copolymer remains constant; and the system cannot form vacancies, so the incommensurability must be accommodated by adjustment of the sphere size or the packing structure. The ability to form ordered 3-dimensional arrangements for a range of film thicknesses makes block copolymers attractive for the fault-tolerant templated self-assembly of nanoscale periodic arrays.

16. 专利号： US20130327636A1

专利名称：Making patterned dot array, comprises e.g. providing a substrate having layer in which the array is to be fabricated, depositing, onto layer a nanoparticle layer comprising surfactant and nanoparticle, and treating the surfactants

专利发明人：CHENG J; KIM H; RETTNER C T; SANDERS D P; SOORIYAKUMARAN R; SUNDBERG L

专利权人：UNIV CARNEGIE MELLON(UYCM-C)

申请日: 2013-12-12

摘要： NOVELTY - Controlling orientation of microphase-separated domains in block copolymer film involves:

USE – For controlling orientation of microphase-separated domains in block copolymer film (claimed) used as alternative low-cost nanopatterning material for generating periodic nanoscale structures and in the production of article of manufacture e.g. computer hardware product such as permanent or rewriteable data storage media such as hard disks readable by a machine, employing computer usable media; in the fabrication of semiconductors including microprocessors including those with memory

caches, ASICs, and/or memory chips including dynamic random access memory (DRAM), static random access memory (SRAM), and Flash.

ADVANTAGE - The orientation control composition imparts controlled orientation of micro-domains in films of block copolymers subsequently disposed on the orientation control layer. The composition and method forms an orientation control layer at the surface of a substrate that can provide orientation control of micro-domains in a block copolymer layer disposed on it. The method allows for formation of self-assembling preparation of nanoscale structural features and directional control of the nanopatterned features, by sequential deposition of the orientation control layer using conventional solution coating techniques, providing greater control of the desired feature patterns, integrability into different post-patterning processes useful for obtaining different topographies by substrate etch, and thereby obtaining reduced processing and cycle time in the fabrication of such structures, and for the preparation of a wide variety of features in a wide variety of compositional or topographic substrates. The method generates a film of a crosslinked orientation control layer from epoxy-based crosslinkable orientation control material that is compatible with a wide variety of surfaces. The orientation control materials when coated on substrate in a film-forming process provides a crosslinked orientation control layer having neutral surface energy that can be tuned to be compatible with a variety of microdomain-forming layers comprising the block copolymers.

17. 专利号： US7521090B1

专利名称：Controlling orientation of microphase-separated domain in block copolymer film used in nanoscale structure involves forming epoxy-containing cycloaliphatic acrylic polymer layer, heating, forming copolymer assembly layer and removing domain

专利发明人：CHENG J; KIM H; RETTNER C T; SANDERS D P;

SOORIYAKUMARAN R; SUNDBERG L

专利权人：INT BUSINESS MACHINES CORP (IBMC-C)

申请日: 2009-04-21

摘要： NOVELTY - Method (M1) for fabricating a patterned dot array, comprises e.g.: (a) providing a substrate having at least one layer in which the patterned dot array is to be fabricated; and (b) depositing, onto at least one layer in which the patterned dot array is to be fabricated, a nanoparticle layer, where the nanoparticle layer comprises at least one surfactant and nanoparticle, with the nanoparticles being coated with the surfactants in the nanoparticle layer, and with portions of the surfactants filling spaces among the nanoparticles in the nanoparticle layer.

USE – The method is useful for fabricating a patterned dot array and a patterned antidot array (claimed), where dot array is pillar array and antidot array is pit or hole.

ADVANTAGE - The method provides patterned dot array and a patterned antidot array with desired feature size, which are fabricated quickly, reliably, and inexpensively.

18. 专利号： US20110147984A1

专利名称：Forming layered structure for creating patterned layers involves disposing photoresist layer on substrate; exposing, heating and developing the layer; casting the material and allowing to self-assemble to form layered structure

专利发明人：CHENG J; COLBURN M; COLBURN M E; HARRER S; HINSBERG W; HINSBERG W D; HOLMES S; HOLMES S J; KIM H; SANDERS D P

专利权人：INT BUSINESS MACHINES CORP (IBMC-C)

申请日: 2011-06-23

摘要： NOVELTY - Forming layered structure comprises self-assembled (SA) material (78) involving disposing non-crosslinking photoresist layer (73) on substrate (10); developing layer to form patterned layer, treating layer photochemically,

thermally or chemically to form treated patterned layer; casting solution of orientation control material (58) and heating control layer to bind material to second substrate surface; forming pre-pattern; casting solution of material dissolved in second solvent on pre-pattern; and allowing casted material to self-assemble with heating/annealing to form layered structure.

USE – To form layered structures comprising metal wiring lines, holes for contacts or vias, insulation sections (e.g. damascene trenches or shallow trench isolation), and trenches for capacitor structures suitable for the design of integrated circuit devices; also useful in context of creating patterned layers of oxides, nitrides or polysilicon.

ADVANTAGE - The method utilizes high resolution, positive-tone photoresists to make the initial patterned photoresist layer, either by positive-tone or negative-tone development. The photoresist material that has been exposed to higher radiation doses and undergone further polarity increase during baking is even less soluble in low polarity solvent (preferably anisole). This behavior can be utilized to control photoresist solubility without cross-linking the photoresist. The method can utilize commercially available optical lithography tools, processes and materials to generate chemical pattern without any additional etch process. Also has ability to trim photoresist pattern prior to application of orientation control material which allows the size of pinning regions to be less than resolution of optical lithography tool. The photoresist consist of surface-active components that control the surface properties of the coated photoresist and limit the extraction of photoresist components into immersion fluid. The method utilizes self-assembled material with reduced feature size and increased periodicity relative to pre-pattern.

19. **专利号：** US20100314767A1

专利名称： Self-aligned interconnect structure comprises substrate, low-dielectric constant material having interconnect pattern, another low-dielectric constant

material having interconnect pattern, and conductive material

专利发明人：CHEN S; LIN Q; PURUSHOTHAMAN S; SPOONER T A; WALSH S M

专利权人：INT BUSINESS MACHINES CORP (IBMC-C)

申请日: 2010-12-16

摘要： NOVELTY - A self-aligned interconnect structure comprises a first patterned and cured low-dielectric constant (low-k) material (18') provided on surface of substrate (12) and including first interconnect pattern(s); a second patterned and cured low-k material (22') provided atop the first low-k material and having second interconnect pattern(s) different from the first interconnect pattern, in which portion of second low-k material partially fills the first interconnect pattern; and a conductive material (25) filling the first and second interconnect patterns.

USE – Self-aligned interconnect structure.

ADVANTAGE - The use of patternable low-k material eliminates use of separate photoresist, and reduces plasma etching and complex sacrificial film stack and processes required for patterning. This saves cost and provides improved performance and reliability.

20. 专利号： US20100279062A1

专利名称：Self-assembled block copolymer film within trenches in substrate, where the film in a first trench comprises perpendicular cylinders and the film in a second trench containing parallel-oriented half-cylinders

专利发明人：MILLWARD D B; SANDHU G; WESTMORELAND D

专利权人：MICRON TECHNOLOGY INC (MCRN-C)

申请日: 2010-11-04

摘要： NOVELTY - A self-assembled block copolymer film within trenches in a substrate, where the film in a first trench comprises perpendicular cylinders and the

film in a second trench comprises parallel-oriented half-cylinders.

USE – As self-assembled block copolymer film within trenches in a substrate useful as template (claimed) or mask.

ADVANTAGE - The block copolymer film anneals to cause the component polymer blocks to separate phase and is self assembled. The annealed and ordered film is treated to crosslink the polymer segments to fix or enhance the strength of the self-assembled polymer blocks within the trenches.

21. 专利号： US20100102415A1

专利名称：Forming layered structure for creating patterned layers involves disposing photoresist layer on substrate; exposing, heating and developing the layer; casting the material and allowing to self-assemble to form layered structure

专利发明人：GREELEY J N; MILLWARD D B; QUICK T A

专利权人：MICRON TECHNOLOGY INC (MCRN-C)

申请日: 2010-04-29

摘要： NOVELTY - The method comprises applying a material comprising two polymeric blocks that are immiscible with one another over a trench in a material overlying a substrate (102), annealing the material to form a film comprising repeating domains comprising one of the polymeric blocks surrounded by a matrix comprising another of the polymeric blocks, exposing the film to a swelling agent comprising a metal oxide precursor, which selectively bonds to the repeating domains, and oxidizing the metal oxide precursor to form a metal oxide. The application of the material comprises applying a block copolymer.

USE – The method is useful for forming metal oxide structures, which are useful in a semiconductor structure (claimed).

ADVANTAGE - The method is capable of economically and easily forming the metal oxide structures with enhanced density and reliability, improves the etch

selectivity of the self-assembled domains, and reduces or prevents the buckling or wrinkling of the metal oxide structure.

政策计划

白宫发布美国制造业创新战略规划

2016 年 2 月 19 日，美国商务部部长、总统行政办公室、国家科学与技术委员会、先进制造国家项目办公室，向国会联合提交了首份国家制造创新网络年度报告和战略计划。

《国家制造创新网络计划年度报告》（NATIONAL NETWORK FOR MANUFACTURING INNOVATION,NNMI, PROGRAM ANNUAL REPORT）中描述了 NNMI 计划的主要目标和早期进展。

NNMI 计划旨在解决与制造相关的复杂的技术转移方面的挑战，为了持续关注并引导利益相关者实现最终的技术产业化。NNMI 在 2015 年提出了一个愿景、一个使命及一组计划目标，如下图：

Figure 3. NNMI Program Vision, Mission, and Goals

NNMI 计划致力于建立引导创新的产业生态链及提升转移转化的能力。NNMI 计划包括一批制造业创新研究机构，呈战略性分布，旨在将制造和研究汇聚起来，截止 2015 年 9 月，已建立的机构包含：

- America Makes，即国家增材制造创新机构，位于俄亥俄州杨斯顿，关注增材制造和 3D 打印技术。
- Digital Manufacturing and Design Innovation Institute，位于伊利诺伊州芝加哥，关注数字设计与制造的集成。

- PowerAmerica，即下一代电力电子制造创新机构，位于北卡罗来纳罗利，关注基于宽能带隙半导体的电子器件。
- Lightweight Innovations for Tomorrow，即美国轻质材料制造创新机构，位于密歇根州的底特律，关注轻金属制造技术。
- Institute for Advanced Composites Manufacturing Innovation，位于田纳西州诺克斯维尔，关注先进纤维增强聚合物复合材料。
- AIM Photonics，即美国集成光子制造创新机构，位于纽约州罗彻斯特，关注集成光子电路制造。
- NextFlex，即柔性混合电子制造创新机构，位于加利福尼亚州圣何塞，关注半导体与柔性电子器件的制造和集成。

这些研究机构是 NNMI 计划的基本核心，这些研究机构发挥着产业、研究及教育之间的桥梁作用，从而形成一个创新的生态系统，协同解决高风险制造业的挑战，并协助厂商保持并扩大美国的工业生产。创新生态系统的成员与联邦政府合作投资，形成强大的公私合作伙伴关系，旨在加速美国先进制造力开发部署的非联邦投资，从而增强美国制造业的竞争力。下图显示了围绕 NNMI 研究机构的制造业创新生态系统的主要内容：

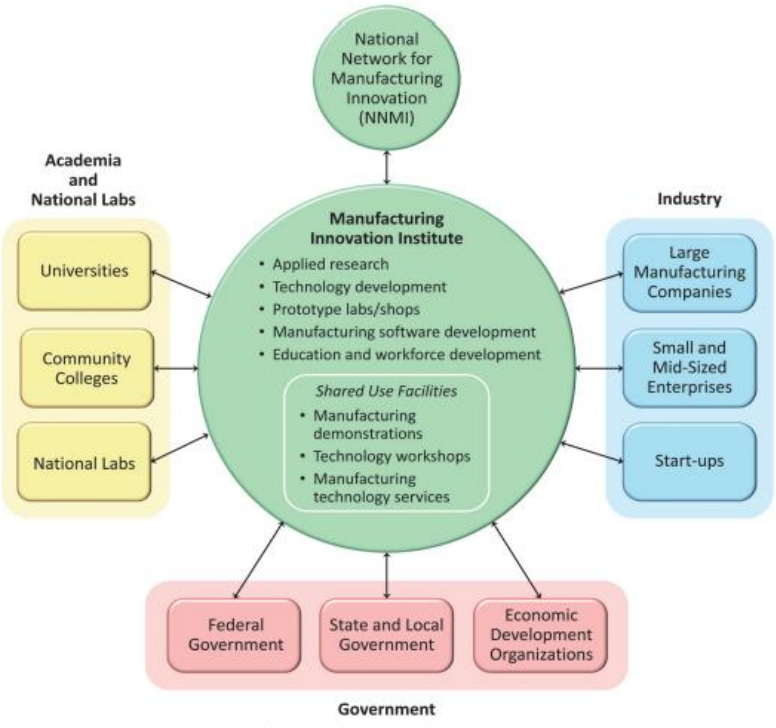


Figure 5. Institute Innovation Ecosystem

NNMI计划的一个重点就是要连接的创新和制造，为此，NNMI研究机构的主要活动包含：

- 竞争前的应用研究、开发和生产规模扩大研究，以便在新制造技术商业化及现有技术、工艺、产品改进过程，做到节约成本、缩短时间和降低风险。
- 制定和实施教育和培训计划。
- 面向供应链整合及新技术引进发展创新方法和实践，。
- 推广并参与到中小型企业及大型制造企业。

王丽 摘译自：

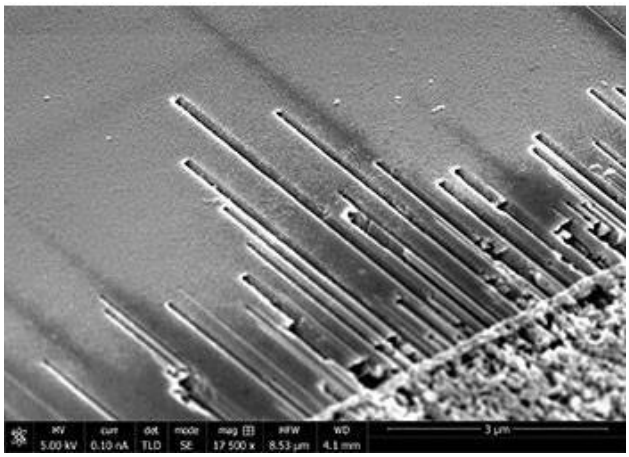
https://www.manufacturing.gov/files/2016/02/2015-NNMI-Annual-Report.pdf

前沿研究

研究人员取得定向自组装半导体制程突破

美国国家标准与技术研究所(NIST)与 IBM 的研究人员开发了一种沟槽(trenching)技术，能被用以透过定向自组装(self-directed assembly)来打造元件。研究人员表示，金奈米粒子能像是铲雪机那样运作，在磷化铟(indium phosphide)或其他半导体材料层翻搅而过，形成奈米通道。这种技术可望被用来在所谓的实验室单晶片(lab-on-a-chip)元件上整合雷射、感测器、波导(wave guides)与其他光学零组件，支援疾病诊断、筛选实验性材料与药物、DNA 检验等等。

金粒子的通道挖掘 能力是偶然被发现的，在一个因为污染物而失败的奈米线(nanowires)形成实验中；NIST 化学研究员 Babak Nikoobakht 表示：“一开始我们非常失望，”但是研究团队无心插柳，发现污染物是水。该实验的扫描电子显微镜影像显示，结合水汽的金奈米粒子导致 了长长直直的奈米通道。



在磷化铟半导体的表面上形成的表面定向奈米通道电子显微镜影像；那些奈米通道是利用金催化汽态-液态-固态蚀刻制程所形成，而其位置则是由沉积的金图形(pattern)所定义（来源：NIST）

研究团队接下来梳理出实现该蚀刻制程所需的化学机制与必要条件，选择性地在半导体表面涂布金并将之加热；一旦加热完成，底层的磷化铟就会融入金奈米粒子， 形成金合金。他们接下来将加热的水蒸汽导入系统，发现当水蒸汽温度达到摄氏 440 度以上时，会形成长长的 V 型奈米通道；那些通道下方的直线路径，是由结晶 半导体内的规律重复晶格所支配。

研究人员也能将上述技术应用于磷化镓(gallium phosphide)与砷化铟(indium arsenide)，这两种半导体材料也是属于三五族；这类化合物半导体被用以制作LED，或是支援通讯、高速电子等应用。Nikoobakht 表示，他 相信这种蚀刻制程经过调整之后，能被用以在矽等材料上制作通道图案。

原文标题：Researchers Claim Self-directed Assembly Breakthrough

滕飞选摘自：

http://www.p-e-china.com/zhuanti/zhuannei.asp?newsid=75963

利用耗散力子动力学研究定向自组装光刻长程有序层状结构的稳定性

为了获得定向自组装光刻长程有序层状结构，研究人员进行了耗散粒子动力学（DPD）模拟研究。二嵌段共聚物的自组装结构（DBCS）取决于不同块的长度和它们溶解度参数的差。在 DPD 模拟中，DBCS 由粗颗粒形成，溶解度参数差是由斥力参数表示。研究人员研究了使用一个沟槽模型系统密闭的 DBCS 相分离形态。DBC 颗粒层状结构组装的斥力参数从六种类型的参数中进行选择。所述层状结构的取向是由所描述的颗粒和系统壁垒之间的斥力的排斥参数控制。研究人员改变了沟槽的宽度，并研究了层状结构的生成率，发现层状结构可以不可以通过增加宽度来获得。为了提高生成率，研究人员在底壁的中心安置一个脊，同时发现，脊的存在增加了长距离有序层状结构的形成概率。

相关研究发表于“MOLECULAR SIMULATION 卷: 41 期: 18 页: 1459-1465”题目： Study of the stability of long-range-ordered lamellar structures for directed self-assembly lithography, performed using dissipative particle dynamics（DEC 12 2015）

张迪摘译自：

http://apps.webofknowledge.com/full_record.do?product=WOS&search_mode=GeneralSearch&qid=3&SID=3AxxFcEXrEmBukeTVBs&page=1&doc=1

利用浸没式光刻生成定向自组装（DSA）图形外延模板

研究人员提出了一种利用浸没式光刻和图形外延定向自组装（DSA）制备次分辨率接触模板的最优化方法。研究人员展示了 DSA 利用 Monte Carlo 模拟的双重 60nm 间距触点的设计流程。研究人员引入模板错误增强因子（TEEF）的概念来衡量 DSA 印刷的敏感度，并评估了利用 TEEF 指标优化设计的模板。最终数据表明，利用 193i，SMO 能够使 DSA 图案实现亚 80nm 的非 L0 间距。

相关研究发表于“ALTERNATIVE LITHOGRAPHIC TECHNOLOGIES VII 卷: 9423” 题目：Directed Self-Assembly (DSA) Grapho-Epitaxy Template Generation with Immersion Lithography（2015）

张迪摘译自：

http://apps.webofknowledge.com/full_record.do?product=WOS&search_mode=GeneralSearch&qid=3&SID=3AxxFcEXrEmBukeTVBs&page=1&doc=10

逆 DSA 和反向光刻：用于定向自组装光刻掩模优化

在定向自组装光刻（DSAL）中，掩模包含的引导图案（GPs），是通过光学光刻在晶片上形成的，然后晶片通过 DSA 过程形成图案接触。DSAL 的掩模设计，则和上述方法相反，包括两个主要步骤：逆 DSA 和反向光刻。对于逆 DSA，研究人员逐步完善 GPs，直到形成尽可能接近的目标接触，GP 被定义为一些几何参数的函数，接触对参数的敏感度也得到计算，从而引导 GP 加以改进。对于反向光刻，掩模逐步细化，使目标 GPs 产生。掩模是通过像素值和他们的梯度引导实现精确的。有很多算法来进行梯度计算，研究人员选择了一个近似算法。逆 DSA 和反向光刻被扩展到处理过程变化。研究人员修改基本反向光刻

使得掩模变得对光刻变化不太敏感；基本逆 DSA 也被修改，使得它提供敏感性可以检查的方法。

相关研究发表在“2016 21st Asia and South Pacific Design Automation Conference (ASP-DAC) Page(s):83 - 88 ”题目：Mask optimization for directed self-assembly lithography: Inverse DSA and inverse lithography（25-28 Jan. 2016）

张迪摘译自：

http://ieeexplore.ieee.org/xpl/articleDetails.jsp?arnumber=7427993&action=search&sortType=&rowsPerPage=&searchField=Search_All&matchBoolean=true&queryText=(%22Document%20Title%22:directed%20self-assembly%20lithography)&ranges=2015_2017_Year

定向自组装光刻（DSAL）的物理设计和掩模优化

在 DSAL 中，接触孔由引导图案（GPs）间接形成。因此，GPs 的完整性是非常重要的，特别是当 GP 形状大而复杂的时候。尤其如此。在物理设计阶段，GP 形状的限制需要仔细考虑。在掩模优化方面，综合 GP 的理想形状和验证合成的 GP 是否正确都是很重要又困难的问题。对于物理设计和掩模优化方面的一些挑战，研究人员给出了可能的一些解决方案。

相关研究发表在“2015 IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC) Page(s):80 – 85” 题目：Physical design and mask optimization for directed self-assembly lithography (DSAL)（5-7 Oct. 2015）

张迪摘译自：

http://ieeexplore.ieee.org/xpl/articleDetails.jsp?arnumber=7314396&action=search&sortType=&rowsPerPage=&searchField=Search_All&matchBoolean=true&queryText=(%22Document%20Title%22:directed%20self-assembly%20lithography)&ranges=2015_2017_Year

利用纳米压印光刻在纳米图案 POSS 基板上形成大面积定向自组装聚苯乙烯-嵌段-聚二甲基硅氧烷嵌段共聚物软图外延

Polyhedral oligomeric silsequioxane（POSS）衍生物已成功用于嵌段共聚物(BCPs)外延定向自组装（DSA）基板。用于纳米压印光刻（NIL）的调整表面化学的定制 POSS 材料可以形成尺寸与 BCP 块长度相称的地形图案基板。聚苯乙烯-嵌段-聚二甲基硅氧烷（PS-B-PDMS）的 BCP 是由苯乙烯和六甲基顺序的活性阴离子聚合来合成。图案化的 POSS 材料为 DSA 提供了一个表面化学和地形。PDMS 柱体衬底平面的取向可以通过选择沟槽壁内的 POSS 材料来控制。BCP 图案被成功地用在晶片上，从而使蚀刻掩模的图案转移到下面的硅衬底。这种软制图外延法在新式光刻装置的质量保障方面产生了理想的效果，并且可以同时适用于硬和软衬底。该方法可能有几个应用，包括设备和互连制造，纳米压印光刻印章制作，纳米流体装置，实验室晶片上，或在需要简单纳米尺寸图案的其他技术应用。

文章题目：Soft Graphoepitaxy for Large Area Directed Self-Assembly of Polystyrene-block-Poly(dimethylsiloxane) Block Copolymer on Nanopatterned POSS Substrates Fabricated by Nanoimprint Lithography

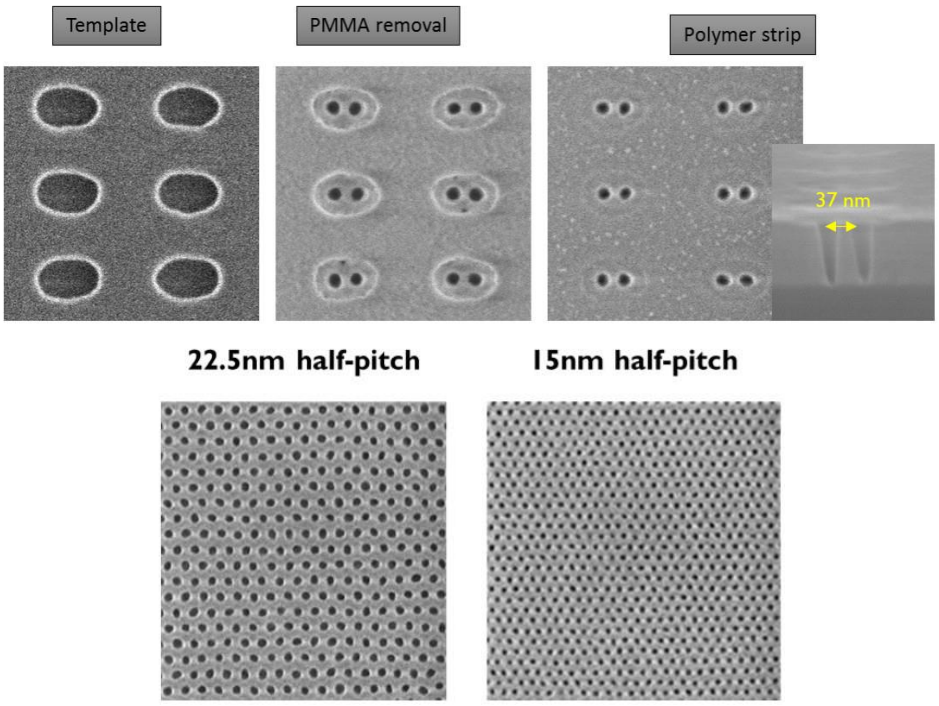
张迪摘译自：

http://onlinelibrary.wiley.com/doi/10.1002/adfm.201500100/full

应用实施

IMEC 宣布突破性技术：193nm 沉浸式光刻技术延伸至 7nm

在 2015 年举办的 SPIE 先进光刻技术会议上，比利时微电子研究中心 IMEC 提交了一份关于定向自组装（Directed self-assembly，DSA）工艺开的突破性成果。这是 IMEC 同 Tokyo Electron 和 Merck 共同合作开发出的，通过一年的努力，有效地改善了 DSA 缺陷，并使其接近个位数值。



王阳 编译自：

Imec Reports Breakthrough Results on Directed Self-Assembly at SPIE Advanced Lithography 2015

中科院自主研制新型紫外纳米压印光刻机

中科院光电技术研究所微电子专用设备研发团队已自主研制出一种新型紫外纳米压印光刻机，其成本仅为国外同类设备 1/3，将有力推进我国芯片加工等

微纳级结构器件制造水平迈上新的台阶。

光刻机是微纳图形加工的专用高端设备。光电所微电子装备总体研究室主任胡松介绍，这套设备采用新型纳米对准技术，将原光刻设备的对准精度由亚微米量级提升至纳米量级。“对准是光刻设备三大核心指标之一，是实现功能化器件加工的关键。”胡松表示，在国家自然基金的连续资助下，光电所研究团队完成了基于莫尔条纹的高精度对准技术自主研发，取得专利20余项。该技术在光刻机中的成功应用，突破了现有纳米尺度结构加工的瓶颈问题，为高精度纳米器件的加工提供了技术保障，未来可广泛应用于微纳流控芯片加工、微纳光学元件、微纳光栅等微纳结构器件的制备，目前该设备已完成初试和小批生产。

产品技术特征：

- 大面积一次压印；
- 自动脱模；
- 由 PLC 控制工艺过程，可实现自主定制；
- 可与接近接触式光刻机兼容；
- 友好的人机交互，触模屏操作。

产品主要技术指标：

- 分辩力： ≤15nm；
- 大功率紫外固化 UV LED；
- 样片尺寸：4 英寸（可定制）；
- 压印面积：2 英寸（可定制）；
- 模板尺寸：5 × 0.090 英寸（可定制）；
- 压印压力：0 - 25 PSI（可升级到 100 PSI）；
- 产量：＜5 分钟/片；
- 使用方便：Step-by-step Menu；
- 应用领域广泛。

王阳 选摘自：

【科技日报】紫外纳米压印光刻机提升我国微纳级制造业能力

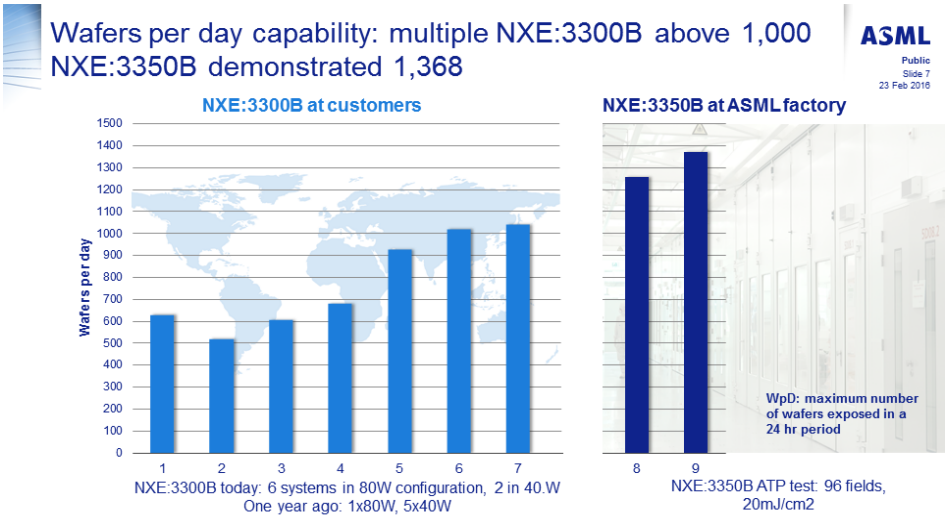
http://www.ioe.ac.cn/xwdt/kydt/201604/t20160407_4579811.html

产品信息

http://www.ioe.cas.cn/kycg/gkjcp/201204/t20120420_3559842.html

7nm 工艺关键设备 EUV 光刻机产能提升

荷兰 ASML 及 TSMC 台积电宣布他们的原型机上测试了 85W 光源，之后很快会提升到 125W。ASML 之前演示过 185W 光源的 EUV 光刻机，并许诺年底前会进一步提高到 250W。



现在的 EUV 光刻机可靠性已经提高到了有 70%的工作时间，每天可以处理 500-600 个晶圆，相比去年的情况已经有很大改善，但这远远不够量产水平。ASML 公司 EUV 项目总监 Frits van Hout 表示现在距离 EUV 应该达到的水平还有 2-3 步。现在出货的 EUV 光刻机会升级，预计今年底达到应有的水平。

芯片制造商预计会在 2018 年使用 EUV 工艺生产芯片，届时 ASML 的 EUV 光刻机有助于降低 7nm 工艺的成本。

虽然 EUV 工艺确实实现了预定目标，但由于产能和可靠性的问题，该项目已经多次延期，到了 5nm 及 3nm 节点，EUV 可能还需要一次升级。ASML 正为

此与相关方讨论具体的配置和时间细节。

值得一提的是，目前在 EUV 工艺上，TSMC 比 Intel 要积极得多，此前 TSMC 就表示会在 10nm 工艺上使用 EUV 工艺，而 Intel 表示过就算没有 EUV 工艺，他们也懂得如何制造芯片。不过如果 EUV 工艺真的能如期量产，Intel 也会在 7nm 节点上启用 EUV 工艺。

王阳选摘自：

7nm 工艺关键设备 EUV 光刻机产能提升

http://www.pcpop.com/doc/1/1890/1890676.shtml

ASML 携手台积电锁定 5 纳米 EUV 世代

尽管市场上对于晶圆代工龙头台积电第 2 季之财测不甚满意，不过长期来看，台积电仍在先进製程上成为业界领航员角色，半导体设备龙头 ASML 预计第 2 季将出现营收高成长，主因系浸润式机台可量产 10 奈米，DUV 机台已经在第 1 季出货 6 台，而未来 EUV 机台更可望携手台积电等业者锁定 5 奈米等更先进製程。

据了解，EUV 机台已经出货给台积电，准备迎接下一世代的 5 奈米先进製程。不过，近期的主力产品仍是预计 2016 年第 1 季量产的 10 奈米製程，而市场也传出，业界最重视的是 7 奈米部分，10 奈米约略是过渡性的阶段任务角色。而 ASML 所提供之浸润式微影系统成为几大半导体业者的强力支柱。

据 ASML 日前公布之 2016 年第 1 季营收，约达 13.3 亿欧元，毛利率约达 42.6%，估计 2016 年第 2 季营收淨额约为 17 亿欧元，毛利率则小减至 42%。而 2016 年第 1 季下单未出货金额部分约 30.18 亿欧元，相较 2015 年的 31.84 亿欧元小幅缩减。

ASML 于 2016 年第 1 季推出最新的浸润式微影系统 TWINSCAN NXT:1980，以及新一代量测系统 YieldStar 350E，并强调在 EUV 极紫外光微影技术的发展上也持续进展。据表示，过去 3 个月 ASML EUV 系统的生产力和妥善率方面提

升，未来客户也会陆续导入製程。

ASML 深紫外光(DUV)最新型浸润式机台 NXT:1980 在第 1 季完成 6 台出货，并将生产力拉升到每天 4,000 片晶圆的水准。全方位微影优化方案(Holistic)则从本季开始推出最新一代的整合式量测系统 YieldStar 350E。

- **TWINSCAN NXT:1980Di 产品参数**

透镜	Wavelength	193 nm
	NA	0.85–1.35 (variable)
	Resolution	≤ 38 nm (single exposure)
	Field size, for reticle with pellicle	
	Max X	26.0 mm
	Max Y	33.0 mm
套刻精度	Single-machine (dedicated chuck)	≤ 1.6 nm full wafer coverage
	Matched-machine (to reference wafer)	≤ 2.5 nm full wafer coverage
生产量	30 mJ/cm^2 exposure dose	
	300-mm wafers, 96 shots	≥ 275 wph

ASML 表示，极紫外光(EUV)产品目标是在 2016 年持续强化 EUV 系统的生产力和妥善率，并计画在 2016 年将机台生产力提升到每天曝光 1,500 片晶圆。第 1 季 EUV 系统即展现每天可达到曝光 1,350 片晶圆水准。

王阳 选摘自：

ASML EUV 机台陆续出货 携手台积电锁定 5 纳米世代

http://laoyaoba.com/ss6/html/95/n-598395.html

TWINSCAN NXT:1980Di 产品信息

https://www.asml.com/asml/show.do?lang=en&ctx=46772&dfp_product_id=10567

《集微技术信息简报》

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