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Performance Enhancement Technologies in III-V/Ge MOSFETs

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CMOS utilizing high mobility III-V/Ge channels on Si substrates is expected to be one of the promising devices for high performance and low power advanced LSIs in the future, because of the enhanced carrier transport properties. However, the device/process/ integration technologies of Ge/III-V n- and pMOSFETs for satisfying requirements of future node MOSFETs have not been established yet. In this paper, we address gate stack and channel engineering for enhancing the MOSFET performance with emphasis on thin EOT and ultrathin body, which are mandatory in the future nodes. As for Ge MOSFETs, GeO_x/Ge interfaces formed by plasma post oxidation are shown to realize thin EOT, low D_{it} and high mobility. By using these $HfO_2/Al_2O_3/GeO_x$/Ge gate stacks, Ge n- and p-MOSFETs with EOT of 0. 76 nm have been demonstrated with high electron (690 cm^2/Vs) and hole (550 cm^2/Vs) mobility. As for III-V MOSFETs, ultrathin InAs channels with MOS interface buffer layers are shown to provide high electron mobility for an InAs thickness of 3 nm. By utilizing this channel engineering, 55 nm-L_{ch} quantum well channel InAs-OI n-MOSFETs have been demonstrated with superior short channel effect immunity and fairly high on current.

Introduction

CMOS utilizing high mobility Ge/III-V channels on Si substrates is expected to be one of the promising devices for high performance and low power advanced LSIs in the future [1, 2]. Here, several CMOS structures using III-V/Ge channels can be used. One of the ultimate CMOS can be the co-integration of a III-V nMOSFET and a Ge pMOSFET [1-4]. While Ge or III-V CMOS is also plausible in terms of the simplicity of the process/material integration, the key issues are the realization of high performance III-V pMOSFETs or Ge nMOSFETs. Thus, viable CMOS structures using III-V and/or Ge channels are still strongly dependent on coming progress in the device/process/integration technologies of Ge/III-V n- and pMOSFETs. Also, even in Ge pMOSFETs and III-V nMOSFETs, intensively studied so far, the CMOS technologies for satisfying the requirements of future node MOSFETs have not been established yet. In this paper, we address gate-stack and channel engineering for enhancing the MOSFET performance with emphasis on thin EOT and ultrathin body, which are mandatory in the future nodes.

Ge MOSFET Improvement

The realization of superior Ge MOS interfaces is mandatory for yielding high mobility in inversion layers of Ge MOSFETs. Among a variety of gate insulators and/or interface

control layers on Ge, attention has recently been paid to GeO_2/Ge interfaces, because of the superior interface properties and resulting high carrier mobility in Ge MOSFETs [7-30]. Particularly, high electron mobility can be obtained only for Ge n-MOSFETs with GeO_2/Ge interfaces [14-20, 22, 24, 26-30]. The GeO_2/Ge interfaces with a quite low interface state density can be realized by direct thermal oxidation of Ge substrates [11, 13]. The interface state density systematically decreases as the oxidation temperature increases. As for the capacitors oxidized at 575 ºC, we obtained a minimum D_{it} value of 1.1×10^{11} $eV^{-1}cm^{-2}$ measured in the range from the valence band edge (E_v) to midgap and 9×10^{10} $eV^{-1}cm^{-2}$ measured in the range from the conduction band edge (E_c) to midgap without any interface passivation annealing. Judging from the energy distribution, a minimum value near midgap is expected to be lower than these results. These D_{it} values are quite low values for Ge MOS interfaces. These superior interface properties of the GeO_2/Ge interfaces are expected to lead to higher channel mobility. Thus, we have fabricated p- [19, 25] and n-channel [14, 17] MOSFETs with thick GeO_2/Ge interfaces, formed by thermal oxidation. As a result, we have obtained high electron and hole mobility values of 1020 and 575 cm^2/Vs, respectively [17, 19].

While recent studies [7, 8, 16, 18, 20, 21] have also revealed that Ge oxide interfacial layers (IL) with high k can provide superior MOS interfaces with low D_{it}, thinning EOT is still challenging. In order to realize low D_{it} and thin EOT at the same time, we have proposed a novel IL formation process employing ECR oxygen plasma to form GeO_x ILs after thin Al_2O_3 ALD [22-26]. In this plasma post-oxidation method, a thin GeO_x IL is formed by oxidizing a Ge surface beneath a thin ALD Al_2O_3 layer using ECR oxygen plasma exposure. The Al_2O_3 layer serves as a sufficient oxygen barrier that suppresses the growth of unnecessarily thick GeO_x IL, thanks to its intrinsic oxygen permeability. Also, the Al_2O_3 layer effectively prevents Ge surfaces from receiving the direct exposure of ECR oxygen plasma and any damage during the fabrication processes. In addition, low processing temperature in the ECR plasma oxidation is expected to sufficiently suppress any thermal degradation of the GeO_x/Ge interface.

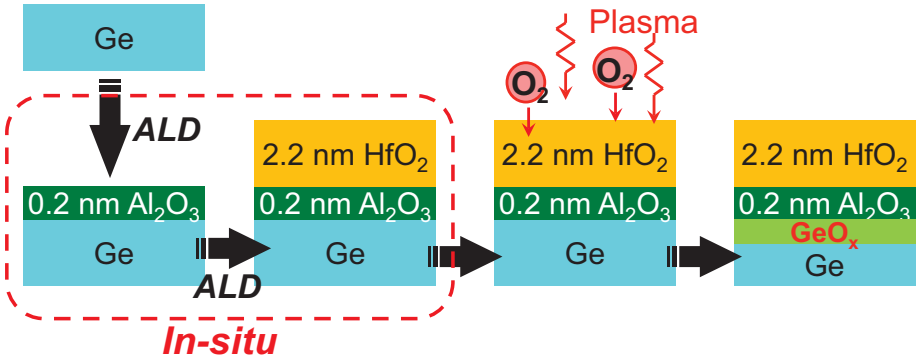

Fig. 1. Proposed GeO_x IL formation process by using ECR oxygen plasma oxidation through ALD HfO_2/Al_2O_3.

Also, we have recently demonstrated a revised version of gate insulator formation using ALD HfO_2/Al_2O_3 stacks for further reducing EOT [27-31]. While the Al_2O_3/GeO_x/Ge gate stacks can realize the superior interfaces, the low permittivity of Al_2O_3 poses a limitation on thinning EOT around 1 nm, meaning the necessity of HfO_2 for further scaling EOT. Here, the plasma post-oxidation is applied to ALD

$HfO_2/Al_2O_3/Ge$ structures. It should be noted here that plasma oxidation of HfO_2/Ge direct stacks provides inferior MOS interface properties with high D_{it}, because of the inter-mixing of HfO_2 and GeO_x. Thus, the insertion of ultrathin Al_2O_3 films is needed as an inter-diffusion control layer (DCL). The basic process flow is shown in Fig. 1. This ultrathin GeO_x IL is found to effectively reduce D_{it}, as shown in Fig. 2(a). Fig. 2(b) shows D_{it} at E_i-0.2 eV as a function of EOT of $HfO_2/Al_2O_3/Ge$ and Al_2O_3/Ge MOS interfaces with and without GeO_x formed by plasma post oxidation. As a consequence, EOT of the $HfO_2/Al_2O_3/GeO_x/Ge$ gate stacks is scaled down to 0.7~0.8 nm with maintaining D_{it} around 10^{11} $cm^{-2}eV^{-1}$ level.

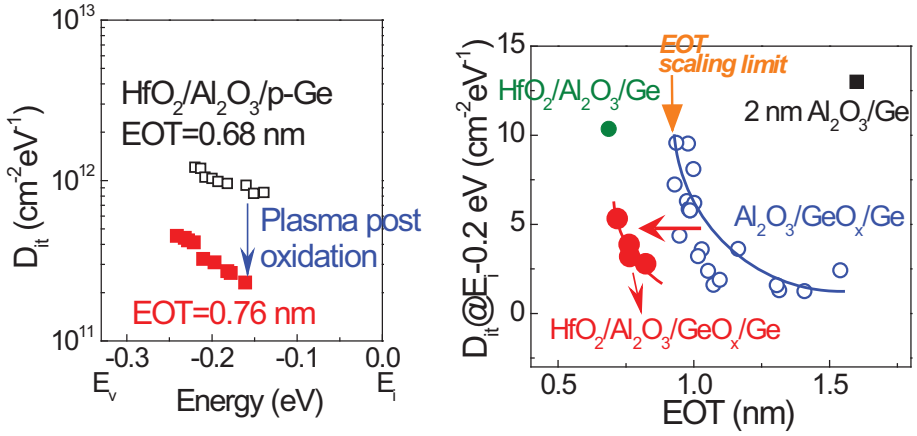

Fig. 2. (a) Energy distribution of D_{it} before and after post plasma oxidation for $HfO_2/Al_2O_3/Ge$ interfaces. (b) D_{it} at E_i-0.2 eV as a function of EOT of $HfO_2/Al_2O_3/Ge$ and Al_2O_3/Ge MOS interfaces with and without GeO_x formed by plasma post oxidation.

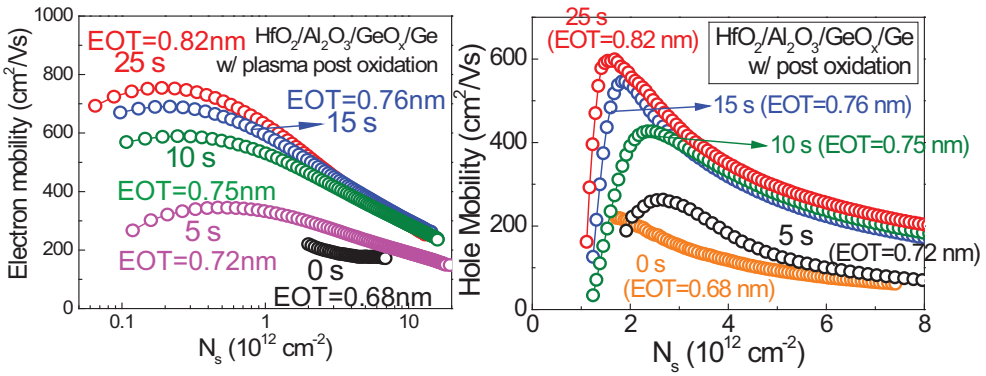

Fig. 3. (a) Electron and (b) hole mobility of the Ge n- and p-MOSFETs with the HfO_2 (2.2 nm)/Al_2O_3 (0.2 nm)/GeO_x/Ge gate stacks as a parameter of the interfacial GeO_x thickness.

As a result, n- and p-MOSFETs with $HfO_2/Al_2O_3/GeO_x/Ge$ gate stacks exhibit excellent electrical characteristics under EOT of 0.76 nm. This is the first report of Ge n-MOSFETs with EOT less than 1 nm (the thinnest EOT of 0.72 nm). Fig. 3(a) and (b) shows the electron and hole mobility of the Ge n- and p-MOSFETs, respectively, with HfO_2 (2.2 nm)/Al_2O_3 (0.2 nm)/GeO_x/Ge gate stacks as a parameter of the interfacial GeO_x thickness. The Ge p- and n-MOSFETs with HfO_2 (2.2 nm)/Ge and HfO_2 (2.2 nm)/Al_2O_3 (0.2 nm)/Ge gate stacks show relatively low hole and electron mobility, which

is attributed to the poor qualities of direct HfO_2/Ge and Al_2O_3/Ge MOS interfaces. It is found, on the other hand, that the insertion of interfacial GeO_x and the increase in the thickness significantly enhance the effective mobility. The HfO_2 (2.2 nm)/Al_2O_3 (0.2 nm) /GeO_x/Ge Ge p- and n-MOSFETs exhibit significantly enhanced mobility, attributed to sufficient passivation of Ge MOS interfaces by the GeO_x ILs. The electron mobility in the $HfO_2/Al_2O_3/GeO_x$/Ge n-MOSFET is comparable to the Si universal electron mobility and approaching the ~20-nm-thick thermal oxidation GeO_2/Ge n-MOSFET [29, 30]. The hole mobility is much higher than the Si universal one and even higher than that in the thick thermal oxidation GeO_2/Ge p-MOSFETs is obtained for the $HfO_2/Al_2O_3/GeO_x$/Ge p-MOSFET [27, 29, 30].

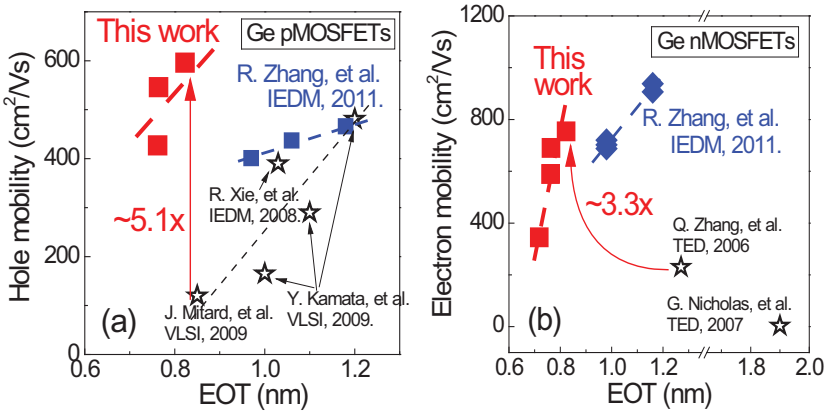

Fig. 4. Peak hole (a) and electron (b) mobility of the Ge p and n-MOSFETs with $HfO_2/Al_2O_3/GeO_x$/Ge gate stacks vs. EOT, compared with the Ge MOSFETs with Al_2O_3/GeO_x/Ge gate stacks and the data reported in other previous studies.

The present and reported data [32-36] of the peak hole and electron mobility of Ge p- and n-MOSFETs with EOT of around 1 nm are summarized as a function of EOT in Fig. 4 (a) and (b), respectively. A clear decrease of both the electron and the hole mobility with a decrease in EOT is observed for the values already reported, attributable to the significant degradation of the Ge MOS interfaces. In the Al_2O_3/GeO_x gate stacks fabricated by the plasma post-oxidation method, the degradation of mobility with decreasing EOT is found to be effectively suppressed because of the sufficient passivation of Ge MOS interfaces even in the ultrathin EOT region. However, the EOT scaling is not available beyond 1 nm because of the insufficient permittivity of Al_2O_3. In the present $HfO_2/Al_2O_3/GeO_x$/Ge gate stacks, thanks to the higher permittivity of HfO_2 than Al_2O_3 and the successful formation of GeO_x/Ge MOS interfaces by employing the plasma post oxidation method and thin Al_2O_3 DCL, further EOT scaling is realized while maintaining the low D_{it} Ge MOS interfaces, resulting in the significant improvement of the peak mobility of Ge p- and n-MOSFETs. The peak mobility in the Ge p-MOSFET with EOT of 0.82 nm has been enhanced by 5.1 times over the previously-reported results [33] with similar EOT. On the other hand, since there is no previous data of Ge n-MOSFETs with EOT thinner than 1.3 nm, we cannot compare the peak mobility with the previous results. Even when comparing with the previous data with EOT of 1.3 nm [35], the peak mobility in the Ge n-MOSFET with EOT of 0.82 nm has been enhanced by 3.3 times. A much higher enhancement factor is expected in comparison with the peak mobility of Ge n-MOSFETs with any other MOS interfaces under the same EOT, because the mobility generally tends to decrease with reducing EOT.

III-V MOSFET Improvement

The MOS interface control is more critical for III-V semiconductors than for Ge in terms of obtaining higher effective mobility in MOS channels, because it is well known that MOS interfaces between III-V materials and gate insulators include a large number of interface states and interface defects. Thus, the realization of high quality MOS gate stacks on III-V is of paramount importance. One recent important discovery in III-V MOS interface control is the effectiveness of ALD Al_2O_3 [37-43] on suppression of interface defects. Also, it has been reported that sulfur (S) passivation [44-46] can improve the Al_2O_3/InGaAs MOS interface properties. We have found that the S passivation, obtained by immersing InGaAs epitaxial surfaces into $(NH_4)_2S$ solutions, can also improve the effective electron mobility in InGaAs n-MOSFETs [46]. It has been found that μ_{eff} can be improved by using the (111)A surface and the $(NH_4)_2S$ treatment, though the physical origin of this mobility improvement has not been fully understood yet.

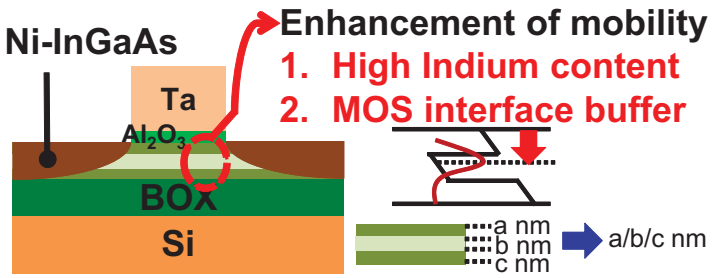

Fig. 5. Schematic image of the device structure and channel engineering for $In_xGa_{1-x}As$-OI MOSFETs.

Another critical factor for the electron mobility reduction in InGaAs MOSFETs is the influence of the ultrathin body channels, which are mandatory for short channel MOSFETs. It has been reported that ultrathin Si channels severely reduce the channel mobility, because of increased body thickness fluctuation scattering [47, 48]. It is also found for III-V MOSFETs that, when the body thickness, T_{body}, is less than 10 nm, the mobility significantly decreases with a decrease in T_{body}, which is consistent with the expectation in the mobility limited by body thickness fluctuation scattering [49-52]. Therefore, we have introduced two kinds of channel engineering [53-56]. Fig. 5 shows the schematic image of the device structure and channel engineering for $In_xGa_{1-x}As$-OI MOSFETs. One is the higher In content (InAs) channels and the other is the insertion of a MOS interface buffer layer at both the bottom and the top of a channel layer using InGaAs with a low In content, which has a higher band gap than that of the channel InGaAs, to distance the channel carriers from the MOS interface. The lower-In-content MOS buffer layers are expected to reduce MOS interface Coulomb scattering. In addition, the thickness fluctuation of the high-In content channel layers can be mitigated, because both the lower- and higher-In content InGaAs channels are epitaxially grown successively, while the thickness of the single layer InGaAs-OI channels are formed by etching processes during direct wafer bonding (DWB). Also, higher In content (InAs) channels are expected to provide higher phonon-limited mobility.

In order to realize this device structure, $In_xGa_{1-x}As$-OI structures on Si were fabricated by DWB. The process details are shown in [49]. Also, MOSFETs with Ni-InGaAs metal source/drain (S/D) were fabricated on the $In_xGa_{1-x}As$-OI substrates. The III-V-OI wafers were cleaned by acetone, 9.5 % NH_4OH, and 0.6 % $(NH_4)_2S$ solutions for 1, 1, and 10 min, respectively. Then, 10-nm-thick Al_2O_3 was deposited at 200 °C by ALD using $Al(CH_3)_3$ and H_2O as the liquid sources. Subsequently, Ta gate deposition by sputtering and gate patterning were carried out. Post-metal-annealing was carried out at 350 ºC for 10 sec in N_2 ambient. After that, 20 nm Ni for S/D was deposited by electron beam evaporation with lift off process and rapid-thermal-annealing was carried out at 250 ºC in N_2 ambient to form the Ni-InGaAs S/D regions. Next, unreacted Ni was removed by a 6 % HCl solution with high etching selectivity between Ni and the formed Ni-InGaAs alloy. Finally, Al for pad electrodes and back contact were evaporated.

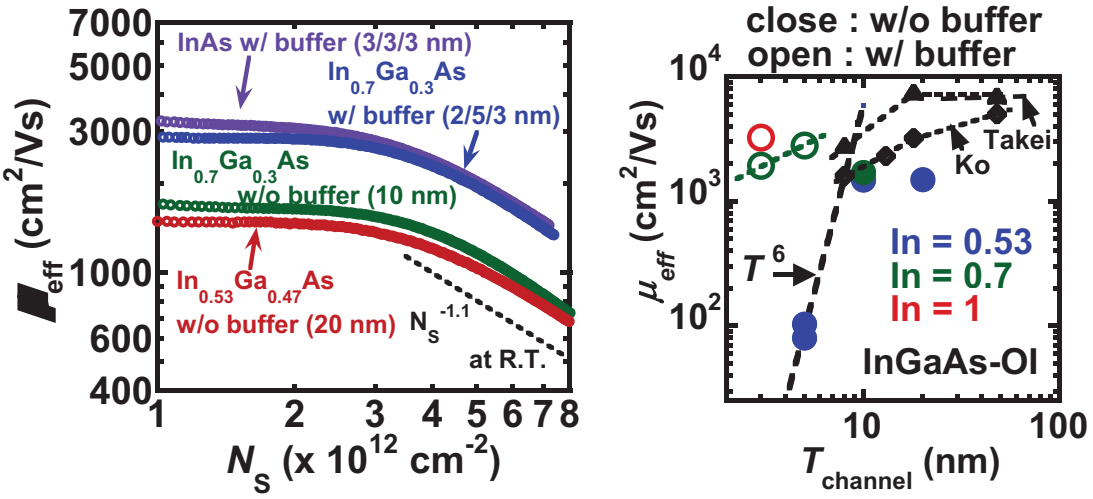

Fig. 6. (a) N_s dependence of effective electron mobility at room temperature for InGaAs-based ultrathin body MOSFETs. (b) Comparison of the effective electron mobility of $In_xGa_{1-x}As$-OI MOSFETs with that of other studies on InAs-OI MOSFETs [50, 52] as a function of $T_{channel}$.

The effective electron mobility (μ_{eff}) characteristics of $In_xGa_{1-x}As$-OI MOSFETs with a T_{body} between 10-20 nm at room temperature (R.T.) are shown in Fig. 6(a). It is found that the $In_xGa_{1-x}As$ channels with higher In content show higher μ_{eff} even though the higher In content channel has thinner T_{body}. Also, MOSFETs with a buffer layer shows higher μ_{eff}. The InAs-OI MOSFETs with $T_{channel}$ of 3 nm exhibit high peak mobility of 3180 cm^2/Vs. Fig. 6(b) shows the comparison in μ_{eff} of $In_xGa_{1-x}As$ MOSFETs with that of other studies as a function of $T_{channel}$. The data from the other studies of InAs-OI MOSFETs [50, 52] are also shown. It is found that μ_{eff} of InGaAs-OI MOSFETs in this work is higher than the previous data taken from the other studies exploring ETB InAs MOSFETs [50-52], attributable to the existence of the MOS interface buffer layer.

By utilizing this device structure, we have also demonstrated operation of 55-nm-L_{ch} MOSFETs on Si [55, 57]. In order to realize short channel devices, EB lithography of the gate electrode patterning and Ni encroachment were employed. In Ni-InGaAs metal S/D formation, Ni diffused toward the lateral direction of the channels by a diffusion length of

around 50 nm during 1 min. RTA. This encroachment allows us to fabricate the deeply-scaled MOSFETs under the several hundred nm gate patterns. The cross-sectional transmission electron microscope (TEM) images of a fabricated MOSFET with the buffer layer (3/3/3 nm) are shown in Fig. 7. It can be seen that ETB InAs-OI MOSFETs were fabricated on a Si substrate with the metal S/D structures. The large area TEM image shows that the formed InGaAs-OI and the buried oxide (BOX) layer have good uniformity. The laterally-diffused Ni-InGaAs layer was observed and, as a result, the effective L_{ch} was estimated to be 55 nm with a defined gate length of 160 nm.

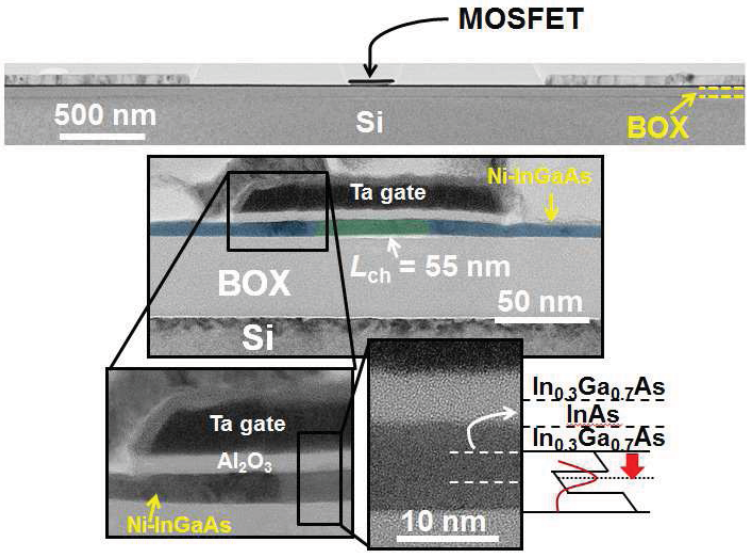

Fig. 7. Cross-sectional TEM images of the fabricated InAs-OI MOSFETs with L_{ch} of 55 nm and T_{body} of 3/3/3 nm.

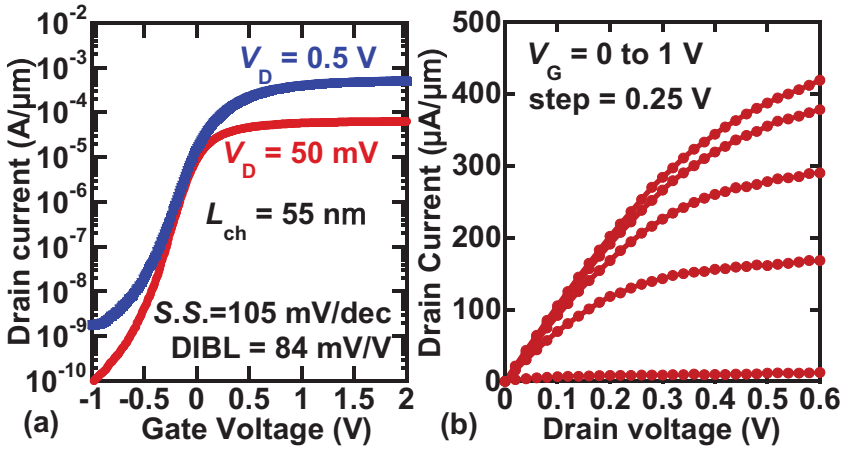

Fig. 8. (a) I_D-V_G and (b) I_D-V_D characteristics of InAs-OI MOSFETs with T_{body} of 3/3/3 nm and T_{ox} = 6 nm.

The I_D-V_G and I_D-V_D characteristics of the InAs-OI MOSFET with L_{ch} of 55 nm, T_{body} of 3/3/3 nm and Al_2O_3 gate dielectric thickness (T_{ox}) of 6 nm are shown in Figs. 8(a) and 8(b), respectively. The device shows good transfer and output characteristics with small DIBL in spite of quite thick EOT of around 3.5 nm. High I_{on} of 278 μA/μm is obtained at

V_{dd} of 0.5 V. This I_{on} value of the present device is comparable to that of the Tri-gate MOSFETs [58-62], reported so far, in spite of the ETB planar structure. This result demonstrates the operation of ETB InAs-OI MOSFETs on Si substrates with a L_{ch} region of sub-100 nm. Figs. 9(a) and 9(b) show the *S.S.* and DIBL benchmark comparing those of the present InGaAs-OI MOSFETs with the recent results of the III-V 3-D FETs [58-62]. The present $In_xGa_{1-x}As$-OI MOSFETs show comparable or better electrostatic characteristics against the 3-D Tri-gate FET or gate-all-around (GAA) FETs [58-62], even though quite thick EOT and the planar structure have been used.

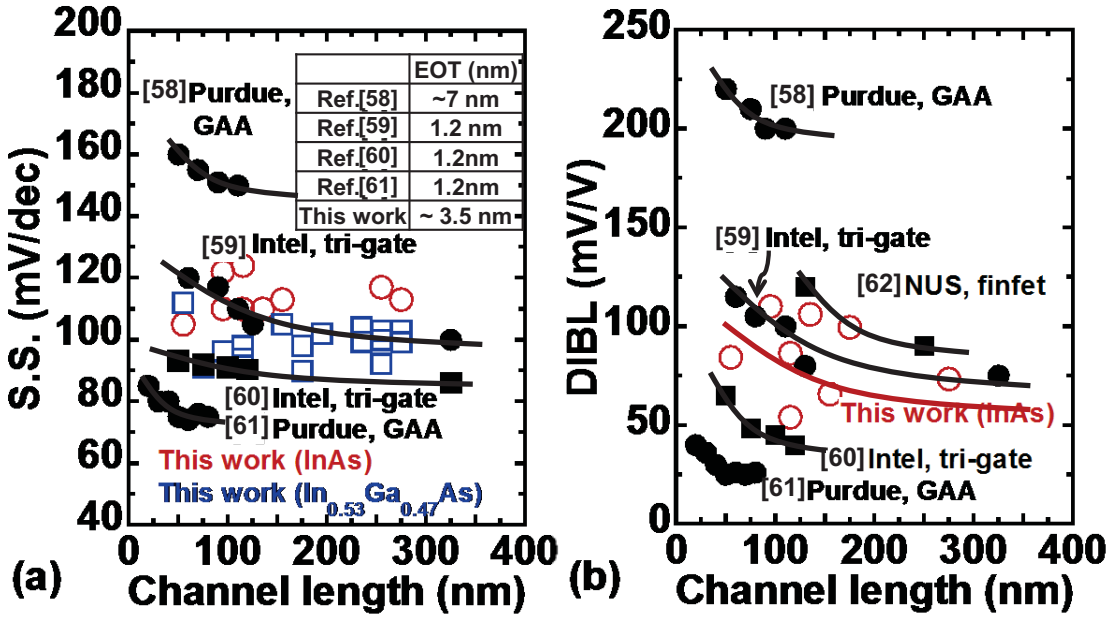

Fig. 9. Benchmark of (a) S.S. and (b) DIBL characteristics between several 3-D FETs and the present devices.

However, the above devices still suffered from fairly high parasitic resistance due to high contact resistance between contact metals and Ni-InGaAs. Recently, we present 20-nm-channel length (L_{ch}) high performance InAs-on-insulator (-OI) MOSFETs on Si substrates with Ni-InGaAs metal source/drain (S/D) employing a new contact resistance reduction technology [63]. These devices provide high maximum I_{on} and maximum transconductance (G_m) of 2.38 mA/μm and 1.95 mS/μm at V_D of 0.5 V. This high performance is attributable to the low S/D parasitic resistance, which was realized by a cleaning process of Ni-InGaAs surfaces before pad electrode deposition as well as increase in In content in the channel layer. Furthermore, it has been found that the interface resistance between Ni-InGaAs and InGaAs channels can be reduced down to 50 Ω·μm by increasing In content in the channel layers.

Conclusions

In this paper, we address key issues to enhance the performance of III-V/Ge MOSFETs. As for Ge MOSFETs, the formation of the superior gate stacks is a key issue. It was shown that ECR plasma post oxidation through HfO_2/Al_2O_3 is quite effective in realizing Ge gate stacks with EOT less than 1 nm with low D_{it} and resulting high electron

and hole mobility in Ge MOSFETs. Record high mobility Ge n- and p-MOSFETs with EOT of 0. 76 nm have been demonstrated by using $HfO_2/Al_2O_3/GeO_x$/Ge gate stacks. As for InGaAs MOSFETs, the channel structure engineering for mitigating the mobility reduction mechanisms such as channel thickness fluctuation scattering and MOS interface Coulomb scattering is a key issue. We have proposed MOS interface buffer quantum well channels by using InGaAs/InAs/InGaAs-On-Insulator structures. It was shown that significant electron mobility enhancement is observed down to 3 nm of InAs channels. By utilizing this engineering, we have realized 55-nm-L_g InGaAs-OI MOSFETs with Ni-InGaAs S/D on Si substrates, realized by direct wafer bonding between InGaAs and Si substrates with ultrathin Al_2O_3 buried oxides (BOX). The superior short channel immunity and fairly high I_{on} have been obtained.

Acknowledgments

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