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A high speed 1000 fps CMOS image sensor with low noise global shutter pixels

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Abstract A low read noise 8T global shutter pixel for high speed CMOS image sensor is proposed in this paper. The pixel has a pixel level sample-and-hold circuit and an in-pixel amplifier whose gain is larger than one. Using pixel level sample-and-hold circuit, the KTC noise on FD node can be effectively cancelled by correlated double sampling operation. The in-pixel amplifier with a gain larger than one is employed for reducing the pixel level sample-and-hold capacitors thermal noise and their geometric size. A high speed 1000 fps 256×256 CMOS image sensor based on the pixel is implemented in 0.18 μm CMOS process. The chip active area is 5 mm × 7 mm with a pixel size of 14 μm×14 μm. The developed sensor achieves a read noise level as low as 14.8e- while attaining a high fill factor of 40%. The full well capacity can contain 30840e- and the resulting signal dynamic range is 66 dB.

Keywords global shutter, CDS, low noise, fill factor, high speed image sensor

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1 Introduction

Recently, CMOS image sensor technology has promoted the development of high speed cameras and high speed video systems. High speed CMOS image sensor can be applied widely in various fields, such as broadcast, sports and scientific research applications. To capture fast-moving object images without motion distortion, the global shutter pixel rather than the rolling shutter pixel is required in high speed CMOS image sensor, which means that all pixels are exposed at the same time. One of the challenges for high speed global shutter image sensors is how to develop a low noise pixel.

Several high speed CMOS global shutter image sensors have been reported in the recent years [1–10]. The global shutter mode function can be realized by adding an analog data memory in conventional 3T active pixel [1,2]. Because the analog data memory cannot keep both reset signal and light signal, the pixel reset noise (called KTC noise) cannot be cancelled by correlated double sampling (CDS) technique [11–13]. The large photo diode (PD) dark current further deteriorates the read noise performance of the

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pixel. Beside, this pixel has low sensitivity because photo-generated charges are integrated directly on the large PD capacitor. The capacitive transimpedance amplifier (CTIA) global shutter pixel can possibly achieve better sensitivity as the integration is done on a separate capacitor [3]. But, the CTIA high speed CMOS image sensor still does not overcome the problem of large read noise. A five-transistor (5T) global shutter pixel with pinned photo diode (PPD) was normally adopted in high speed CMOS image sensors [4–6]. The pixel has a simple device structure and a high fill factor. Though the PPD has a smaller dark current than PD, the floating diffusing (FD) node of 5T pixel plays both roles of photo-generated carrier charge-to-voltage conversion and analog memory so that the KTC noise on the node cannot be cancelled by CDS. Therefore, the 5T pixel also suffers from a large read noise. In order to reduce the read noise, an eight-transistor (8T) global shutter pixel was proposed [7]. Because a sample-and-hold circuit is integrated in pixel, this pixel KTC noise of FD node can be reduced by CDS technique. Unfortunately, to ensure a sufficiently high fill factor the sample-and-hold capacitors in the pixel have to be designed to be small. This results in large thermal noise which increases the pixel noise floor. In addition, there are two source followers in the pixel. Because the gain of the source follower is smaller than one, the sensitivity of the 8T pixel is lower. Another alternative two-stage charge transfer global shutter pixel with low read noise was implemented [8–10]. This pixel has two pinned diodes: pinned photo diode (PPD) and pinned storage diode (PSD). The photo-generated charges are generated in PPD. Then the charges are transferred and stored in PSD. Finally the charges are transferred into FD node and converted into signal voltage. Thus, the KTC noise of the FD can be cancelled by CDS circuit without additional in-pixel sample-and-hold capacitors. The read noise of this global shutter pixel is lower than the above 8T pixel. But, a sufficient potential difference between two pinned diodes must be made to transfer efficiently charges from PPD to PSD. The potential well of PSD is much deeper so that it is difficult to read out the photo-generated charges. After readout operation, some photo-generated charges may be left in PSD. These remaining photo-generated charges will induce image lag [14–16]. Moreover, since the PSD cannot be designed to be too small in order to maintain enough well capacity, the fill factor of the two-stage charge transfer global shutter pixel is normally smaller than 30%.

This paper proposes a novel global shutter pixel for high speed CMOS image sensor and deigns a high speed CMOS image sensor. The pixel is an 8T pixel with a pixel level sample-and-hold circuit and an in-pixel amplifier of larger gain than one. The KTC noise on the FD can be suppressed by CDS circuit. Two PMOS transistors form the in-pixel amplifier with a gain larger than one. The reset voltage and the signal voltage can be amplified by the amplifier before they are stored on sample-and-hold capacitors. Thus, the thermal noise of the sample-and-hold capacitors and their geometric size are drastically reduced. We can design two small capacitors as sample-and-hold capacitors to get high fill factor without sacrificing pixel read noise property. Furthermore, the sensitivity of the pixel is improved. The proposed pixel with in-pixel amplifier and sample-and-hold circuit has the advantages of low read noise and high fill factor. A 256×256 high speed CMOS image sensor is designed and fabricated in 0.18 μm CMOS process. The measurement results demonstrate that the sensor has better performance.

2 High speed image sensor design

2.1 Global shutter pixel structure

Figure 1 shows the proposed pixel structure. The pixel consists of one PPD, eight transistors and two MOS-capacitors. The transistor M_{TG} is used to transfer the photo-generated charges from PPD to FD node. M_{RST} is a reset transistor. The two PMOS transistors M_1 and M_2 constitute the in-pixel amplifier, with the gain of A ($A > 1$). When the gate of M_2 is connected to ground, this amplifier starts to work. The in-pixel sample-and-hold circuit consists of two switch transistors: M_{S1} and M_{S2}, and two capacitors: C_S and C_R. These capacitors are used to store the signal voltage and the reset voltage, respectively. The source follower transistor M_{SF} and select transistor M_{SEL} form the pixel level second readout stage.

Figure 2 shows the operation timing diagram of the pixel. First, the PPD and the FD are both reset by concurrently turning on M_{RST} and M_{TG}. M_{RST} and M_{TG} are controlled by signals RST and TG,

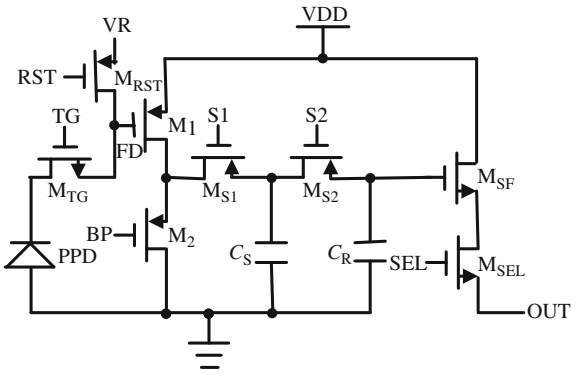

Figure 1 Structure of the proposed pixel.

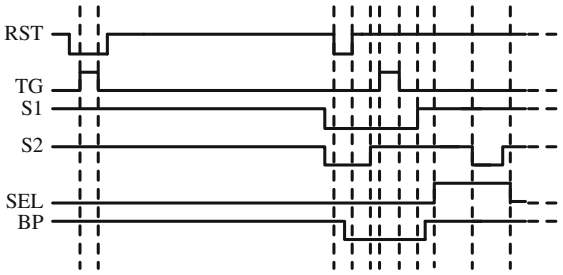

Figure 2 Timing diagram of the proposed pixel.

respectively. The photo-generated carrier charges are drained out from PPD diode junctions to form a complete depletion layer. After M_{TG} is turned off, integration of photo-generated charge in pixel starts. During the integration period, the PPD receives light and converts it into photo-generated charges. Second, after a sufficient photo-generated charge accumulation, the control signal RST turns on M_{RST} to perform the second reset of FD. After turning off M_{RST}, the reset noise is retained in the FD. Meanwhile, the switch M_{S1} and M_{S2} and the transistor M_2 are turned on by signals S1, S2 and BP, respectively. Thus, the reset voltage of FD is amplified by the in-pixel amplifier and then sampled by both C_S and C_R. Then switch M_{S2} is turned off, and the amplified reset voltage V_{CR} remains stored on C_R. Next, M_{TG} is turned on. The photo-generated charges are transferred from PPD to FD. When charge transfer process is completed, the signal TG turns off M_{TG} again and the voltage on FD becomes signal voltage. The signal voltage is amplified by in-pixel amplifier and sampled on C_S. After sampling, the amplified signal voltage V_{CS} remains stored on C_S. Then the pixel is ready for the start of the next frame integration. Furthermore, the in-pixel amplifier is shut down to reduce the pixel power consumption. Finally, the switch transistor M_{SEL} is turned on by signal SEL so that the amplified reset voltage stored on C_R is readout first. Afterwards, M_{S2} is turned on by S2 to short C_S and C_R. This operation mixes the amplified signal voltage V_{CS} with amplified reset voltage V_{CR}. Finally, the mixed voltage V_{CS+CR} is readout.

2.2 Analog signal processing circuit

Figure 3 shows the pixel analog signal processing circuit. The signal path includes the pixel circuit, current source, column programmable-gain amplifier (PGA), column sample-and-hold stage, analog multiplexers (MUX) and output buffer. The current source provides current bias to the source follower of the pixel. The column PGA consists of a CMOS operational amplifier (OPAMP), an input capacitor C_1, a programmable feedback capacitor C_2 and an MOS switch S3. The ratio of the input capacitor C_1 to the feedback capacitor C_2 determines the gain of each PGA, which can be set to 2 or 4. The column sample-and-hold stage is utilized for sampling and holding the analog signal from column PGA. The output signal of column sample-and-hold stage will be readout through multiplexers and output buffer.

Figure 4 shows the operation timing diagram of the analog signal processing circuit. First, when the amplified reset voltage V_{CR} of the pixel is readout, the column PGA amplifier is initialized by turning on the switch S3. This operation sets the output of the PGA amplifier to the reference voltage V_{REF}. Then the switch S3 is turned off and the switch M_{S2} is turned on. The mixed pixel signal voltage V_{CS+CR} is readout and amplified by PGA. Thus, the output signal voltage of the column amplifier becomes $V_{COPA} = \frac{C_1}{C_2}(V_{CR} - V_{CS+CR}) + V_{REF}$. The PGA performs CDS operation too. Finally, this output signal voltage V_{COPA} will be sampled on capacitance C_3 and outputted into the multiplexers and output buffer. The pixel level sample-and-hold circuit makes the image sensor operate at full frame integration while reading out the previously integrated frame (IWR) mode. The IWR mode accelerates the sensor frame rate greatly.

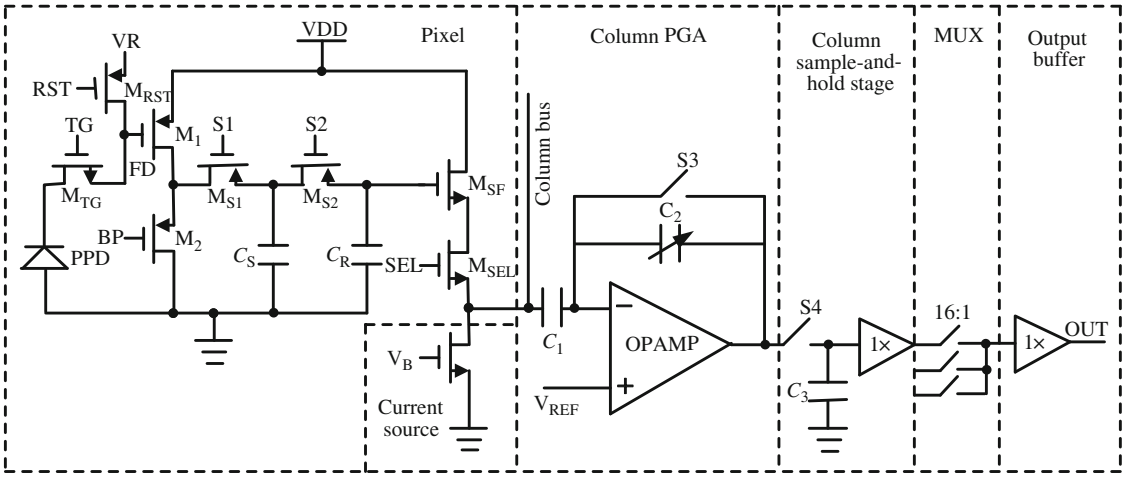

Figure 3 Analog signal processing circuit.

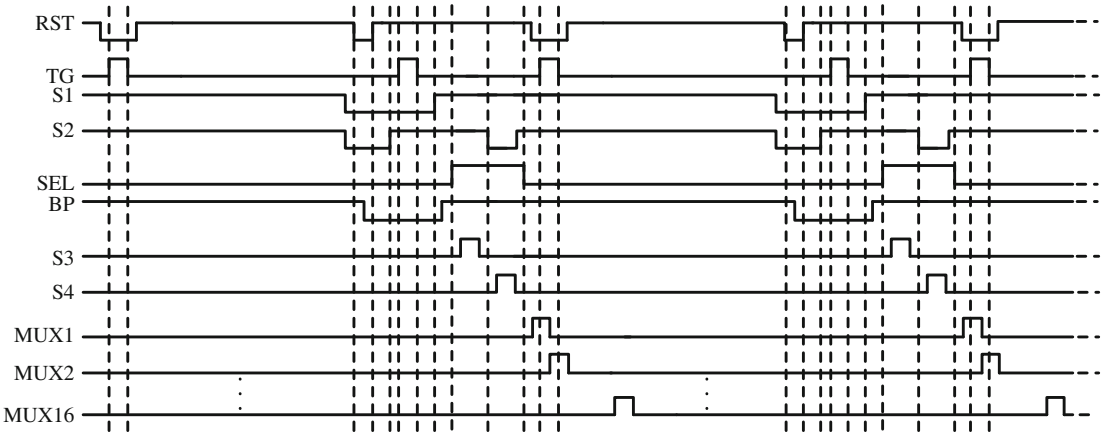

Figure 4 Operation timing for pixel analog signal processing circuit.

3 Pixel noise discussion

The dominating noise source in the proposed pixel is the KTC noise caused by the in-pixel sample-and-hold capacitors. We just consider KTC noise from the capacitors of $C_{\rm S}$ and $C_{\rm R}$ here, because the CDS operation reduces the other noises of the pixel significantly [17,18]. After finishing the second reset of FD, the voltage on capacitor $C_{\rm R}$ is the amplified reset voltage $V_{\rm CR}$. $V_{\rm CR}$ is calculated as

$$V_{\rm CR} = \sqrt{A^2\left(\sqrt{\frac{{\rm k}T}{C_{\rm FD}}}\right)^2 + \left(\sqrt{\frac{{\rm k}T}{C_{\rm R}}}\right)^2} - AV_{\rm RST}, \tag{1}$$

where A is the gain of the in-pixel amplifier, k is Boltzmann constant, T is temperature, $C_{\rm FD}$ is the parasitic capacitor of FD, $V_{\rm RST}$ is the reset voltage on FD, $\sqrt{\frac{{\rm k}T}{C_{\rm FD}}}$ is the KTC noise from FD, and $\sqrt{\frac{{\rm k}T}{C_{\rm R}}}$ is the KTC noise introduced by $C_{\rm R}$. Similarly, after the switch $\rm M_{S2}$ is turned off, the voltage stored on $C_{\rm S}$ is amplified signal voltage $V_{\rm CS}$. The $V_{\rm CS}$ is expressed as

$$V_{\rm CS} = \sqrt{A^2\left(\sqrt{\frac{{\rm k}T}{C_{\rm FD}}}\right)^2 + \left(\sqrt{\frac{{\rm k}T}{C_{\rm S}}}\right)^2} - A\left(V_{\rm RST} - V_{\rm SIG}\right), \tag{2}$$

where $V_{\rm SIG}$ is the light signal voltage converted by the photo-generated charges in FD, and $\sqrt{\frac{{\rm k}T}{C_{\rm S}}}$ is the KTC noise introduced by $C_{\rm S}$.

The amplified reset voltage $V_{\rm CR}$ is readout in the front part of the readout phase. Then the switch $\rm M_{S2}$ is turned on to make the amplified reset voltage $V_{\rm CR}$ and amplified signal voltage $V_{\rm CS}$ shared between

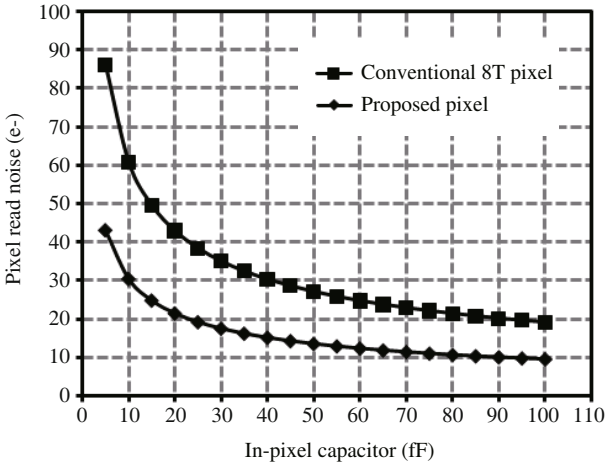

Figure 5 Comparison of calculated pixel noise between the proposed pixel and 8T pixel (in [7]) at different $C_{\rm S}$ and $C_{\rm R}$.

$C_{\rm S}$ and $C_{\rm R}$. Adding two non-correlated noises can simply superpose their noise power. However, we will get four times of the total noise power by adding two unity correlated noises. These three KTC noises, caused by $C_{\rm FD}$, $C_{\rm R}$ and $C_{\rm S}$ respectively, are not correlated with each other. But $V_{\rm CR}$ and $V_{\rm CS}$ both comprise a correlated noise source of KTC noise induced by FD. As a result, after sharing, the mixed voltage $V_{\rm CS+CR}$ stored on $C_{\rm S}$ and $C_{\rm R}$ can be defined as

$$V_{\rm CS+CR} = \frac{AC_{\rm S}}{C_{\rm R}+C_{\rm S}}V_{\rm SIG} - AV_{\rm RST} + \frac{\sqrt{A^2\left(C_{\rm R}+C_{\rm S}\right)^2\frac{{\rm k}T}{C_{\rm FD}} + {\rm k}TC_{\rm R} + {\rm k}TC_{\rm S}}}{C_{\rm R}+C_{\rm S}}. \tag{3}$$

CDS operation is implemented by subtracting the voltage $V_{\rm CR}$ from voltage $V_{\rm CS+CR}$ so that light signal voltage $V_{\rm SIG}$ can be obtained. The key point is that the switch $\rm M_{S2}$ should be turned off after CDS operation. If $\rm M_{S2}$ is switched off during the CDS operation, an additional KTC noise of $C_{\rm R}$ will be added to total pixel noise [7]. The KTC noise on FD is cancelled completely, because it is a correlated noise source for $V_{\rm CR}$ and $V_{\rm CS+CR}$. The KTC noise in $C_{\rm R}$ is also correlated, but in $V_{\rm CR}$ it includes a full noise power while the voltage $V_{\rm CS+CR}$ just includes $(\frac{C_{\rm R}}{C_{\rm R}+C_{\rm S}})^2$ of the full noise power. After subtracting, the remained noise is $(\frac{C_{\rm S}}{C_{\rm R}+C_{\rm S}})^2$ of the full noise power. The other uncorrelated noise sources only need to be simply added. The final pixel output after CDS is $V_{\rm OP}$, which is given by

$$V_{\rm OP} = \frac{AC_{\rm S}}{C_{\rm R}+C_{\rm S}}V_{\rm SIG} + \sqrt{\frac{{\rm k}TC_{\rm S}^2}{C_{\rm R}(C_{\rm R}+C_{\rm S})^2} + \frac{{\rm k}TC_{\rm S}}{(C_{\rm R}+C_{\rm S})^2}}. \tag{4}$$

In our design, capacitances $C_{\rm S}$ and $C_{\rm R}$ are both equal to C. Thus, the final pixel output $V_{\rm OP}$ is then simplified into

$$V_{\rm OP} = \frac{A}{2}V_{\rm SIG} + \sqrt{\frac{{\rm k}T}{2C}}. \tag{5}$$

The second term of (5) is the noise voltage of the pixel output. The equivalent noise electron number on FD, $N_{\rm noise}$, can be calculated as

$$N_{\rm noise} = \frac{C_{\rm FD}}{q}\sqrt{\frac{2{\rm k}T}{A^2C}}, \tag{6}$$

where q is electron charge. Formula (6) indicates that, thanks to the pixel-level amplifier gain A is larger than one, the in-pixel sample-and-hold capacitances ($C_{\rm R} = C_{\rm R} = C$) of the proposed pixel required to reach a desired noise level is divided by A^2 in comparison to the capacitances required by conventional pixel [7] with a gain smaller than one. In other words, under the condition of the same capacitances, the noise level can be decreased by A times. Therefore, the low read noise pixel with two small sample-and-hold capacitors can be realized.

Figure 5 shows the comparison of calculated pixel noise between the proposed pixel and 8T pixel in [7] at different $C_{\rm S}$ and $C_{\rm R}$. In calculation, the FD parasitic capacitor $C_{\rm FD}$ is 10.7 fF, the gain of in-pixel

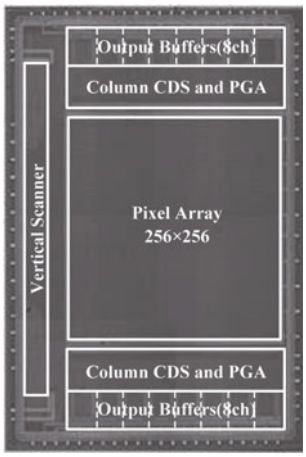

Figure 6 Die photograph of the sensor chip.

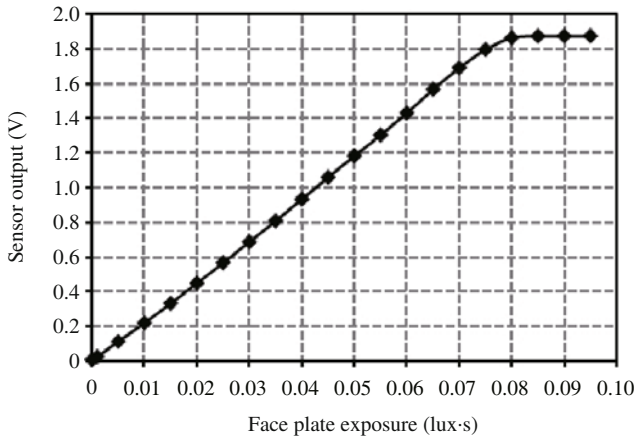

Figure 7 Photo conversion characteristic.

Table 1 Performance summary

Parameter	Performance	Parameter	Performance
Process	0.18 μm CMOS 1P4M	Dynamic range	66 dB
Chip size	5 mm × 7 mm	Signal to noise ratio	44 dB
Array size	256 × 256	Well capacity	30840e-
Pixel size	14 μm × 14 μm	Read noise	14.8e- (PGA gain 4×)
Fill factor	40%	Pixel power consumption	59 nA
Sensitivity	6.1 V/lux·s	Frame rate	1000 fps
Conversion gain	15 μV/e-	Linearity	98.6%
Fixed pattern noise	< 2% (pixel-to-pixel)		

amplifier A is 2, and the temperature is 27 °C. Figure 3 demonstrates that using small $C_{\rm S}$ and $C_{\rm R}$ to get lower read noise is possible in the proposed pixel.

4 Implementation and measurement results

A prototype high speed CMOS image sensor with the proposed pixel was implemented in a 0.18 μm CMOS process. Figure 6 shows the die photograph of the fabricated CMOS image sensor chip. The image array has 256 × 256 effective pixels. And all of the pixels share a common x-y pitch of 14 μm. The PGAs with CDS function are used for both the odd and even columns. The final image signals are outputted by eight-channel analog buffers for each side. The overall die dimensions are 5 mm × 7 mm. The in-pixel amplifier gain A is designed of 2 and the pixel level sample-and-hold capacitance is close to 70 fF for both $C_{\rm S}$ and $C_{\rm R}$. The sensor chip runs at 1000 fps, with 16 off chip 14 bit ADCs.

The designed global shutter pixel power consumption is 59 nA per pixel at a supply voltage of 3.3 V. Figure 7 is a measured photo conversion curve with an analog gain of 4. The designed sensor has a good linearity of 98.6% over a linear output range of approximately 1.7 V. The sensor achieves 14.8e- RMS noise (in which case, the PGA gain is set at 4) and 15 μV/e- conversion gain. The sensitivity is 6.1 V/lux·s. The full well capacity is 30840e-. Therefore, the signal dynamic range of the sensor reaches 66 dB. The signal-to-noise ratio of the sensor is 44 dB which is high enough for the visibility of the noise. However, the sensor chip suffers from a large pixel-to-pixel fixed pattern noise of 2%. One possible reason for this phenomenon is as follow. The whole pixel array has the same reset voltage which may exceed the linear amplification region of in-pixel amplifier for some pixels. Thus, a high pixel-to-pixel fixed pattern noise appears in image reconstruction. A technology in which every pixel has self reset voltage will be adopted in future design to decrease pixel-to-pixel fixed pattern noise. The sensor characterization result is summarized in Table 1. Our work is compared with other previous designs in Table 2. The comparison

Table 2 Performance summary Comparison with previous designs

	Ref. [1]	Ref. [3]	Ref. [4]	Ref. [7]	Ref. [9]	This work
Process (μm CMOS)	0.6	0.25	0.35	0.18	0.18	0.18
Array size	512 × 512	514 × 530	512 × 512	2048 × 1088	1024 × 1024	256 × 256
Pixel size (μm × μm)	20 × 20	20 × 20	16 × 16	5.5 × 5.5	7.5 × 7.5	14 × 14
Fill factor (%)	44	40	N.A.	42	N.A.	40
Sensitivity (V/lux·s)	N.A.	19.9	9	4.64	0.95	6.1
Conversion gain (μV/e-)	10.7	N.A.	16	85	33	15
Dynamic range (dB)	66	60	59	61	N.A.	66
Read noise	65.4e-	1.8 mV	70e-	13e-	6.3e- (pixel only)	14.8e-/222 μV
Frame rate (fps)	255	3500	5000	340	1000	1000
Linearity (%)	N.A.	Good	98.5	N.A.	Bad	98.6

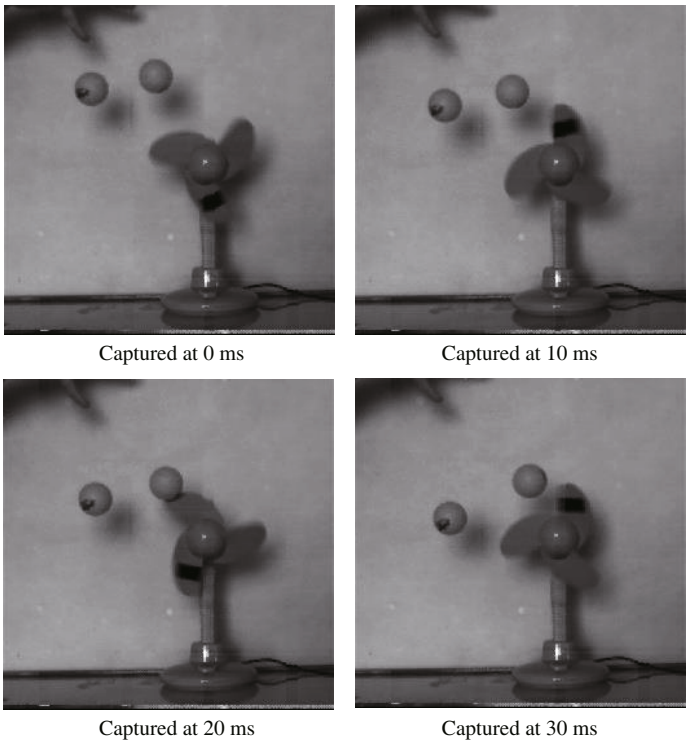

Figure 8 Consecutive images taken at 1000 fps.

result indicated that the in-pixel amplifier and sample-and-hold circuit effectively improve the sensor noise performance. The noise can be further reduced by increasing conversion gain. If the conversion gain is increased to 85 μV/e- and the pixel level sample-and-hold capacitance is reduced to 15 fF (the same as [7]), the sensor read noise is calculated to be 4.4e- by (6). This calculated read noise (4.4e-) is much lower than the read noise in [7,9]. The bad linearity of [9] predicts that the incomplete charge transfer causes a large residual charge in its PSD region. Four frames from a video sequence at 1000 fps are shown in Figure 8. The interval time between each two images is 10 ms. The impact process between one of the table tennis balls and the rotating electric fan is recorded.

5 Summary

This paper has proposed a novel global shutter pixel for high speed CMOS image sensor and implemented a high speed 1000 fps 256 × 256 CMOS image sensor. The pixel is an 8T pixel with pixel level sample-

and-hold circuit and amplifier of larger gain than one. The KTC noise on the FD can be effectively suppressed by CDS circuit. Two PMOS transistors form the in-pixel amplifier with larger gain than one. The thermal noise of the sample-and-hold capacitors is drastically reduced. Meanwhile the fill factor of the pixel is also increased. The pixel size is 14 μm × 14 μm. The measured results indicate that the proposed pixel noise level is lower than 14.8e- and its fill factor is larger than 40%. The full frame rate of 1000 fps has been also demonstrated in this global shutter sensor chip.

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