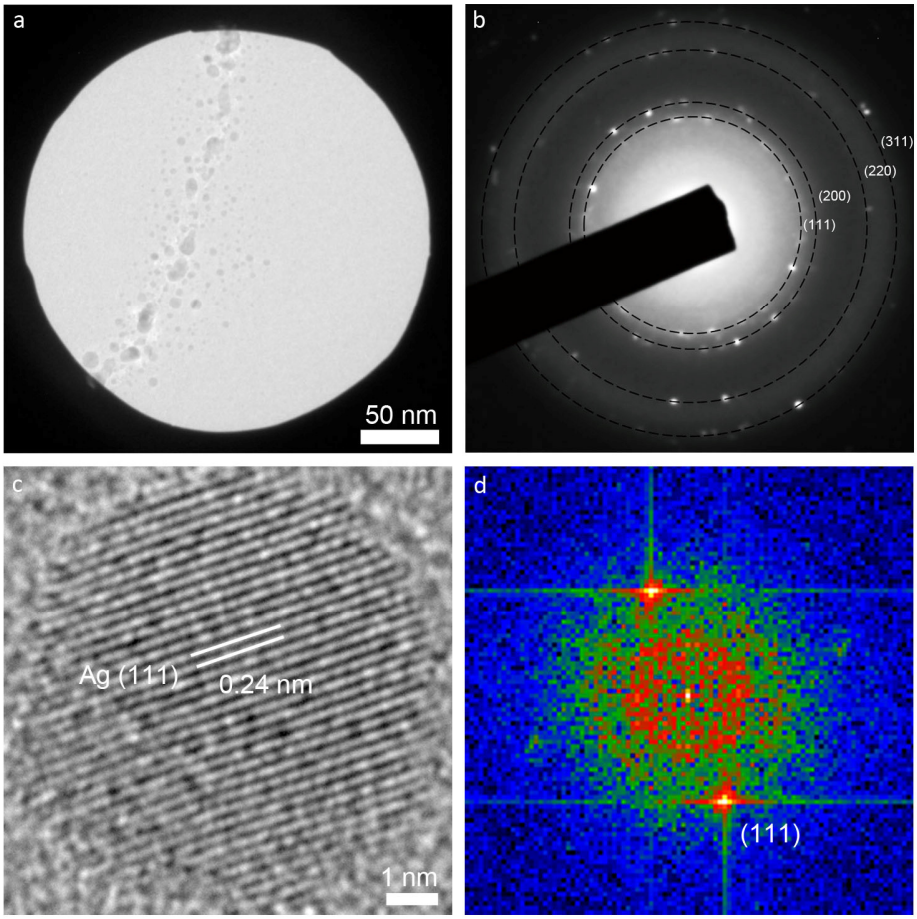
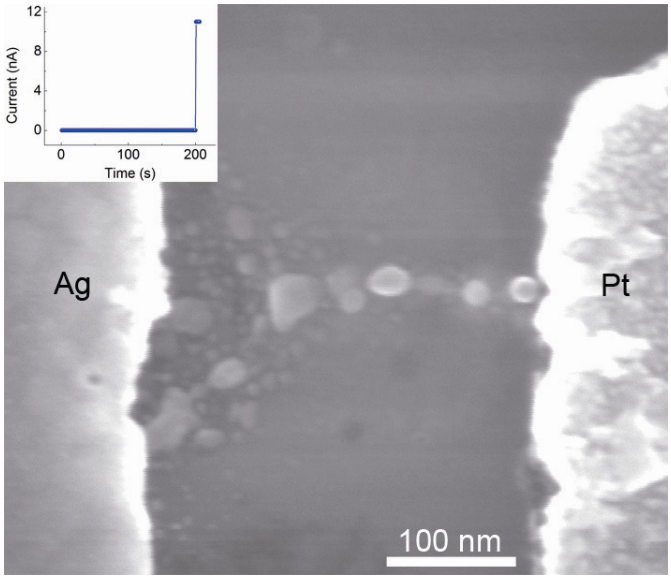
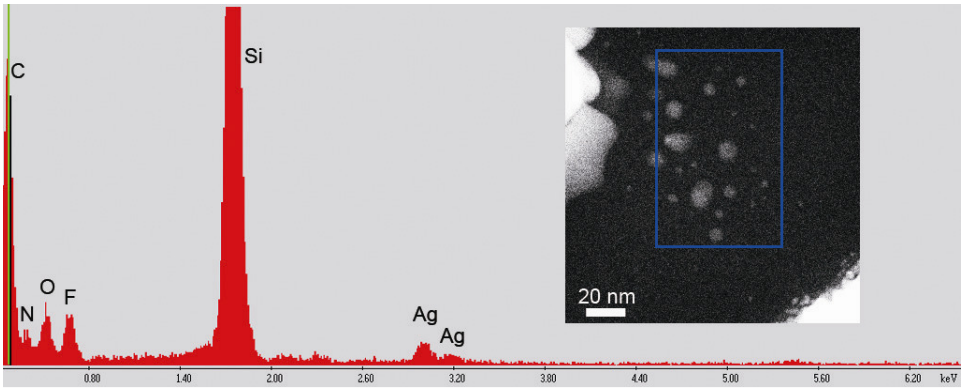


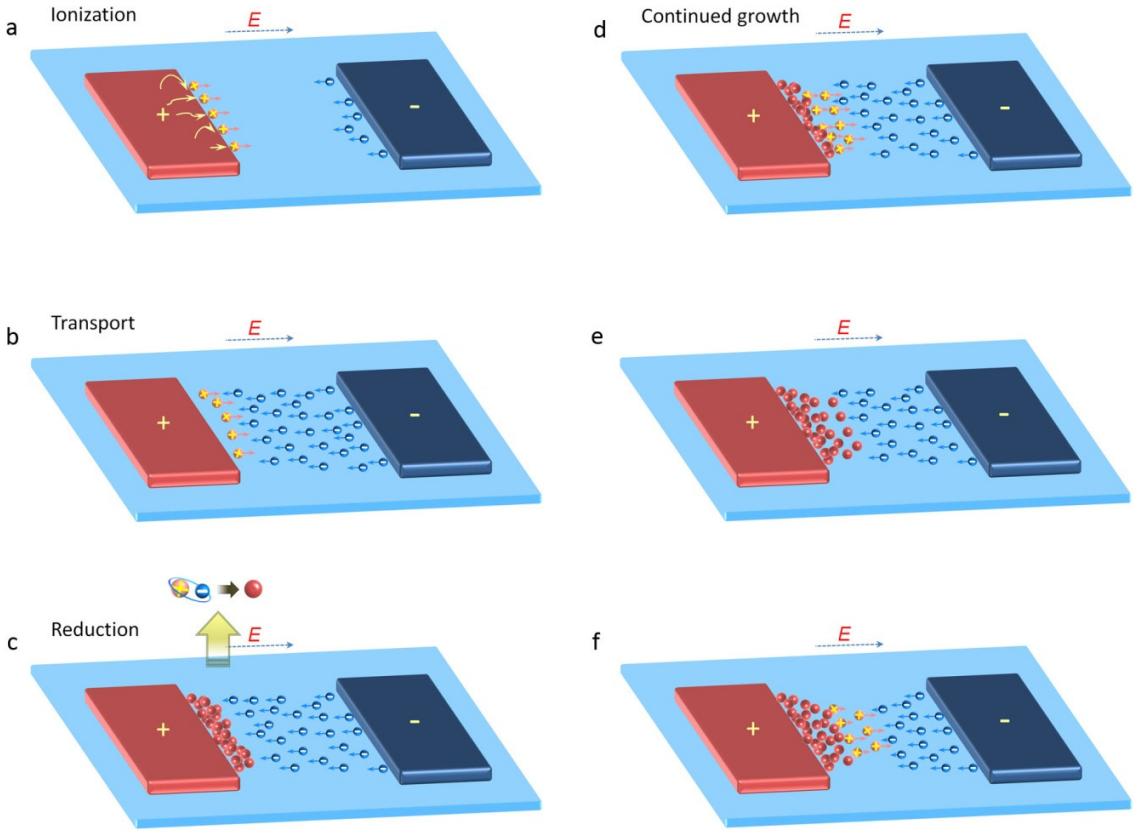

**Supplementary Figure S1 | Crystal structure of the conducting filaments in sputtered $SiO_2$ based devices.** (**a**) TEM image of the conducting filament in a $SiO_2$ based memory device used for SAED analysis. (**b**) Corresponding SAED pattern of the filament, which can be indexed with elemental Ag with fcc structure. (**c**) HRTEM image of a Ag nanoparticle in the filament shown in (**a**). Ag (111) planes can be clearly resolved. (**d**) Corresponding FFT results of the HRTEM image shown in (**c**).




**Supplementary Figure S2 | Forming and filament growth in $Al_2O_3$ based devices.** Resistive switching characteristics were studied in resistive memories based on $Al_2O_3$ films deposited by ALD. A single conducting filament was observed after the forming process, whose *I–t* curve is shown in the inset. The results obtained from $Al_2O_3$-based resistive switches are in line with those from sputtered $SiO_2$, and the thinnest part of the filament is also at the dielectric/IE interface. The typical forming time in $Al_2O_3$ based resistive switches is ~200 s under an electric field of ~0.5 MV/cm. This electric field is relatively low compared with the electric field required to switch the a-Si based devices in a similar time (e.g. Fig. 3a).

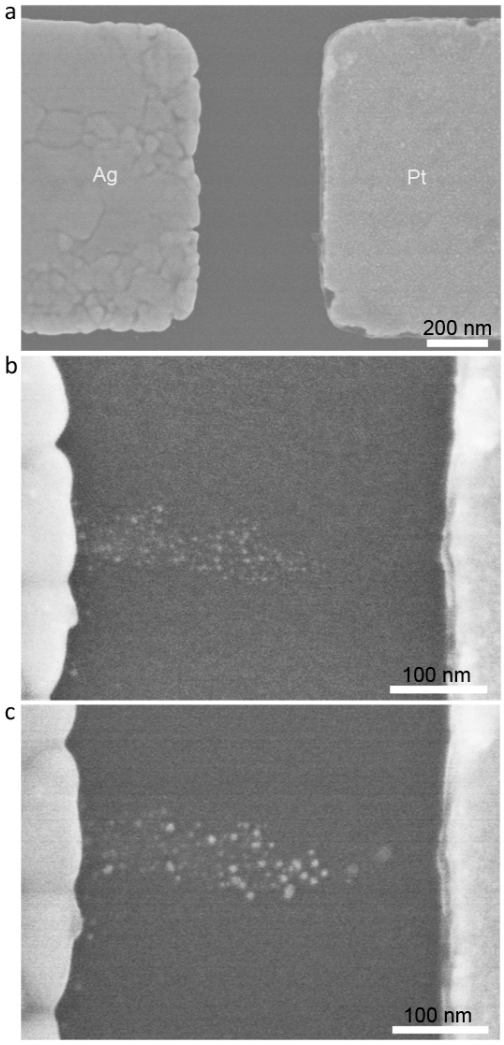



**Supplementary Figure S3 | EDS spectrum of the conducting filament in a-Si based devices.** The composition of the conducting filaments was studied by EDS. The rectangular box in the inset indicates the region of interest used for EDS analysis. The presence of Ag was clearly detected in the conducting filament region, verifying the composition of the filament. The signals of Si and N come from the a-Si layer and the $SiN_x$ membrane, while other signals such as C and O may originate from surface adsorptions of the TEM specimen.

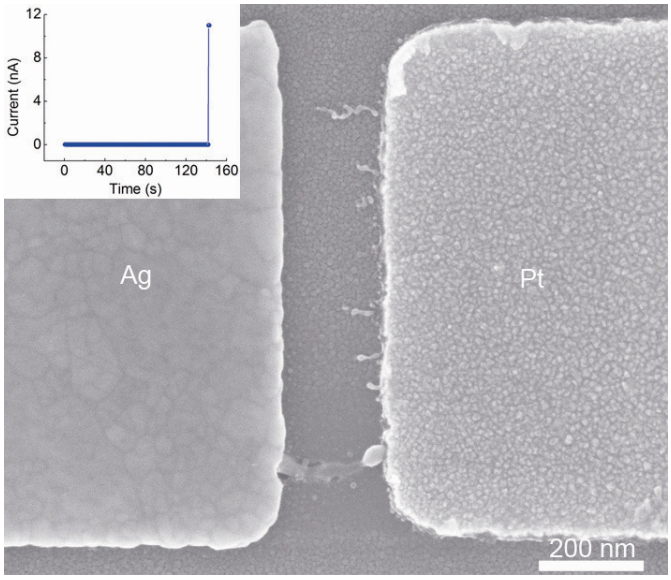



**Supplementary Figure S4 | Filament growth dynamics in a-Si based memory devices.** Supplementary Figure S4 shows a schematic of the filament growth model in dielectric-based memory devices with low cation mobility (e.g. in the case of a-Si). During the filament growth, the Ag cations are initially created and injected into the dielectric film from the anode (supplementary Fig. S4a). Driven by the electric field the cations then move towards the cathode. However, due to their low mobility, the cations can only travel a short distance (supplementary Fig. S4b) before becoming reduced by the incoming electrons (supplementary Fig. S4c). Since the Ag cations are reduced near the anode, the created metal nuclei share similar (positive) electrostatic potential as the anode and become an extension of the anode. This explanation is consistent with data obtained from *in-situ* TEM (Figs. 5c-5d) and *ex-situ* observations (Figs. 3,

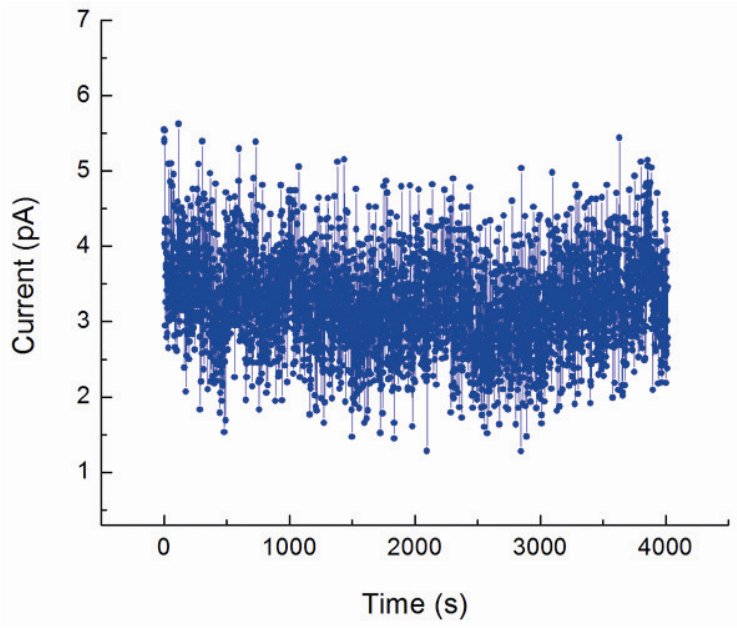
supplementary Fig. S5). The process can then be repeated, as new Ag ions are created and injected from the tip of the extended Ag anode and become reduced nearby, as shown schematically in supplementary Figs. S4d-S4f. These processes therefore lead to a gradual filament growth from the active electrode to the inert electrode, as observed experimentally.



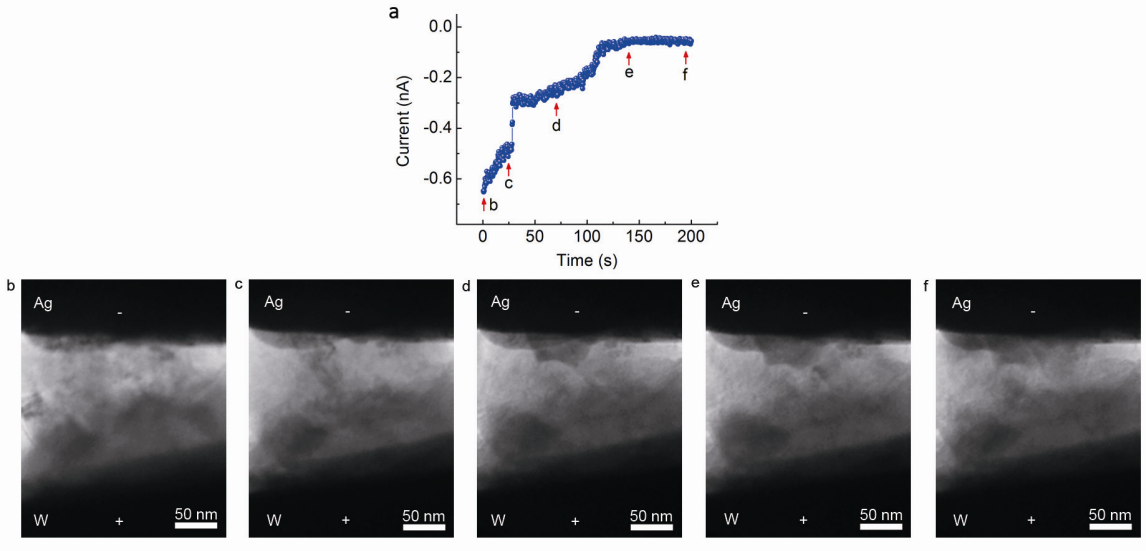

**Supplementary Figure S5 | Step-by-step filament growth.** (**a**) SEM image of the as-fabricated planar resistive switch based on a-Si. (**b**) Growth of an incomplete conducting filament after forming. (**c**) When a positive bias was applied again on the Ag electrode, the conductance of the device was increased for a second time. SEM imaging of the device shows an extension of the previous filament toward the Pt electrode.




**Supplementary Figure S6 | Resistive switching and filament growth in sputtered $SiO_2$.** Supplementary Figure S6 shows a typical forming *I–t* curve and the resulting conducting filaments obtained in a sputtered $SiO_2$-based device. The device was fabricated on a Si substrate with a 120 nm thick high-quality thermal $SiO_2$ layer. In agreement with the TEM results in Fig. 1, the partially formed conducting filaments suggest that the filament growth direction in sputtered $SiO_2$ based devices is from the inert electrode to the active electrode and the thinnest region of the filament is at the inert electrode interface. It is noteworthy to point out that some of the partially formed filaments also showed dendrite structures with branches pointing toward the active electrode, which is again consistent with the results in Fig. 1.




**Supplementary Figure S7 | Resistive switching in thermal $SiO_2$.** Planar resistive switching devices were also fabricated on high-quality furnace-grown amorphous $SiO_2$ films. These control experiments showed that devices based on dense, thermal $SiO_2$ could not be formed in 4,000 s under a high electric field of 1.2 MV/cm, in contrast to typical conditions of 20 s, 0.4 MV/cm used for sputtered $SiO_2$ based devices or 500 s, 0.8 MV/cm used for a-Si based devices. This experiment shows the choice of the dielectric has a very large impact on the forming process and the filament formation critically depends on the cation mobility in the dielectric film. In this case, the thermally grown $SiO_2$ film has a very dense structure which effectively blocks the migration of Ag ions and impedes the formation of conducting filaments. The more defective structures in sputtered $SiO_2$ and ALD $Al_2O_3$ films are beneficial for ion diffusion and are thus favorable for filament growth.




**Supplementary Figure S8 | *In situ* TEM observation of filament dissolution in vertical Ag/a-Si/W devices.** (**a**) *I–t* characteristics during the erase process of a vertical Ag/a-Si/W device. (**b-f**) *In-situ* TEM images of the device corresponding to data points b-f in (**a**). The re-deposition of Ag atoms at the Ag electrode during erase is visible from b-f. These observations are in agreement with the findings from planar devices (e.g. Fig. 1) that the dissolution of filament is from the inert electrode to the active electrode.