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Characterization of precisely width-controlled Si quantum wires fabricated on SOI substrates

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Abstract

Silicon quantum wire structures with precisely controlled widths have been successfully fabricated on an SOI substrate by an anisotropic etching technique. The width of the wires does not depend on the lithography limit but solely on the thickness of the Si film of the SOI substrate. It is demonstrated that the wires are straight even if the lithography patterns are fluctuated. The minimum width is estimated to be less than 10 nm. This technique has been applied to fabricating a quantum wire FET, which shows fine peaks in drain current as a function of the gate voltage at low temperatures due to the Coulomb blockade of the single electron tunneling. The oscillations remain even at room temperature.

Keywords: Si quantum wire; SOI; Coulomb blockade; Quantum dots

1. Introduction

Recently, Si nanostructures have attracted much attention from technological point of view. This situation is mainly based on the idea that new Si nanostructure devices such as single electron devices would have advantage of extremely low-power consumption and would be integrated into LSI chips in the future. It is very important to develop the fabrication technology of Si nanostructures in LSI compatible processes. Several fabrication processes of Si nanostructures have been reported previously on Si substrates [1] and silicon on insulator (SOI) substrates [2–4]. However, those processes have utilized very fine electron-beam (EB) lithography, or complicated etching processes. The uniformity and reproducibility have been poor and the width has often been fluctuating. Most of these processes are not compatible to the LSI process.

The purpose of this study is to develop and characterize the fabrication technique of Si quantum wire structures which are precisely width-controlled and uniform over the wafer. The process makes use of the anisotropic etching technique [5] utilizing TMAH (Tetramethylammonium-hydroxide) and does not require the fine lithography steps. It is fully compatible to the LSI process.

2. Fabrication process

KOH has been often used for the anisotropic etchant [5] which etches (1 0 0) surface much faster than (1 1 1) surface. However, KOH is not

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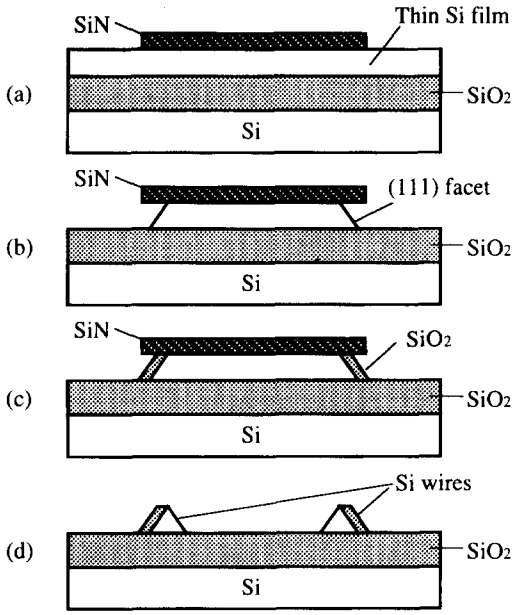

Fig. 1. Fabrication steps of Si quantum wires by the anisotropic etching technique.

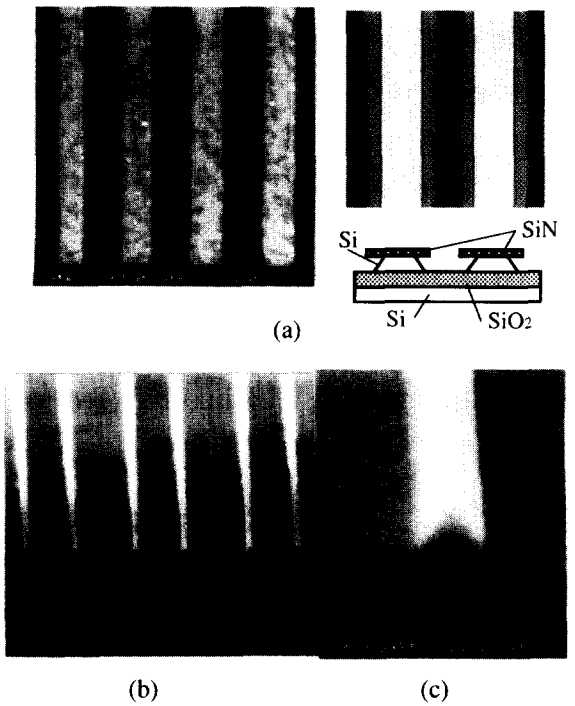

Fig. 2. SEM micrographs of (a) a sample just after the first anisotropic etching with schematic illustrations of top and cross-sectional views, (b) array of quantum wires, and (c) a quantum wire in an enlarged scale.

compatible to Si LSI process because the potassium is a serious contaminant for MOS devices and causes a severe degradation of device characteristics. In this study, TMAH, which is often used for a developer of photoresists or EB-resists and compatible to the LSI process, is examined.

Fig. 1 illustrates the fabrication steps. The Separation by IMplanted Oxygen (SIMOX) wafers are employed as an SOI substrate because of its uniform Si film thickness, which is easily controlled by thermal oxidation. The thickness variations of the Si film and the thermal oxide are less than 2% and 3%, respectively. First, the thermal oxide is formed to make the Si film thinner (40 nm). After the removal of the thermal oxide, SiN film is deposited and patterned (Fig. 1(a)). Then, the Si film is subjected to the first anisotropic etching by TMAH. Two Si (1 1 1) facets are formed at the edges as shown in Fig. 1(b). The facets are covered by thermal oxidation (30 nm, Fig. 1(c)), and after the SiN removal, the second anisotropic etching is performed. Two triangle Si wire structures are formed as shown in Fig. 1(d). Since the height and width of the wires are determined only by the thickness of the SOI Si layer, the wire width is precisely controlled and uniform. Moreover, the minimum width is not dependent on lithography and could be much narrower than the lithography limit.

3. Results

Fig. 2(a) shows a SEM image and schematic views (top and cross-section) of the sample just after the first anisotropic etching (corresponding to Fig. 1(b)). The bright region is Si and the darkest one is the region where the SiN is removed. It is clearly seen that, even though the SiN lines are very fluctuated, the (1 1 1) facet is very straight. Fig. 2(b) and (c) show SEM images of the fabricated Si quantum wires. The width of the wires is uniform and is not fluctuated. Since the wire in Fig. 2(c) contains the 30 nm oxide as shown in Fig. 1(d), the width of Si region is estimated to be less than 10 nm.

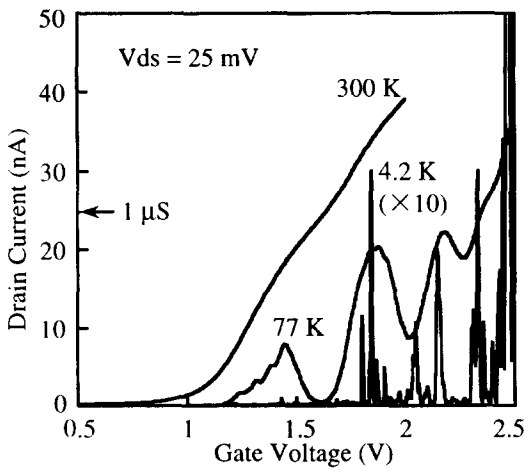

Fig. 3. The gate voltage dependence of the drain current of the quantum wire FET at 4.2, 77, and 300 K.

This fabrication technique of the wire structure has been applied to fabricating a quantum wire FET. A wire, with a length of 0.1 μm defined by the EB lithography, is fabricated and a poly-Si gate is formed after the gate oxidation of 20 nm. The final width of the Si wire is estimated to be less than 10 nm. Fig. 3 shows the gate voltage dependence of the drain current of the fabricated wire FET at 4.2, 77, and 300 K. The drain current exhibits very fine oscillations at 4.2 K.

These oscillations are typical characteristics of Si nanostructures and caused by the Coulomb blockade effect [3,4,6]. Considering that the ratio of length to width of the wire is more than 10, the wire could be separated into several quantum dots just above the threshold voltage, forming a multijunction device which causes aperiodic Coulomb blockade oscillations [7]. This is consistent with the experimental results which show aperiodic fine oscillations at 4.2 K. It should be noted that at 77 K large oscillations are observed which remain even at room temperature, indicating that the sizes of the quantum dots and capacitances are very small. The detailed experimental results will be reported elsewhere.

4. Conclusions

Si quantum wires with precisely controlled widths have been successfully fabricated by an anisotropic etching technique on an SOI substrate. The minimum width does not depend on lithography and can be much less than the lithography limit. A quantum wire FET, fabricated by this technique, shows at low-temperature fine Coulomb blockade oscillations which remain even at room temperature.

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