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ELECTRICAL PROPERTIES OF HAFNIUM OXIDE GATE DIELECTRIC DEPOSITED BY PLASMA ENHANCED CHEMICAL VAPOR DEPOSITION

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Hafnium oxide thin films were deposited at 300℃ on p-Si (100) substrates by plasma enhanced chemical vapor deposition (PECVD). The gate dielectric formed by PECVD was $HfO_2/SiO_2/Si$ structure. The thickness of the HfO_2 thin films decreases with increasing RTA temperature because of its high density. The $Pt/HfO_2/SiO_2/Si$ structure showed accumulation, depletion and inversion. After the RTA treatment, the capacitances of the $Pt/HfO_2/SiO_2/Si$ structures were increased because, the thickness of HfO_2 thin film decreased. The counterclockwise hysteresis of the C-V curve is believed to be due to charge trapping at the negative gate bias. Hysteresis of as-deposited gate dielectric is quite large, but rapidly decreases with increasing RTA temperature. The increase in leakage current density by the O_2 anneal seems to be related to the grain growth of the HfO_2 thin film. After forming gas annealing, the electrical properties did not largely improve.

Keywords: PECVD; Gate dielectrics; HfO_2

INTRODUCTION

Considering the technology roadmap, and equivalent oxide thickness of less than 15Å will be necessary to meet the requirements for 0.1 ㎛ technology.[1] As the SiO_2 thickness scales below 20 Å the gate leakage of the metal oxide semiconductor field effect transistor (MOSFET) becomes unacceptably high due to excessive tunneling current. For SiO_2 layers, direct tunneling of electrons becomes quite important for layers thinner than 15Å, leading to a leakage current at operating voltage of 1 × 10 A/㎠.[2]

Since technology roadmaps predict the need for 15 Å and below gate dielectrics in the near future, many high-k gate dielectric materials, such as HfO_2, ZrO_2, La_2O_3 and their silicates have been studied as alternatives for SiO_2.[3-12] HfO_2, especially, has desirable properties such as high dielectric constant (~30), high heat of formation (271 kcal/mol),[13] and relatively large band gap (5.86 eV).[14] HfO_2 also is very resistive to impurity diffusion and intermixing at the interface because of its high density (9.68 g/㎤).[14] These properties make HfO_2 one of the most promising candidates for alternative gate dielectric application.

So far, HfO_2 thin films have been prepared by sputtering[3, 5-6] and thermal chemical vapor deposition (CVD).[4] The thermal CVD method has actually produced pertinent HfO_2 thin film quality at a temperature around 500℃ using $Hf[OC(CH_3)_3]_4$. It should be noted that a PECVD method of deposited HfO_2 thin films has not been reported. Compared with thermal CVD method, the PECVD technique of formation of the thin films has some other advantages, such as the low deposition temperature and control of deposition.

In this study, HfO_2 gate dielectric thin films were deposited by plasma enhanced chemical vapor deposition (PECVD). The physical and electrical properties were evaluated as a function of annealing temperature and ambient.

EXPERIMENTAL PROCEDURE

The HfO_2 films were deposited on p-type Si (100) substrates by PECVD in O_2 ambient at 300℃. The $Hf[OC(CH_3)_3]_4$ was vaporized in the bubbler at 30℃ and was carried to the reactor using argon as the carrier gas. The chamber was maintained at 1 Torr during deposition. The HfO_2 deposition parameters were as follows: the Ar flow rate was 100 standard cubic centimeters per minute (sccm), the O_2 flow rate was 100 sccm, and the radio frequency (rf) power was 40 W. These samples were transferred to the RTA chamber and annealed at 600℃~ 800℃ for 3 min in O_2 and N_2 ambient. After RTA, a Pt electrode to measure electrical properties was sputter deposited, patterned, and etched using aqua regia solution ($1HNO_3$:$9HCl$:$10H_2O$) at 100℃. The capacitor area for the MOS ($Pt/HfO_2/SiO_2/Si$) structure was 3×10^{-4} cm^2. After gate patterning, the backside of the sample was etched to expose the silicon substrate and metallized with Pt to reduce the series resistance. Forming gas annealing (FGA) was performed at 350℃ for 30 min in 4% H_2.

The physical thickness of HfO_2 thin film was measured using high-resolution transmission electron microscopy (TEM, CM20T/STEM, Philips). Carbon contamination of HfO_2 thin film was analyzed using auger electron spectroscopy (AES, VG Scientific Microlab 310-D). The capacitance-voltage (C-V) curves of the MOS capacitor were measured using a HP4194A impedance/gain-phase analyzer. Capacitance equivalent oxide thickness (CET) was extracted from the accumulation capacitance at 1 MHz and quantum mechanical correction was not applied. A Keithley 617 programmable electrometer was used for leakage current density measurements.

RESULTS AND DISSCUSION

Figure 1 shows the high-resolution transmission electron microscopy (HR TEM) image of the HfO_2 thin films. This images clearly shows the formation between HfO_2 thin films and Si substrate of the amorphous interfacial layer

having a thickness of 19Å because, at the initial stage of deposition, Si substrate was exposed at O_2 ambient. The thickness of the interfacial layer did not change after RTA. The thickness of the HfO_2 thin films decreases with increasing RTA temperature because of its high density.

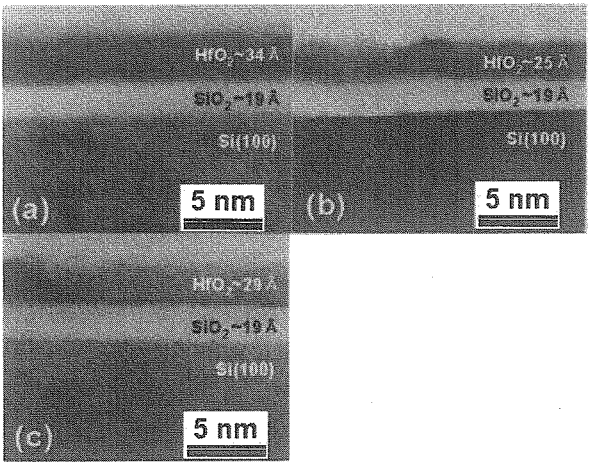

FIGURE 1 HR TEM images of $HfO_2/SiO_2/Si$ structure (a) as-deposited and annealed in (b) O_2 and (c) N_2 ambient at 800℃ for 3 minute.

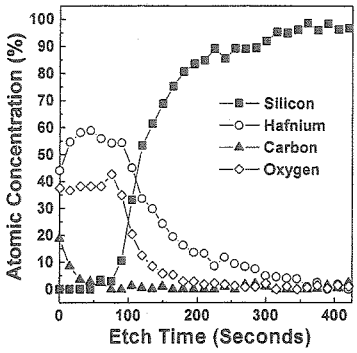

FIGURE 2 AES depth profile of $HfO_2/SiO_2/Si$ structure before RTA

To analyze the carbon contamination of the $HfO_2/SiO_2/Si$ structure, AES depth profiling was performed. Figure 2 show the AES depth profile of the $HfO_2/SiO_2/Si$ structure before RTA. The AES depth profile shows the presence of approximately 20 at. % carbon at surface. While some carbon is likely residual from the metalorganic deposition process, carbon contamination is also expected from the in-air sample transfer to the analysis chamber. The carbon content of the films was below the detection limit after RTA.

High frequency (1 MHz) C-V curves of $Pt/HfO_2/SiO_2/Si$ (a) before FGA and (b) after FGA are shown in figure 3. The $Pt/HfO_2/SiO_2/Si$ structure showed accumulation, depletion and inversion. After the RTA treatment, the capacitances of $Pt/HfO_2/SiO_2/Si$ structures were increased because, the thickness of HfO_2 thin film decreased. In Fig. 3(a), large flatband voltage shifts were observed after RTA. We speculate that the HfO_2 thin film contain positive charges. After RTA, the flatband shifts toward the positive gate voltage. In addition, it is thought that the $HfO_2/SiO_2/Si$ structure annealed in O_2 had more negative charges than the $HfO_2/SiO_2/Si$ structure annealed in N_2, thus showed larger flatband voltage shift. After FGA, the capacitance and flatband voltage shift slightly improved.

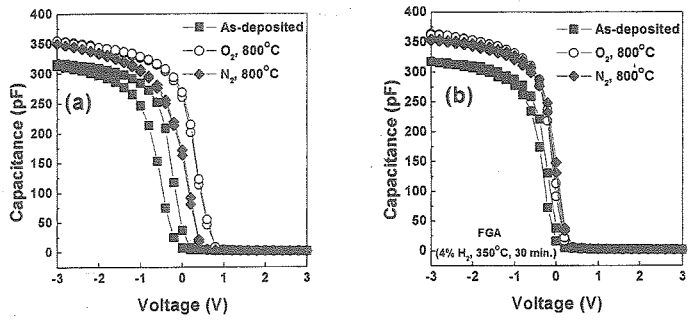

FIGURE 3 High frequency (1 MHz) C-V curves of $Pt/HfO_2/SiO_2/Si$ structure (a) before forming gas annealing (FGA) and (b) after FGA. The capacitor area is $3x10^{-4}$ ㎠.

Figure 4 shows the capacitance equivalent oxide thickness (CET) and hysteresis of $Pt/HfO_2/SiO_2/Si$ structure. The CET of the HfO_2 thin films annealed at 800℃ in O_2 ambient is about 29Å. The counterclockwise hysteresis of C-V curve is believed to be due to charge trapping at the negative gate bias. The hysteresis of as-deposited gate dielectric is quite large, but rapidly decreases with increasing RTA temperature for 3 minutes. The hysteresis in samples annealed at 800°C in O_2 and N_2 was reduced to a negligible level of about 20 mV. After FGA, the CET slightly decreased and the hysteresis did not change.

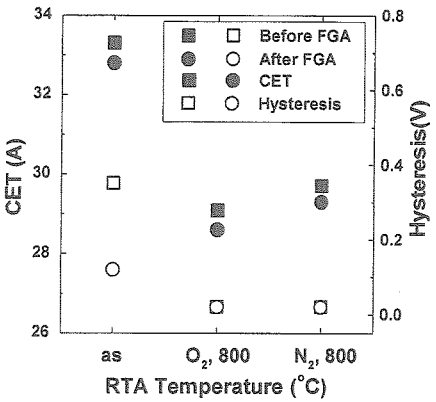

FIGURE 4 Capacitance equivalent oxide thickness (CET) and hysteresis of $Pt/HfO_2/SiO_2/Si$ structure before FGA and after FGA. The capacitor area is 3×10^{-4}㎠.

Interface trap density can be measured by a high frequency method developed by Terman.[15] Interface trap density of the HfO_2 thin film annealed at 800℃ in O_2 was about 5.5×10^{11} $cm^{-2}eV^{-1}$. After FGA, the interface trap density did not change.

The leakage current characteristics of $Pt/HfO_2/SiO_2/Si$ structure annealed in

O_2 and N_2 ambient were shown in figure 5(a). The leakage current densities of the films annealed in O_2 at 800℃ is about 8×10^{-5} A/cm^2 at –1 V. However, the leakage current density of the samples heat treated in N_2 at 800℃ is improved, which is about 3×10^{-6} A/cm^2 at an applied voltage of –1 V. The higher leakage current densities of films annealed in O_2 ambient than those in N_2 were due to the increase of crystallinity of HfO_2 films, as shown in Fig. 1. After FAG, the leakage current density increased. Figure 5(b) shows the variation of leakage current densities of samples annealed in hydrogen ambient at 350℃. The leakage current densities were abruptly increased by hydrogen forming gas anneal because oxygen loss in HfO_2 films during forming gas anneal increases oxygen vacancies and then increases charge carriers such as electron to achieve the charge neutrality.

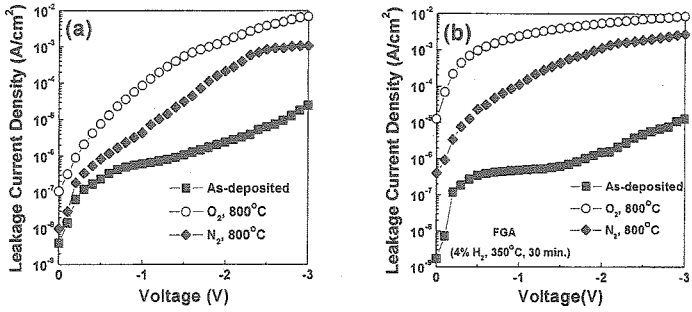

FIGURE 5 Leakage current density of $Pt/HfO_2/SiO_2/Si$ structure before FGA and after FGA. The capacitor area is 3×10^{-4}㎠.

CONCLUSIONS

Hafnium oxide thin films for gate dielectric were deposited at 300℃ on p-type Si(100) substrates by plasma enhanced chemical vapor deposition. The thickness of HfO_2 thin films decreases with increasing annealing temperature because of its high density. From the accumulation capacitance at 3 V, the CET of HfO_2 thin films annealed at 800℃ in O_2 ambient are about 29Å.

Hysteresis of as-deposited gate dielectric was quite large but that of gate dielectric annealed at 800℃ in O_2 and N_2 ambient was reduced to a negligible level without increase of the capacitance equivalent oxide thickness. The hysteresis in samples annealed at 800°C in O_2 and N_2 was reduced to a negligible level of about 20 mV. The leakage current densities of HfO_2 gate dielectric annealed at 800°C in O_2 and N_2 ambient were about 8×10^{-5} and 3×10^{-6} A/cm^2 at -1 V, respectively. After FAG, the electrical properties were not largely improved.

ACKNOWEDGMENTS

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