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Direct Wafer Bonded Abrupt Junction Tunnel Diodes

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Abrupt junction tunnel diodes have been fabricated using hydrophobic direct wafer bonding to join together highly n- and p-type doped wafers. Low reverse resistance backward diodes were achieved. The reverse bias behavior of the diodes is purely ohmic with a total reverse resistance of 0.0015 Ω cm^2, which produces a reverse voltage of 150 mV at 100 A/cm^2. Although Esaki tunneling is observed under forward bias, there is no observed negative differential resistance due to high excess current. The current work is the first step in creating low-loss stacked diode structures for high blocking voltage electric power applications.
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Wafer bonding is an enabling technology that allows fabrication of a variety of complicated structures that would be difficult or impossible to make by other means. Direct wafer bonding is a method of combining two or more substrates without an intermediate material layer such as glue or solder or requiring electric charge manipulation as in anodic bonding. When exposed to atmosphere for a significant period of time, or when cleaned in an oxidizer, silicon develops a thin native oxide on the surface. This native oxide would reduce or destroy performance by creating traps and electrical discontinuities that affect the current-voltage (I-V) and capacitance-voltage (C-V) characteristics at the interface.[1] However, with hydrophobic processing, the thin native oxide is removed by a hydrofluoric acid etch and the surface is passivated by silicon dihydride.[2] Thus, for bonded structures that require conduction through the bond interface, hydrophobic direct bonding is the preferred solution.[1]

Wafer bonding has been used to fabricate several important high-power bulk conduction devices such as thyristors[3] and double-sided insulated gate bipolar transistors.[4] Another useful device for power applications is a stacked diode. In this structure, multiple diodes are physically and electrically stacked in series to provide a device with high reverse blocking voltage. One method of stacking diodes is to use ohmic contacts and thermocompression bonding.[5] Series-connected diodes with semi-ohmic tunnel diode interconnections have been proposed as a method to increase breakdown voltage without degrading switching time.[6] Tunnel diode structures are also used in multijunction solar cells.[7] The advantage of direct bonding is a significant reduction of processing steps and their associated costs and impact on reliability and yield. Because most ohmic junctions are essentially tunnel junctions, a significant source of this improvement is the elimination of the interface metallization and thus the reduction of two metal ohmic contacts into one $p^{++}n^{++}$ semi-ohmic junction.

Between each diode of a stacked diode structure (pn/pn/pn) is an interface diode of the reverse orientation. In order for the stacked diode structure to have low overall forward voltage drop, the interface diodes must have a low resistance tunnel characteristic in the reverse bias direction. For the present application, a high-quality reverse or backward diode has minimum reverse bias resistance. In this application, performance of the tunnel diode under forward bias is not an important factor, because any drop incurred only adds to the reverse voltage, which is very large by design. An important step in fabricating a stacked diode structure is design and optimization of the interfacial tunnel diodes, which is the primary focus of this paper.

There has been some work on wafer-bonded tunnel diodes; however, that work[8] utilized hydrophilic wafer bonding which incorporates an oxide at the bond interface. The diodes reported in that work were not stable at high current densities, and the reverse voltage drop was significantly larger than for the tunnel diodes reported here. A potential method of eliminating the interface oxide found in hydrophilic wafer bonding is a high-temperature anneal (>1000°C),[9] which has implications for maintaining the abrupt nature of the dopant profiles. Figure 1 shows simple calculations of dopant diffusion for a variety of temperatures and times, using the familiar diffusion approximation $x = 2\sqrt{Dt}$, with the constants for B diffusing in Si as $D_0 = 0.76$ and $E_a = 3.46$ eV, and P diffusing in Si as $D_0 = 3.85$ and $E_a = 3.66$ eV.[10] As can be seen, an anneal of 1000°C, even for short times, has a significant effect on the doping profile of the wafers. For example, a 10 s anneal at 1000°C allows boron to diffuse 10 nm in silicon. Thus, for wafer-bonded tunnel diodes with precisely engineered dopant profiles, it is important to utilize a low-temperature process. An advantage of using low-temperature hydrophobic direct wafer bonding to fabricate tunnel diodes is that it has the capability of producing extremely abrupt junctions.

Experimental

Backward tunnel diodes were fabricated by direct hydrophobic bonding of a highly doped p-type wafer to a highly doped n-type wafer. The wafers were 125 mm diam (001) Czochralski (CZ) silicon. A 30 nm screening oxide was grown on all wafers at 925°C. The n-type wafers were arsenic doped to approximately to 1×10^{19}/cm^3 with nominal resistivity of between 0.0015 and 0.0070 Ω cm and were implanted with phosphorus with a 5×10^{15}/cm^2 dose and 110 keV energy on a high-current implant tool. The p-type wafers were (001) boron-doped to approximately 5×10^{18}/cm^3 with a nominal resistivity of between 0.0090 and 0.020 Ω cm. The p-type wafers were implanted with boron at a dose of 1×10^{16}/cm^2 and energy of 40 keV. All wafers were annealed at 600°C for 1 h to remove implant damage followed by a rapid thermal anneal of 1000°C for 1 min to activate the implants. They were then thinned with a DISCO grinder to approximately 200 μm each to render the heavily doped wafers infrared (IR) transparent.

The wafers underwent the following cleaning and bonding preparation steps: Oxygen plasma clean in a Plasma Preen system with a pressure of approximately 200 mTorr, an oxygen flow rate of 2 sccm, and power of 425 W for 5 min; 10 min ultrasonic clean in Piranha ($4{:}1 :: H_2SO_4{:}H_2O_2$) at 40°C; 10 min flowing deionized water; 4000 rpm spin dry for 60 s in atmosphere and at room temperature; UV/ozone (Samco model UV-1 with 110 W low-pressure Hg lamp) for 20 min at 150°C, 0.5 L/min O_2; 10 min ultrasonic clean in SC1 ($NH_4OH{:}H_2O_2{:}4H_2O$) at 40°C; 10 min flowing deionized water; 180 s in dilute 1:10 HF dip (until hydrophobic); spin dry as previously. The wafers were bonded immediately after the spin dry step and annealed at various temperatures using furnace anneals (FA) and rapid thermal anneals (RTA) as outlined later. Wafer bonding was performed manually in a jig fabricated out of Teflon. Unless otherwise stated, processing steps occurred at room temperature and ambient atmosphere. After the bonding step, there was a significant amount of particle-related interfacial voids observed using infrared transmission imaging. This was most likely due to processing damage that occurred during the implant and thin-

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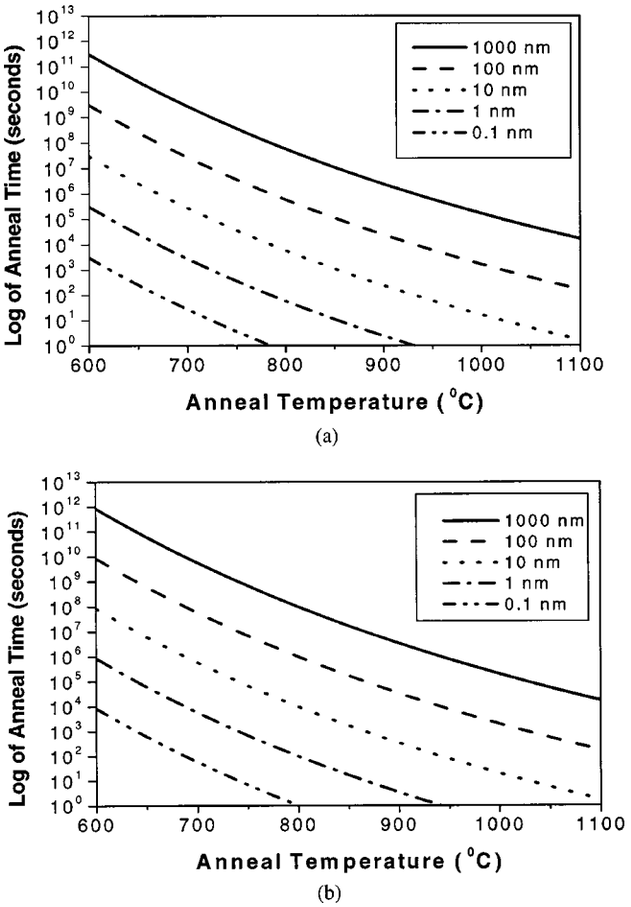
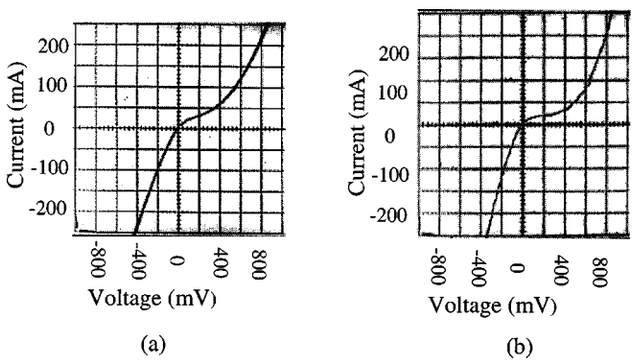


Figure 1. Constant dopant (P and B) diffusion lengths in silicon as a function of anneal time and temperature: diffusion lengths for (a) boron and (b) phosphorus in silicon.



ning steps. While the void areas eventually delaminated, the bonded regions yielded useful devices. There were also voids noted due to thermal desorption of hydrogen after the anneal steps. The number of voids is low, and the void size is large for typical 400°C furnace anneals. For the RTA samples, there is a high density of voids and the size is too small to be observed using IR transmission techniques.

To complete diode fabrication, the wafers were metallized with 500 nm Al/50 nm Ti/50 nm Pt/200 nm Au using electron-beam evaporation. To isolate individual diodes, wafers were placed on a diamond saw with the blade depth set to cut through the top wafer and part way into the lower wafer. This provided electrical isolation of the diodes on one side and the ability to probe individual diodes with a common (back side) ground. The dicing blade was approximately 50 μm wide and the cut pitch was 0.5, 1.0, and 2.0 mm, resulting in six combinations of diode geometry ($2 \times 2, 2 \times 1$...). The 0.5 mm square diodes were the preferred test structure, because the square geometry minimized edge effects and the small size lowered the current requirements needed to obtain 100 A/cm^2, the target operation current of the stacked diode. The actual area of the nominal 0.5×0.5 mm square diodes was 0.2025 mm^2, which accounts for the blade thickness. A sidewall etch step was necessary to remove damage from the sawing step for minimum reverse resistance. Figure 2 is a comparison of no sidewall etch to sidewall etch of 90 s in $10{:}1 :: HNO_3 : HF$, which etches approximately 10 μm.

Electrical testing was performed on a Tektronix Type 576 Curve Tracer. A four-probe measurement technique was used with two probes providing the current and two probes measuring the voltage. This arrangement eliminates the measurement error associated with the resistance of the probes and leads as well as the probe to metal contact resistance.

Results and Discussion

A study was performed to optimize the diode fabrication process to reduce interfacial voids, maximize device performance, and generate sufficient bond strength to allow wafer dicing. Initially, a moderately high-temperature RTA was thought to produce void-free bonds; however, acoustic microscopy inspection indicated that the rapid thermal processing resulted in a high density of small voids due to hydrogen desorption as typically experienced at temperatures from 400 to 800°C.[11] FAs at temperatures <800°C result in few large voids, while RTAs result in many small voids. By combining an initial FA at 400°C with a subsequent RTA at higher temperatures, the voids due to desorption occur only as in the 400°C case, which is a few large voids. Thus, it is possible to avoid the high density of voids typically experienced in RTA. Further, it was found that at a minimum, a furnace anneal of 400°C for 5 h was required for sufficient bond strength, approximately 300-400 ergs/cm^2, to saw a 125 mm wafer pair into several smaller pieces to study annealing effects without subsequent wafer delamination. The FA, with a ramp rate of approximately 0.5°C/s, produced a few large voids which resulted in some diode structures failing during wafer dicing and diode processing. The simple diffusion calculations also indicated that the 400°C anneals would not have a significant effect on the doping profile as compared to subsequent RTA processing. After the FA, wafers were RTA annealed at a ramp rate of 100°C/s at temperatures of 600-1025°C for times of 10 s (120 s for the 600°C case).

Resulting diode forward and reverse voltages at 100 A/cm^2 are shown in Fig. 3, which is achieved at approximately 200 mA. The diode shows classic backward diode characteristics for the 400 and 600°C anneals as compared with Sze.[12] With increasing anneal temperature, the diode behavior moved from that of a backward diode to a normal diode, as seen in Fig. 3e. Figure 4 is a graph of forward and reverse voltage at 100 A/cm^2 as a function anneal temperature. As can be seen, reverse diode performance is degraded slightly for anneals over 400°C, however, not significantly until a temperature of 750°C is exceeded. Any further anneal produced a significant degradation of backward diode performance. Annealing above 750°C resulted in normal diode behavior, as opposed to the desired reverse diode tunneling behavior. It is thought that diffusion of dopants either across the interface or to the interface itself results in a broadened p-n junction profile and thus depletion width, which can be viewed as the tunnel barrier width. Dopants that diffuse across the interface compensate the dopant concentration on the opposite side of the junction, resulting in an additional increase in the depletion width. The current of a tunnel diode is inversely proportional to the exponential of the depletion width.[10] The strong observed pro-

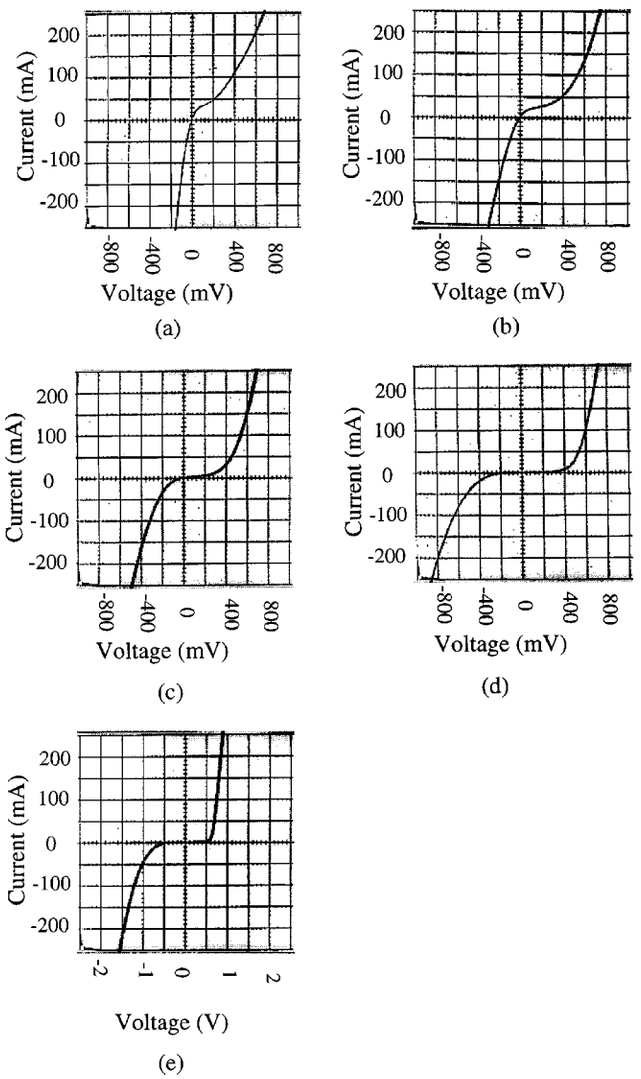
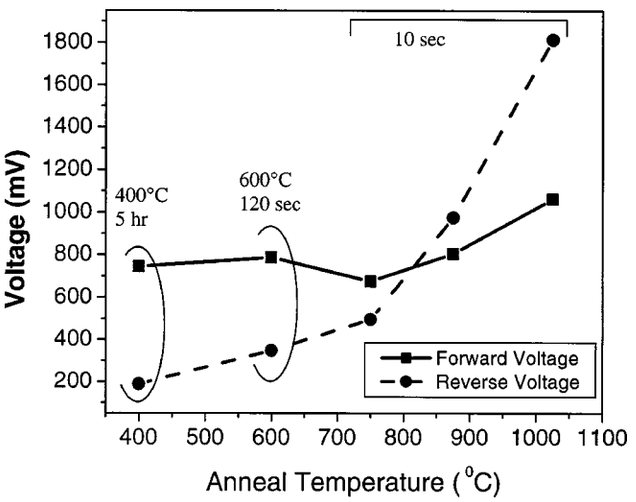


Figure 3. C-V curves for tunnel diode structures for different states of annealing ranging from 400 to 1025°C: (a) 400°C 5 h, (b) 600°C 120 s, (c) 750°C 10 s, (d) 875°C 10 s, and (e) 1025°C 10 s. (Note changed scale.)

cessing temperature dependence of the tunneling behavior indicates that the low-temperature, as-bonded junction is highly abrupt.

While forward or Esaki tunneling are observed in these diodes, the negative differential resistance region is not. The lack of negative resistance is the result of excess tunneling current in the forward direction, possibly due to interface defects.[5] There are several possible sources of defects for the excess current. Excess current is usually due to energy states in the bandgap[13] and could result from any number of sources. At the interface, there are misfit dislocations[14] and dangling silicon bonds.[15] Implant damage is another source of states in the bandgap.[13] The excess forward current is not of great concern because the primary application for this work is in the fabrication of stacked power diodes for high-blocking-voltage applications where low reverse resistance is desired. The most important characteristic for our experiment is the low reverse voltage at a target operating current of 100 A/cm^2. The voltage drop achieved for 0.5 × 0.5 mm diodes was less than 150 mV. Because the tunnel diode is a majority carrier device, it is appropriate to characterize the reverse C-V characteristics with specific resistance. Figure 3a shows diode characteristics for the processing conditions with the lowest specific resistance, which is 0.0015 Ω cm^2.



Conclusion

The results indicate it is possible to create tunnel diodes with high reverse current density and low voltage drop by using direct wafer bonding. This is an important step in realizing the stacked diode structure, which results in a compact high-voltage diode with low forward drop. Further development may be necessary to address interfacial voids and their effect on device reliability, performance, and yield.[11]

Tunnel diodes were fabricated using direct wafer bonding. The diodes performed linearly in reverse bias with only 150 mV voltage drop at 100 A/cm^2, resulting in a specific reverse resistance of 0.0015 Ω cm^2.

These diodes exhibited excess forward current, which was probably due to interfacial defects inherent to the low-temperature wafer bonding or caused by the implant step. While these devices did show evidence of tunneling under forward bias, negative differential resistance was not observed (*i.e.*, a current peak-to-valley ratio of ~1). Etching the sidewall to control damage effects was required to minimize the reverse resistance as well as excess current. Furnace anneals at 400°C for 5 h or more produced bond strength sufficient for subsequent wafer dicing and device fabrication. Further annealing at higher temperatures degraded backward diode behavior. Annealing above 750°C resulted in normal diode behavior.

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