ITSU LABORATORIES LTD.
Mr. Furuhashi, Manager of
s kind advises since the start of
lanager and Mr. Ikeda, Chief
is Optical Co. Ltd., for their
ing and manufacturing.

n of Gaussian Beam Optics," Appl.

Bulk Data Storage," Bell Lab. Rec.,

nt of Focal Lengths of Lenses,"

p. 235, Asakura, (1968).

tics," 3rd ed., p. 77, McGraw-Hill,

i and Y. Hayamizu: "Accurate
UTURI, Vol. 43, No. 12, p.1198,

4, Pergamon, (1970).

eodetic and Engineering Surveys,"

the Measurement of Small Wedge

Low Noise GaAs Field-Effect Transistors

By Shinji Ohkawa, Katsuhiko Suyama and Hajime Ishikawa

(Manuscript received November 19, 1974)

By the analysis of the noise and gain of the GaAs FET from an equivalent circuit including parasitic elements, its source series resistance and gate metallization resistance were found to have direct effects upon these items of performance. New techniques were developed to get very low contact resistance of source, drain ohmic contact and to decrease source lead inductance. The techniques for device fabrication and epitaxial growth were improved. Applying these techniques, a GaAs FET having good high frequency performance (NF 4.9db at 8GHz) was developed.

1. Introduction

GaAs field-effect transistors with Schottky-barrier gates were proposed by Mead[1]. The GaAs with its high electron mobility were expected to have excellent features for fabrication of microwave FET's. Recent advances in GaAs materials and fabrication technology have made possible good high-frequency performance of GaAs FET's[2,3].

In order to realize low noise GaAs FET's, noise behavior together with high gain performance has to be taken into account. In this paper, the design and performance of low noise GaAs FET's are described. Gain and noise parameters of the GaAs FET including parasitic elements are derived in chapter 2. Chapter 3 describes fabrication process and technology of GaAs FET, especially for low ohmic contacts. In chapter 4, measured small-signal and noise parameters of the GaAs FET are shown.

2. Design consideration

2.1 Small-signal properties of the intrinsic FET

The small-signal behavior of the intrinsic GaAs FET can be described by the

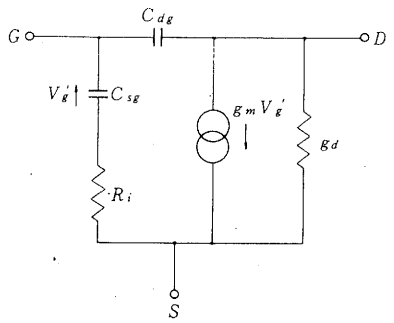


Fig. 1—Intrinsic equivalent circuit of the GaAs FET.

equivalent circuit shown in Fig. 1. In this diagram the gate input circuit of the FET consists of the gate capacitance C_{sg} and the effective channel resistance R_i. The drain current is controlled by the effective input voltage applied to C_{sg}.

The current-voltage characteristics of the FET have been calculated from Shockley's gradual channel approximation[4]. Since a microwave FET has a gate length as small as 1 μm, the saturation of the electron drift velocity has to be taken into account. The electric field in the channel can reach the saturation field of about 3 kV/cm at a relatively small values of drain-source voltage, therefore the electron drift velocity reaches 2×10^7 cm/s.

In order to calculate the small-signal parameters, the electron drift velocity is approximated[5] by

$$v_d = \frac{\mu_0 E}{1 + \mu_0 E / v_s} \quad \cdots\cdots\cdots (1)$$

where μ_0 is the low-field mobility and v_s is the saturation drift velocity. Figure 2 shows the transconductance g_m as a function of the doping density N_D in the current saturation or pinch-off region. This figure indicates that g_m is nearly proportional to $N_D^{1/2}$. The drain saturation current is represented approximately by:

$$I_{DSS} \doteqdot \frac{1}{2} g_m V_p \quad \cdots\cdots\cdots (2)$$

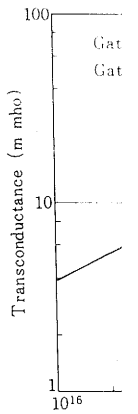
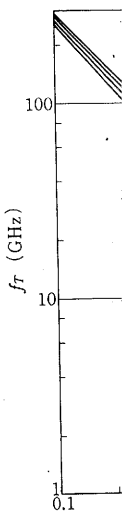
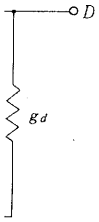


Fig. 2—Tran



Fig



the GaAs FET.

n the gate input circuit of the
effective channel resistance R_i.
ut voltage applied to C_{sg}.
T have been calculated from
a microwave FET has a gate
ctron drift velocity has to be
nnel can reach the saturation
alues of drain-source voltage,
^{7} cm/s.
ers, the electron drift velocity

. . . . . (1)

ration drift velocity. Figure 2
the doping density N_D in the
e indicates that g_m is nearly
is represented approximately

. . . . . (2)

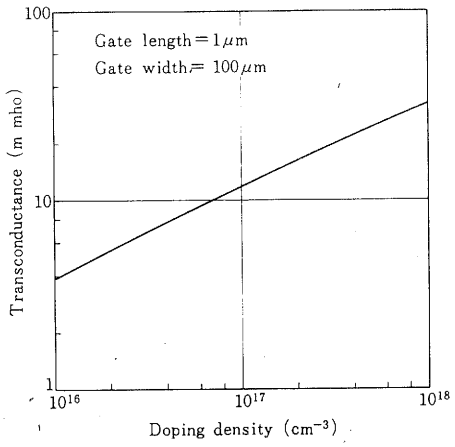


Fig. 2—Transconductance versus doping density.

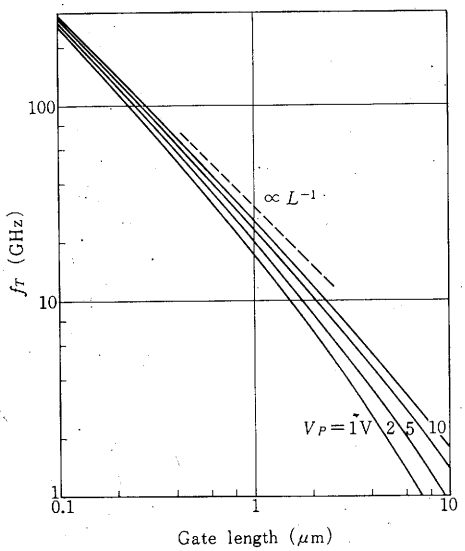


Fig. 3—f_T versus channel length.

where V_p is the pinch-off voltage. The current cut-off frequency f_T as a function of the channel length L with V_p as a parameter is shown in Fig. 3. It was predicted that f_T was proportional to $1/L^2$ by Shockley's classical theory. For short gate lengths, however, f_T is proportional to $1/L$ rather than $1/L^2$. This result suggests that g_m is almost independent of L due to the drift velocity saturation while C_{sg} is proportional to L.

2.2 High-frequency performance of the FET with the extrinsic elements

In order to describe the small-signal behavior of the FET properly, the parasitic elements have to be taken into account. The source series resistance R_s, the gate metallization resistance R_g, the Miller feedback capacitance C_{dg} and the

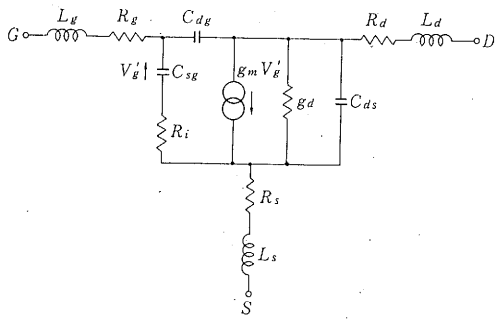


Fig. 4—Equivalent circuit of the FET including the parasitic elements.

Table 1. Typical values of equivalent circuit elements of GaAs FET

$V_{DS}=4$V $I_{DS}=15$ mA Gate: 1.5μm x 300μm	
g_m = 22 mmho	C_{sg} = 0.75 pF
g_d = 2.1 mmho	C_{dg} = 0.035 pF
R_g = 2.5 ohms	L_s = 0.07 nH
R_s = 5 ohms	L_g = 0.6 nH
R_d = 8 ohms	L_d = 0.4 nH
f_T = 4.5 GHz	

common source lead inductar
lead inductance L_g is likel
frequencies. L_g and L_s toget
resonance frequency, the eff
constant and above that f
frequency. In this situation, t
rather than a voltage controll
similer to a bipolar transistor.

Figure 4 represents the
including the extrinsic eleme
Typical values of the equivaler
equivalent circuit, the h-param

$$h_{11} = (R_i + R_s + R_g$$

$$- \frac{1}{\omega C_{sg}} (1 +$$

$$h_{12} = \left\{ \frac{C_{dg}}{C_{sg}} + (g_d +$$

$$+ j\omega \left\{ C_{dg}(R_i$$

$$h_{21} = - \left\{ \frac{C_{dg}}{C_{sg}} + (g_d$$

$$h_{22} = (g_d + \omega_T C_{dg})$$

with

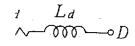
$$\omega_T = 2\pi f_T = \frac{g}{C_{sg}}$$

From these h-parameters
Neglecting the real part of h
maximum stable gain.

ff frequency f_T as a function
r is shown in Fig. 3. It was
ockley's classical theory. For
$1/L$ rather than $1/L^2$. This
L due to the drift velocity

ıe extrinsic elements

r of the FET properly, the
ıe source series resistance R_s,
ack capacitance C_{dg} and the



ıe parasitic elements.

ıents of GaAs FET

μm x.300μm

pF
5 pF
nH
nH
nH

common source lead inductance L_s are of particular interest. Besides, the gate lead inductance L_g is likely to dominate the input impedance at high frequencies. L_g and L_s together with C_{sg} form a resonance circuit. Near the resonance frequency, the effective input voltage applied to C_{sg} is no longer constant and above that frequency, it decreases rapidly with increasing frequency. In this situation, the FET is regarded as a current controlled device rather than a voltage controlled device for the convenience of analysis, which is similer to a bipolar transistor.

Figure 4 represents the common source equivalent circuit of the FET including the extrinsic elements, which is valid up to microwave frequencies. Typical values of the equivalent circuit elements are shown in Table 1. From this equivalent circuit, the h-parameters of the FET are approximately as follows:

$$h_{11} = (R_i + R_s + R_g + \omega_T L_s) + j\left\{\omega(L_s + L_g) - \frac{1}{\omega C_{sg}}(1 + g_m R_s)\right\}, \quad \cdots\cdots\cdots (3)$$

$$h_{12} = \left\{\frac{C_{dg}}{C_{sg}} + (g_d + \omega_T C_{dg})R_s - \omega^2 (C_{dg} + C_{ds})L_s\right\} + j\omega\left\{C_{dg}(R_i + R_s) + (g_d + \omega_T C_{dg})L_s\right\}, \quad \cdots\cdots\cdots (4)$$

$$h_{21} = -\left\{\frac{C_{dg}}{C_{sg}} + (g_d + \omega_T C_{dg})R_s - \omega^2 (C_{dg} + C_{ds})L_s\right\} - j\frac{\omega_T}{\omega}, \quad \cdots (5)$$

$$h_{22} = (g_d + \omega_T C_{dg}) + j\omega(C_{dg} + C_{ds}) \quad \cdots\cdots\cdots (6)$$

with

$$\omega_T = 2\pi f_T = \frac{g_m}{C_{sg} + C_{dg}}. \quad \cdots\cdots\cdots (7)$$

From these h-parameters, the gain parameters of the FET can be calculated. Neglecting the real part of h_{21} and higher order terms of ω, one obtains the maximum stable gain.

$$G_{MS} = \left| \frac{h_{21}}{h_{12}} \right| = \left(\frac{f_T}{f} \right) \Big/ \left\{ \frac{C_{dg}}{C_{sg}} + (g_d + \omega_T C_{dg}) R_s \right\}. \quad \cdots\cdots\cdots (8)$$

The stability factor K is given by,

$$K = \frac{2\,R_e\,(h_{11}) \cdot R_e\,(h_{22}) - R_e\,(h_{12} \cdot h_{21})}{|h_{12} \cdot h_{21}|}. \quad \cdots\cdots\cdots (9)$$

By the use of the equivalent circuit elements it is represented as

$$K = \left(\frac{f}{f_T} \right) \frac{2\,g_d \left(R_i + R_s + R_g + \dfrac{\omega_T L_s}{2} \right) + \omega_T C_{dg} (R_i + R_s + 2R_g + \omega_T L_s)}{\dfrac{C_{dg}}{C_{sg}} + (g_d + \omega_T C_{dg}) R_s}. \quad \cdots\cdots\cdots (10)$$

when $K \geqq 1$, the maximum available gain is defined by,

$$G_{MA} = \left| \frac{h_{21}}{h_{12}} \right| \frac{1}{K + \sqrt{K^2 - 1}}. \quad \cdots\cdots\cdots (11)$$

If $K^2 \gg 1$, which holds at sufficiently high frequencies, G_{MA} is approximated by,

$$G_{MA} \fallingdotseq \left| \frac{h_{21}}{h_{12}} \right| \frac{1}{2K}. \quad \cdots\cdots\cdots (11\text{-b})$$

Putting equations (8) and (10) into equation (11-b), one obtains,

$$G_{MA} \fallingdotseq \left(\frac{f_T}{f} \right)^2 \Big/ \left\{ 4\,g_d \left(R_i + R_s + R_g + \frac{\omega_T L_s}{2} \right) + 2\omega_T C_{dg} (R_i + R_s + 2R_g + \omega_T L_s) \right\}. \quad \cdots\cdots\cdots (12)$$

The unilateral gain is given by

$$U = \frac{|}{4\{R_e(h_{11}) \cdot R_e}$$

In the equivalent circuit form,

$$U = \left(\frac{f_T}{f} \right)^2 \Big/ \left\{ 4g_d (R \right.$$

From equations (12) and
drop per octave for frequency
frequency of oscillation f_{max}

$$f_{max} = f_T \Big/ \left\{ 2\sqrt{g_d (R} \right.$$

To improve the gain char
input resistance and the c
resistances R_s and R_g add to
possible. In addition, the
capacitance C_{dg} degrade the
feedback effects. They should

2.3 Noise parameters calculat

The noise equivalent ci
elements is shown in Fig. 5.
caused by the thermal noise c
effects[6]. It is written as

$$\langle i_{nd}^2 \rangle = 4k_B T \Delta f g_n$$

where k_B is Boltzmann's
bandwidth and P is a consta
noise is induced by the capac
noise source has to be intro
is written as

$\omega_T C_{dg}) R_s \Big\}$. ..... (8)

$h_{21})$ ..... (9)

epresented as

$\frac{}{g_d(R_i + R_s + 2R_g + \omega_T L_s)}$.

..... (10)

by,

..... (11)

ies, G_{MA} is approximated by,

..... (11–b)

), one obtains,

$\frac{T L_s}{2}$

$) \Big\}$. ..... (12)

$$U = \frac{|h_{12} + h_{21}|^2}{4\{R_e(h_{11}) \cdot R_e(h_{22}) + I_m(h_{12}) \cdot Im(h_{21})\}} \quad \text{..... (13)}$$

In the equivalent circuit form, it is written as

$$U = \left(\frac{f_T}{f}\right)^2 \Big/ \left\{ 4g_d(R_i + R_s + R_g) + 4\omega_T C_{dg} R_g \right\}. \quad \text{..... (14)}$$

From equations (12) and (14), it is evident that G_{MA} and U have a 6 dB drop per octave for frequency and U is slightly larger than G_{MA}. The maximum frequency of oscillation f_{max} at which U has unity gain, is written as

$$f_{max} = f_T \Big/ \left\{ 2\sqrt{g_d(R_i + R_s + R_g) + \omega_T C_{dg} R_g} \right\}. \quad \text{..... (15)}$$

To improve the gain characteristics, one should make f_T higher keeping the input resistance and the output conductance lower. Since the parasitic resistances R_s and R_g add to the input loss, they should be lowered as much as possible. In addition, the common lead inductance L_s and the feedback capacitance C_{dg} degrade the ratio of the output to input impedance due to feedback effects. They should be also made as low as possible.

2.3 Noise parameters calculation and influence of the extrinsic elements

The noise equivalent circuit of the GaAs FET including the parasitic elements is shown in Fig. 5. As is well known, the noise current source i_{nd} is caused by the thermal noise of the conducting channel, modified by modulation effects[6]. It is written as

$$\langle i_{nd}^2 \rangle = 4k_B T \Delta f g_m P \quad \text{..... (16)}$$

where k_B is Boltzmann's constant, T is absolute temperature, Δf is the bandwidth and P is a constant depending on biasing conditions. Since the gate noise is induced by the capacitive coupling between the channel and the gate, a noise source has to be introduced at the gate terminal[7]. The noise current i_{ng} is written as

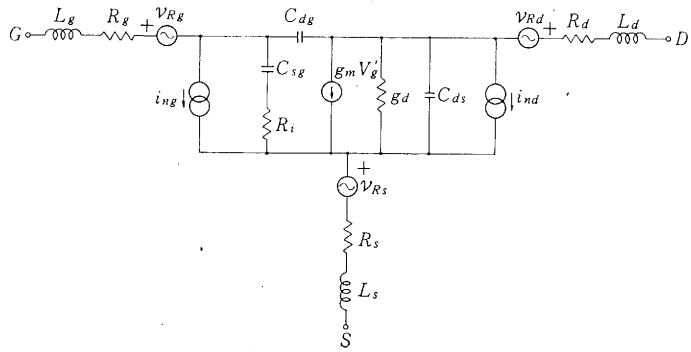


Fig. 5—Complete noise equivalent circuit of the FET.

$$\langle i_{ng}{}^2 \rangle = 4k_B T \Delta f \frac{\omega^2 C_{sg}{}^2}{g_m} R \qquad \cdots\cdots\cdots (17)$$

where R is a constant depending on biasing conditions. The two noise currents $\langle i_{nd}{}^2 \rangle$ and $\langle i_{ng}{}^2 \rangle$ come from the same origin, therefore a correlation has to be expected as

$$\langle i_{ng}\, i_{nd}^{*} \rangle = 4k_B T \Delta f j \omega C_{sg} C \qquad \cdots\cdots\cdots (18)$$

where C is a constant depending on biasing conditions. In addition, the parasitic resistances R_s, R_g and R_d show the thermal noise

$$\langle v_{nR_x}^2 \rangle = 4k_B T \Delta f R_x. \qquad \cdots\cdots\cdots (19)$$

The noise figure of a linear noisy two-port network is defined as the ratio of the total output noise power to the output noise power caused by the input noise. Therefore, the noise figure can be represented as a function of the source impedance $z_s = r_s + jx_s$ by

$$F = F_0 + \frac{G_n}{r_s}\left\{(r_s - r_{so})^2 + (x_s - x_{so})^2\right\} \qquad \cdots\cdots\cdots (20)$$

where F_o is the minimum n
impedance and G_n is the
minimum noise figure can be

$$F_0 = 1 + 2\left\{a + \sqrt{a^2}\right.$$

where

$$a = \left(\frac{f}{f_T}\right)^2 \left\{g_m R_i (P -\right.$$

$$\beta = \left(\frac{f}{f_T}\right)^2 \left\{PR - C^2\right.$$

If $\beta \gg a^2$, which holds at lower

$$F_0 \doteqdot 1 + 2\left(\frac{f}{f_T}\right)\sqrt{P}$$

It is evident that $(F_o\text{-}1)$ is
frequencies, $(F_o\text{-}1)$ is, howe
frequency f_c for noise at
changes from f to f^2, is given

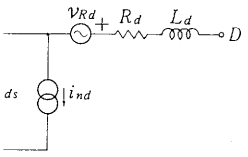
$$f_c = f_T \frac{\sqrt{PR -}}{g_m R_i (P - C)}$$

The noise conductance is exp

$$G_n = g_m \left(\frac{f}{f_T}\right)^2 (P + R$$

The real part of the optimum

$$r_{so} = \frac{1}{G_n}\sqrt{a^2 + \beta}.$$



rcuit of the FET.

. . . . . (17)

tions. The two noise currents
therefore a correlation has to

. . . . . (18)

ions. In addition, the parasitic

. . . . . (19)

work is defined as the ratio of
e power caused by the input
ed as a function of the source

. . . . . (20)

where F_o is the minimum noise figure, $z_{so} = r_{so} + jx_{so}$ *is the optimum* source impedance and G_n is the noise conductance. With respect to Fig. 5, the minimum noise figure can be calculated as

$$F_0 = 1 + 2\left\{a + \sqrt{a^2 + \beta}\right\} \quad \ldots\ldots\ldots (21)$$

where

$$a = \left(\frac{f}{f_T}\right)^2 \left\{g_m R_i (P - C) - \frac{C_{dg}}{C_{sg}} C + g_m (R_s + R_g)(P + R - 2C)\right\} \quad \ldots (22)$$

$$\beta = \left(\frac{f}{f_T}\right)^2 \left\{PR - C^2 + g_m (R_s + R_g)(P + R - 2C)\right\}. \quad \ldots\ldots\ldots (23)$$

If $\beta \gg a^2$, which holds at lower frequencies, F_o is approximated by

$$F_0 \doteq 1 + 2\left(\frac{f}{f_T}\right)\sqrt{PR - C^2 + g_m (R_s + R_g)(P + R - 2C)} \quad \ldots\ldots (24)$$

It is evident that $(F_o\text{-}1)$ is proportional to frequency f. At sufficiently high frequencies, $(F_o\text{-}1)$ is, however, proportional to f^2, because $\beta \ll a^2$. The critical frequency f_c for noise at which the frequency dependence of noise figure changes from f to f^2, is given by

$$f_c = f_T \frac{\sqrt{PR - C^2 + g_m (R_s + R_g)(P + R - 2C)}}{g_m R_i (P - C) - \frac{C_{dg}}{C_{sg}} C + g_m (R_s + R_g)(P + R - 2C)} \quad \ldots (25)$$

The noise conductance is expressed as

$$G_n = g_m \left(\frac{f}{f_T}\right)^2 (P + R - 2C). \quad \ldots\ldots\ldots (26)$$

The real part of the optimum source impedance z_{so} is written as

$$r_{so} = \frac{1}{G_n}\sqrt{a^2 + \beta}. \quad \ldots\ldots\ldots (27)$$

If $\beta \gg a^2$ i.e. $f \ll f_c$, equation (27) is approximately

$$r_{so} \doteqdot \frac{1}{\omega C_{sg}} \frac{\sqrt{PR - C^2 + g_m(R_s + R_g)(P + R - 2C)}}{P + R - 2C} \quad \cdots\cdots\cdots (28)$$

The imaginary part of z_{so} is written as

$$x_{so} = \frac{1}{\omega C_{sg}} \cdot \frac{P - C}{P + R - 2C} - \omega(L_s + L_g). \quad \cdots\cdots\cdots (29)$$

In order to realize the low noise GaAs FET, one should lower the noise figure while increasing the gain. To lower the noise figure, one should increase f_T keeping the parasitic resistances R_s and R_g lower. Fortunately, this points in the same direction as the consideration of gain. In most practical cases, both R_s and R_g are greater than the channel resistance R_i and are thus the dominant factors for noise behavior. Therefore one should make every effort to lower the parasitic resistances R_s and R_g.

3. Device fabrication

The fabrication process of a GaAs FET is illustrated in Fig. 6. A substrate was Cr-doped semi-insulating GaAs oriented to (100) on which an n-type layer doped with S was epitaxially grown by Ga-$AsCl_3$-N_2 system. Doping density and thickness of the epitaxial layer were $5 - 10 \times 10^{16}$ atoms/cm^3 and 0.2-0.4 μm, respectively.

In order to determine impurity profile, a Schottky barrier was formed on the epitaxial layer by evaporating Al. An impurity concentration N_D at a distance x from the surface was obtained by applying the following equations to the junction capacitance C_j of the barrier measured as a function of reverse biased voltage V.

$$N_D = \frac{2}{q\epsilon A^2} \left\{ \frac{d(1/C_j^2)}{dV} \right\}^{-1} \quad \cdots\cdots\cdots (30)$$

$$x = \frac{\epsilon A}{C_j} \quad \cdots\cdots\cdots (31)$$

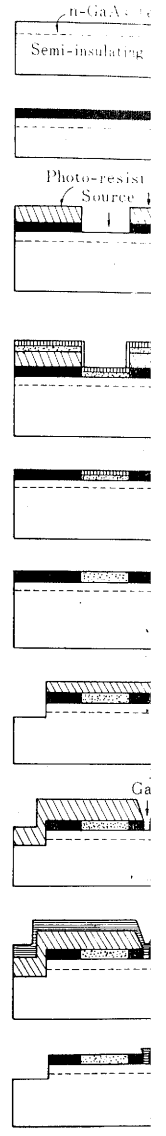


Fig. 6—Process

$\overline{R - 2C)}$ . . . . . (28)

. . . . . (29)

', one should lower the noise
figure, one should increase f_T
Fortunately, this points in the
st practical cases, both R_s and
are thus the dominant factors
ry effort to lower the parasitic

strated in Fig. 6. A substrate
00) on which an n-type layer
2 system. Doping density and
6 atoms/cm^3 and 0.2-0.4 μm,

ıottky barrier was formed on
ırity concentration N_D at a
ing the following equations to
ıred as a function of reverse

. . . . . (30)

. . . . . (31)

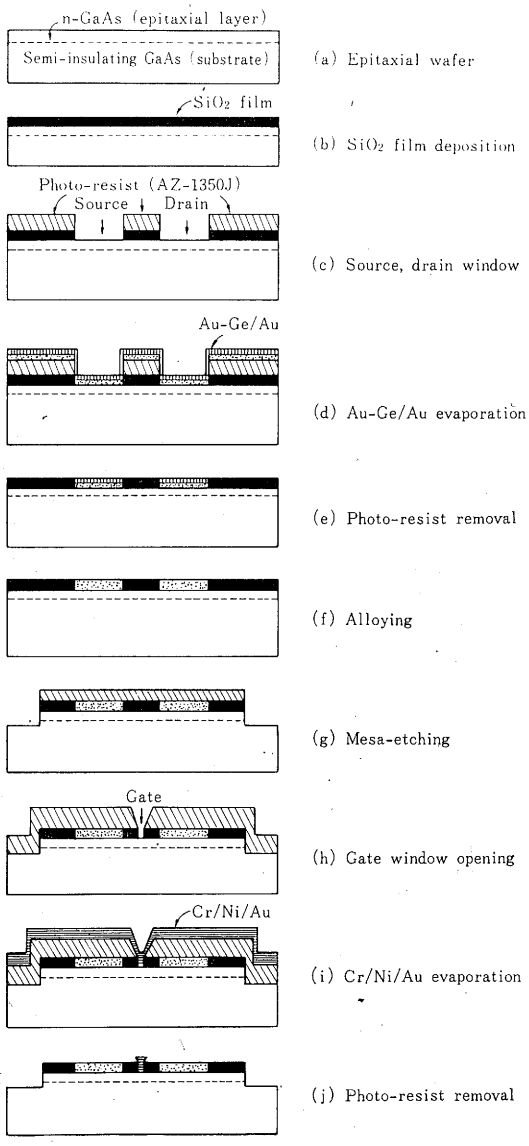


Fig. 6—Process steps for the fabrication of the GaAs FET.

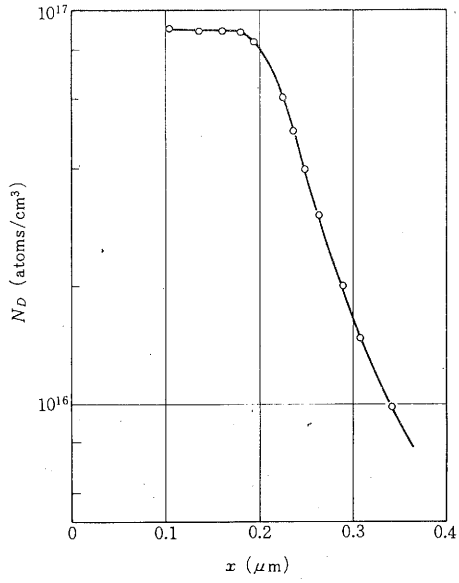


Fig. 7—Impurity profile of the GaAs epitaxal wafer.

where q is electron charge, ϵ is the permittivity of GaAs and A is the junction area. An example of the impurity profile is shown in Fig. 7. When the epitaxial layer was thicker than that needed for the device, it was thinned by chemical etching. SiO_2 film of 3000Å thick was deposited on the wafer by chemical vaper deposition using SiH_4 and O_2 for masking. The deposition was carried out at the relatively low temperature of 350°C to avoid degradation of the electrical properties of GaAs.

The ohmic source and drain contacts were made of Au-Ge alloyed into GaAs. The lift-off method was employed to define ohmic contact metal, Au-Ge, in source and drain regions, as shown in Fig. 6(c), (d) and (e). The wafer coated with SiO_2 film was covered with photo-resist film and exposed to light through a mask containing source and drain patterns. The photo-resist film was developed by dipping into developing solution so that the source and drain windows were opened in photo-resist film and also in the SiO_2 film after etching in buffered etching solution. Metal films consisting of Au-Ge of 400 Å and Au of 3000 Å

thick were deposited onto the
regions was still covered with
by immersing in removing so
regions remain covered with A
remaining metal film is the sa
mask alignment using the lift-o
that chemical etching is not n
use of a metal system, for wh
other hand, it is required that
not react with GaAs and metal
type photo-resist usually cont
these material, while positive
organic solvent inactive to the
type resist is better than that
fairly thickly. For these reaso
Shipley, was employed to fabri

An ohmic contact with
electrical characteristics of
dependent on the heating cyc
up to 450°C from room tem

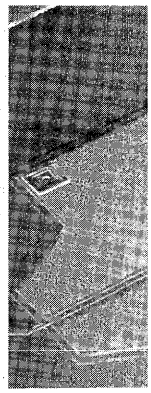
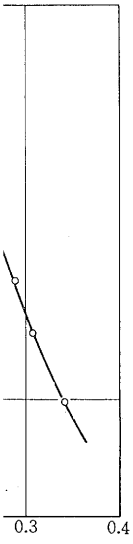


Fig. 8—Scanning e



epitaxal wafer.

f GaAs and A is the junction
ı in Fig. 7. When the epitaxial
e, it was thinned by chemical
n the wafer by chemical vaper
deposition was carried out at
l degradation of the electrical

made of Au-Ge alloyed into
ohmic contact metal, Au-Ge,
(d) and (e). The wafer coated
nd exposed to light through a
ıoto-resist film was developed
urce and drain windows were
film after etching in buffered
of 400 Å and Au of 3000 Å

thick were deposited onto the wafer all of which except for the source and drain regions was still covered with the photo-resist film. The resist film was removed by immersing in removing solution with the result that only source and drain regions remain covered with Au-Ge/Au film. Thus the shape and position of the remaining metal film is the same as the window opened in the SiO_2 film with no mask alignment using the lift-off method. This method has the further advantage that chemical etching is not needed for selective metal removal. This enables the use of a metal system, for which chemical etching is not usually applied. On the other hand, it is required that the developing solution and removing solution do not react with GaAs and metal system used here. Removing solutions of negative type photo-resist usually contain organic acid or halogens which can react with these material, while positive type photo-resist can be easily removed by an organic solvent inactive to the materials. In addition, the resolution of a positive type resist is better than that of negative type resist when resist film is coated fairly thickly. For these reasons, the positive type photo-resist, AZ-1350J by Shipley, was employed to fabricate GaAs FET.

An ohmic contact with low contact resistance is necessary for good electrical characteristics of GaAs FET. The contact resistance is greatly dependent on the heating cycle of the alloying procedure. The wafer was heated up to 450°C from room temperature within 5 sec, at which the alloying of

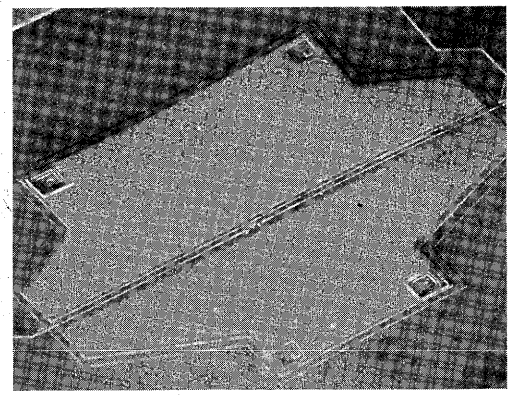


Fig. 8—Scanning electron micrograph of the finished device.

Au-Ge and GaAs was carried out in a N_2 ambient. This rapid temperature rise produces uniform alloying in whole area of the source and drain regions and this lowers the effective contact resistance.

The epitaxial layer was etched off outside the active area so that the gate bonding pad could be placed directly on the semi-insulating substrate to decrease

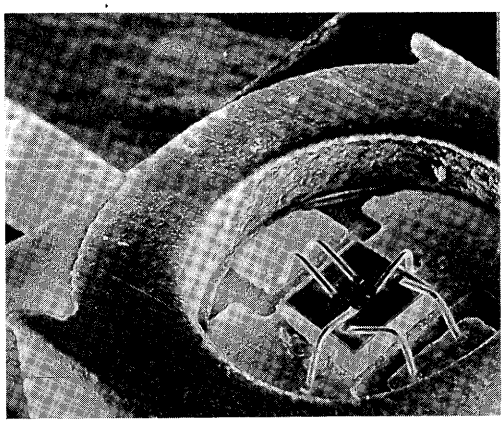


Fig. 9—Scanning electron micrograph of the GaAs FET mounted in strip-line package.

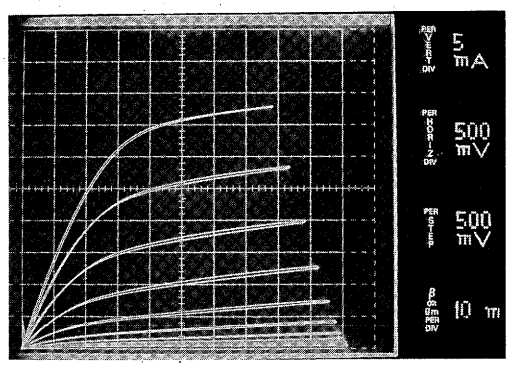


Fig. 10—d.c. current-voltage characteristics of the GaAs FET.

the capacitance under gate p

The gate Schottky barri
and Au of 3000 Å thick o
and drain. The lift-off meth

Figure 8 shows the sca
which the length and the wi
gate-source separation is 1.5

As shown in Fig. 9, t
measure its electrical chara
shown in Fig. 10.

4. Small-signal and nois

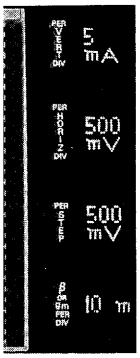
The high-frequency per
scattering-parameter measur
mounted in the strip-line pa
microstrip test fixture show
measured over the frequen
Model 8410A), are shown i
calculated from these s-parar

Fig. 11

. This rapid temperature rise
rce and drain regions and this

: active area so that the gate
sulating substrate to decrease

GaAs FET mounted in



ı of the GaAs FET.

the capacitance under gate pad.

The gate Schottky barrier was formed by evaporating a multi-layer of Cr, Ni and Au of 3000 Å thick onto the gate window which opened between source and drain. The lift-off method is also applicable to this gate process.

Figure 8 shows the scanning electron micrograph of the finished device in which the length and the width of gate are 1.5 μm and 300 μm, respectively, and gate-source separation is 1.5 μm.

As shown in Fig. 9, the FET was mounted into a strip-line package to measure its electrical characteristics. An example of its d.c. characteristics is shown in Fig. 10.

4. Small-signal and noise parameter measurement

The high-frequency performance of the GaAs FET is evaluated by means of scattering-parameter measurements. For these measurements, the GaAs FET is mounted in the strip-line package shown in Fig. 11 and then is inserted into the microstrip test fixture shown in Fig. 12. Typical common-source s-parameters measured over the frequency range 2-10 GHz with a network analyzer (HP's Model 8410A), are shown in Fig. 13 and 14. Figure 15 shows the h-parameters calculated from these s-parameters.

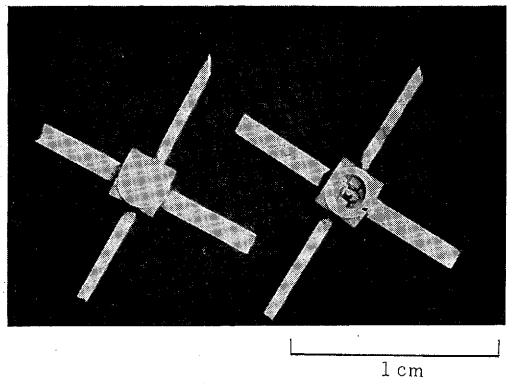


Fig. 11—Strip-line package for GaAs FET.

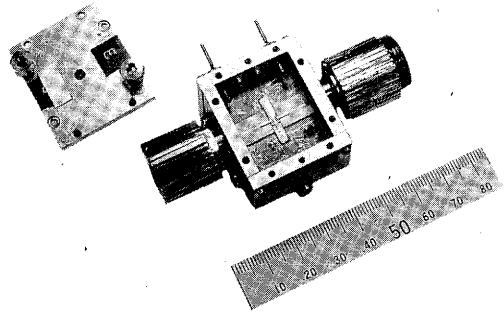


Fig. 12—Microstrip test fixture.

In order to evaluate the elements of the equivalent circuit represented in Fig. 4 completely, additional measurements are necessary. The s-parameter measurements of the FET under no biasing conditions are most important. From the equivalent circuit of Fig. 16 under no biasing conditions, the z-parameters on parasitics are as follows:

$$Z_{11} = \left(R_s + R_g + \frac{R_{ch}}{2}\right) + j\left\{\omega(L_s + L_g) - \frac{1}{\omega C_g}\right\} \quad \cdots\cdots\cdots (32)$$

$$Z_{12} = Z_{21} = \left(R_s + \frac{R_{ch}}{2}\right) + j\omega L_s \quad \cdots\cdots\cdots (33)$$

$$Z_{22} = \left(R_s + R_d + \frac{R_{ch}}{2}\right) + j\omega(L_s + L_d). \quad \cdots\cdots\cdots (34)$$

From the measured s-parameters under no biasing conditions and the above equations, the parasitic elements can be estimated. The equivalent circuit elements evaluated from the h-parameters of Fig. 15 and the z-parameters on parasitics, are listed in Table 1.

From measured s-parameters of Figs. 13 and 14, the maximum stable gain G_{MS}, the stability factor K, the maximum available gain G_{MA} and the unilateral gain U are calculated and are plotted in Fig. 17. In this figure, the values

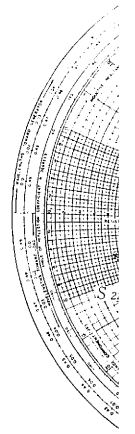


Fig. 13—s_{11} and

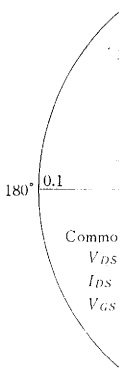


Fig. 14—s_{21} and

re.

iivalent circuit represented in
: necessary. The s-parameter
ons are most important. From
onditions, the z-parameters on

$$\left.\cdot) - \frac{1}{\omega C_g}\right\} \quad \cdots\cdots\cdots (32)$$

$$\cdots\cdots\cdots (33)$$

$$\cdots\cdots\cdots (34)$$

ng conditions and the above
ated. The equivalent circuit
15 and the z-parameters on

14, the maximum stable gain
: gain G_{MA} and the unilateral
7. In this figure, the values

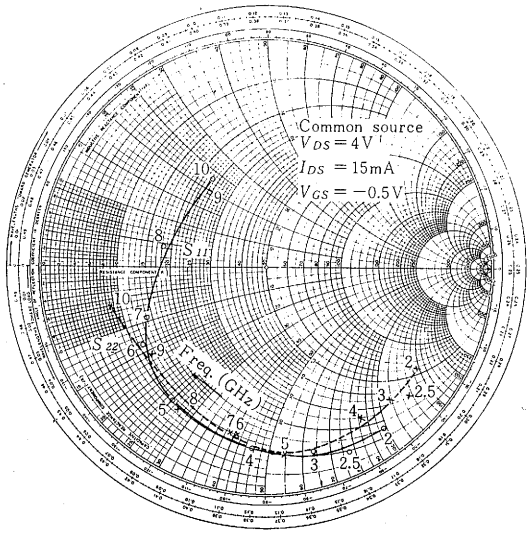


Fig. 13—s_{11} and s_{22} in a 50-ohm system for various frequencies.

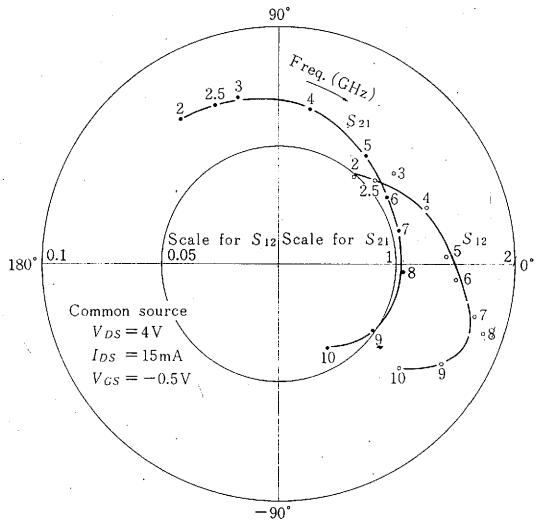


Fig. 14—s_{21} and s_{12} in a 50-ohm system for various frequencies.

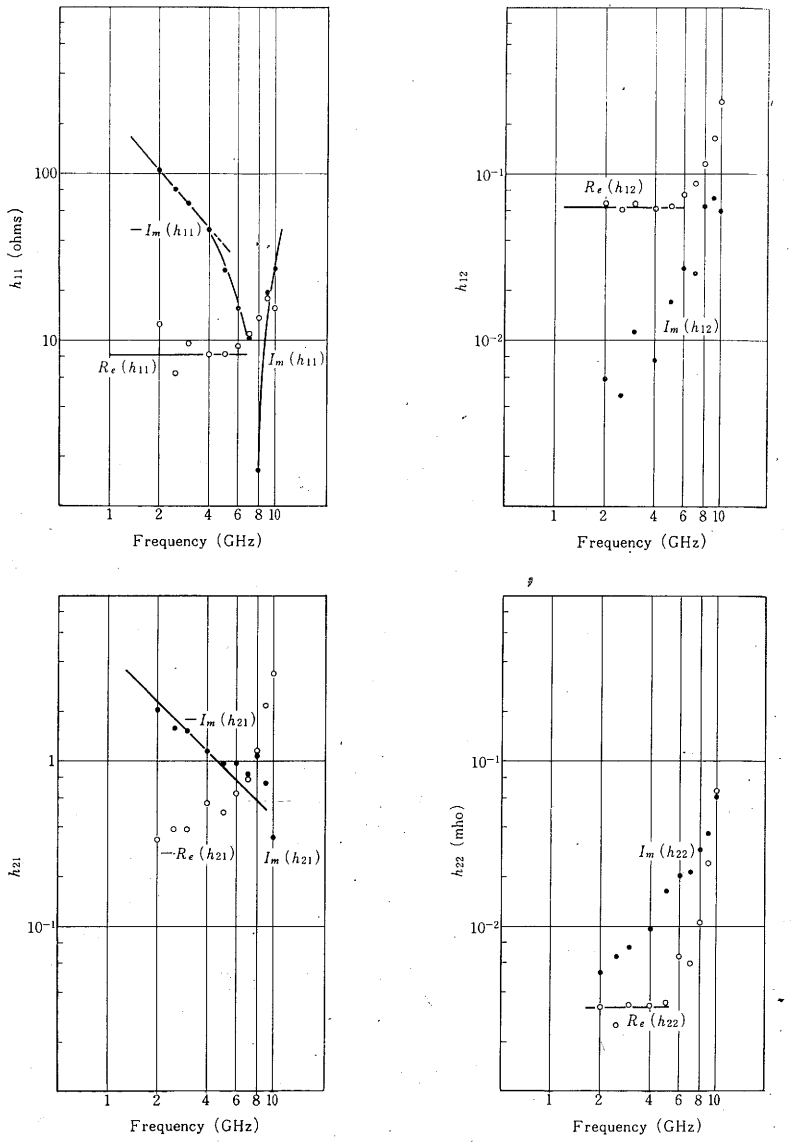


Fig. 15—h-parameters of a GaAs FET calculated from measured s-parameters at V_{DS}=4V, I_{DS}= 15mA.

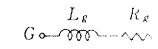


Fig. 16—Equival

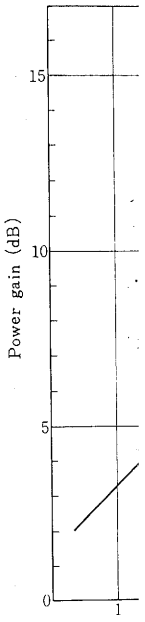
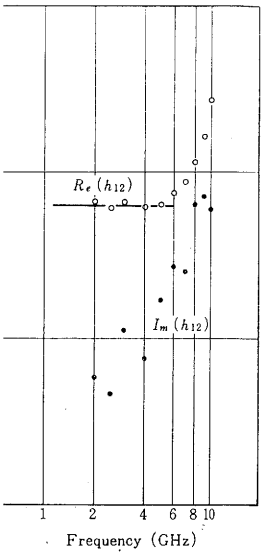
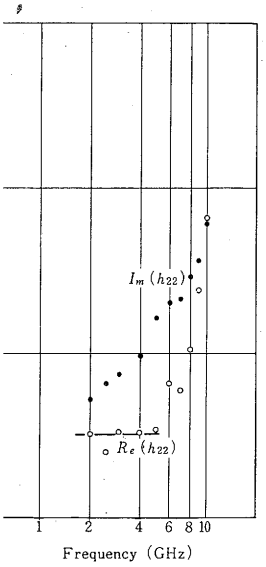


Fig. 17—Maximum st
gain and ur
measured s-
circuit.





ted from measured
A.

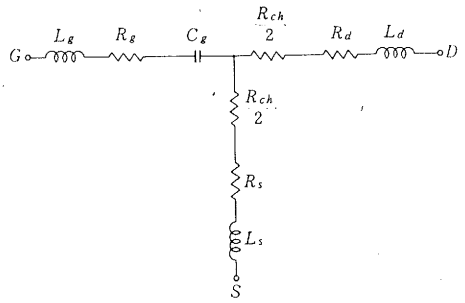


Fig. 16—Equivalent circuit under no biasing conditions.

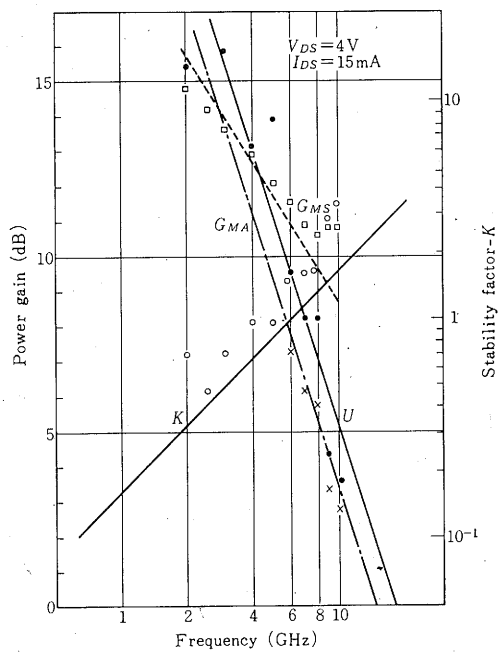


Fig. 17—Maximum stable gain, stability factor, maximum available gain and unilateral gain of a GaAs FET. Points; from measured s-parameters, lines; calculated from equivalent circuit.

calculated from the equivalent circuit or equations (8), (10), (12) and (14), are also shown with solid lines. Since K is less than unity for frequencies below 6 GHz, the device is potentially unstable and, therefore, G_{MA} is undefined. Above 6 GHz, G_{MA} is defined and is about 1.5dB less than U due to feedback effects.

The noise measurements of the GaAs FET are carried out with the test setup shown in Fig. 18. A method is used which allows measurement of the noise figure and the available gain at the same time. The test fixture is same as for the s-parameter measurements and in which input and output tuning circuits are inserted. The source impedance is adjusted by the use of the input tuning

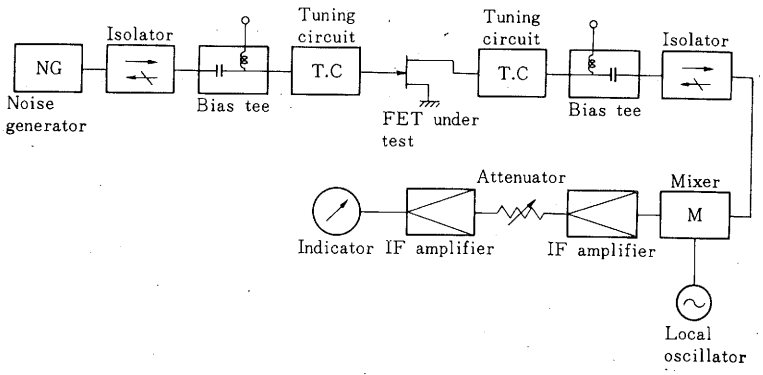


Fig. 18—Block diagram for noise measurements.

Table 2. Noise characteristics of a GaAs FET

V_{DS} = 4V I_{DS} = 10 mA

	Noise minimum concition		Gain maximum condition	
Freq. (GHz)	F_0 (dB)	G_A (dB)	F (dB)	G_{MA} (dB)
4	3.0	7.6	—	—
6	4.0	5.4	4.7	6.6
8	4.9	3.7	5.2	4.1

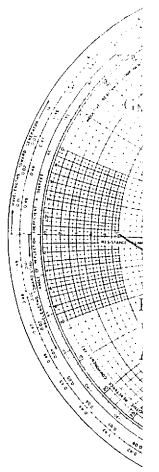


Fig. 19—Constant avai
plane at 6 GH

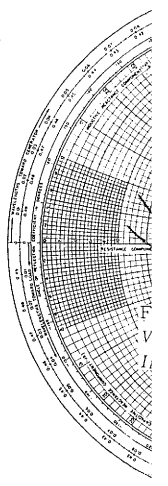
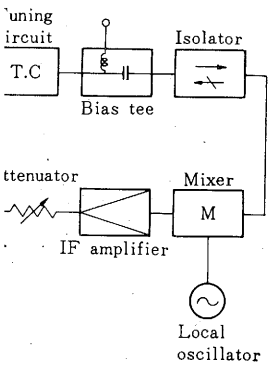


Fig. 20—Constant n
plane at 6 (

ns (8), (10), (12) and (14), are
unity for frequencies below 6
ore, G_{MA} is undefined. Above
han U due to feedback effects.
are carried out with the test
h allows measurement of the
ne. The test fixture is same as
put and output tuning circuits
y the use of the input tuning



surements.

GaAs FET

Gain maximum condition

F (dB)	G_{MA} (dB)
—	—
4.7	6.6
5.2	4.1

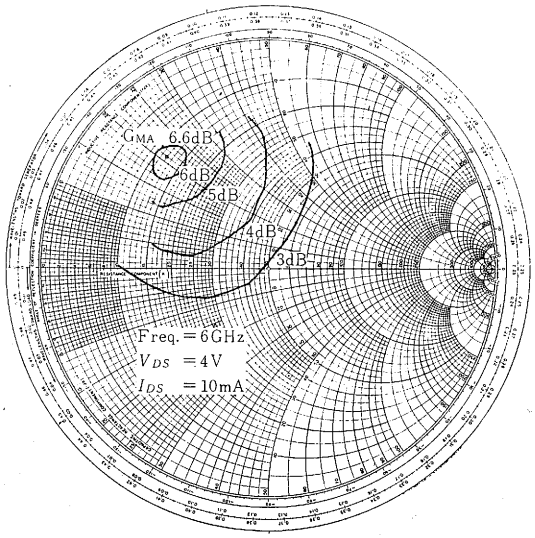


Fig. 19—Constant available gain contours plotted on source impedance plane at 6 GHz.

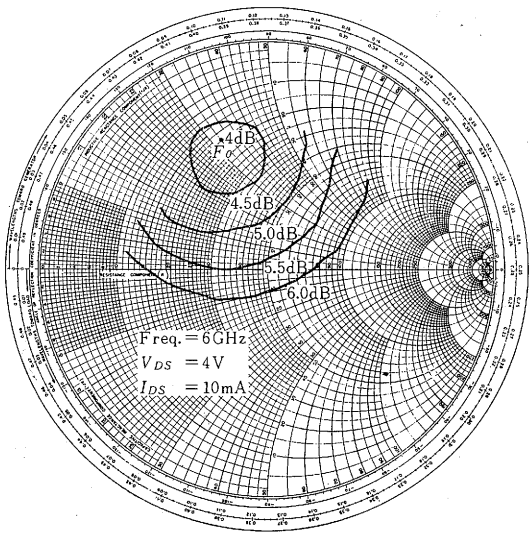


Fig. 20—Constant noise figure contours plotted on source impedance plane at 6 GHz.

circuit. The load is conjugate-matched to the FET by the output tuning circuit.

Constant available gain and constant noise figure contours plotted on the source impedance plane which are measured at 6 GHz, are shown in Figs. 19 and 20, respectively. From these figures, it is evident that the source impedance for maximum gain is different from that for optimum noise figure. These measurements are performed at frequencies 4, 6 and 8 GHz and are listed in Table 2.

5. Conclusion

In this paper, described is the development of GaAs low noise microwave FET in our laboratories.

The authors found that source series resistance, gate metallization resistance and source lead inductance have direct effects upon the performance of the FET by analysis using the equivalent circuit of the FET which includes parasitic elements. From these results, we developed the low noise FET and got NF= 4.9 dB at 8GHz.

In the near future, by the up-grading of the epitaxial layer and the introduction of a buffer layer, it is possible to decrease the noise figure and increase the high frequency performance of the FET.

As to other applications of the GaAs FET, we are developing a high speed logic IC.

6. Acknowledgement

The authors wish to thank Dr. T. Misugi, Mr. Y. Fukukawa, and Dr. M. Maeda for valuable guidance, Dr. O. Ryuzan, and the staff of Semiconductor Materials Laboratory for their cooperative study of epitaxial growth, the staff of the GaAs FET group of Semiconductor Laboratory for device fabrication and evaluation.

References

1. C.A. Mead: "Schottky Barrier Gate Field Effect Transistor," Proc. IEEE, Vol. 54, No. 2, pp. 307-308, Feb., (1966).
2. C.A. Liechti et al.: "GaAs Microwave Schottky-Gate FET," ISSCC Digest Tech. Papers, pp. 158-159, (1972).

3. W. Baechtold et al.: "Si Transistors, "Electron. Le
4. W. Shockley: "A Unipol 1365-1376, Nov., (1952).
5. K. Lehovec and R. Zulee Hot Electron Range," Soli
6. A. Van der Ziel: "Therma 8, pp. 1808-1812, Aug., (1
7. idem; "Gate Noise in Fiel IEEE, Vol. 51, No. 3, pp.

l' by the output tuning circuit.
'igure contours plotted on the
6 GHz, are shown in Figs. 19
lent that the source impedance
optimum noise figure. These
and 8 GHz and are listed in

of GaAs low noise microwave

e, gate metallization resistance
upon the performance of the
e FET which includes parasitic
ow noise FET and got NF= 4.9

the epitaxial layer and the
decrease the noise figure and
T.
e are developing a high speed

lr. Y. Fukukawa, and Dr. M.
d the staff of Semiconductor
f epitaxial growth, the staff of
ory for device fabrication and

nsistor," Proc. IEEE, Vol. 54, No.

FET," ISSCC Digest Tech. Papers,

3. W. Baechtold et al.: "Si and GaAs 0.5 μm – Gate Schottky-Barrier Field – Effect Transistors, "Electron. Lett., Vol. 9, No. 10, pp. 232-234, May, (1973).
4. W. Shockley: "A Unipolar Field-Effect Transistor," Proc. IRE, Vol. 40, No. 11, pp. 1365-1376, Nov., (1952).
5. K. Lehovec and R. Zuleeg: "Voltage-Current Characteristics of GaAs J-FET's in the Hot Electron Range," Solid-State Electron., Vol. 13, pp. 1415-1426, (1970).
6. A. Van der Ziel: "Thermal Noise in Field-Effect Transistors," Proc. IRE, Vol. 50, No. 8, pp. 1808-1812, Aug., (1962).
7. idem; "Gate Noise in Field Effect Transistors at Moderately High Frequencies," Proc. IEEE, Vol. 51, No. 3, pp. 461-467, Mar., (1963).