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Experimental Study on the Subthreshold Swing of Silicon Nanowire Transistors

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SOI based wrap-gate silicon nanowire FETs are fabricated through electron beam lithography and wet etching. Dry thermal oxidation is used to further reduce the patterned fins cross section and transfer them into nanowires. Silicon nanowire FETs with different nanowire widths varying from 60 nm to 200 nm are fabricated and the number of the nanowires contained in a channel is also varied. The on-current (I_{ON}) and off-current (I_{OFF}) of the fabricated silicon nanowire FET are 0.59 μA and 0.19 nA respectively. The subthreshold swing (SS) and the drain induced barrier lowering are 580 mV/dec and 149 mV/V respectively due to the 30 nm thick gate oxide and 10^{15} cm^{-3} lightly doped silicon nanowire channel. The nanowire width dependence of SS is shown and attributed to the fact that the side-gate parts of a wrap gate play a more effectual role as the nanowires in a channel get narrower. It seems the nanowire number in a channel has no effect on SS because the side-gate parts fill in the space between two adjacent nanowires.

Keywords: Subthreshold Swing (SS), Silicon-on-Insulator (SOI), Nanowire, Wrap Gate, Side Gates.

RESEARCH ARTICLE

1. INTRODUCTION

The subthreshold swing (SS) degradation is one of the main short channel effects (SCEs) and thus SS is an important parameter for determining the scalability of the MOS transistors.[1]

There has been many presented models for SS of devices with single gate,[2] double gates,[3] tri-gates[4] and cylindrical gate-all-around (GAA) structures.[5] Many simulations show that by decreasing Si film thickness and adoping multi-gate structures the SS can be improved.[2,4,6–8] Experimentally, Kedzierski et al.[9] have reported that SS of a silicon-on-insulator (SOI) based double-gate FET decreases with the increasing ratio of effective channel length to Si film thickness. Suk et al.[10] have reported an SS increase when the nanowire diameter is below 4 nm. It was attributed to the enhanced influence of surface conditions on the channel with smaller nanowires, and also the vertical electrical field increase causing oxide trapping easily. However, Suk's study object is nanowire FETs with nanowire diameter below 10 nm, where quantum effects would play a role.

In this work, SOI based wrap-gate silicon nanowire FETs are fabricated through electron beam lithography, wet etching and thermal oxidation. Silicon nanowire FETs with different nanowire widths varying from 60 nm to 200 nm are fabricated and the number of the nanowires contained in a channel is also varied. The output characteristic and the transfer characteristic of the fabricated silicon nanowire FET are analysed. Furthermore, the nanowire width dependence of SS is explained and the effect of nanowire number on SS is investigated.

2. EXPERIMENTAL DETAILS

The fabrication flow of the silicon nanowire FETs is illustrated in Figure 1. Boron doped ($\rho = 10\ \Omega \cdot cm$) (100) SOI wafers with top silicon thickness of 55 nm was used as a starting material. 25 nm thick silicon dioxide hardmask was obtained by wet thermal oxidation at 875 °C. Electron-beam lithography was performed to define the active region mesa and the multiple finlike channels in poly-methyl methacrylate (PMMA) resist. The pattern was transferred to the silicon dioxide hardmask by isotropic wet etching in buffered hydrofluoric acid (BHF) solution, and then to SOI using anisotropic wet etching in tetramethyl-ammonium-hydroxide (TMAH) solution. As shown in Figure 2(a), the fins in a FET channel can be patterned as narrow as 30 nm. After the silicon dioxide

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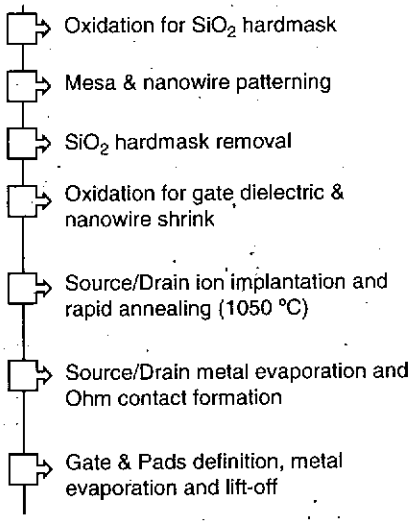

Fig. 1. Fabrication flow of the silicon nanowire FETs.

hardmask removal by BHF solution, dry themal oxidation was carried out at 900 °C for 60 minutes to shrink the fins into nanowires and also to grow the gate dielectric. The second time electron-beam lithography was performed to define the windows in PMMA resist for source/drain ion implantation. Following the selective removal of dry oxide in source/drain regions, phosphorous ion was implanted with 12 keV in energy and 1×10^{15} cm^{-2} in dose and activated using a spike anneal at 1050 °C. Then the third time electron-beam lithography was executed to define the source/drain contact windows in PMMA resist. 10 nm thick nickel film was deposited by electron-beam evaporation and then was lifted off, followed with an alloy process to form NiSi silicide contact to the source/drain regions.

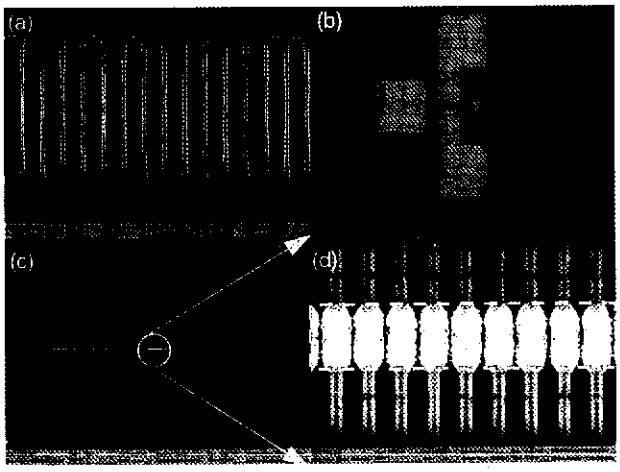

Fig. 2. (a) SEM image of the fins in a FET channel after anisotropic wet etching of silicon, the fin width is 30 nm. (b) Optic microscope image of the fabricated multi-nanowire FET after gate and pads formation at magnification of 200. (c) SEM image of the same device as (b) at magnification of 1 k. (d) SEM image of the multi-nanowire channel of the FET at magnification of 40 k, the aluminum gate is shown in the dashed box.

The fourth time electron-beam lithography was carried out to define the gate and source/drain electrodes in PMMA resist, and the device fabrication process was finished with aluminum evaporation and lift off to form the metal gate and electrode pads.

Figures 2(b, c and d) show the optic microscope image and the SEM images of the fabricated multi-nanowire FET after gate and pads formation. The aluminum gate, shown inside the dashed box in Figure 2(d), wraps the middle part of the nanowire channel. The device dimensions are 30 nm in channel thickness, 1.8 μm in channel length, 30 nm in gate oxide thickness and 630 nm in physical gate length. Devices with different silicon nanowire (core) widths varying from 60 nm to 200 nm were fabricated and the number of the silicon nanowires contained in a channel was also varied.

3. RESULTS AND DISCUSSION

Figure 3 shows the output characteristic (the I_D–V_D curves, where I_D is the drain current and V_D is the drain voltage) of a silicon nanowire FET with 30 nm thick and 60 nm wide nanowires. As shown in Figure 3, with the gate voltage (V_G) increasing, the separation between two adjacent curves first increases till $V_G = 3$ V and then decreases. The increase is due to the square-law dependence of drain current upon gate voltage in the saturation region, while the decrease is due to the mobility degradation under high gate voltage resulting in transconductance (g_m) degradation. This can be seen more evidently in the transfer characteristic discussed below.

Figure 4 shows the transfer characteristic (linear plot and semilog plot of the I_D–V_G curve) of the same nanowire FET at 0.1 V drain bias. The threshold voltage (V_{TH}) of this FET is 1.55 V extrapolated from the g_m–V_G curve and 3 V extrapolated from the $I_D/g_m^{0.5}$–V_G curve, both of which are extracted from the linear operation region of the FET. Though the threshold voltage extrapolation from the $I_D/g_m^{0.5}$–V_G curve is demonstrated independent of mobility

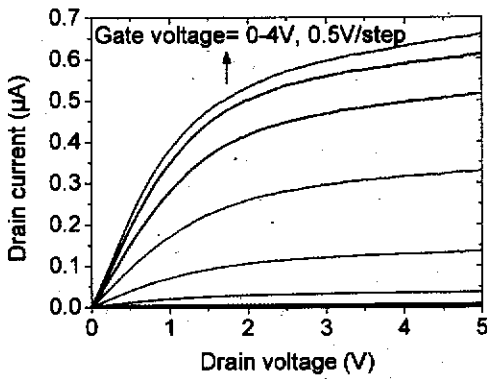

Fig. 3. Output characteristic of a multi-nanowire FET with 30 nm thick and 60 nm wide nanowires.

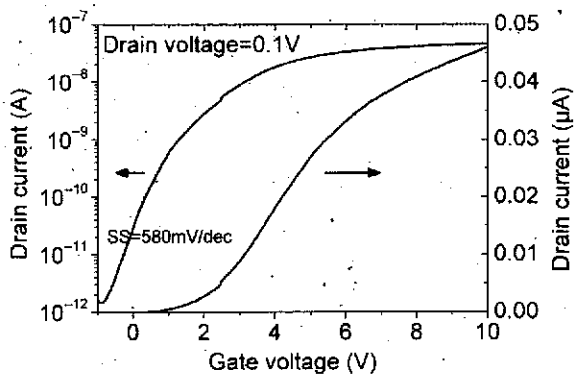

Fig. 4. Transfer characteristic of the same multi-nanowire FET as Figure 3.

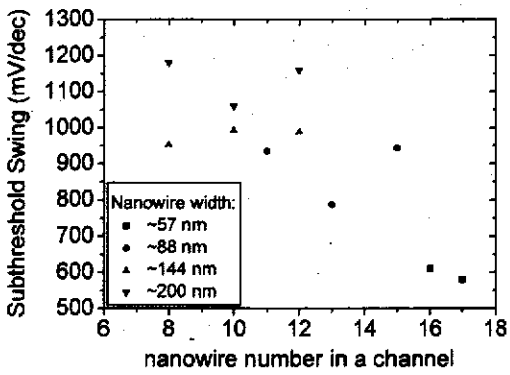

Fig. 6. SS versus the number of the nanowires contained in a FET channel.

degradation, parasitic series resistance and velocity saturation effects,[11] the V_{TH} value of 3 V is inconsistent with the I_D–V_D curves in Figure 3, where the drain current can reach 0.47 μA when the drain is biased 3 V and the transconductance begins to degrade. The V_{TH} value extrapolated from the $I_D^{0.5}$–V_G curve in the saturation operation region of this FET is 0.82 V, and hence the drain induced barrier lowering (DIBL) is 149 mV/V. The on-current (I_{ON}) and off-current (I_{OFF}) of this FET are 0.59 μA and 0.19 nA respectively, defined with the method presented in Ref. [12]. Thus the ratio I_{ON}/I_{OFF} is of the order of 3×10^3. The normalized on-current by multiple nanowire width is 0.52 μA/μm.

As shown by semilog plot of the I_D–V_G curve in Figure 4, the device shows a large subthreshold swing ($SS = 580$ mV/dec) in spite of wrap-gate structure. This is due to the 30 nm thick gate oxide and no additional doping process for the channel region ($\sim 10^{15}$ cm^{-3}). On one hand, the thick gate oxide degrades the gate capacitive coupling with the channel. On the other hand, in such lightly doped channel, the channel potential at nanowire center is a little greater than that at nanowire surfaces and the free electrons spread evenly in the vertical direction of the nanowire, known as volume inversion.[4] Thus the effective conducting path should be somewhere in-between the nanowire surfaces and center, rather than the Si/SiO_2 interface, resulting in a degraded SS.

Figure 5 shows the nanowire width dependence of SS. As shown, the SS lowers with the decreasing nanowire width, which can be explained as follows. It has been demonstrated that the wrap gate or multi-gate structure has a stronger electrostatic control of the channel than the single gate, leading to an improved subthreshold swing.[6] For a wrap gate nanowire FET, if the nanowire in a channel is so wide that the side-gate parts cannot fully depleted the nanowire in the lateral direction, thus the full depletion of the nanowire occurs only when the gate-induced depletion depth reaches the thickness of the nanowire channel, and in this case the top-gate part dominates the electrostatic control of the nanowire channel. However, if the nanowire is narrow enough, the condition for full depletion involves not only the nanowire thickness but also the nanowire width,[13] because the nanowire can be fully depleted laterally when the depletion from each side wall merges, and in this case the nanowire channel is under the control of the top gate and the side gates combination (i.e., a wrap gate). Therefore, in spite of physical wrap gate, the side-gate parts can make a role only when the side-gate depletion width exceeds the nanowire width, and the side-gate parts can be more effectual as the nanowires in a channel get narrower.

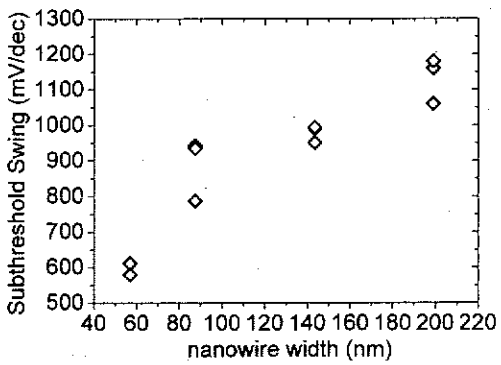

Fig. 5. The nanowire width dependence of SS.

Figure 6 shows the relationship between SS and the number of the nanowires contained in a FET channel. It seems no effect of the nanowire number on SS, because the side gates fill in the space between two adjacent nanowires in a channel and thus whether the nanowires are fully depeleted has no relation with the nanowire number but with the nanowire width.

4. CONCLUSIONS

Silicon nanowire FETs with different nanowire widths varying from 60 nm to 200 nm are fabricated through electron beam lithography, wet etching and thermal oxidation. The number of the nanowires contained in a channel

is also varied. The nanowire width dependence of SS is shown and attributed to the fact that the side-gate parts of a wrap gate play a more effectual role as the nanowires in a channel get narrower. It seems the nanowire number in a channel has no effect on SS because the side-gate parts fill in the space between two adjacent nanowires.

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