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High Growth Rate (up to 20 μm/h) SiC Epitaxy in a Horizontal Hot-wall Reactor

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Abstract A high growth rate SiC CVD epitaxial process has been developed in a horizontal hot-wall reactor for thick epilayer growth. The effect of growth conditions on growth rate and thickness uniformity has been investigated. Growth rates up to 20 μm/h have been achieved. Good thickness uniformity of 5% over 2" epiwafers is reproducibly obtained for a growth rate of 15 μm/h. Smooth surface morphology has been observed for epilayers with thickness up to 50 μm. The high growth rate process feasibility in this reactor configuration has been demonstrated by the growth of 119 μm thick epiwafer with good thickness line uniformity of 5.2% along gas flow direction and a background doping of below 7×10^{14} cm^{-3}.

Introduction

For high power device applications, thick and low-doped SiC epilayers are required to realize the rated blocking voltage [1]. Epitaxial growth of thick SiC layers is a key technology for fabricating power devices. For thick epilayer growth, a high growth rate process offers considerable economical advantages due to the substantially reduced growth time. High growth rate SiC epitaxy has been extensively investigated in vertical CVD reactors during the past years [2,3,4]. Growth rates above 40 μm/h have been reported in [3]. It is however, most desirable to develop a high growth rate epitaxy process in the horizontal hot-wall configuration, since this reactor type is the most commonly used one in SiC CVD thanks to its commercial availability as well as its simple handling. Although high growth rates have also been reported in horizontal hot-wall reactors [5], thick epilayers in this type of reactor are mostly grown at much lower growth rates to maintain reasonable quality. In this paper, we will present the development of high growth rate SiC epitaxy for thick epilayer growth in a horizontal hot-wall reactor.

Experimental

The epitaxial growth was conducted in a horizontal hot-wall reactor with a capacity of 1×2" or 1×3" wafer. H_2 was used as carrier gas, and SiH_4 and C_3H_8, both diluted in H_2, as precursor gases. The H_2 flow varied in the range of 25 to 55 slm, the SiH_4 flow between 7 and 50 sccm. The C/Si ratio was kept around 1.5. The reactor pressure was below 250 torr and the growth temperature 1550 to 1600 °C. Commercially available 2", 4H, Si-face, 8° off-axis SiC substrates were used in this investigation. The thickness was measured by FTIR for epilayers with thickness less than 50 μm. For epilayers thicker than 50 μm, the thickness was obtained by inspecting the cleaved cross section in SEM. The surface morphology was examined in an optical microscope with Nomarski interference contrast and surface roughness was measured by Atomic Force Microscopy (AFM). Capacitance-voltage (CV) measurements were performed to obtain the net carrier concentration.

The epilayer purity was examined by low temperature Photoluminescence (LTPL) and Secondary Ion Mass Spectroscopy (SIMS).

Results and Discussion

High growth rate with good thickness uniformity

The growth rate of the conventional process in the horizontal hot-wall reactor lies normally in the range of 3–5 μm/h. The key parameter to boost the growth rate is the SiH_4 flow rate. The growth rate increases with increased SiH_4 flow rate at a constant C/Si ratio. A critical limiting factor in developing a high growth rate process is the gas phase nucleation [6]. The gas phase nucleation involves Si-cluster formation in the gas phase due to a too high concentration of Si vapor generated from SiH_4 decomposition. The formed Si-clusters are carried away by the gas stream without being used for the deposition on the substrate, considerably reducing the efficiency of SiH_4 utilization. Growth conditions, such as pressure and carrier flow rate should therefore be adjusted to minimize gas phase nucleation to achieve high growth rates. Under more optimized conditions, the growth rate increases continuously with the SiH_4 flow rate and can be pushed up to 20 μm/h, as shown in Figure 1. Also indicated in Figure 1 is that a higher H_2 flow was needed for the higher SiH_4 flow rates to minimize the gas phase nucleation effect. At higher growth rates, the precursor depletion effect becomes more pronounced and maintaining good uniformity at high growth rates requires careful adjustment of process parameters. After process optimization, we have reproducibly obtained good thickness uniformity of 5% over 2" wafers even at a growth rate of 15 μm/h. An example is shown in the FTIR 3D thickness map in Figure 2.

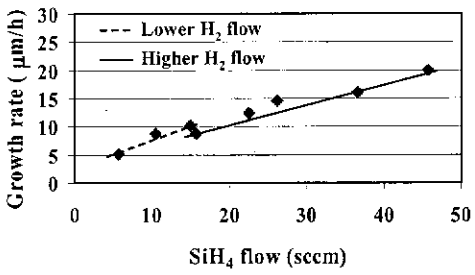

Figure 1: Growth rate dependence on SiH_4 flow rate at a constant C/Si ratio.

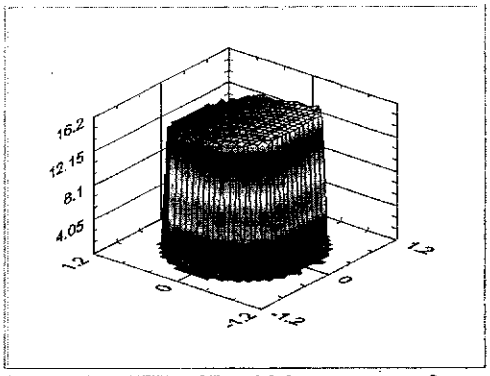

Figure 2: FTIR 3D thickness map for an epilayer grown at 15 μm/h with a thickness uniformity of 4.6%. The unit in x-axis is inch, and y-axis is μm.

Surface morphology and epilayer purity

In general it is more difficult to obtain smooth surface morphology for thick epilayers grown at high growth rates. The SiC epitaxial growth on off-axis substrates proceeds through step-flow controlled epitaxy [7]. Under non-optimized growth conditions, step-bunching will become more severe with increased epilayer thickness. In addition, the morphological defects extend with the step-flow growth and grow larger in thicker epilayers and the growth parameter window for obtaining smooth surface morphology becomes narrower for thick epilayers. To maintain smooth morphology at high growth rates, the growth parameters such as H_2 flow and growth pressure need to be carefully tuned. The parameters that enhance surface diffusion or surface adatom mobility generally improve the surface smoothness. These conditions include higher H_2 flow or lower pressure. We have

obtained very smooth surface morphology for 50 μm epilayer growth at 8.3 μm/h, as depicted by the Nomarski microscope image in Figure 3. AFM measurement on the 50 μm thick epilayer gives a surface mean roughness of 0.27 nm for an area of 20 μm × 20 μm. Under current conditions, for epilayers thicker than 50 μm, the surface starts to display pronounced step-bunching. To maintain smooth surface for very thick epilayers, the pre-growth etching and initial growth procedure need to be further improved.

The epilayer purity is an important property for achieving a long minority carrier lifetime. The purity of the thick epilayers has been monitored through both SIMS and PL measurements. The background doping has been measured by mercury C-V. The PL spectra in Figure 4 is obtained from a 42 μm thick epilayer with a background n-type doping of below $8x10^{14}$ cm^{-3}. This near bandgap PL spectra shows sharp nitrogen bound exciton (NBE) lines. The free exciton line $I_{76.9}$ is clearly discernable, while the Al bound exciton lines are small relative to the NBE lines, indicating high purity and negligible compensation.

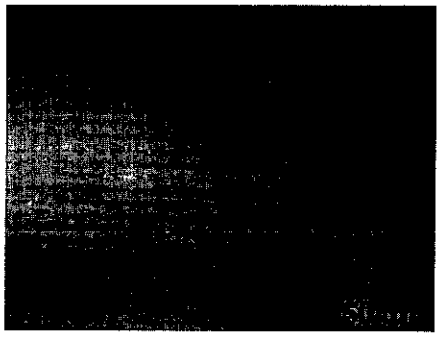

Figure 3: Nomarski image of a 50 μm thick epilayer with very smooth surface. Magnification: ×330.

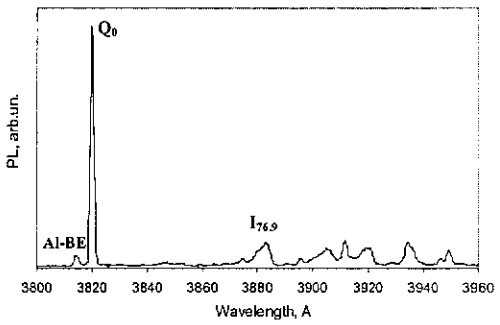

Figure 4: Low temperature PL spectra recorded on a 42 μm thick epilayer with a background doping below $8x10^{14}$ cm^{-3}.

Sustained growth of thick epilayers

For the growth of epilayers thicker than 100 μm, higher technological challenges associated with the prolonged growth time are imposed on the process stability and susceptor design. Both the process parameters and the thermal environment in the growth area need to be stable throughout the whole growth time. In addition, parasitic deposition on the susceptor walls may become so severe after long time growth that the conditions may be altered in the growth zone, or particles may be generated and transported onto the growing layer. We have achieved growth of 119 μm thick epilayer at a growth rate of 15 μm/h in the horizontal hot-wall reactor, clearly demonstrating the feasibility of thick epitaxy at high growth rates in this reactor configuration. Figure 5 is a line plot of the thickness of this epilayer along the gas flow direction. Slight growth depletion can be observed with the thickness varying from 125 μm at the upstream end to 110 μm at the downstream end. The average thickness is 119 μm and the line uniformity calculated as σ/mean is 5.2%. The background doping of this epilayer is below $7x10^{14}$ cm^{-3}, p-type. Figure 6 is the doping depth profile as measured by mercury C-V. Boron has been identified as the major p-type impurity through the SIMS measurement.

Summary

Thick SiC epitaxial growth at high growth rates has been developed in a horizontal hot-wall CVD reactor. Growth rates up to 20 μm/h have been obtained. An epilayer with thickness of 119 μm has been successfully grown at a growth rate of 15 μm/h and with a background doping below 7×10^{14} cm^{-3}. Good thickness uniformity of 5% over 2" epiwafers has been reproducibly obtained at a growth rate of 15 μm/h. Smooth surface morphology has been obtained for epilayers with thickness up to 50 μm.

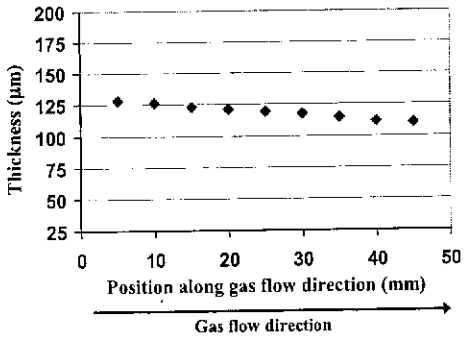

Figure 5: Thickness plot along gas flow direction for a 2" epiwafer grown for 8 hours. Average thickness: 119 μm and thickness line uniformity (σ/mean): 5.2%.

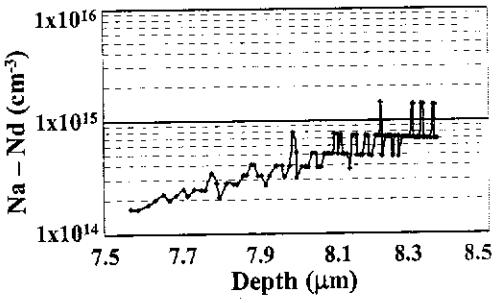

Figure 6: Doping depth profile measured by mercury C-V for the same epilayer as shown in Figure 5.

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