Very Large Capacitance Enhancement in a Two-Dimensional Electron System

Lu Li, *et al.*

Science **332**, 825 (2011);
DOI: 10.1126/science.1204168

This copy is for your personal, non-commercial use only.

If you wish to distribute this article to others, you can order high-quality copies for your colleagues, clients, or customers by clicking here.

Permission to republish or repurpose articles or portions of articles can be obtained by following the guidelines here.

The following resources related to this article are available online at www.sciencemag.org (this infomation is current as of May 12, 2011):

Updated information and services, including high-resolution figures, can be found in the online version of this article at:
http://www.sciencemag.org/content/332/6031/825.full.html

Supporting Online Material can be found at:
http://www.sciencemag.org/content/suppl/2011/05/11/332.6031.825.DC1.html

This article **cites 18 articles**, 2 of which can be accessed free:
http://www.sciencemag.org/content/332/6031/825.full.html#ref-list-1

This article appears in the following **subject collections:**
Physics, Applied
http://www.sciencemag.org/cgi/collection/app_physics

Downloaded from www.sciencemag.org on May 12, 2011

Science (print ISSN 0036-8075; online ISSN 1095-9203) is published weekly, except the last week in December, by the American Association for the Advancement of Science, 1200 New York Avenue NW, Washington, DC 20005. Copyright 2011 by the American Association for the Advancement of Science; all rights reserved. The title *Science* is a registered trademark of AAAS.

Very Large Capacitance Enhancement in a Two-Dimensional Electron System

Lu Li,[1] C. Richter,[2] S. Paetel,[2] T. Kopp,[2] J. Mannhart,[2] R. C. Ashoori[1]*

Increases in the gate capacitance of field-effect transistor structures allow the production of lower-power devices that are compatible with higher clock rates, driving the race for developing high-κ dielectrics. However, many-body effects in an electronic system can also enhance capacitance. Onto the electron system that forms at the $LaAlO_3/SrTiO_3$ interface, we fabricated top-gate electrodes that can fully deplete the interface of all mobile electrons. Near depletion, we found a greater than 40% enhancement of the gate capacitance. Using an electric-field penetration measurement method, we show that this capacitance originates from a negative compressibility of the interface electron system. Capacitance enhancement exists at room temperature and arises at low electron densities, in which disorder is strong and the in-plane conductance is much smaller than the quantum conductance.

The concept of negative compressibility describes an effect of electron-electron interactions, in which the exchange and correlation energies among electrons lower the chemical potential of an electron system as the electron density increases (*1*–*9*). This effect has been observed to enhance the capacitance of semiconductor two-dimensional (2D) electronic systems by a few percent (*7*) beyond the expected geometric capacitance. Here, we report very large capacitance enhancements (>40%) in capacitor devices that are made with the electron system generated at the TiO_2-terminated $LaAlO_3/SrTiO_3$ (LAO/STO) interface (*10*, *11*). Simple modifications to the structures described could yield a capacitance enhancement greater than 100%. Strong electronic correlations (*12*–*14*) may be used to engineer yet larger capacitances (*15*).

We fabricated capacitor devices on LAO/STO heterostructures through in situ growth of $YBa_2Cu_3O_{7-\delta}$ (YBCO) or Au films on the surface of the LAO. As shown in Fig. 1A, we then patterned the films on top of the LAO surface. Nb films were deposited into ion-milled holes to make ohmic contacts to the conductive layer at the LAO/STO interface (*16*). Each top gate provides a two-terminal capacitor. The thickness of the LAO layer was either 10 or 12 unit cells. A photograph of a sample is displayed in Fig. 1B, with electrical leads wire-bonded to the ohmic contacts near the edge of the wafer and a lead connected to a circular top gate.

The two-terminal capacitance of the capacitor device was measured with a home-built capacitance bridge, which enabled us to measure the capacitance in the frequency range between 1 Hz to 2 MHz with ~20-μrad resolution in the phase measurement of the impedance. We were able to vary the DC voltage on the top gate and track the capacitance change with gate voltage (*16*).

We measured the capacitance between a top gate and the interface at frequencies f ranging from 8 to 2000 Hz while varying a top gate voltage V_g. Device 1 was fabricated on a sample with 12 unit cells of LAO. On the top surface of the LAO film, a circular YBCO top gate with a diameter of 200 μm was patterned. Figure 2A displays the capacitance C versus V_g curves of device 1 at 4.2 K. Similar curves are shown in Fig. 2B for device 2 with an LAO thickness of 10 unit cells and a 350-μm-diameter YBCO top gate. Substantial leakage (resistances less than 5 megohms) through the LAO barrier occurred at voltages to the left of the red line in Fig. 2A and to the right of the red line in Fig. 2B. Data in these regions were not used in the analysis because the leakage resistance dropped to the magnitude of the in-plane resistance. We expect that such leakage current alters the voltage across the device and changes the charge distribution within the sample. By examining the capacitance at high electron densities at which interaction effects on the capacitance are usually small, we determined the dielectric constant of the insulating LAO layer. Given the capacitance values at V_g = 0 and at large positive V_g for device 1, the size of the gate, and the thickness of the LAO film, we found the LAO dielectric constant $D \sim 18D_0$, where D_0 is the dielectric constant of vacuum. This value is lower than the dielectric constant of single crystals of LAO but agrees with one of the molecular beam epitaxy–grown films (*17*).

Both of the capacitor devices showed a sharp depletion signal at well-defined gate fields. For device 1, at $V_g < 0.2$ V the capacitance is strongly diminished, which suggests that the electron density underneath the circular gate was substantially suppressed by the electric field. For device 2, a positive $V_g \geq 0.28$ V is needed to create a conducting channel underneath the top gate. In this case, we observed a clear and sharp depletion in the capacitance curves, which suggests that the mobile carrier density at the interface is tuned to zero by V_g.

For device 2, the interface underneath the gate was not conductive at $V_g = 0$, even though the regions away from the YBCO circular pads were conductive (the two-terminal resistance between the Nb ohmic contacts is of order 500 ohms at 4.2 K). In testing these samples during at least four different coolings from room temperature to 4.2 K for each sample, we noticed that the depletion voltage varied slightly with thermal cycling. However, the depletion voltage of devices with 12–unit cell LAO was always negative, whereas that for devices with 10–unit cell LAO layers was positive. This difference suggests that the YBCO top gate tends to deplete the interface underneath the gate: The larger the

[1]Department of Physics, Massachusetts Institute of Technology (MIT), Cambridge, MA 02139, USA. [2]Center for Electronic Correlations and Magnetism, University of Augsburg, Augsburg 86135, Germany.

*To whom correspondence should be addressed. E-mail: ashoori@mit.edu

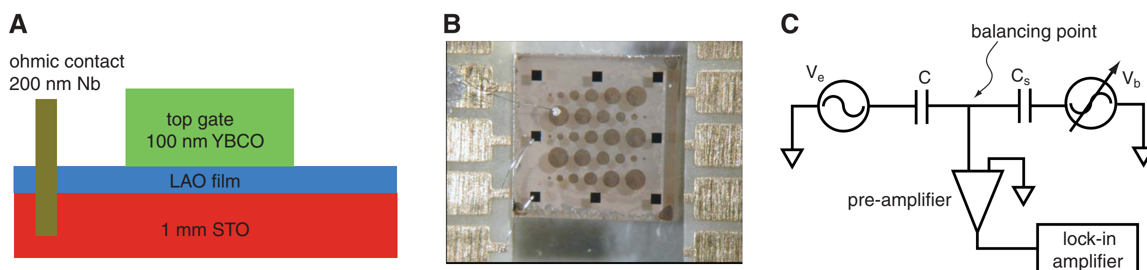

Fig. 1. Sample layout and capacitance bridge setup. (**A**) Sketch of the oxide interface layout. A thin layer of LAO (10 or 12 unit cells thick) is deposited onto the top of a TiO_2-terminated STO substrate. YBCO top gates are deposited and patterned above the LAO layer, and Nb ohmic contacts are deposited close to the corners of the wafer. (**B**) Picture of a YBCO/LAO/STO sample with leads attached. The wafer is square with a side length of 5 mm. The diameter of the YBCO circular top gates varies between 50 and 500 μm. (**C**) Setup sketch of the capacitance bridge. In one arm of the bridge, C stands for the sample capacitor, excited by an ac excitation voltage V_e. In the other arm, another ac voltage V_s with the same frequency is applied to a standard capacitor C_s. The signal at the balancing point is measured with a pre-amplifier and a lock-in amplifier. During the measurement, with the phase and the amplitude of V_e held stable, V_s is varied both in phase and in amplitude to null the signals at the balancing point.

Downloaded from www.sciencemag.org on May 12, 2011

distance is between the interface and the gate, the smaller is the depletion effect. This response might be attributable to the difference between the work function of YBCO and the vacuum, to the polar nature of the YBCO ionic layers, or to strain by lattice mismatch.

Near depletion, we observed a large enhancement of the capacitance, shown in detail in the inset of Fig. 2A. At its peak, the capacitance considerably exceeds C_{hd}, the capacitance at high densities $C_{hd} \sim C_{geom} = DA/d$, where A and d are the cross sections and the dielectric thicknesses of the capacitors, respectively. The difference between C_{hd} and C_{geom} is usually small. (Below, all the C_{geom} values are treated to be the same as C_{hd}.) The capacitance upturn at small n, where n is the carrier density, was observed at low frequency ($f < 15$ Hz). As shown by Fig. 2A, as the frequency f decreases from 20 kHz to 20 Hz, C is independent of frequency over a large range of V_g. However, at low densities the peak in C continues to grow and moves to lower V_g as f is reduced. This frequency dependence is reproduced in other devices. Figure 2B shows the $C - V_g$ curves of device 2 with 10–unit cell LAO film, displaying a considerably larger low-density capacitance enhancement than that of device 1. For measurements at two different frequencies, the upturns coincide between $0.33 \text{ V} \leq V_g \leq 0.4$ V. Below $V_g = 0.33$ V, the curve taken at $f = 14.231$ Hz diminishes, whereas that at $f = 5$ Hz keeps increasing and drops at lower V_g. The overlapping part of these two capacitance curves is the dc limit of the capacitance curve. In this regime, the out-of-phase charging signal stays small, displaying a different trend (*16*).

Measuring at frequencies as low as 5 Hz, we have not found a limit to the divergence. For these low frequencies, we observed a >40% enhancement in the sample capacitance, which is far larger than ever previously observed, even in high-mobility GaAs-based devices (*7*). Presumably, at sufficiently low frequencies disorder and the proximity of the metal-insulator phase transition limits the sharpness of the upturn. The greater capacitance upturn in device 2 (10 unit cells thick) than that in device 1 (12 unit cells thick) may reflect less disorder. The capacitance enhancement observed at low frequencies does not arise from the frequency dependence of the LAO dielectric constant. Instead, the low-frequency upturn arises from the large *RC*-time constants of the devices. Because the mobile carrier density is strongly suppressed near the depletion (*16*), the resistance *R* of the long-distance lateral current path through the interface is high.

As a quantum paraelectric (*18*), STO is ferroelectric-like at low temperature, at which its dielectric constant is enhanced greatly. The enhancement of STO dielectric constant vanishes above 30 to 50 K. However, we still observed a capacitance enhancement similar to the one found at 4 K at room temperature. Figure 2C shows the $C - V_g$ curves (*16*) close to the depletion in device 3. In this device, a circular Au pad with 350 μm was deposited to serve as top gate because it was found that at 300 K, gold caused less leakage than did YBCO (*16*). Although a leakage current to the gate appeared below –0.6 V [the gate-to-channel resistance drops to the megohm range near depletion (fig. S3) (*16*)], the room-temperature $C - V_g$ curves are similar to those of the YBCO-gated devices shown in Fig. 2, A and B. As V_g decreased from 0 V, C decreased slowly. However, near depletion C increased rapidly at low f. Measured at $f = 5$ Hz, the peak of C was 10% greater than that of C_{hd}. This room-temperature behavior provides additional evidence ruling out anomalies of the dielectric function of STO as the origin of the capacitance enhancement.

Charging a capacitor C with charge e does not simply require a change in voltage $\delta V = e/C_{geom}$. Because of the finite $dn/d\mu$, an extra voltage $(d\mu/dn)/eA$ is required, where μ is the chemical

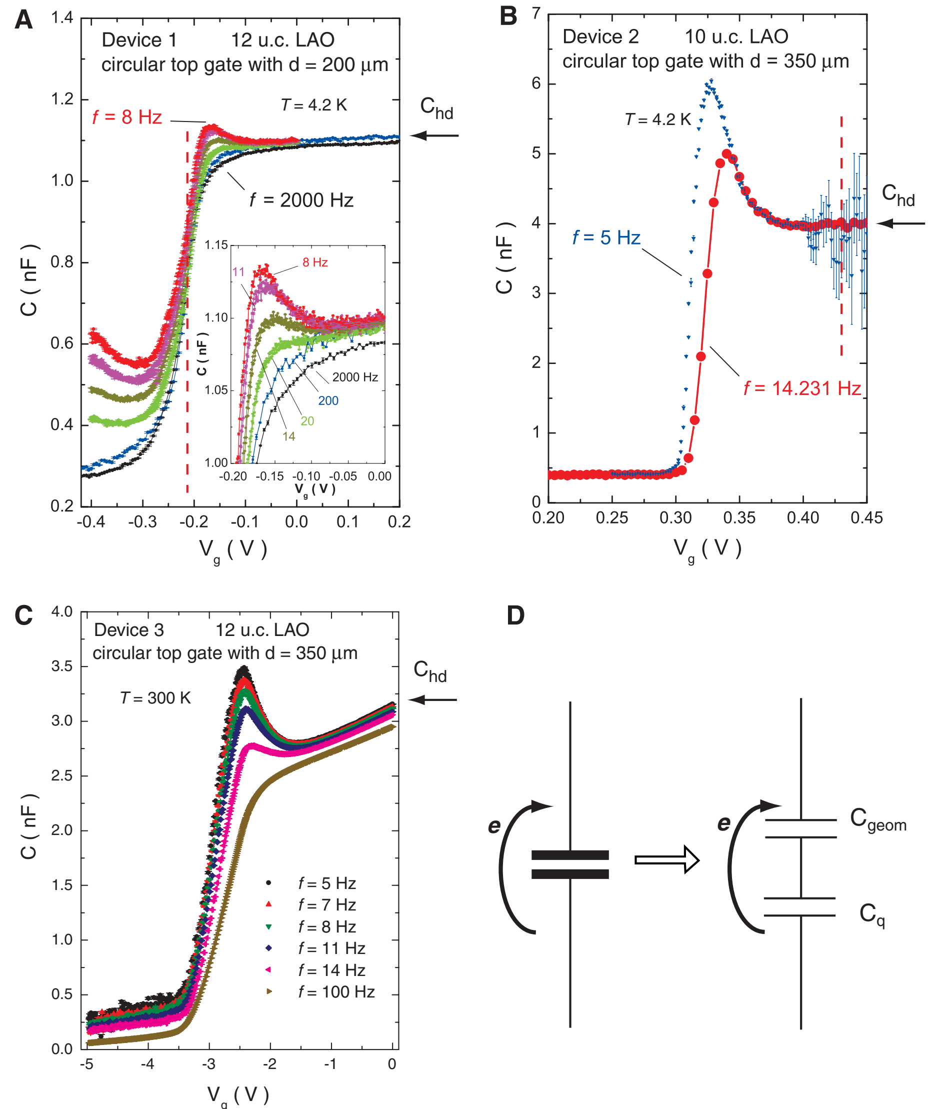

Fig. 2. The gate voltage dependence of the capacitance. (**A**) The C versus V_g curve of device 1 with a diameter of 200 μm and LAO 12 unit cells thick. The curves are taken at $T = 4.2$ K at various frequencies between 8 and 2000 Hz. The capacitance at high carrier density C_{hd} is marked with an arrow. As shown in the inset for the region near depletion, the capacitance values increase and exceed C_{hd}. At V_g smaller than −0.22 V, marked by the red dashed line, the capacitance curves are frequency dependent, which is probably a result of dc leakage through the LAO barrier. (**B**) The $C - V_g$ curve of device 2 with diameter 350 μm and LAO 10 unit cells thick. The enhancement of the capacitance is even more pronounced because the peak of C is about 40% larger than C_{hd} at $f = 5$ Hz. For this device, a leakage current develops at higher V_g, and the 5 Hz capacitance measurement becomes noisier. The red dashed line indicates a leakage resistance of 5 megohms. (**C**) The $C - V_g$ curve of device 3 with 350 μm gold top gate and LAO 12 unit cells thick, measured at room temperature. (**D**) Equivalent circuit of geometric capacitance C_{geom} and the quantum capacitance C_q. The charging of the electrodes is represented by arrows. The geometric capacitance C_{geom} is determined by the device dimensions, marked as C_{hd} in (A) to (C).

Downloaded from www.sciencemag.org on May 12, 2011

potential. As shown in Fig. 2D, the measured capacitance C is the in-series combination of the geometric capacitance C_{geom} and the quantum capacitance $C_q = Ae^2 dn/d\mu$:

$$1/C = 1/C_{\text{geom}} + 1/C_q = 1/C_{\text{geom}} + 1/[Ae^2(dn/d\mu)] \quad (1)$$

The observed enhancement of C reveals that $dn/d\mu$ is negative, providing evidence for a negative electronic compressibility (*3*). In measurements that display negative compressibility in semiconductor samples, the effect arises from the electron-electron interactions beyond the Hartree approximation (*1*, *2*). These interactions increase the chemical potential with decreasing electron density.

One consequence of the negative quantum capacitance is that the interface overscreens the external electric fields (*4*–*8*). To explore the possible existence of this overscreening effect, we carried out a field penetration measurement using a technique developed by Eisenstein (*4*, *5*). As shown in Fig. 3A, the interface was grounded, and we measured the current to the top gate as we applied a small ac excitation voltage V_{ac} on the back gate. The current I_y is proportional to the electric field penetrating from the back gate through the grounded interface (*16*). The results are shown in Fig. 3, B and C, in which I_y/f is proportional to $d\mu/dn$, the inverse of the compressibility. A negative divergence of the penetration field occurs close to depletion, at which the carrier density is below 2×10^{12} cm^{-2}. Here, the carrier density is estimated by integrating the

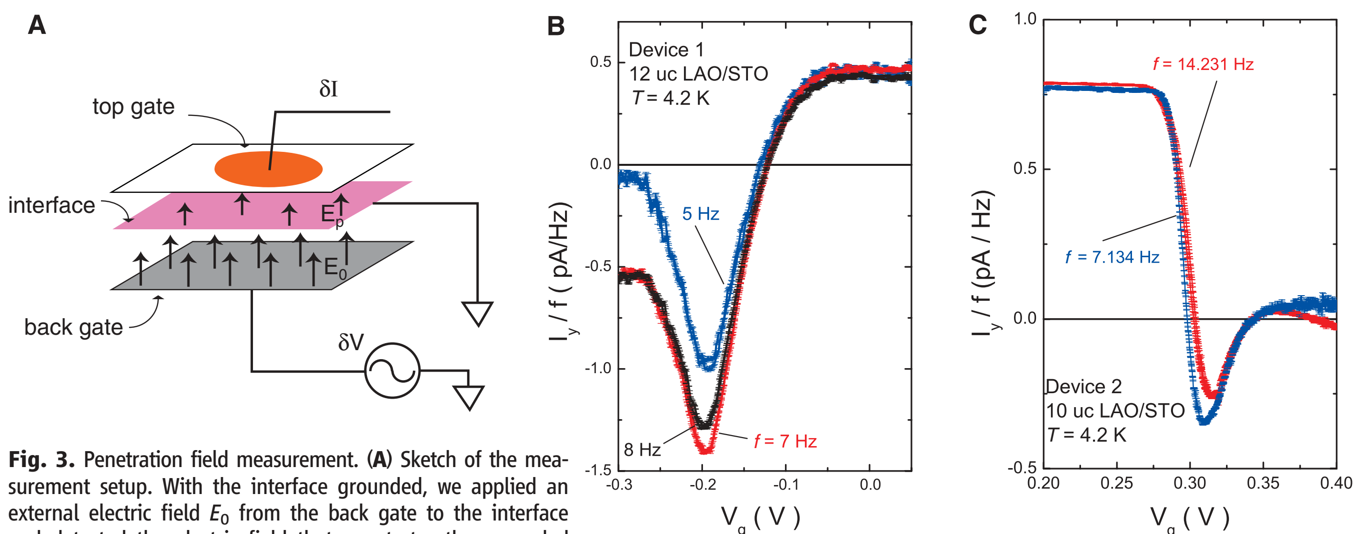

Fig. 3. Penetration field measurement. (**A**) Sketch of the measurement setup. With the interface grounded, we applied an external electric field E_0 from the back gate to the interface and detected the electric field that penetrates the grounded interface layer. The penetration field E_p is determined by measuring the current from the device top gate. (**B**) The penetration current I_y divided by the measurement frequency for device 1 at $T = 4.2$ K measured at three excitation frequencies. At V_g near zero, the penetration current is proportional to f and is constant over a broad range of -0.05 V $\leq V_g \leq 0.05$ V. For $V_g < -0.18$ V, I_y/f displays a frequency dependence, which is probably caused by effects of current leakage through the LAO layer. (**C**) The penetration signal for device 2 at $T = 4.2$ K measured at two selected frequencies. At 0.31 V $< V_g <$ 0.34 V, the negative values of the penetration current demonstrate that E_p is opposite to E_0; the conductive interface overscreens the external fields at low carrier densities. At larger $V_g >$ 0.37 V, again a f-dependent signal is present, together with a measurable current leakage through the LAO barrier.

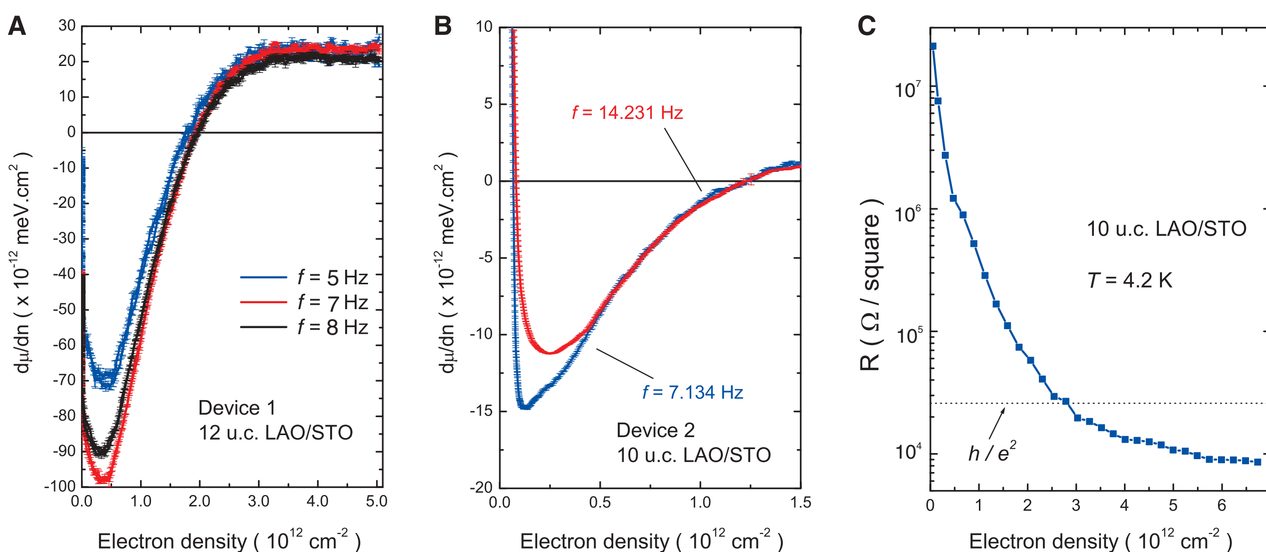

Fig. 4. The inverse of compressibility $d\mu/dn$ determined from penetration field measurements on (**A**) device 1 and (**B**) device 2. The electron density at the interface is determined by integrating the C versus V_g curve at the lowest frequency achieved. (**C**) The density n dependence of the lateral resistivity of a different device fabricated in the same 10–unit cell LAO/STO wafer. The device diameter is 500 μm. The resistivity is determined by tracking the frequency dependence of the out-of-phase charging signals (figs. S1 and S2) (*16*).

Downloaded from www.sciencemag.org on May 12, 2011

capacitance between the top gate and the interface at the lowest measurement frequency. The negative current observed at low carrier densities reveals that the electric field penetrating through the metallic interface is negative, which arises from overscreening of the external field by the mobile electrons at the LAO/STO interface. Such a negative signal cannot be reconciled with any change of the dielectric properties of the LAO layer or the STO substrate. To further explore the electronic properties of the interface, we follow the analysis of (*6*), which has shown that for low frequencies f the penetration current I_y goes as

$$I_y = 2\pi f C_1 C_2 V_{ac}/C_q \quad (2)$$

where C_2 is the geometric capacitance between the top gate and the interface and C_1 is that between the back gate and the interface normalized by the area of the top gate. We measured C_1 and C_2 directly. For device 1, $C_1 = 4.67$ pF, $C_2 = 1.1$ nF, and $V_{ac} = 20$ mV. For device 2, $C_1 = 14.3$ pF, $C_2 = 4.01$ nF, and $V_{ac} = 10$ mV. [For device 3, the penetration signal was small and difficult to resolve at 300 K because the STO dielectric constant decreases by three orders of magnitude (figs. S4 and S5)].

For device 1, at $V_g < -0.18$ V, the penetration current I_y was no longer proportional to f, which might be attributed to the dc leakage in this region, although we do not know the precise mechanism by which a dc leakage would affect the measurement. The same deviation occurred with device 2 at positive $V_g > 0.37$ V. Thus, we excluded these regions in the analysis.

Using the penetration current data, we determined the quantum capacitance C_q and used Eq. 2 to compute $d\mu/dn$. Figure 4, A and B, shows the $d\mu/dn(n)$ dependence of devices 1 and 2, respectively. The zero of density was not well defined because the measurement frequency at very small densities was not sufficiently low to charge the device fully. In a wide-density range, $d\mu/dn$ stayed negative, which provides direct evidence of the negative compressibility of the interface electron system.

The observed enhancement of capacitance and negative compressibility exist in a disordered electron system. As shown in Fig. 4C, near depletion the sheet resistivity of the interfacial layer becomes much larger than the resistance quantum h/e^2. Thus, the electrons are localized at low densities, and the system is well outside the range of the free electron approximation (figs. S1 and S2).

The large capacitance enhancement that results from the negative compressibility offers a possible gating mechanism to switch transistors by using small gate voltages. This could diminish heating in future devices (*15*, *19*, *20*). We emphasize that the observed large enhancement of C is affected by the large geometric capacitance C_{geom}. Taking derivatives on both sides of Eq. 1, we get $\delta C/C = C\delta C_q/C_q^2$; a device with larger C_{geom} per unit area will have a larger relative enhancement of the total capacitance. An interface capacitor device with a thinner $LaAlO_3$ layer may thus reveal an even larger capacitance enhancement at low carrier densities. As material quality improves, it is plausible that at low densities the effective gate-layer capacitance could increase to several times the geometric value. Transistors fashioned from the oxide interface or other systems with small carrier densities could then have an effectively very "high-κ" electrode, allowing the creation of small transistors that switch at low voltages and minimal gate-to-channel leakage (*20*).

References and Notes

1. B. I. Bello *et al.*, *Zh. Eksp. Teor. Fiz.* **80**, 1596 (1981) [Sov. Phys. JETP 53, 822 (1981)].
2. B. Tanatar, D. M. Ceperley, *Phys. Rev. B* **39**, 5005 (1989).
3. S. V. Kravchenko, D. A. Rinberg, S. G. Semenchinsky, V. M. Pudalov, *Phys. Rev. B* **42**, 3741 (1990).
4. J. P. Eisenstein, L. N. Pfeiffer, K. W. West, *Phys. Rev. Lett.* **68**, 674 (1992).
5. J. P. Eisenstein, L. N. Pfeiffer, K. W. West, *Phys. Rev. B* **50**, 1760 (1994).
6. S. C. Dultz, H. W. Jiang, *Phys. Rev. Lett.* **84**, 4689 (2000).
7. G. Allison *et al.*, *Phys. Rev. Lett.* **96**, 216407 (2006).
8. S. Shapira *et al.*, *Phys. Rev. Lett.* **77**, 3181 (1996).
9. R. C. Ashoori, R. H. Silsbee, *Solid State Commun.* **81**, 821 (1992).
10. A. Ohtomo, H. Y. Hwang, *Nature* **427**, 423 (2004).
11. S. Thiel, G. Hammerl, A. Schmehl, C. W. Schneider, J. Mannhart, *Science* **313**, 1942 (2006).
12. S. Okamoto, A. J. Millis, N. A. Spaldin, *Phys. Rev. Lett.* **97**, 056802 (2006).
13. J. Mannhart, D. G. Schlom, *Science* **327**, 1607 (2010).
14. J. Mannhart, D. H. A. Blank, H. Y. Hwang, A. J. Millis, J.-M. Triscone, *MRS Bull.* **33**, 1027 (2008).
15. T. Kopp, J. Mannhart, *J. Appl. Phys.* **106**, 064504 (2009).
16. Materials and methods are available as supporting material on *Science* Online.
17. A. F. Edge *et al.*, *Appl. Phys. Lett.* **88**, 112907 (2006).
18. K. A. Müller, H. Burkard, *Phys. Rev. B* **19**, 3593 (1979).
19. M. S. Loth, B. Skinner, B. I. Shklovskii, *Phys. Rev. E Stat. Nonlin. Soft Matter Phys.* **82**, 056102 (2010).
20. P. M. Solomon, in *Future Trends In Microelectronics: From Nanoparticles to Sensors and Energy*, S. Luryi, J. M. Xu, A. Zaslavsky, Eds. (Wiley IEEE Press, Hoboken, NJ, 2010), pp. 127–140.

21. The authors gratefully acknowledge helpful discussions and interactions with O. E. Dial, M. M. Fogler, R. Jany, P. A. Lee, L. S. Levitov, A. J. Millis, B. Shklovskii, P. Solomon, and J.-M. Triscone. This work was supported by ARO-54173PH, by the National Science Foundation through the Nanoscale Science and Engineering Center program, by the Deutsche Forschungsgemeinschaft (TRR 80), the European Commission (OxIDes), and by the Nanoscale Research Initiative. L. Li thanks the MIT Pappalardo Fellowships in Physics for support.

Supporting Online Material
www.sciencemag.org/cgi/content/full/332/6031/825/DC1
Materials and Methods
SOM Text
Figs. S1 to S5
References

11 February 2011; accepted 28 March 2011
10.1126/science.1204168

Downloaded from www.sciencemag.org on May 12, 2011

Beating Crystallization in Glass-Forming Metals by Millisecond Heating and Processing

William L. Johnson,* Georg Kaltenboeck, Marios D. Demetriou, Joseph P. Schramm, Xiao Liu, Konrad Samwer, C. Paul Kim, Douglas C. Hofmann

The development of metal alloys that form glasses at modest cooling rates has stimulated broad scientific and technological interest. However, intervening crystallization of the liquid in even the most robust bulk metallic glass-formers is orders of magnitude faster than in many common polymers and silicate glass-forming liquids. Crystallization limits experimental studies of the undercooled liquid and hampers efforts to plastically process metallic glasses. We have developed a method to rapidly and uniformly heat a metallic glass at rates of 10^6 kelvin per second to temperatures spanning the undercooled liquid region. Liquid properties are subsequently measured on millisecond time scales at previously inaccessible temperatures under near-adiabatic conditions. Rapid thermoplastic forming of the undercooled liquid into complex net shapes is implemented under rheological conditions typically used in molding of plastics. By operating in the millisecond regime, we are able to "beat" the intervening crystallization and successfully process even marginal glass-forming alloys with very limited stability against crystallization that are not processable by conventional heating.

A glass is formed when a liquid is undercooled below the melting point, T_M, of the competing crystalline solid(s) and then freezes at a glass transition temperature, T_g, without crystallizing. Undercooled liquids and glasses are metastable phases, implying that given sufficient time, both will transform to more stable crystalline solids. The glass-forming ability of a liquid is a measure of its metastability; that is, its resistance to crystallization in the undercooled temperature region between T_g and T_M. Robust glass-forming silicate, polymer, and molecular melts exhibit superior metastability, with

Keck Laboratory of Engineering, California Institute of Technology, Pasadena, CA 91125, USA.

*To whom correspondence should be addressed. E-mail: wlj@caltech.edu