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A Robust Process for Ion Implant Annealing of SiC in a Low-Pressure Silane Ambient

S. Rao,[1] S.E. Saddow,[1] F. Bergamini,[2] R. Nipoti,[2] Y. Emirov,[1] and Anant Agrawal[3]

[1] Electrical Engineering, Univ. of South Florida, Tampa, FL 33620, USA
[2] CNR - IMM Sezione di Bologna, via Gobetti 101, I-40129 Bologna, Italy
[3] Cree, Inc., 4600 Silicon Drive, Durham, NC 27703, USA

Abstract

High-dose Al implants in n-type epitaxial layers have been successfully annealed at 1600°C without any evidence of step bunching. Anneals were conducted in a silane ambient and at a process pressure of 150 Torr. Silane, 3% premixed in 97% UHP Ar, was further diluted in a 6 slm Ar carrier gas and introduced into a CVD reactor where the sample was heated via RF induction. A 30 minute anneal was performed followed by a purge in Ar at which time the RF power was switched off. The samples were then studied via plan-view secondary electron microscopy (SEM) and atomic force microscopy (AFM). The resulting surface morphology was step-free and flat.

1. Introduction

The mechanical strength of Silicon Carbide does not permit introduction of dopants by diffusion, as dopant diffusion in SiC is slow and requires very high temperatures [1]. Thus ion implantation of dopants in SiC has been demonstrated to be ideally suitable because of the possibility to accurately control the dopant concentration and the thickness of the implanted region without any chemical or thermodynamic constraints [2]. However implantation causes significant lattice damage and most of the implanted ions reside at the interstitial sites resulting in poor electrical activity [3]. The damage can range from point defects caused by single atom displacements at low ion doses to amorphization at high dose rates. Thermal annealing normally performed after ion implantation processing serves the dual purpose of removing defects and activating dopants, but may result in surface damage due to the high temperatures needed in SiC [refs].

For the electrical activation of p-type implanted dopant temperature in excess of 1600°C are required [2]. One possible consequence of such a high temperature annealing of SiC is the step bunching issue that concerns the surface morphology of the sample [1,4]. At such elevated temperatures the SiC crystal surface may decompose due to selective out-diffusion of Si from the SiC lattice leading to severe degradation in surface morphology which is well known [5]. Hence some means to permit high temperature annealing of SiC implants while suppressing the out-diffusion of Si from the surface is required. Several approaches have been performed in this field but with limited success [5, 6].

In this paper preliminary implant anneals performed using silane overpressure in a CVD reactor are presented and are compared with Ar only anneals. Variations in surface morphology caused by high-temperature post-annealing have been observed using the atomic force microscopy AFM and the secondary electron microscopy SEM. The electrical properties of the implanted regions are currently under investigation and will be presented at a later date [7].

2. Experimental Method

In this study, a 4H-SiC (0001) Si face Cree epiwafer with an 8° miss-cut towards the [11-20] direction and a low-doped ($N_D - N_A \sim 3$? 10^{15} cm^{-3}) epitaxial layer was used. A 1.7 MV Tandetron accelerator was used to implant Al^+. An energy absorber layer was necessary to implant a thin SiC layer next to the sample surface. The implanted profile, as determined by SRIM [8], had a box shape with an ion concentration of 8 ? 10^{19} cm^{-3} and an implant depth of 0.16 ?m from an integrated dose of 1.75 ? 10^{15} cm^{-2}. In spite of this high fluence value, the crystal damage was weak because the implantation temperature was equal to 400 °C. The ion beam impinged on the 4H-SiC crystal at 15° with respect to the <0001> axis while remaining within a plane at 12° from the {11-20} crystal plane. Taking into account the presence of the energy absorber layer this beam to crystal orientation guarantees random implantation geometry. After the implantation process the wafer was diced into pieces so that various sections of the wafer could be processed under differing annealing conditions.

A Silane based CVD reactor suitable for performing high-temperature anneals in a silicon rich ambient was used for all the annealing experiments. Samples were placed on a SiC coated graphite susceptor and a RF induction coil was used to heat these susceptors. Annealing temperatures in excess of 2000°C are possible in this kind of arrangement.

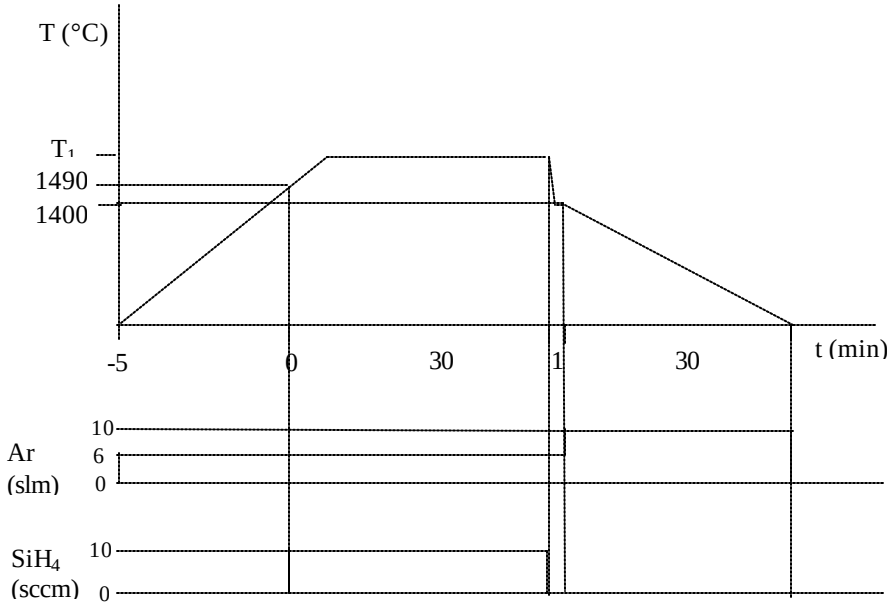


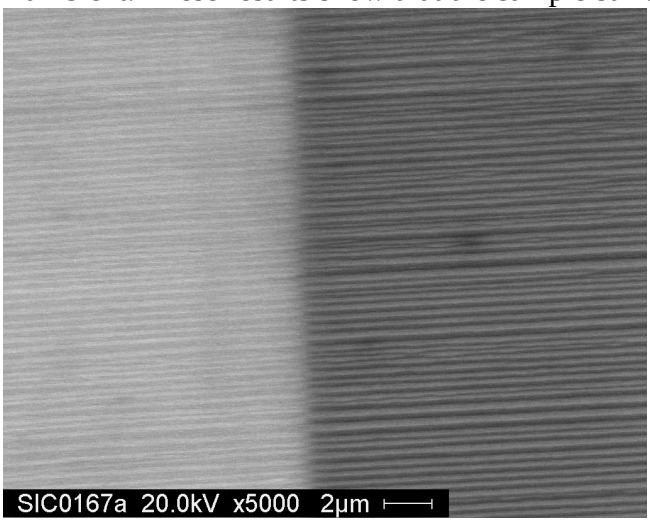
Figure 1: Implant annealing process schedule for a LPCVD reactor, indicating gas flow timing versus sample temperature.

The basic principle behind the silane overpressure model is that when implanted SiC wafer is annealed at high temperatures (? 1600 °C), Si atoms on the surface of the wafer may be exchanged with Si atoms provided by the silane gas in the vapor phase. This is believed to prevent the selective out-diffusion of Si from the SiC lattice at the surface. However this technique is effective only if the Si overpressure is below the level where Si droplets can form (i.e., gas-phase nucleation of Si which is then adsorbed onto the SiC surface). Earlier work presented by Saddow et. al. discusses implant annealing process under atmospheric conditions in a similar CVD system [9]. It is important to anneal under low pressure conditions as many SiC reactors operate at low pressure and this would permit a silane overpressure process to be most rapidly utilized by these systems. But most importantly, the shift in gas

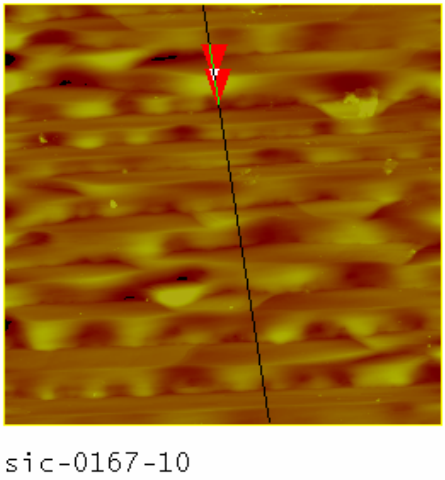
phase equilibrium that occurs at low pressures helps to suppress Si cluster formation in the gas phase during sample annealing. Hence a serious defect in SiC, Si droplets, can be avoided during implant annealing if the process is transferred to low-pressure process conditions. The process schedule that was developed during this work is as shown in Figure 1.

For direct comparison, a piece of the same implanted sample was annealed in a J.I.P.ELEC^{TM} furnace at 1650°C for 30 min in high purity Ar ambient. Using silane overpressure process, anneals were performed at two different temperatures, 1600 and 1650°C while every other process parameter was maintained constant with the aim to reduce the number of variables in this first silane overpressure process performed at low pressure. Silane and argon were the two process gases used, where Ar not only serves as a dilutant gas but also as a carrier gas to transport silane molecules to the crystal surface Initially a 6 slm UPH Ar flow was established in the reactor. The susceptor was heated to the annealing temperature using a controlled ramp (the susceptor heats to 1600 °C in approximately 6 minutes). 3% Silane, premixed in 97% UHP Ar, is then introduced into the reactor once the susceptor temperature reaches 1490°C. After 30 minutes of annealing in the Silane / Ar ambient the silane flow is turned off and the temperature lowered to 1400°C. The reactor is then purged with Ar for 1 min at this temperature after which the RF is turned off. The cool down of the susceptor occurrs under an Ar flow of 10 slm for 30 minutes. Although it is expected that the silane flow would need to increase with increasing annealing temperature, the silane flow was held constant for both IA experiments reported here – 1600 and 1650 °C. This was done to determine the process stability over a small (50 °C) temperature range and it was expected that slight step bunching would be observed at the higher IA temperature due to the increased vapor pressure of Si in the SiC lattice.In this work surface analysis was performed using an Hitachi 800 Field Emission SEM and a Digital Instruments Nanoscope Dimension 3000 AFM run in tapping mode. For all the SEM images the samples were tilted away from viewer to better reveal the surface features.

Figure 2 shows the SEM micrographs and the AFM data of the sample annealed at 1650°C in Ar ambient. These results show that the sample surface exhibited severe step bunching.



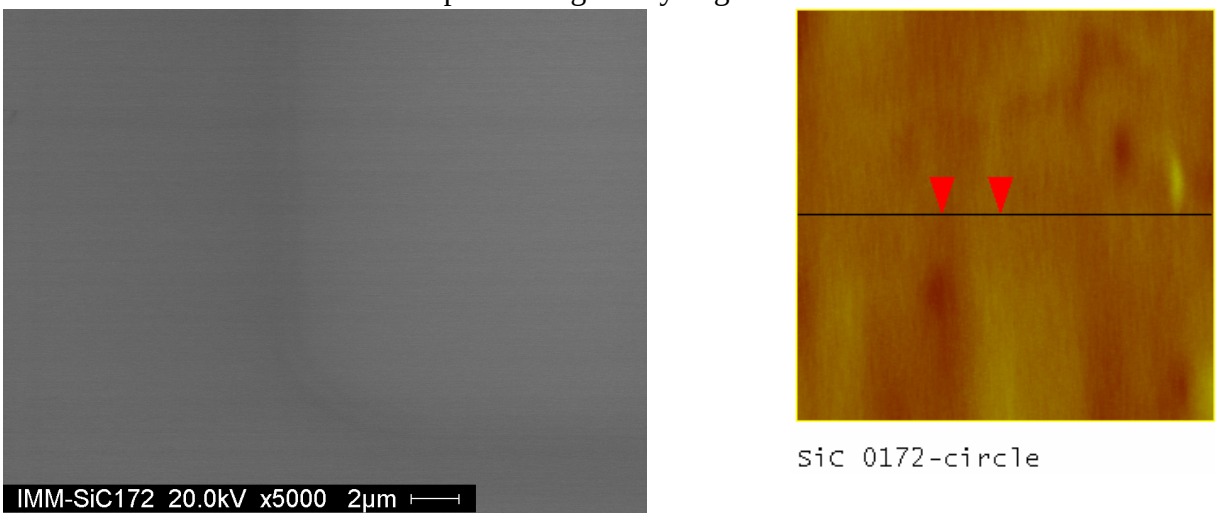
(a)



(b)

Figure2: J.I.P.ELEC^{TM} furnace annealing at 1650°C for 30 min in high purity Ar: **(a)** Plan view SEM micrograph of surface morphology. The step bunching phenomenon at the sample surface is evident. **(b)** AFM data showing the location of the section analysis (see line). RMS roughness ~ 13.76 nm. The dimension of the scan is 10µm x 10µm.

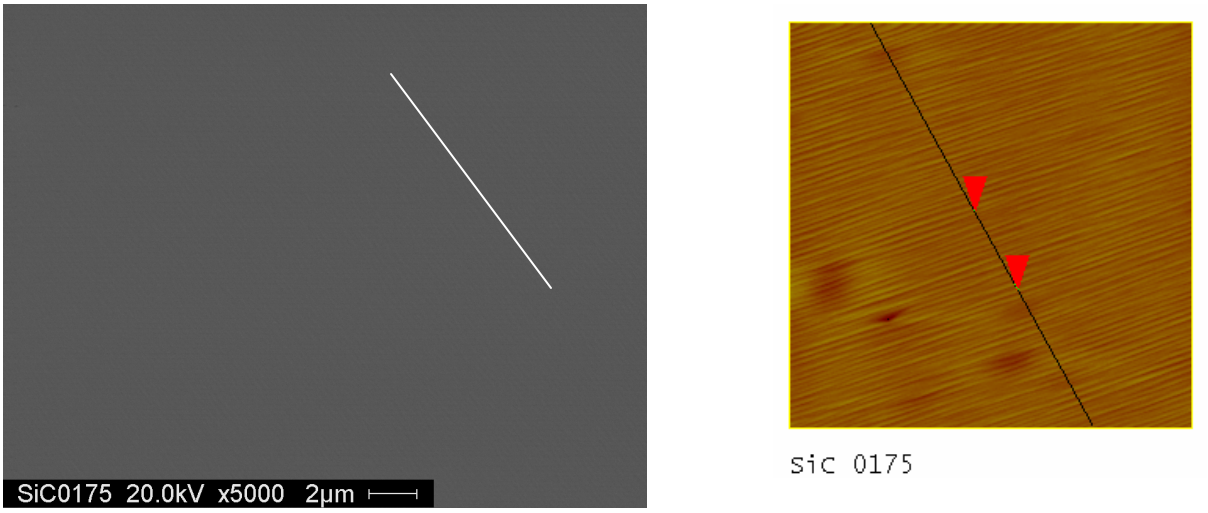
Figure 3 shows an SEM micrograph (5000X magnification) and AFM data of the sample that was annealed at 1600°C. No step bunching or any degradation of the surface was observed.



(a) **(b)**

Figure 3: Silane overpressure annealing at 1600°C fro 30 min: **(a)** Plan view SEM micrograph of surface morphology. **(b)** AFM data showing the location of the section analysis (see line). RMS roughness ~ 0.38 nm. The dimension of the scan is 10µm x 10µm.

Figure 4 shows the SEM micrograph and AFM data of a sample that was annealed at 1650°C. A slight amount of step bunching was observed, but well below the value seen in the Ar only experiment (see Fig. 2). Clearly optimization of the silane flow (i.e., partial pressure) as a function of temperature should provide adequate process stability and experiments are currently underway to verify this assertion up to 1750 °C.



(a) **(b)**

Figure 4: Silane overpressure annealing at 1650°C for 30 min: **(a)** Plan view SEM micrograph of surface morphology Slight step bunching was noticed in the direction indicated by the line in the micrograph. **(b)** AFM data showing the location of the section analysis (see line). RS roughness ~ 0.90 nm. The dimension of the scan is 10µm x 10µm.

3. Conclusion

A low-pressure SiC CVD reactor has been used to successfully anneal Al implanted n-type SiC epiwafers at a temperature of 1600 °C using a silane overpressure process. Comparisons of the surface morphology between samples annealed in an Ar ambient and anneals performed with the silane overpressure process were made via AFM and SEM. Severe surface degradation was observed in case of samples annealed under Ar flow. The silane anneals conducted at 1600°C revealed no step bunching while the anneals performed at 1650°C under non-optimized conditions showed a slight degree of step bunching. Electrical characterization is being performed and will be reported at a later date.

Acknowledgements

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References

[1] G. J. Phelps, N.G. Wright, E.G. Chester, C. M. Johnson and A.G. O'Neil, , "Step bunching fabrication constraints in silicon carbide", *Semicond. Sci. Technol.* 17, L17 (2002).
[2] M. Capano, S. Ryu, M. R. Melloch, J. A. Cooper, and M. R. Buss, "Dopant activation and surface morphology of ion implanted 4H- and 6H-Silicon Carbide," *J. Electron. Mater.* 27, 370 (1998).
[3] S. Ahmed, C.J. Barbero , and T.W. Sigmon, "Activation of ion implanted dopants in α-SiC", *Appl. Phys. Lett.* 66, 712 (1995).
[4] Seshadri S, Eldridge G W and Agarwal A K 1998, "Comparison of the annealing behavior of high-dose nitrogen-, aluminum-, and boron-implanted 4H–SiC", *Appl. Phys. Lett.* 72, 2026 (1998).
[5] M. Capano, S. Ryu, M. R. Melloch, J. A. Cooper, K. Rottner, S. Karlsson, N. Nordell, A. Powell and D. E. Walker, "Surface roughening in ion implanted 4H-Silicon Carbide", *J. of Electron. Mater.* 28, 214 (1999).
[6] K.A. Jones et al., "AlN as an encapsulate for annealing SiC," *J. Appl. Phys*. 83, 8010 (1998)
[7] F.Bergamini, S. Rao, A. Poggi, S.E. Saddow, R. Nipoti, and A. Agarwal, "Silane annealing at 1600°C for the electrical activation of Al^+ implanted ions: J-V characteristics of p^+/n 4H-SiC diodes", submitted to 5th *European Conf. on Silicon Carbide and Related Materials* (ECSCRM2004), August 31-Sepetember 4, 2004, Bologna, Italy.
[8] SRIM download at the web page: http://www.srim.org/SRIM