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INVESTIGATION OF THE MOST CHANNEL CONDUCTANCE IN WEAK INVERSION

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Abstract—The drain-source conductance of several MOS transistors has been studied as a function of the silicon surface-potential ψ_s in the weak and intermediate inversion region, under the condition of quasi-thermal equilibrium at room temperature. The silicon surface conductance per square $G_\square$ has been measured to vary exponentially with $q\psi_s/kT$ in weak inversion for excess minority carrier densities extending over the range 10^5–10^{11} cm^{-2}. The exponential behaviour of $G_\square$ vs. $q\psi_s/kT$ appeared to be insensitive for the presence of interface states, when distributed around peak values as large (As) 6×10^{11}/cm^2 eV at $\approx$ 200 meV energy distance from midgap.

Garrett and Brattain predicted theoretically that the excess minority carrier surface charge for weak inversion should also be an exponential function of $q\psi_s/kT$, we conclude that the minority carrier mobility remains constant over the entire weak inversion region.

A refined version of the low frequency CV method the so-called 'split' CV method has been introduced, which allows a simple determination of the charge trapped in interface states in weak and intermediate inversion as well as a determination of the bulk dope density.

1. INTRODUCTION

THE development of the first stable MOS transistors[1] actuated many workers to initiate comprehensive studies of the conduction of inverted silicon surfaces[2–10] under various surface conditions. The channel conduction for the condition of weak inversion (less than 10^{-7} mho$_\square$) was found to vary more or less exponentially with gate voltage [11–14].

The object of our paper comprises an investigation of the channel-conductance $G_\square$ of various MOS transistors with different amounts of interface state densities as a function of the actually measured silicon surface potential ψ_s under the condition of quasi-thermal equilibrium.

A definition of the channel conductance will be given in Section 2. For the determination of ψ_s, the low frequency CV method, adopted from Berglund [15] is used. This low frequency CV method will therefore be described concisely in Section 3. Furthermore a 'split' low-frequency CV measurement technique will be introduced in Section 4, which allows a simple determination of the trapped charge in interface states and the interface state density in the weak inversion condition as well as the bulk dope density. In Section 5 low frequency capacitance and static surface conductance measurements on a typical n- and p-channel MOST are described, which measurements are evaluated in Section 6. Sections 7 and 8 follow with an interpretation and discussion of the measurement results. The main conclusion which has been drawn from the measurement results is that at room temperature and in the conductance range between 10^{-11} and 10^{-5} mho$_\square$, the surface mobility of the excess minority carriers remains constant, irrespective of the amount of surface minority carriers trapped in interface states.

For the sake of simplicity all theoretical derivations and descriptions of principles of measurement will be based on n-channel devices on p-type silicon material.

2. THE DEFINITION OF THE SURFACE CONDUCTANCE PER SQUARE

The surface or channel conductance per square $G_\square$ of an MOS transistor under the conditions of quasi-thermal equilibrium and uniform channel is defined as $q\mu_n\Delta n$, μ_n and Δn being the surface mobility and density of the excess minority carriers (electrons) in the channel. According to the expressions derived by Garrett and Brattain[16] Δn is proportional to exp $(q\psi_s/kT)$ in weak inversion and to exp $(q\psi_s/2kT)$ in strong inversion.

The relation between $G_\square$ and the source drain

current I_{ds} is expressed by the equation:

$$G_{\square} = \frac{I_{ds}(V_g)}{(W/L)V_{ds}}, \quad (1)$$

where W/L is the MOST aspect ratio; V_g the gate voltage and V_{ds} the drain-source voltage (10 mV).

3. LOW FREQUENCY *CV* MEASUREMENT METHOD FOR THE DETERMINATION OF THE SURFACE POTENTIAL ψ VS THE GATE VOLTAGE

3.1 *Description of the measurement principle*

A small low frequency signal $dV_g \exp(j\omega t)$ superimposed on a d.c. bias V_g, is applied to the gate of a MOS transistor with the source, drain and bulk shorted.

If the requirement of quasi-equilibrium during the measurement is met, then the small signal charge in the silicon underneath the gate assumes the form $(dQ_s + dQ_{ss}) \exp(j\omega t)$, where dQ_s and dQ_{ss} denote the maximum small signal charges inside the silicon and in the interface states, respectively. Moreover, the generated small signal gate current will be leading the gate voltage by 90 deg: $dI_g \exp j(\omega t + \pi/2)$.

Provided that parasitic capacitances may be neglected the low frequency gate capacitance C is defined by:

$$C = Im\left\{\frac{1}{\omega}\frac{dI_g \exp j(\omega t + \pi/2)}{dV_g \exp(j\omega t)}\right\} = \frac{1}{\omega}\frac{dI_g}{dV_g}. \quad (2)$$

An example of a low frequency *CV* plot, in a normalized form, has been given in Fig. 1.

As Berglund[15] already pointed out, one of the attractions of a low frequency *CV* plot is that it allows a determination of the d.c. surface potential ψ_s as a function of the gate potential V_g. it is fairly easy to derive that:

$$\frac{d\psi_s}{dV_g} = 1 - \frac{C}{C_0}, \quad (3)$$

where C_0 = the gate oxide capacitance.

An integration of $1-(C/C_0)$ over V_g yields the surface potential difference $\psi_{s,q} - \psi_{s,p}$ between two arbitrary gate voltages $V_{g,q}$ and $V_{g,p}$ as is shown by the shaded area in Fig. 1.

In order to establish the absolute relationship between ψ_s and V_g a 'matchpoint', or in other words the knowledge of ψ_s for one arbitrary gate voltage V_g is required. The so called flat band condition is the most commonly used reference point in *CV* measurements. However it is advantageous to use the intrinsic condition of the silicon surface as a match-point[17, 18].

The procedure for its determination is simple, as will be shown in the next section.

3.2 *Determination of the intrinsic condition*

When we consider two points A and B, located at the *CV* plot of Fig. 2, in very strong accumulation and very strong inversion respectively, we may assume that the corresponding silicon charges $Q_{s,A}$ and $Q_{s,B}$ consist primarily of excess charge carriers inside the silicon, rather than the interface state charges $Q_{ss,A}$ and $Q_{ss,B}$. If furthermore points A and B are chosen in such a way as to make $Q_{s,A}$ and $Q_{s,B}$ equal, then one can easily derive[17] that the mean value of the surface potential between $c_{s,A}$ and $\psi_{s,B}$ will be equal to the potential $\psi_{s,i}$ for which the surface becomes intrinsic:

$$\psi_{s,i} = \frac{\psi_{s,A} + \psi_{s,B}}{2} = \frac{kT}{q}\ln\frac{C_B}{n_i}, \quad (4)$$

where C_B is the bulk dope density.

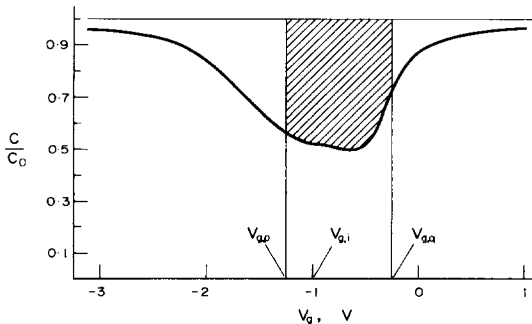

Fig. 1. Low frequency *CV* plot of a *n*-channel MOS transistor with bulk dope density $C_B = 3\times 10^{15}\,cm^{-3}$ and oxide thickness d_0: 1280 Å. Measurement frequency: 16 Hz.

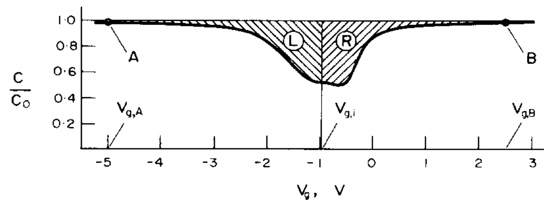

Fig. 2. The same low frequency *CV* plot as in Fig. 1, drawn on a reduced scale.

Equations (3) and (4) imply that the intrinsic gate voltage $V_{g,i}$ can be found by drawing a vertical line, as shown in Fig. 2. This line divides the area envelloped by the normalized CV curve and the horizontal line $C/C_0 = 1$, between the points A and B, in two parts of equal magnitude.

Whereas the intrinsic gate voltage can be located without prior knowledge of the bulk dope density C_B, for the determination of the exact value $\psi_{s,i}$ a knowledge of C_B still remains essential, according to equation (4).

As we shall see the bulk dope concentration may be obtained from a low frequency 'split' CV measurement, a measurement method which will be proposed in the next section. When the bulk dope density is known, Fig. 3 may be used for the determination of the intrinsic surface potential $\psi_{s,i}$.

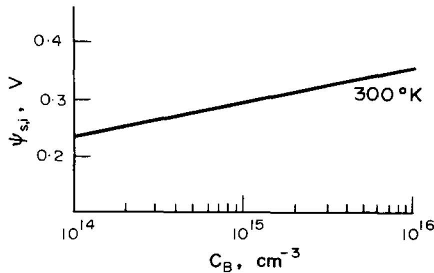

Fig. 3. The intrinsic surface potential $\psi_{s,i}$ as a function of C_B, at a temperature of 300°K.

If the low frequency CV method is applied on a MOS transistor then the source and drain junctions have the advantage of providing an efficient supply of minority carriers and thus enhance the surface of the silicon to meet the requirement of quasi-thermal equilibrium during the low-frequency measurement.

The advantage of the presence of the source-drain junctions will be exploited in the low frequency 'split' CV method, to be described in the next section.

4. LOW FREQUENCY 'SPLIT' CV METHOD FOR THE DETERMINATION OF TRAPPED CHARGE IN INTERFACE STATES IN WEAK INVERSION AND BULK DOPE DENSITY

4.1 *Description of the measurement principle*

The difference of this method, in comparison with the low frequency CV method is the separate measurement of the bulk and source-drain contributions to the gate capacitance C as a function of the gate voltage V_g of an MOS transistor. In Fig. 4 the measurement principle is shown.

The small signal charge $dQ_s + dQ_{ss}$, being influenced by a small signal gate voltage dV_g, is supplied by a hole current dI_b via the bulk contact and in addition, if the silicon is in the inverted condition, by an electron current $dI_d + dI_s$ supplied to the surface by the source-drain regions.

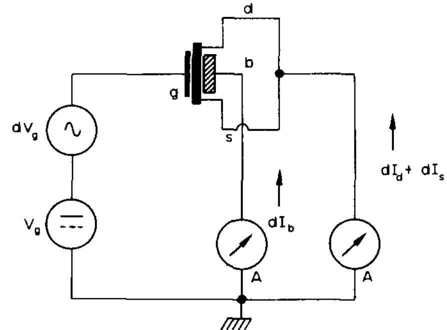

Fig. 4. Scheme of the low frequency 'split' CV measurement.

The source-drain capacitance $C_d + C_s$ is defined as:

$$C_d + C_s = \frac{1}{\omega} \frac{dI_d + dI_s}{dV_g} \tag{5}$$

and the bulk capacitance is defined as:

$$C_b = \frac{1}{\omega} \frac{dI_b}{dV_g}. \tag{6}$$

According to equations (2), (5) and (6) the gate capacitance C is equal to the sum of the bulk and the source-drain capacitances: $C = C_b + C_d + C_s$.

A pair of 'split' CV curves C_b and $C_d + C_s$ obtained from the same n-channel MOS transistor as used in Fig. 1 has been drawn in Fig. 5. The capacitances C_b and $C_d + C_s$ have been measured with respect to their values for the strong inversion and the strong accumulation condition respectively in order to eliminate the influence of parallel parasitic capacitances. From Fig. 5 it is apparent that $C_d + C_s$ starts to increase at $V_{g,i}$ and reaches its maximum value $(C_d + C_s)_{max}$ in strong inversion. Simultaneously C_b tends towards a zero value in strong inversion.

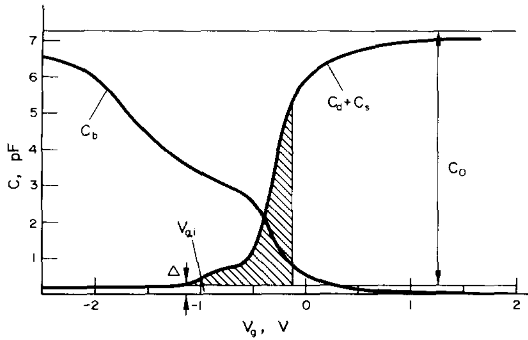

Fig. 5. Low frequency 'split' CV curves obtained from the same MOS transistor as in Fig. 1.

The value Δ of C_d+C_s at the onset of its increase at $V_{g,i}$ is due to the decrement of the active gate area in its passage through the accumulation and depletion region. Hence Δ is considered as the zero value of the capacitances C_d+C_s and C for the inversion region. Consequently the capacitance $(C_d+C_s)_{\max}-\Delta$ is referred to as the oxide capacitance C_0 corresponding to the active gate region, which oxide capacitance was used to obtain the normalized low frequency capacitance curve C/C_0 in Fig. 1.

4.2 *Requirements to impose on the MOS transistor to make the low frequency 'split'* CV *measurement technique applicable*

At the root of the application of the 'split' CV method lies the supposition that the MOS transistor, being under evaluation, should meet the requirement that in the inversion condition of the surface of the silicon:

(a) the small signal excess majority carrier charge $q\mathrm{d}(\Delta p)$ is supplied by a bulk hole current $\mathrm{d}I_b$ and

(b) the interface state charge $\mathrm{d}Q_{ss}$ as well as the excess minority carrier charge $q\mathrm{d}(\Delta n)$ is supplied by an electron current $\mathrm{d}I_d+\mathrm{d}I_s$, which originates from the source-drain diffused regions.

Consequently for the condition of surface accumulation, the bulk current will be the dominant contribution to the small signal gate capacitance and for strong inversion the source-drain current.

In the intermediate region of weak inversion, where the electron supply from the source and drain is still very small, generation–recombination processes near the surface may act as competing electron sources. Their influence will be discussed in the appendix. The electron supply from the source and drain is favoured by the choice of a sufficiently small channel-length L of the MOS transistor. On the other hand a minimum channel length is required owing to the influence of the source-drain junctions on the CV curve as indicated in Section 4.1.

These two conflicting prerequisites lead to a range of optimum-channel-lengths for the application of the 'split' CV measurement method as shown in Fig. 6 for both hole and electron channels and different bulk dope densities. The criteria leading to these optimum channellength values are considered more extensively in the appendix.

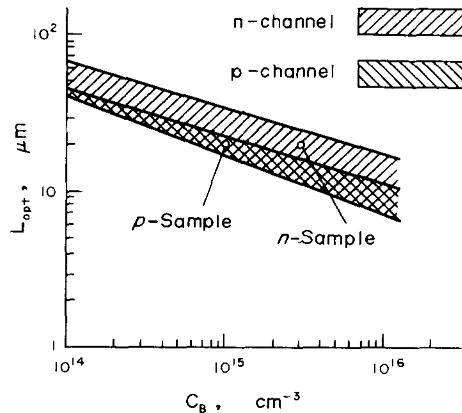

Fig. 6. Ranges of optimum channellengths for the application of the 'split' CV measurement technique on n-channel and p-channel MOS transistors, for various bulk dope concentrations.

4.3 *The determination of the charge trapped in interface states in weak inversion*

The considerations in the previous Section 4.2 lead to the conclusion that C_d+C_s starts to increase in the intrinsic condition (see Fig. 5) and is in inversion equal to:

$$C_d+C_s=\frac{\mathrm{d}Q_{ss}}{\mathrm{d}V_g}+q\frac{\mathrm{d}(\Delta n)}{\mathrm{d}V_g}. \tag{7}$$

Provided that C_d+C_s constitutes a quasi-static change of charges, the integration of equation (7) between $V_{g,i}$ and an arbitrary gate voltage in the

inversion region yields the total inversion layer charge:

$$\int_{V_{g,i}}^{V_g} (C_d + C_s)\,dV_g = q\Delta n_{ss} + q\Delta n, \quad (8)$$

where: $q\Delta n_{ss} = Q_{ss}(V_g) - Q_{ss,i}$.
The total inversion layer charge $q\Delta n_{ss} + q\Delta n$ is graphically represented as a function of V_g by the shaded area in Fig. 5. In practice it is found, that in weak inversion $q\Delta n$ can generally be neglected in comparison with $q\Delta n_{ss}$ and equation (8) reduces to:

$$\int_{V_{g,i}}^{V_g} (C_d + C_s)\,dV_g = q\Delta n_{ss}. \quad (9)$$

Like the total amount of trapped charge in interface states in weak inversion, the incremental interface state charge $dQ_{ss}/d\psi_s$ may also be found from the $C_d + C_s$ values, as described in the next section.

4.4 *The determination of the interface state density* N_{ss} *in weak inversion*

The interface state capacitance $dQ_{ss}/d\psi_s$ can be expressed like $qN_{ss}(\psi_s)$[15], where $N_{ss}(\psi_s)$ denotes the interface state density per electron volt. Hereby it is assumed that $N_{ss}(\psi_s)$ does not vary too much over a surface potential interval of magnitude kT/q on both sides of ψ_s.

The information about the interface state density N_{ss} is concealed in equation (7). A combination with equation (3) yields for N_{ss}:

$$qN_{ss} = \frac{C_0}{C_0 - C}(C_d + C_s) - q\frac{d\Delta n}{d\psi_s}. \quad (10)$$

Generally the interface state capacitance qN_{ss} dominates over $q(d\Delta n/d\psi_s)$ in the weak inversion region.

This means that for the condition of weak inversion equation (10) reduces to:

$$qN_{ss}(\psi_s) = \frac{C_0(C_d + C_s)}{C_0 - C}. \quad (11)$$

4.5 *The determination of the bulk dope density*

A consequence of the assumption that in inversion the small signal surface charge is completely supplied by minority carriers entering from the source and drain diffused regions is that the simultaneously appearing bulk hole current will be related exclusively to the small signal silicon depletion charge variations.

This means that the integration of C_b over the inversion region (as shown by the shaded area in Fig. 7) is a measure of the total amount of repelled majority carrier charge from the depletion region:

$$q(\Delta p)_{\max} - q(\Delta p)_i = \int_{V_{g,i}}^{\infty} C_b\,dV_g, \quad (12)$$

where $(\Delta p)_{\max}$ and $(\Delta p)_i$ are the maximum and intrinsic values of the excess majority carrier densities.

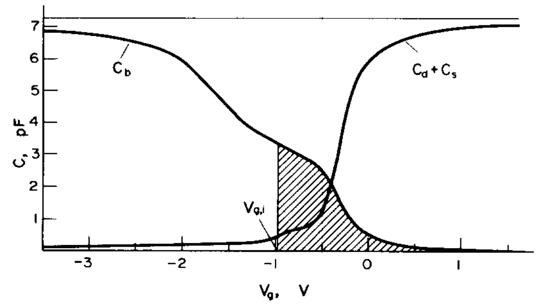

Fig. 7. Low frequency 'split' CV plot, identical to Fig. 5.

The difference $q(\Delta p)_{\max} - q(\Delta p)_i$ is in turn a function of the bulk dope density. This function has been depicted in Fig. 9.

Summarizing we may conclude that the low frequency CV method, extended with the procedure for finding the intrinsic surface potential, together with the low frequency 'split' CV method allow the determination of

(a) the relationship between the gate and surface potentials
(b) the determination of charge trapped in interface states in weak inversion
(c) the interface state density in weak inversion
(d) the bulk dope density.

5. MEASUREMENTS

Investigations have been performed on different types of MOS transistors all of circularly symmetrical geometry. For reasons of brevity only measurements on an n-channel and an p-channel MOS transistor shall be presented. The n-channel MOS transistor has a relatively low density of

interface states in weak inversion ($N_{ss} \approx 10^{10}$/cm^{2}eV) whereas the p-channel MOST has a relatively large interface state density ($N_{ss} \approx 6 \times 10^{11}$/cm^{2}eV). The measurements on these two samples are sufficient to illustrate the behaviour of the channel conductance versus the surface potential in weak inversion. A survey of the characteristics of the MOS transistors has been given in Table 1.

Table 1. Survey of the characteristics of the MOS transistors used for the measurements

Type of channel*	n	P
Surface orientation	100	111
Bulk dope density (cm^{-3})	3×10^{15}	$1 \cdot 1 \times 10^{15}$
Surface mobility (cm^2 V^{-1}sec^{-1})	785 [28]	200
Thickness of oxide (Å)	980	1300
Thickness of P_2O_5 Layer (Å)	300	0
Aspect ratio	56	56

For n-channel MOST: 'dry' oxide is grown at 1200°C.
For p-channel MOST: 'wet' oxide is grown at 1200°C.
Heat treatment to remove interface states:
For n-channel MOST: 450°C – wet N_2: 80°C – H_2O.
For p-channel MOST: 450°C – dry N_2.
*The MOS transistors were manufactured at Philips Research Laboratories, Eindhoven, The Netherlands, and were obtained from Dr. M. V. Whelan.

The MOS transistors were, besides to a low frequency CV measurement also subjected to a low frequency 'split' CV measurement represented in Figs. 5, 7 and 10, respectively. The measurement frequency was 16 Hz. The gate voltage $V_{g,i}$ corresponding to the intrinsic condition of the silicon surface is indicated by its proper location and was obtained by the method as described in Section 3.2.

We found that no change in the shape of the CV and 'split' CV curves occurred when the measurement frequency was varied between 1·6 and 20 Hz. From this we concluded that quasi thermal equilibrium did exist during the capacitance measurements.

The current between the source and drain I_{ds} was measured, while the source and bulk potentials were kept at ground potential and a small voltage (10 mV) between drain and source was maintained. The measured currents I_{ds} have been represented on a logarithmic scale as a function of the gate voltage in Figs. 8 and 11.

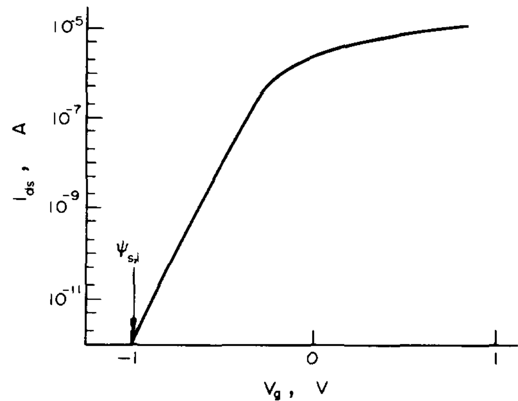

Fig. 8. Log I_{ds} vs V_g plot of the n-channel MOS transistor.

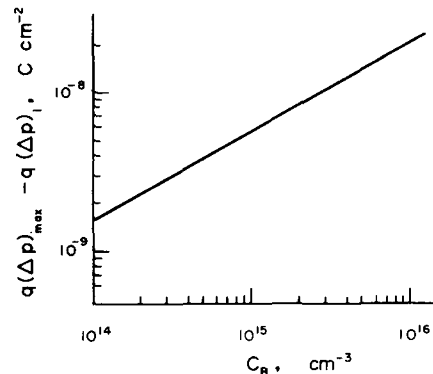

Fig. 9. Total amount of excess majority carrier charge: $q(\Delta p)_{\max} - q(\Delta p)_i$ repelled from the silicon surface if the surface potential ψ_s makes a full excursion throughout the inversion region. This function has been computed for various bulk dope densities.

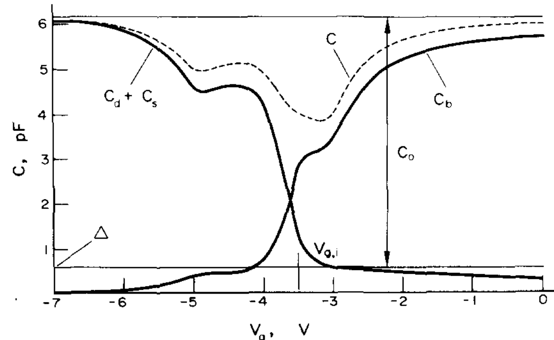

Fig. 10. Low frequency 'split' CV curves of the p-channel MOS transistor with C_B: $1 \cdot 1 \times 10^{15}$ and d_0: 1300 Å.

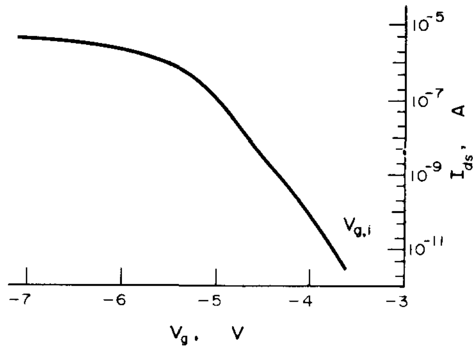

Fig. 11. Log I_{ds} vs V_g plot of the p-channel MOS transistor.

6. EVALUATION OF THE MEASUREMENTS

The MOST channel conductance per square $G_\square$ has been determined graphically as a function of the surface potential ψ_s from the relation $G_\square$ vs. V_g through the use of equation (1) combined with the relation ψ_s vs V_g, determined as described in Sections 3.1 and 3.2. The functions $G_\square(\psi_s)$, thus obtained are represented as log $G_\square$ vs. ψ_s, curves in Figs. 12 and 13 for the n- and p-channel MOS transistors respectively.

The total inversion layer charges $q\Delta n_{ss} + q\Delta n$ of the MOS transistors are determined graphically as a function of ψ_s from the relations $q\Delta n_{ss} + q\Delta n$ vs. V_g and ψ_s vs. V_g. The relation $q\Delta n_{ss} + q\Delta n$ vs. V_g has been obtained by the 'split' CV method as described in section 4.3. The total inversion layer charges have been depicted in Figs. 12 and 13. Also the interface state density N_{ss} in weak and intermediate inversion has been measured by means of the 'split' CV technique, as described in Section 4.4, and is also shown in Figs. 12 and 13.

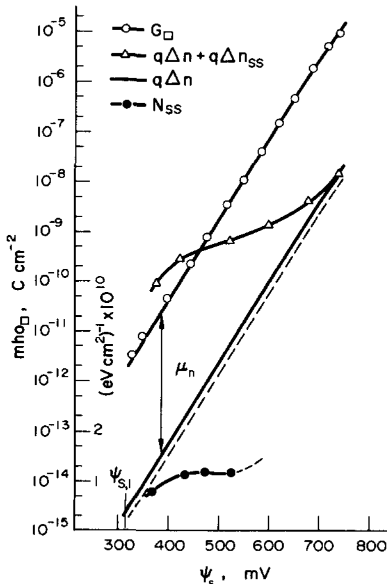

Fig. 12. Log $G_\square$; log $q\Delta n$, log $(q\Delta n + q\Delta n_{ss})$ and N_{ss} vs ψ_s curves of the n-channel MOS transistor.

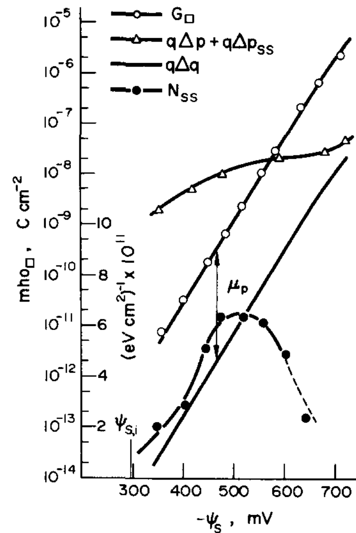

Fig. 13. Log $G_\square$; log $q\Delta p$, log $(q\Delta p + q\Delta p_{ss})$ and N_{ss} vs ψ_s curves of the p-channel MOS transistor.

The bulk dope densities have been deduced from the low frequency 'split' CV curves as described in Section 4.5 and are included in Table 1. These bulk dope densities are verified by the comparison with the results of two other independent measuring methods, also used in Ref. [17].

The surface mobilities listed in Table 1 are derived from the slope of the linear portion of I_{ds} vs. V_g[5]. We found this linear relationship to occur over the surface conductance range between 5×10^{-6}–2×10^{-5} mho$_\square$ for the n-channel MOST and between 1×10^{-6}–5×10^{-6} mho$_\square$ for the p-channel MOST.

7. INTERPRETATION OF THE MEASUREMENTS

As we see from Figs. 12 and 13, the channel conductance is practically proportional to exp $(q\psi_s/kT)$ in weak inversion. The knowledge of ψ_s and C_B enables us to calculate $q\Delta n$ theoretically [16] as is shown by the broken line in Fig. 12. Because $q\Delta n$

varies also with exp $(q\psi_s/kT)$ we surmise that the channel conduction is linearly related to $q\Delta n$ in weak inversion. This means that the surface mobility of the excess minority carriers should be constant in weak inversion.

Because a small error in ψ_s will have a large effect on the computed Δn, we determined the excess minority carrier charge density $q\Delta n$ also by the division of the channel conductance $G_\square$ by the surface mobility, measured in the condition of intermediate inversion as described in the preceding section (solid lines for $q\Delta n$ in Figs. 12 and 13). The voltage shift between the potential scales corresponding to the broken and solid lines for $q\Delta n$ in Fig. 12 was found to have a magnitude of about $\frac{1}{2}kT/q$. A discrepancy of comparable magnitude was found in Fig. 13, where only the solid line for $q\Delta p$ has been drawn. As these discrepancies lie within experimental error we conclude that the weak-inversion mobility is equal to the moderate inversion mobility within the same experimental accuracy.

A comparison of the measured total inversion layer charge density $q\Delta n_{ss}+q\Delta n$ with the excess minority charge density Δn in Fig. 12 and Fig. 13 shows that in weak inversion the total inversion layer charge is orders of magnitude larger. This is especially the case for the p-channel MOS transistor having a much larger interface state density N_{ss}. Towards strong inversion the measured total inversion layer curves in Figs. 12 and 13 approach the mobile excess minority charge curves $q\Delta n$.

8. DISCUSSION

Generally the drain-source current was found to vary more or less logarithmically with gate voltage in weak inversion in the samples we have studied. This is shown in Fig. 8 and Fig. 11. A similar behaviour was already found by Gusev[12], Declerck[13], Barron[11] and Stuart[14]. For an investigation of the conduction in weak inversion a determination of the surface conductance vs. the surface potential is more appropriate rather than vs. V_g, because when interface states are present, the interpretation of $G_\square$ vs V_g plots become troublesome. For this reason we determined both the surface conductance and the amount of trapped charge in interface states vs the surface potential ψ_s.

Theoretical considerations of Greene[19] and Grover[20] on the surface transport in semiconductors, based on Schrieffers original theory [21], predict an almost constant behaviour of the average surface mobility of the excess minority carriers over the entire weak inversion region, which is in agreement with our findings. Physically such a constancy of the surface mobility may be expected, because over the entire weak inversion region, both the average distance d of the excess minority carriers from the interface, as well as the electric field strength F_Z perpendicular to the interface and inside the weak inversion layer remain practically unchanged for a variation in the excess minority surface carrier densities between 10^5–10^{10} cm^{-2}. Over this range the channel width d varies between 220 Å and 150 Å and the surface field E_Z between 3×10^4–$4{\cdot}5\times10^4$ V cm^{-1}, when the bulk dope $C_B = 1\times10^{15}$ cm^{-3}.

A remarkable result of our measurements is the constancy of the surface mobility, irrespective of the amount of trapped charge in interface states. In the n-channel MOS transistor the increase in charged interface states is lower than 2×10^{10} cm^{-2} over the entire weak inversion region. This value is in fact too low[22] to cause a noticeable reduction in the surface mobility by Coulomb scattering of charged interface states. In the p-channel MOS transistor this increase in charged interface states is somewhat larger: $\approx 10^{11}$ cm^{-2}, but still small with respect to the number of interface state charges per unit area: $\approx 3\times10^{11}$ cm^{-2} already present in the intrinsic condition. It should be remarked that for moderate inversion (between 10^{-5} and 10^{-6} mho$_\square$) the value of the surface mobility has been found to be subject to the influence of interface states[9] and bulk dope density[7, 11].

The measured exponential behaviour of $G_\square$ with $q\psi_s/kT$ in Figs. 12 and 13, complies with the weak inversion MOST theories recently developed by Barron[11] Swansson[23] and Memelink[24].

The strong increase in surface mobility between the surface conductance values 10^{-7} and 10^{-5} mho$_\square$, as deduced from Hall measurements [2–4, 6, 7] does not agree with our observations. However doubt has been expressed about the validity of Hall measurements for surface conductances less than $3-10^{-6}$ mho$_\square$[7].

9. CONCLUSION

The measurements and analysis of the MOS transistors as described in Sections 6, 7 and 8

contribute to the following physical picture for the conduction of the MOS transistor in weak and intermediate inversion.

(a) The surface mobility of the excess minority carriers in the channel may be considered to be constant in the conductance range between 10^{-11} and 10^{-5} $mho_{\square}$.
(b) The total inversion layer charge may be regarded to be composed of two sharply distinted portions of mobile and immobile inversion layer charge, where the mobile inversion layer charge can be described by the formula's of Garrett and Brattain.

Knowledge of the distribution of mobile and immobile inversion layer charge is of value for those who are concerned with the study of the electrical and physical behaviour of the MOS transistor in weak inversion. The low frequency 'split' CV method may be used profitably for the determination of this distribution.

It would be quite interesting also to investigate the behaviour of the surface conductance vs surface potential for the condition of an increased surface field, obtained by a reverse bias applied between the source-drain regions and the bulk. Furthermore it should be useful to study the weak inversion surface conductance as a function of surface potential at different absolute temperatures.

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APPENDIX

Estimate of the optimum channellength of the MOS transistor for the application of the low frequency 'split' CV method.

The application of the 'split' CV method is dependent on the validity of the assumption that in inversion the small signal charges in the interface states dQ_{ss} and in the mobile inversion layer $q\mathrm{d}(\Delta n)$ should be supplied exclusively by minority carriers (electrons) originating from the source and drain regions.

However in weak inversion, where $dQ_{ss} \gg q\mathrm{d}(\Delta n)$ the following processes may act as sources of minority carriers in competition with the source and drain regions.
(a) The supply of electrons into the interface states by depletion layer generation.
(b) The emission and capture of holes from the interface states into the valence band.

We will first be concerned with the contribution of electrons in interface states by depletion layer generation. With regard to this contribution the supply of electrons from the source and drain regions will be predominant if the channel conductance $W/L\ G_{\square}$ is much larger than the depletion layer generation recombination conductance $R_{rg}^{-1}WL$. The depletion layer generation-recombination resistance per unit area and under weak non equilibrium conditions [25] is denoted as R_{rg}. This implies that the channel length of the MOS transistor should be chosen

in such a way as to obey the condition:

$$L^2 \ll 12\mu_n q\Delta n R_{rg}. \quad (13)$$

Over the entire inversion region the time constant $1/2p_s c_p$ associated with the hole transition [26] between the interface states and the valence band is larger than $1/2n_s c_n$, the electron transition time constant between these interface states and the conduction band. The variables p_s and n_s are denoted as the concentrations (cm^{-3}) of the holes and electrons at the silicon surface, while c_p and c_n are the hole and electron capture probabilities.

This means that the compliance with the condition that the time constant $1/2p_s c_p$ is also larger than the time constant associated with the interface state capacitance qN_{ss} and the channel conductance is sufficient for the source and drain supply of electrons to the interface states to be dominant over the hole supply from the valence band. This leads to a second requirement to be fulfilled by the channellength L:

$$L^2 \ll \frac{6\mu_n q\Delta n}{qN_{ss}p_s c_p}. \quad (14)$$

The requirements (13) and (14) point to a short channellength for the measurement samples.

On the other hand disturbing influence of the source-drain junction edges on the CV plot should be avoided as much as possible. For this reason we propose that the channel length L should exceed in length the depletion charge depth by a factor of 10–20.

All these requirements lead to a range of allowed values for the channellength as shown in Fig. 6, which has been calculated for bulk dope densities between 10^{14} and 10^{16} cm^{-3} and for n-channel as well as p-channel MOS transistors.

To this end the following numerical constants have been used:

$$n_i = p_i = 1{\cdot}5 \times 10^{10}\,cm^{-3}; \quad c_p = c_n = 10^{-8}\,cm^3 sec^{-1};$$

$$\mu_n = 6 \times 10^2\,cm^2 V^{-1} sec^{-1}; \quad \mu_p = 2 \times 10^2 cm^2 V^{-1} sec^{-1};$$

$R_{rg} \simeq 10^7\,\Omega\,cm^{-2}$ [25, 27]; $qN_{ss} = 10^{-8}\,C/cm^2 eV$ in an energy interval of magnitude $4\,kT$ (eV) centered around the intrinsic condition and $q\Delta n = q(\Delta n)_i$.