Mater. Res. Soc. Symp. Proc. Vol. 911 © 2006 Materials Research Society 0911-B12-03

Effects of Different Defect Types on the Performance of Devices Fabricated on a 4H-SiC Homoepitaxial Layer

Hui Chen[1], Balaji Raghothamachar[1], William Vetter[1], Michael Dudley[1], Y. Wang[2], and B. J. Skromme[2]
[1]Materials Science and Engineering, Stony Brook University, Stony Brook, NY, 11794-2275
[2]Electrical Engineering, Arizona State University, Tempe, AZ, 85287-5706

ABSTRACT

An 8° off-axis 4H-SiC wafer with circular Schottky contacts fabricated on a CVD grown 4H-SiC homoepitaxial layer was studied to investigate the influence of various defects, including small (closed-core) screw dislocations (Burgers vector of 1*c* or 2*c*), hollow-core (micropipes; Burgers vector larger than 2*c*), threading edge dislocations (from conversion of basal plane dislocations from the substrate into the epilayer), grain boundaries and triangular defects, on the device performance in the form of breakdown voltages. The defects were examined using synchrotron white beam x-ray topography (SWBXT) based techniques and molten KOH etching. The devices commonly contained basal plane dislocations, small screw dislocations and threading edge dislocations, the latter two of which could give rise to low breakdown voltages for the devices. In addition, less commonly observed defects such as micropipes, grain boundaries and triangular defects are much more destructive to device performance than closed-core screw dislocations and threading edge dislocations.

INTRODUCTION

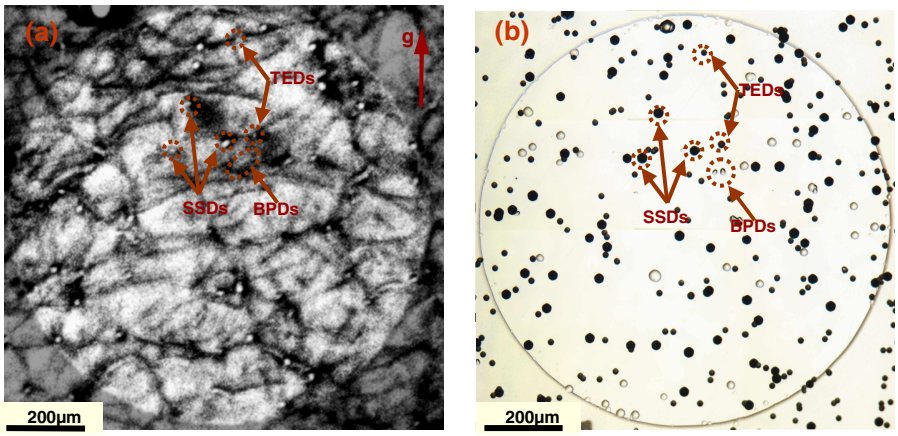
In last few decades, silicon carbide (SiC) has become a prominent material for various applications, such as high temperature, high-power electronics and radiation-hard electronic technologies [1]. SiC technology has advanced rapidly with steady improvements in quality and size [2,3]. Despite these achievements, several factors currently limit the overall crystalline quality of SiC and as a consequence the device performance. In particular, defects in SiC crystals are considered to be a major roadblock to further development. As it is widely recognized that defects in SiC degrade device performance, it would be useful to characterize the effect each defect type has on the device properties. SWBXT is a powerful tool which has high strain sensitivity and provides suitable spatial resolution to image dislocations in crystals [4]. Molten KOH etching has also been proven to be a fast and convenient method to reveal dislocations in SiC [5,6], especially screw dislocations (both 1*c*/2*c* and micropipes) and threading edge dislocations. To this end, a combination of SWBXT and KOH etching has been applied to investigate the influence of different defects, including dislocations, grain boundaries and triangular defects, on Schottky devices fabricated on 4H-SiC homoepitaxial layers deposited on an 8° off-axis 4H-SiC wafer. These defect types were examined using a correlation between grazing incidence and back reflection SWBXT, KOH etching and electrical measurements. Back reflection geometry was adopted to map the distribution of screw dislocations. In order to distinguish dislocations in the epilayer from those in the substrate, grazing incidence geometry was employed to record dislocation information exclusively from the epilayer.

EXPERIMENTAL DETAILS

The 10µm-thick and lightly doped 4H-SiC epilayer (N_D=5x10^{15} cm^{-3}) was grown on an n^+ 4H-SiC substrate (N_D=8x10^{18} cm^{-3}) with 8^o off-cut from [0001] toward the [11-20] direction. Unterminated circular Schottky contacts were formed by evaporation of 500 Å Ni/3000 Å Au through a shadow mask on the wafer, with diameters from 200 to 1000 µm. The breakdown measurements were performed using a Keithley model 237 source-measure unit. The breakdown voltage is defined as the voltage yielding a current density of 0.1 A/cm^2. The metallization was chemically removed on both sides of the sample after breakdown measurements to reduce noise in the SWBXT images. The back side of the wafer was then chemically-mechanically polished to reduce strain. The molten KOH etching was carried out at 500 ^{o}C for 5 minutes.

After KOH etching, SWBXT experiments were carried out at the Stony Brook Topography Facility (Beamline X-19C) at the National Synchrotron Light Source, at Brookhaven National Laboratory. The x-ray beam had a wavelength spectrum ranging from 0.1 to 2.00 Å, with peak intensity at around 0.8 Å. The specimen-film distances were set to be 10-25 cm depending on background noise and desired diffraction patterns. The optical Nomarski microscopy was performed on a Nikon Ellipse E600 JSL Optical Microscope.

DISCUSSION



(a) **(b)**

Fig. 1. (a) Grazing incidence x-ray topograph of defect structure in a typical circular device with g=$11\bar{2}8$; (b) Nomarski optical micrograph of the same device as (a) after molten KOH etching.

Small screw dislocations (SSDs), threading edge dislocations (TEDs) and basal plane dislocations (BPDs) are the major defects present in all the studied devices. Figures 1(a) and (b) show a one-to-one correspondence between defects and their related etch pits in a typical circular Schottky device. As shown in the x-ray topograph [Fig. 1(a)], SSDs and TEDs exhibit white

circular contrast with diameters of more than ten microns and a few microns, respectively, and BPDs appear as dark lines. In Fig. 1(b), the SSD-related etch pits appear as large black hexagons, TED-related etch pits appear as smaller black hexagons and BPD-related etch pits appear as white seashell shapes. The SSDs propagate from the substrate into the epilayer in a nearly perpendicular direction to the surface and are thus readily revealed by KOH etching. This conclusion has been confirmed by correlation of the SWBXT and KOH etching results. In contrast, BPDs can propagate from the substrate into the epilayer in two different ways. Some remain in the basal plane and directly propagate into the epilayer while others are converted into TEDs in the epilayer due to image forces [7]. The TEDs thread almost normal to the epilayer surface and are again be as readily etched as SSDs by molten KOH.

Apart from the three commonly occurring defects discussed above, micropipes (MPs), grain boundaries (GBs) and triangle-shaped defects (TDs) exist in a few devices. Figures 2 and 3 illustrate a device that contains a MP, a GB and a TD. Micropipes are open-core screw dislocations having Burgers vectors larger than 2*c* in 4H-SiC crystals. This causes their strain fields to be correspondingly larger than those of SSDs. Therefore, their etch pits are relatively large and they appear as white contrast features that are larger than SSDs in Figures 3(a) and (b). The GBs can be formed by a row of BPDs or TEDs, which have Burgers vectors in the basal plane. For $\mathbf{g} = 000 \cdot 16$, $\mathbf{g} \cdot \mathbf{b} = 0$ and $\mathbf{g} \cdot \mathbf{b} \times \mathbf{l} = 0$ for threading edge dislocations, so such dislocations should be invisible in this reflection. This condition is consistent with the threading edge boundary being visible in Fig. 3(b) and invisible in Fig. 3(a). The TDs in this sample are found to have a base which intersects the sample surface and is perpendicular to the off-cut direction. Okada *et al.* [8] observed that at the base of the triangular defect, there was a stacking fault (SF) bounded by two partial dislocations. One perfect dislocation oriented in a $[1\bar{1}20]$ direction dissociated into the two partial dislocations to form the base of the 3C-polytype inclusion and the associated stacking fault. Zhou *et al.*[9] suggested that TDs were linked to a 4H to 3C polytype phase transformation initiated by stacking faults that intersect a vertical step ledge during epitaxial growth. The replication of their partial dislocation ledge intersections can give rise to the formation of 3C platelets.

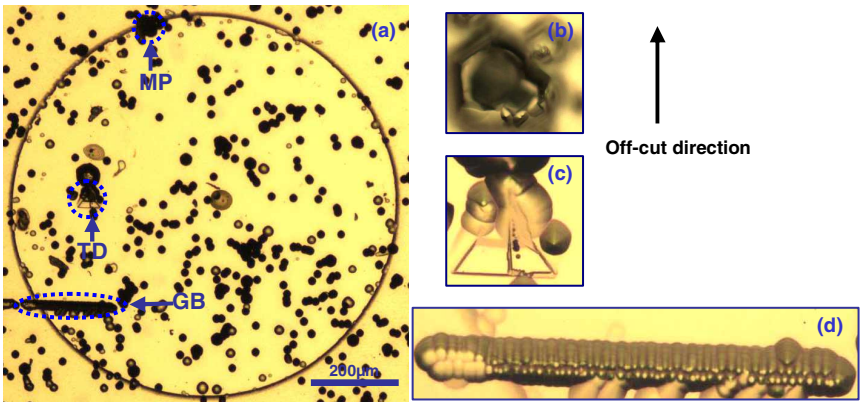
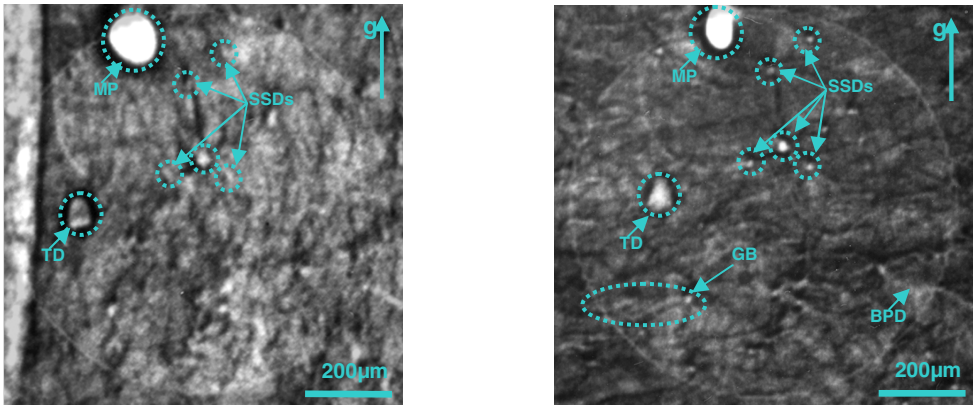


Fig. 2. Optical micrograph of defect structure in a device after KOH etching. (a) Overview of the device; (b) Enlargement of the MP etch pit in (a); (c) Enlargement of the TD etch pit in (a); (d) Enlargement of the GB etch pit in (a).



(a) (b)

Fig. 3. X-ray topographs of structural defects in the same device as Fig.2. (a) Back reflection topograph with g=000•16; (b) Grazing incidence topograph with g=$1\bar{1}28$.

The density of each defect type (except for BPDs) was determined from the results of SWBXT and KOH etching to examine the influence of each defect type on the breakdown behavior of the devices. Since every device has SSDs and TEDs, in order to better study their effects on the electrical properties, the devices containing only those two types of defect were chosen. Figure 4 shows the relationship between the numbers of SSDs and the breakdown voltage in devices of five different sizes. For each device size, the breakdown voltages tend to decrease as the densities of SSDs increase. Therefore, high densities of SSDs can lead to low breakdown voltages, in agreement with the results from Wahab's group [10]. It can also be seen from Fig. 5 that as the number of TED goes up, the breakdown voltage is reduced. The breakdown voltages in these devices are certainly limited by the lack of edge termination, but the low values seen in certain specific devices are likely due to defects rather than to edge effects, which should not change much from device to device.

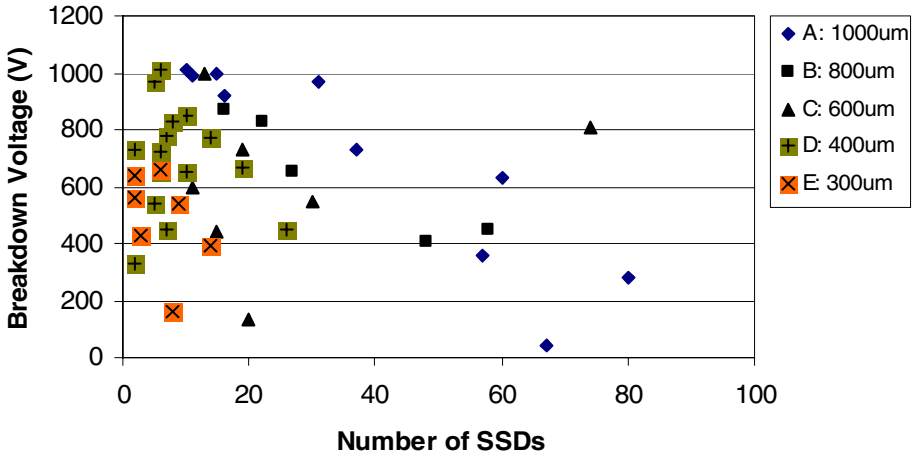


Fig. 4. Correlation between numbers of SSDs and breakdown voltages for different device sizes

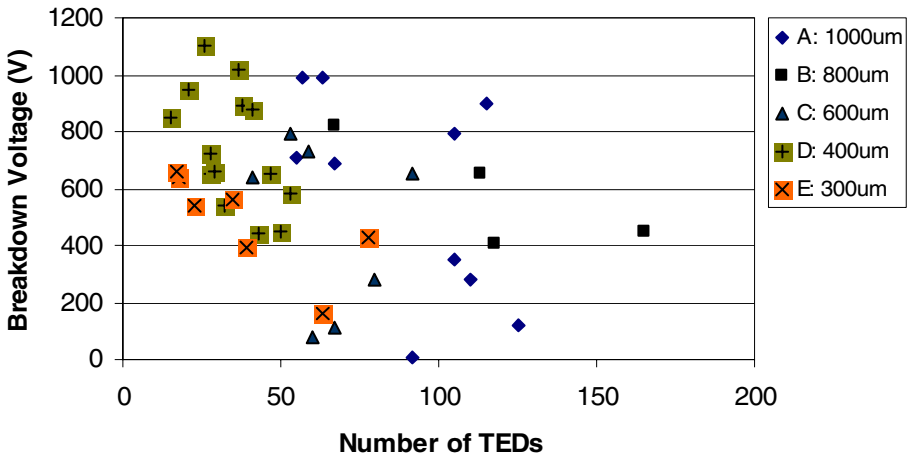


Fig. 5. Correlation between numbers of TEDs and breakdown voltages for different device sizes

Even though the devices containing micropipes, grain boundaries and triangular defects also contain SSDs and TEDs, the effects of these additional defects on device performance could be tentatively explored. Table 1 lists the correlation between the defect densities and the breakdown voltages of the related devices.

Table 1. Summary of the effects of various defects on breakdown voltages in the studied wafer

Defect type	Defect density	Median $V_{breakdown}$ (V)
Threading edge dislocations [a]	1.9×10^4 cm^{-2} (42)[e]	604 (42)[e]
Small screw dislocations [a]	6.3×10^3 cm^{-2} (42)	566 (42)
Micropipes [b]	1 /device (16)	308 (16)
Grain boundaries [c]	5 cm^{-1} (11)	314 (11)
Triangular defects [d]	1 /device (5)	130 (5)

[a] Devices chosen only contain SSDs and TEDs.
[b] Devices chosen only contain SSDs, TEDs and MPs.
[c] Devices chosen only contain SSDs, TEDs and GBs.
[d] Devices chosen only contain SSDs, TEDs and TDs.
[e] Numbers in parentheses represent the numbers of devices from which the averages are obtained.

TEDs and SSDs are much more densely distributed in the devices than other defects, but they have less effect on the breakdown behavior. On the contrary, despite the much lower densities, MPs, GBs and especially TDs influence device performance far more significantly than TEDs and SSDs. Micropipes have been well documented to degrade device performance [11-13]. However, few papers have reported the influence of GBs on SiC devices [14]. The GBs in the present sample comprise continuous rows of TEDs or BPDs. Whereas individual TEDs have a small influence on device performance, tightly spaced arrays such as in a grain boundary are proposed to be much more harmful. Although they have the lowest density, TDs have the most

profound effect on device performance. The much lower breakdown voltages in devices having TDs were proposed to result from the fact that the 3C structure has a lower barrier height than the 4H structure [15,16]. In general, MPs, GBs and TDs are highly detrimental to device performance.

CONCLUSIONS

Small screw dislocations and threading edge dislocations are the most common defects observed in the devices studied. As their densities increase, the device performance deteriorates. On the other hand, while micropipes, grain boundaries and triangular defects were much less commonly observed, they drastically degrade the device performance.

ACKNOWLEDGMENTS

This work was supported by the National Science Foundation under Grant No. ECS 0324350 and by a Motorola Semiconductor Product Sector Sponsored Project. All of the X-ray topography experiments were carried out at Stony Brook Topography Facility (Beamline X19C) at the National Synchrotron Light Source (NSLS), Brookhaven National Laboratory, which is supported by the U.S. Department of Energy (D.O.E.).

REFERENCES

1. H. Morkoc, S. Strite, G. B. Gao, *et al.*, *J. Appl. Phys.* **76**, 1363 (1994).
2. D. Hobgood, M. Brady, W. Brixius, *et al.*, *Mater. Sci. Forum* **338**, 3 (2000).
3. R. L. Myers, Y. Shishkin, O. Kordina, *et al.*, *J. Crystal Growth* **285** (4), 486 (2005).
4. M. Dudley, X. Huang and W. Vetter, *J. Phys. D: Appl. Phys.* **36**, A30 (2003).
5. K. Koga, Y. Fujikawa, Y. Ueda and T. Yamaguchi, *Amorphous and Crystalline Silicon Carbide IV, Springer Proceedings in Physics* **71**, 96 (1992).
6. S. I. Maximenko and T. S. Sudarshan, *J. Appl. Phys.* **97**, 074501 (2005).
7. S. Ha, P.Mieszkowski, M. Skowronski, *et al.*, *J. Crystal Growth* **244**, 257 (2002).
8. T. Okada, T. Kimoto, K. Yamai *et al.*, *Mater. Sci. Engrg*. **A361**, 67 (2003).
9. W. L. Zhou, P. Pirouz and J. A. Powell, *Mater. Sci. Forum* **264-268**, 417 (1998).
10. Q. Wahab, A. Ellison, A. Henry, *et al., Appl. Phys. Lett.* **76** (19), 2725 (2000).
11. M. Dudley, S. Wang , W. Huang , *et al.*, *J. Phys. D: Appl. Phys. A* **28**, 63 (1995).
12. X. R. Huang, M. Dudley, W. M. Vetter, *et al.*, *Appl. Phys. Lett*. **74**, 353 (2000).
13. Y. Wang, G. N. Ali, M. K. Mikhov, *et al.*, *J. Appl. Phys.* **97**, 013540 (2005).
14. S. Izumi, I. Kamata, T. Tawara, *et. al.*, *Mater. Sci. Forum* **457-460**, 1085 (2004).
15. A. Itoh and H. Matsunami, *Phys. Status Solidi A* **162**, 389 (1997).
16. Y. Ding, K. B. Park, J. P. Pelz, *et al.*, *Phys. Rev. B* **69**, 041305 (2004).