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On the Influence of the Position-Dependence of Stress on Device Performance

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We investigate the effect of the position-dependence of stress on device simulation in a 65 nm node technology using mechanical simulations for the stress created by a nitride liner in the n-MOSFETs and by SiGe source /drain pockets in the p-MOSFETs. For gate lengths below 0.1 μm, the difference in the linear and especially the saturation drain current becomes negligible when either considering the position-dependence of stress or using a constant stress picked from the source-side of the channel. In contrast, significant differences in the current enhancements exist for different mobility models (linear piezoresistance versus Intel hole mobility model) and different transport equations (drift-diffusion versus hydrodynamic).

Introduction

Stress engineering has become the major approach for performance enhancement of current CMOS technology. The first realized strained MOSFETs were fabricated by growing a thin Si layer on a SiGe substrate resulting into global biaxial tensile strain. In contrast, process-induced strain involves a stress which varies as a function of the position in the device. Both from the viewpoint of process development and device simulation, this raises the question, at which position the stress influences device behavior most significantly and hence where stress should be optimized and considered most accurately. This issue is addressed in this work by comparing device simulations based either on the stress obtained from mechanical simulation or picked from the source-side of the channel taken as constant in the whole device.

Simulation Approach

The mechanical 2D stress simulations are performed with Sentaurus Process (1) and are based on the anisotropic law of Hook which relates the strain tensor to the stress tensor using the three independent elastic constants of Si (C12=0.65 Mbar, C11=1.675 Mbar and C44=0.8 Mbar). In the case of the n-MOSFETs, stress originates from a 1.6 GPa tensile nitride cap layer with a <100> channel orientation (similar to (2)). The resulting source-side channel stress has a compressive component perpendicular to the Si/SiO2 interface going from 160 MPa in the long-channel device to 450 MPa in the short-channel device, and a tensile component in channel direction ranging from 50 to 350 MPa, respectively. The p-MOSFET is stressed via SiGe source/drain pockets with a Ge-content of 20 % (similar to (3)), leading to a perpendicular tensile stress from 40 MPa to 150 MPa and a longitudinal compressive stress from 140 to 430 MPa, respectively. Shallow trench isolation (STI) was considered in the stress simulation.

Device simulation is done either with the drift-diffusion or the hydrodynamic model using the linear piezoresistance (4) or the Intel hole mobility (5) model, which are applied both to the bulk and the surface low-field mobility. In contrast, the saturation velocity is left unchanged under stress.

Influence of the Position-Dependence of Stress

Figures 1 and 2 show the stress-induced improvements of the linear (Idlin) and the saturation (Idsat) drain currents as a function of the gate length for n- and p-MOSFETs, respectively, for a 65 nm node technology with a supply voltage of 1.1 V.

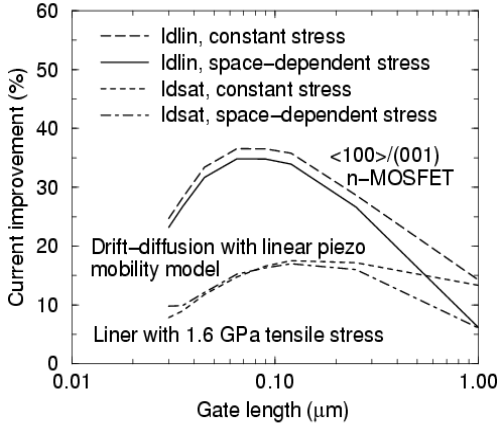

Figure 1. Drift-diffusion simulations with the linear piezoresistance model for n-MOSFETs with a cap layer under tensile stress.

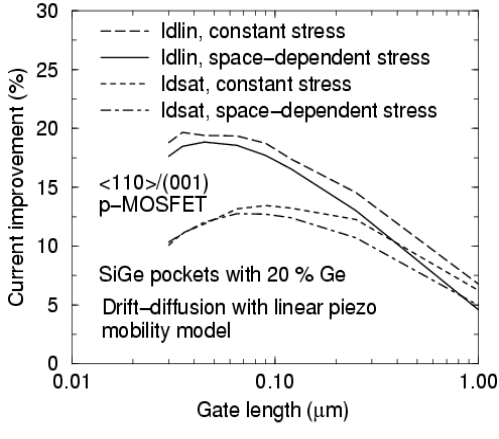

Figure 2. Drift-diffusion simulations with the linear piezoresistance model for p-MOSFETs with source/drain SiGe pockets.

Here, always drift-diffusion simulations with the linear piezoresistance model are employed. It can be seen that taking the space-dependence of stress into account or considering a constant stress, picked from the source-side of the channel, leads for short channels to a similar current improvement, while the results significantly differ for long channels. The reason for the latter effect is that the stress strongly varies in a long-channel device with a peak at the source-side of the channel. Consequently, taking this high stress from the source-side of the channel for the whole device leads to an overestimation of the current improvement. The situation is different for a short-channel device because the stress changes only relatively weakly along the channel and because the quasi-ballistic current of a nanoscale MOSFET is determined in the source-side of the channel (6, 7). Therefore, the difference of the stress-induced improvements for Idlin and especially for Idsat are very small when either picking the stress from the source-side of the channel or when considering the position-dependence of the stress. Finally note that the scaling behavior is governed by two competing effects. On the one hand, the stress level increases for decreasing gate length. On the other hand, the stress-induced drift velocity enhancement becomes smaller for higher longitudinal electric fields and hence shorter gate lengths (8) which explains the decrease of the current improvements for smaller gate lengths.

Influence of the Transport Model

Having established that the current enhancements in the nanoscale regime are almost not influenced by the position-dependence of the stress, the question arises how sensitive the current improvements are to the transport model used in the device simulation. Therefore, we compare in figure 3 the Idsat improvements in p-MOSFETs obtained with three different transport models. On the one hand, two drift-diffusion simulations are

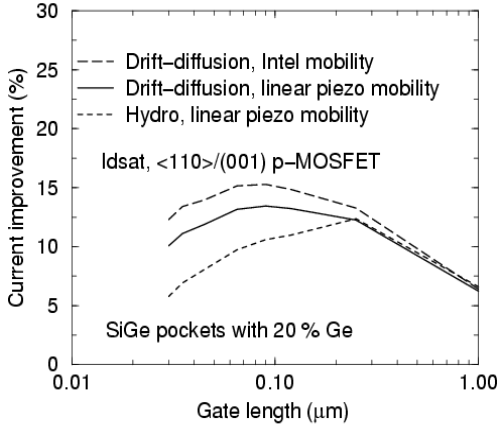

Figure 3. Saturation current improvement in p-MOSFETs as obtained from (i) drift-diffusion simulation with the Intel hole mobility, (ii) drift-diffusion simulation with the linear piezoresistance model and (iii) hydrodynamic simulation with the linear piezoresistance model

done using either the linear piezoresistance model as before or employing the Intel hole mobility model. On the other hand, hydrodynamic simulations with the linear piezoresistance model are performed (without changing the energy relaxation time under stress). The resulting current enhancements not only significantly differ for different mobility models, but also for the same mobility model when using different transport equations. The reason for the latter effect is that different transport equations can exhibit different effects such as velocity overshoot which in turn are influenced by stress in a different manner.

Conclusions

We have investigated the relevance of the position-dependence of stress and the transport model for stress-induced drain current improvements. The position-dependence turns out to have almost no influence in the nanoscale regime, while the current enhancements can strongly differ for different transport models. Our analysis therefore suggests that a good compromise for estimating performance enhancements in nanoscale MOSFETs will be Monte Carlo device simulation based on a band structure computed for the stress in the source-side of the channel.

Acknowledgments

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