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A Self-Aligned Gate-All-Around MOS Transistor on Single-Grain Silicon

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A self-aligned gate-all-around metal-oxide-semiconductor (MOS) transistor technology is proposed and demonstrated. The self-aligned structure is realized by first forming two dummy gates self-aligned to each other, and then replacing them with a real poly-Si gate. The self-aligned gate-all-around transistor is fabricated on a single grain of silicon film. The metal-induced unilateral crystallization technique and subsequent high-temperature annealing are combined to achieve the single grain silicon. The implementation of the self-aligned structure and large size of single-grain silicon is visualized using scanning electron microscopy imaging. Measurement results show that the performance of the fabricated gate-all-around transistor is highly comparable to that of a conventional single-crystal transistor, indicating the successful formation of the single-grain transistor.
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Multigate metal-oxide-semiconductor field-effect transistors (MOSFETs) have been considered the most promising devices for complementary MOS (CMOS) technology scaling into nanoscale generations due to their inherent merits such as high immunity to short channel effect, nearly ideal subthreshold slope, and large drive current.[1-4] Compared to other multigate schemes such as double-gate and trigate, the gate-all-around (GAA) configuration is believed to offer the best scalability because the gate controls channel region on all sides. While the multigate devices are attractive, the fabrications are much more complicated than that of their single-gate MOSFET [both bulk and silicon-on-insulator (SOI)] counterparts. In particular, implementation of the self-aligned structures has been shown to be very difficult. Over the years, self-aligned fabrication processes for the double-gate and trigate devices have been demonstrated.[5-9] However, no self-aligned fabrication method for the gate-all-around structure has been reported so far although some fabrication processes have been demonstrated.[10-12]

In this article, a self-aligned GAA MOS transistor technology is reported. The implementation of the self-aligned structure is described in detail. The formation technique of the large size of single-grain silicon on which the devices are fabricated is also studied. The characteristics of the fabricated devices are presented and elaborated on.

The key processing steps are illustrated in Fig. 1. Silicon wafers with 5000 Å of thermal oxide are used as the starting substrates. 200 Å of nitride, 2000 Å of low-temperature oxide (LTO), 400 Å of a-Si and, again, 2000 Å of LTO are deposited successively by low-pressure chemical vapor deposition (LPCVD). The top three layers of films (LTO, a-Si, and LTO) are then patterned as shown in Fig. 1a. The patterned LTO layers at the top and bottom are dummy gates to be replaced by the real gate. Following that, 2500 Å of a-Si is deposited at 550°C by LPCVD and doped with P^+ implantation. The dose and energy are 4×10^{15} cm^{-2} and 45 keV, respectively. After the implantation, a chemical mechanical polish (CMP) is performed to remove the a-Si on the elevated areas, with the oxide beneath as the polish stop, as shown in Fig. 1b. After the CMP, the remaining a-Si film is crystallized into poly-Si using metal-induced unilateral crystallization (MILC) technique.[13,14]

As shown in the Fig. 1c, the MILC process consists of the deposition of a 4000 Å LTO, the opening of a 2 μm wide seeding window, the evaporation of a 50 Å nickel film, and annealing at 560°C for 24 h in nitrogen ambient. The unconsumed nickel and the LTO are then removed. Figure 2a shows the surface features of the MILC regions. An interesting feature is that the poly-Si grains are almost in a long stick structure, and have the same orientation perpendicular to the nickel strip.

The active area is then defined and the dummy LTO at the bottom is also exposed as shown in Fig. 1d. The LTO is removed in buffered oxide etch (BOE) as shown in Fig. 1e. Figure 1e′ shows the scanning electron microscopy (SEM) picture of the cross section immediately after this step. A thin silicon beam supported by the thick silicon layers at the two sides is formed. The thin silicon beam and the two thick silicon layers are the channel and source/drain regions of the device, respectively. Further, a trench on the beam and a tunnel under the beam are also formed. The trench and tunnel define the geometry of the top gate (TG) and bottom gate (BG), leading to a self-aligned gate structure since they are aligned to each other in nature.

An annealing step is then performed at 900°C for half an hour in N_2 ambient. Figure 2b shows the surface topography of the silicon film after this step. The grain sizes are significantly enlarged in both length and width. The grain enhancement is attributed to the secondary grain crystallization during the high-temperature annealing.[15] During the secondary crystallization, the smaller grains are consumed as a small number of grains expand due to surface energy anisotropy. The process continues until the secondary grains impinge on one another, forming large monomodal-distributed grains. In particular, the secondary grain crystallization in the MILC poly-Si is facilitated because of two unique factors, that is, the same grain orientation and the low activation energy due to the existence of nickel.[16] As a result, very large grains of up to tens of micrometers in size are formed. In addition, the integrity of the silicon crystal is also improved by the high-temperature annealing. This is verified by the transmission electron diffraction (TED) pattern as shown in the insets of Fig. 2. The TED pattern of the MILC region with the high-temperature annealing approaches that of single-crystal silicon, indicating an improvement in crystal integrity. Thus, high quality single-grain silicon with a grain size large enough to accommodate the entire device area can be obtained by incorporating the MILC process and the subsequent high-temperature annealing.

Following the single-grain formation, 80 Å of sacrificial oxide is grown thermally at 850°C and then removed in BOE to improve the surface topography of the silicon beam (channel region). After 100 Å of gate oxide formation, 2500 Å of phosphorus *in situ* doped poly-Si is deposited conformably as gate electrode material and CMP is applied to remove the unwanted poly-Si down to the oxide that acts as a polish stop, as shown in Fig. 1f. After patterning the gate pad, the conventional back-end steps including passivation layer deposition, contact hole opening, and metallizaion, are performed to complete the process. Figure 1f′ shows the SEM photograph of the cross-sectional view of the fabricated device, indicating the successful implementation of the self-aligned structure.

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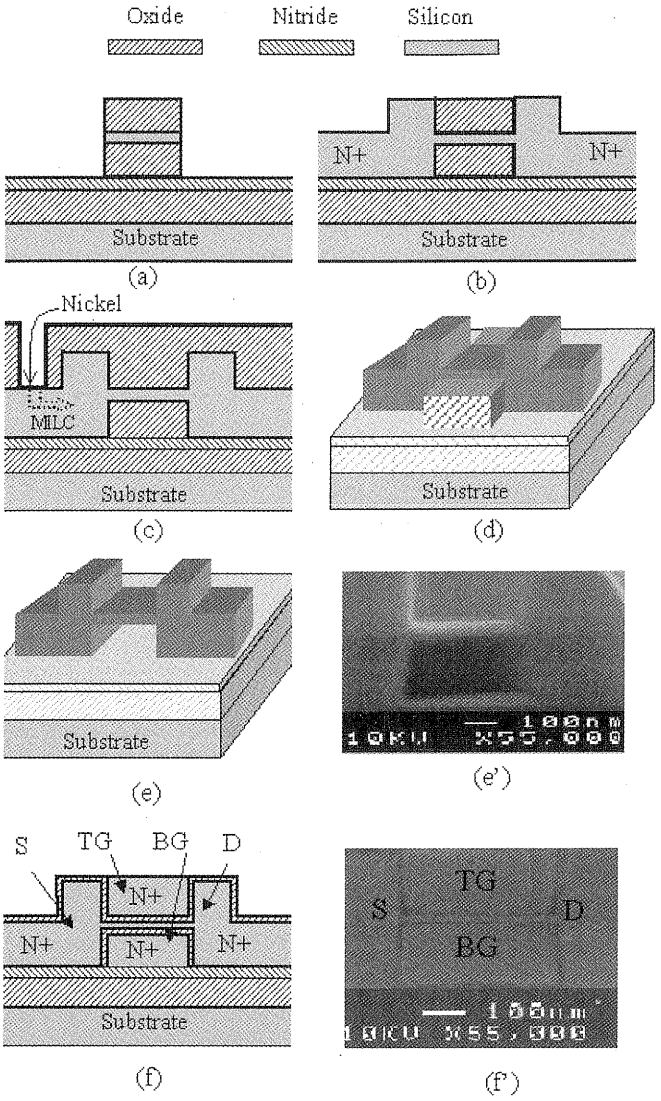

Figure 1. Schematic key fabrication process steps for self-aligned gate-all-around MOSFET.

Figure 3a shows the gate-transfer characteristics of a fabricated GAA device. For comparison, those of a conventional single-gate (SG) SOI MOSFET fabricated in the same run is also included in the figure. Figure 3b shows the output characteristics of the GAA device. The channel length L, channel width W, gate oxide thickness, and the silicon film thickness in the channel region of the devices are 0.37 μm, 0.35 μm, 10 μm, and 25 nm, respectively. The effective electron mobility, subthreshold slope, and threshold voltage of the GAA device are measured to be 346 cm^2/V s, 67.3 mV/dec, and 0.21 V, respectively. Those of the conventional single-gate SOI MOSFET are 327 cm^2/V s, 67.1 mV/dec, and 0.34 V, respectively. It can be seen from these experimental results that the characteristics of the GAA device are in general not inferior to those of the SG device on single-crystal film. This confirms, experimentally, that the GAA device is formed on the single-grain silicon. It is also seen that the value of subthreshold slope of the GAA device is a little larger than the ideal one (60 mV/dec), and that it is slightly inferior to that of the SG SOI device. In theory, the subthreshold behavior of a multigate device should be better than that of a single-gate device, and almost close to the ideal one. It is believed that the nonideal subthreshold slope observed in the GAA device results from the relatively high trap density at the interfaces between the channel region and the gate.

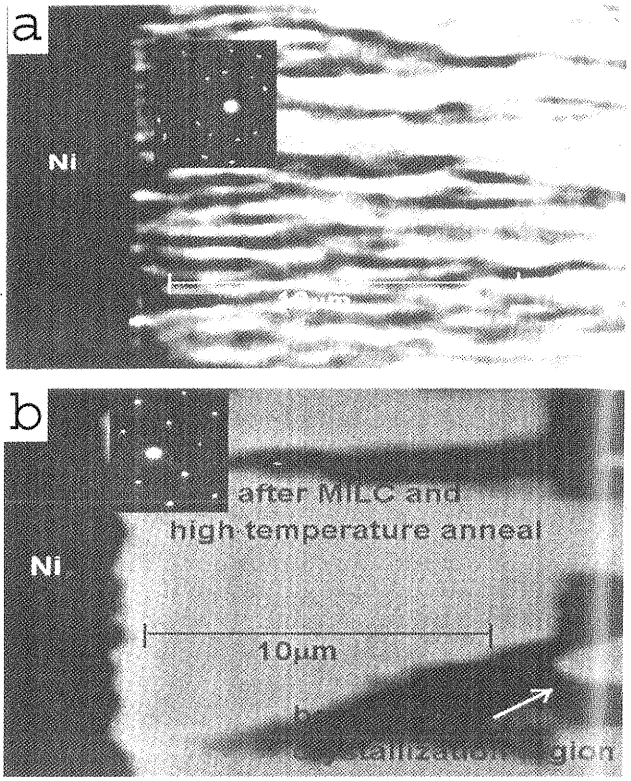

Figure 2. Surface SEM topographies of the crystallized silicon film. (a) Right after low temperature MILC process, and (b) after MILC process and high-temperature annealing. The insets show the TED patterns.

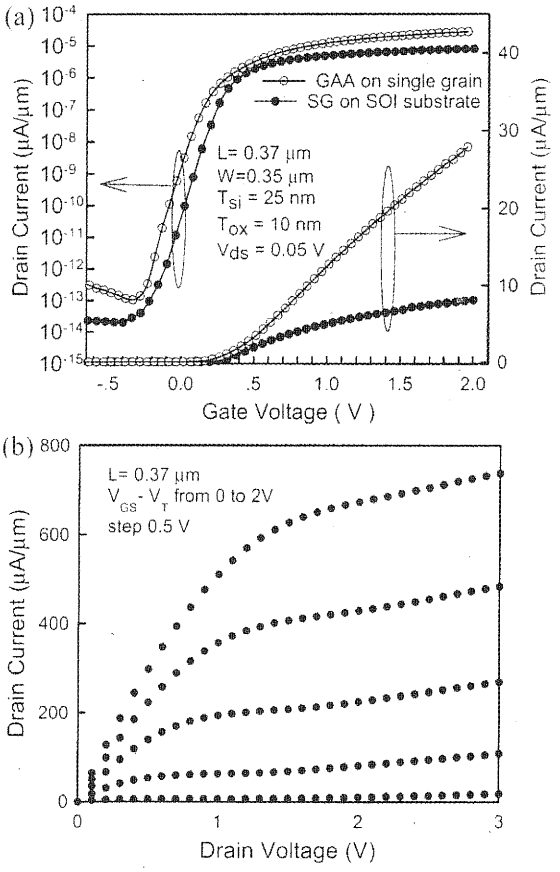

Figure 3. Current-voltage characteristics of the fabricated devices; (a) transfer characteristics and (b) output characteristics.

Moreover, it can be seen that the on-current of the GAA device is over two times larger than that of the SG SOI device at high gate voltages. Although a double-gate device can potentially provide more than two times larger on-current than the single-gate device can if the volume inversion effect appears,[3] it is not true here because the 25 nm of body film is not thin enough to make the volume inversion happen. As shown in the linear coordinate, the on-current of the SOI device becomes saturated at high gate voltages. It is believed that the current degradation is due to the large source/drain (S/D) parasitic resistance caused by the thin S/D region and the nonsilicide process. In the GAA device, the thick S/D region generated by the proposed technology provides a reliable S/D contact and low S/D sheet resistance, resulting in a remarkably low S/D resistance despite the nonsilicide process. The low S/D resistance of the GAA device is also reflected in Fig. 3b where no current crowding is observed at low drain voltages. The leakage current of the GAA device is larger than that of the SG SOI device and depends considerably on the gate biases, as can be seen in Fig. 3a. The larger leakage current could arise from the field emission of carriers through the traps associated with the crystal defects in the channel near the drain since the device is fabricated in the recrystallized silicon film. The field-emission current depends strongly on the maximum lateral electric field ($\mathbf{E}_m$) that usually increases with increasing the negatively biased gate voltages.[17] Therefore, the field emission would be exaggerated in the multigate structure because the multigate device has a higher $\mathbf{E}_m$ than a single-gate device. The crystal defects and the higher lateral electric field in the GAA device lead to the larger leakage current.

In summary, a novel self-aligned GAA MOSFET technology has been proposed and demonstrated. The technology includes the implementation of the self-aligned gate structure and the formation of a large-size of single-grain silicon film. The GAA device has been fabricated using the technology. The visualized self-aligned device structure and the experimentally measured device characteristics have verified the feasibility of the proposed technology.

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