Design trade-offs in ADC architectures dedicated to uncooled infrared focal plane arrays.

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ABSTRACT

This paper presents two different architectures for the design of Analog to Digital Converters specifically adapted to infrared bolometric image sensors. Indeed, the increasing demand for integrated functions in uncooled readout circuits leads to on-chip ADC design as an interface between the internal analog core and the digital processing electronics. However specifying an on-chip ADC dedicated to focal plane array raises many questions about its architecture and its performance requirements. We will show that two architecture approaches are needed to cover the different sensor features in terms of array size and frame speed. A monolithic 14 bits ADC with a pipeline architecture, and a column 13 bits ADC with an original dual-ramp architecture, will be described. Finally, we will show measurement results to confirm the monolithic ADC is suitable for small array, as 160 x 120 with low frame speed, while a column ADC is more compliant for higher array, as 640 x 480 with a 60 Hz frame speed or 1024 x 768 arrays.
Keywords: ADC, Uncooled microbolometer, IRFPA

1 INTRODUCTION

Nowadays infrared sensors successfully follow a road already walked by visible light image sensors. With smaller pixel pitch, higher resolution and easier system integration, uncooled microbolometer infrared sensors intend to address new low-cost/high-volume applications such as automotive for night vision and pedestrian detection [1] [2]. Machine vision and an unattended sensor also benefit from a low-cost and highly integrated infrared focal plane arrays. Thanks to deep submicron technologies, it is now possible to embed image processing, non-uniformity correction [3] or even TEC-LESS algorithms onto the silicon focal plane array. However, bolometric readout circuits remain mostly analog devices [4] [5] and the need for on-chip analog-to-digital converters has been growing tremendously in recent years.

2 ARCHITECTURE

2.1 Trade–off in uncooled infrared imaging

For ADC design trade-off in the uncooled focal plane array four mains points have to be considered: number of bits, power consumption, location in the analog chain and production yields.
Specifying the ADC begins with a full understanding of infrared image sensor key figures related to the intended applications. The goal of this ADC design is to be integrated on an uncooled focal plane array. It has certain impact on the ADC design. First bolometric sensors have a very wide output dynamic range from 1 to 4.2 V on a 5V process. Noise is also an important figure for infrared imagers. The key figure of merit for infrared imager is the NETD (Noise Equivalent Temperature Difference). Very low NETD values with very high operability, has been achieved using uncooled bolometric infrared image sensors. It has been shown that automotive and machine vision applications require at least an 80 mK NETD value [2] [6] , but the improvement of bolometric sensors leads now to < 30 mK performance. It is critical that the ADC itself does not downgrade the imager performance. If we consider a perfectly noise-free ADC, the inherent converter quantification noise given by equation 1 sets the ADC noise floor.

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$$ADC_{noise} = \frac{V_{dyn}}{\sqrt{12} \cdot 2^n} \quad (1)$$

Where ADC_{noise} is the ADC quantification noise expressed in Volts, V_{dyn} is the input dynamic range in Volts and n is the ADC's number of bits. Therefore digital sensor $NETD_{digital}$ can be expressed as a function of analog core $NETD_{core}$, Responsivity *R* and ADC number of bits n as shown by equation 2:

$$NETD_{digital} = \sqrt{NETD_{core}^{\ 2} + \frac{V_{dyn}^{\ 2}}{12.2^{2n}.R^2}} \quad (2)$$

With a 350 µV RMS analog core noise, a 13 bits ADC will add quadratically 112 µV of noise. Assuming now a 50 mK bolometric technology, the use of such an ADC will lead to 52.5 mK digital focal plane array provided that the ADC internal gain is equal to 1. So we can accept a 5 % degradation of NETD while using an internal ADC.
But if consider the non ideality of the ADC, and notably the SNR result, we have to take into account the actual ENOB (Effective Number Of Bit) in the calculation. With a 13 bits pipeline architecture we showed [7] an ENOB=12.3 bits. With this value the degradation of the digital NETD is equal to 11%. Then we see the improvement of the performance of the bolometric sensors also requires the improvement of the ENOB of the ADC.

The second point for design tradeoff is the power consumption in conjunction with sensor floor plan, because the bolometer is a thermal sensor. Therefore its response in temperature as a function of time and incident power depends on focal plane temperature as follows:

$$C_{th} \frac{\partial(T - Tpf)}{\partial t} = -\frac{T - Tpf}{R_{th}} + Pir \quad (3)$$

Where T is the bolometer temperature, *Tpf* the focal plane temperature, *Cth* the bolometer thermal capacitance, *Rth* its thermal resistance to the substrate and *Pir* the incident infrared power received by each bolometer. The impact of the ADC consumption on focal plane temperature non-uniformity must be minimized.

The third important point concerns the location of the ADC in the readout circuit analog chain. Considering noise performance the ADC has to be as close as possible to the pixel, because the noise of analog chain is at the minimum. So the worse case is the monolithic ADC set on the analog video because its performance is degraded by the noise of the analog processing functions: sample and hold , multiplexer and video amplifier. Recently the noise of the actual microbolometer was the main contributor in the chain. But in the future we can assume the noise of readout circuit will become dominant. So the location of the ADC will be more sensitive for global performance.

The last point for the architecture choice is the impact of the ADC on the production yields. It is known in the silicon industry that the yield depends on the die area and therefore on the ADC layout part. CMOS process choice is also a key element when it comes to yield. On the other hand we know the readout circuit is not necessarily processed in a CMOS technology dedicated for ADC design, leading to a non-optimal compactness

2.2 Architecture choice

Now the basic ADC constraints are set, we will present in this section the different possible architectures for an image sensor ADC. Visible light image sensors have experienced various solutions for analog to digital conversion [8] [9]. In certain cases, a monolithic ADC has been designed but column-wise converters are also available on particular devices [9], even pixel level ADC can be found [8]. However due to the accuracy of the visible detector itself, those arrays require only 8 to 10 bits resolution for their ADC, so the area and power-consumption of the converter is smaller than in the infrared readout circuits.

Due to the impossibility to integrate a 13 or 14 bits ADC in the 25 µm infrared pixel pitch with a typical 0.5 µm CMOS process, we eliminated the pixel level ADC choice. Taking into account the yields of the silicon, this solution must be put aside for the moment because the area taken by the ADC in each pixel is widely dominant compared to the rest of the circuitry, even with a very high CMOS density process. Indeed high density layout together with high complexity analog-digital circuitry, exhibit a high failure probability during back-end process.

The first solution developed for ULIS readout circuits was a monolithic ADC with pipeline architecture [7]. In fact this solution is well suited for 160 x 120 to 320 x 240 bolometer arrays. We started with 13 bits resolution and an ENOB of 12.3 bits, then we increased the resolution up to 14 bits when the NETD of the bolometric sensors improved. Today this architecture has an ENOB of 13 bits, and allows a 5% only degradation with NETD = 50 mK as shown earlier in this paper.
If we watch the yield aspects the monolithic ADC is the best choice because the area of the layout is very small compared to the whole readout circuit as presented in table 1. About noise considerations we saw the readout circuit analog part participate less than the bolometer sensor today to the SNR degradation. So on this point the monolithic ADC remains a good choice too.
However for power consumption aspects the choice between monolithic or column-wise converters depends on the array size of the readout circuit. With respect to the target application, let's consider for instance the sensor features 320 x 240 bolometers arrays on a 25 µm pixel pitch. This ¼ TV format is effectively just on the limit of the design trade-off between power consumption and silicon yields. This array is to be read out at 60 frames per second.
To compare the two solutions, we developed a column ADC with original dual-ramp architecture. Comparison figures with our two other monolithic versions are gathered in table 1. Considering the column area dedicated to the ADC in a distributed conversion scheme, it is clear, based on the existing art that a monolithic device would outperform the column-wise version in the 320 x 240 case. In fact, the distributed ADCs are much more suited for very large arrays and/or very high-speed cameras, which benefit in terms of power-consumption from a highly parallel conversion scheme. For example the state of art in cooled infrared readout circuit, is 100 µW to 200 µW per ADC, depending on architecture, CMOS process and resolution [10] [11]. As we can see in figure 1 the power consumption, versus array size, increase less for column converter than for monolithic ADC. This strategy has been successfully demonstrated also in visible light imagers [9] as well as in cooled infrared photovoltaic detectors [10] [11] [12].

Various monolithic analog to digital converters have been demonstrated in imaging devices. Due to the 13 bits ENOB accuracy requirement for our application, the pipelined structure allows relatively high analog frequency with respect to 0.5 µm CMOS technology. Moreover, the accuracy can be achieved with proper capacitor matching. The monolithic architecture sample frequency is around 10 MHz limit with a low-cost 0.5 µm process. As a consequence one has to consider multiple instances of monolithic ADC for large array size: two for 640 x 480 and four for 1024 x 768.

Sensor Array Features	Parameters	Pipeline 13 bits	Pipeline 14 bits	Column 13 bits
320 x 240, 1 digital video output Frame : 60 Hz, Fsample : 7 MHz Pixel pitch : 25 µm	Total Area (mm^2)	1.44	1.8	22
	Power Consumption (mW)	95	110	64
640 x 480, 2 digital video outputs Frame : 50 Hz, Fsample : 8 MHz Pixel pitch : 25µm	Total Area (mm^2)	2.88	3.6	44
	Power Consumption (mW)	190	220	128
1024 x 768, 4 digital video outputs Frame : 50 Hz, Fsample : 10 MHz Pixel pitch : 17 µm	Total Area (mm^2)	5.76	7.2	70
	Power Consumption (mW)	380	440	204

Table 1: Surface and power consumption of column and monolithic ADCs

3 STRUCTURE BASED DESIGN

3.1 Monolithic ADC structure

The ADC structure is presented in figure 1. It consists of six differential stages. Stages 1 to 5 contain a 3 bits Flash ADC. The result of each conversion is fed to a DAC, and the residual difference between the signal and the DAC output is amplified by 4 and passed to the following stage. The last stage only has a 4 bits flash ADC, as there is no

meaningful residual to quantify. This structure is rather classical for a pipeline ADC [13] [14]. Here one bit per stage is used as stage offset compensation using digital correction [13].

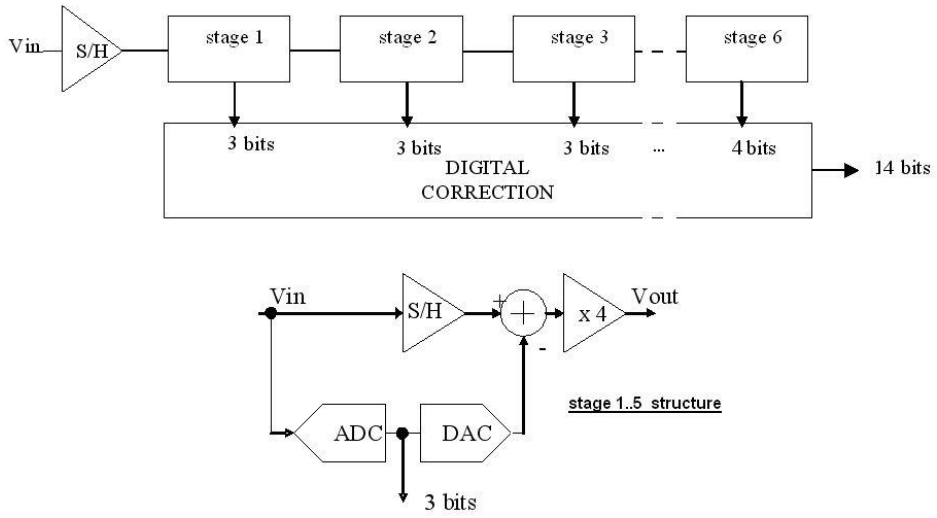

Figure 1: Pipeline ADC structure

The main difficulty for an accurate analog to digital conversion resides in the precision of the amplification by 4 of the residual between each stage. In our approach, the subtraction of the digitized value and the amplification of the remaining voltage are realized synchronously by the circuit presented on figure 2.

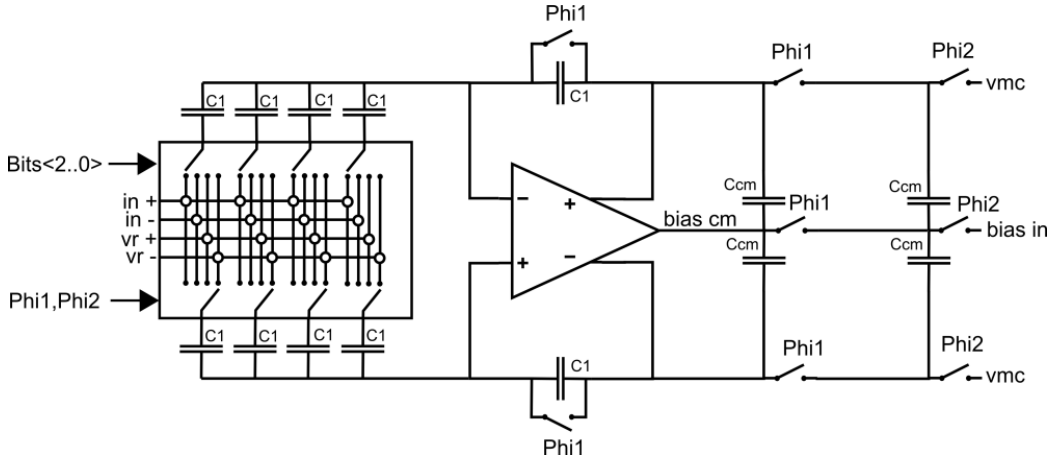

Figure 2: Detailed view of the DAC

As shown in figure 2, the common mode biasing is provided through the 4 Ccm capacitors bank that adapts gradually the common mode to the differential output excursion. During Phi1 Phase the proper values corresponding to the difference between the signal In+/In- and the digital stage output Bits<2.0> are stored on the capacitor bay at the input of the stage. Meanwhile, the feedback capacitors are maintained in reset while the common mode Bias is stored on Ccm capacitors. During Phi2, the residual is amplified by four and sampled by the next stage.
A pipeline ADC model was developed to help us to tweak our design based on a 0.5 µm technology [7]. We first estimated the dimension of the first two stages for a given ENOB. Then the last stages have been downsized using the model to lower the power consumption, without degrading the ADC key figures. The model shows that the last stage capacitor area can be reduced by 60%. Amplifiers can accommodate a gain loss of 20 dB. With this model the design was optimized to improve our initial 13 bits to a 14 bits resolution.

3.2 Column ADC structure

The column ADC structure is based on patented original dual-ramp architecture. The main difference with the classical dual-ramp is the amplification of the second ramp before conversion. The synoptic of the structure is given below in figure 3. We find the classical dual-ramp devices [15]: integrator, programmable current-discharge, comparator and counter. The single loop with the DAC in feedback plus variable gain G allows us to quantify and to amplify the residual value of the first ramp conversion result. So in the second step of conversion the signal holds the maximum of the dynamic range and it is converted with the same analog chain as the first step. The integrator output with the two conversion steps is given in figure 4. With this feedback system the signal to noise ratio is improved for the LSB values, obtained in the second conversion step. Indeed the noise and common mode perturbations are particularly sensitive drawbacks due to the high density and proximity of column ADC. So we avoid sophisticated systems to reach more than 12 bits ENOB, as auto-calibration devices [13] for example.

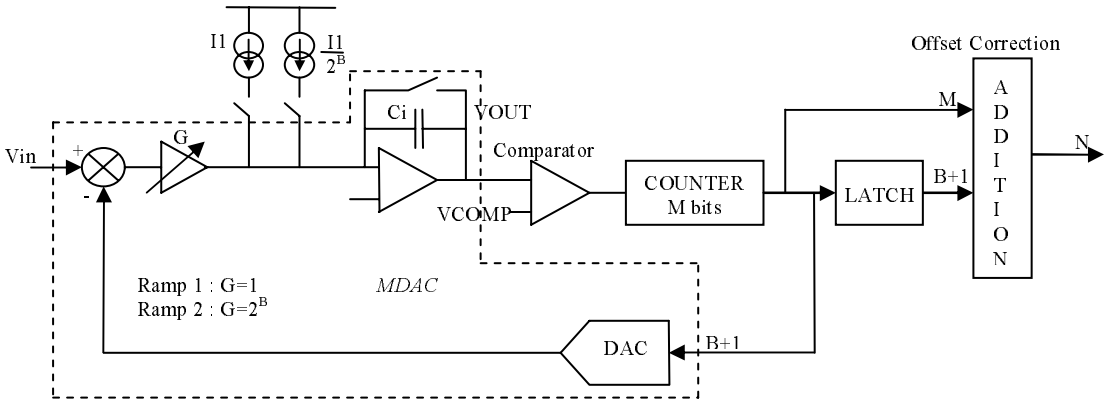

Figure 3: Column ADC structure

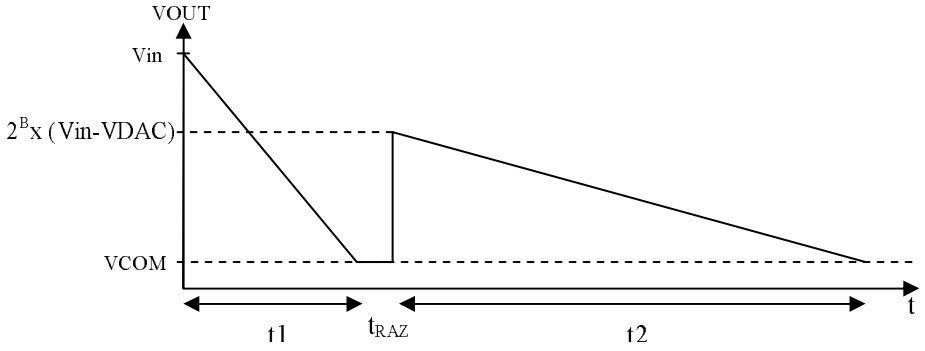

Figure 4: Integrator Output

4 TEST VEHICULE AND CHARACTERISATION

The monolithic 13 bits ADC has been integrated in the two ULIS standard products: 160 x 120 and 384 x 288. As we mentioned previously, this ADC has a 12.2 bits ENOB. This structure was enhanced up to 14 bits and integrated in a 160 x 120, 25 µm pixel pitch, focal plane array. Figure 5 shows the floorplan of the device.
The monolithic 14 bits ADC has been placed as far as possible from the bolometer array to avoid thermal influence through the substrate, as explained in chapter 2.1. Specific features of the test vehicle are presented in table 2. Table 3 shows a summary of the measured ADC characteristics. The device has been tested with the analog core and exhibits very good performances in imaging as shown in figure 6. There is no difference between digital and analog images although the scene dynamic is reduced. The ADC has also been packaged separately for characterization.

The ADC has been tested at 5 MHz sampling rate with an on-chip single-ended / differential converter at the input, which is the usual operating condition in the imager.

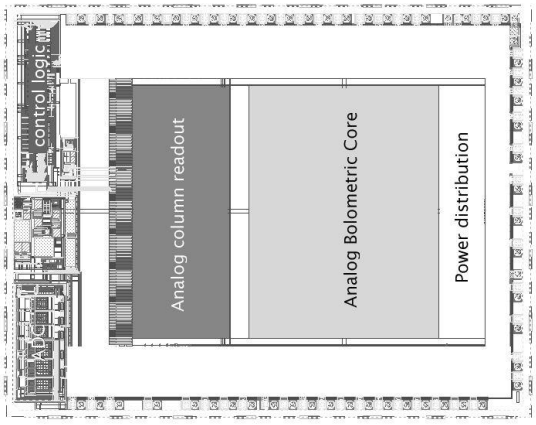

Figure 5: Test vehicle floor plan with monolithic 14 bits ADC specific location

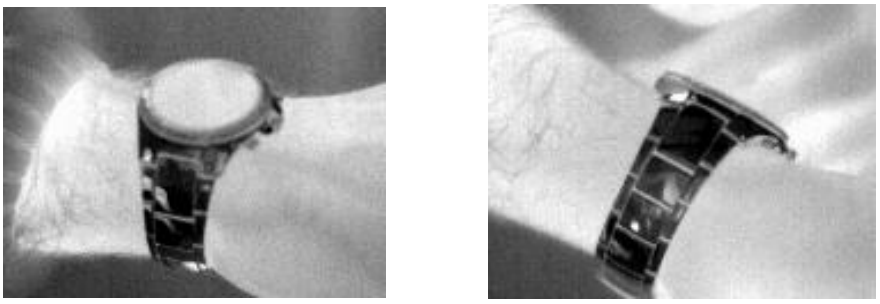

Figure 6: 160 x 120 infrared images with digital output (left) and analog output (right)

Image format	160 x 120
Pixel pitch	25 µm
NETD	50 mK/W (53 mK/W digital)
ADC	On-chip 14 bits pipeline
Digital sequencer	On-chip fully synchronous
Offset correction	On-chip skimming
User interface	2 wires serial programmable link 14 bits parallel out @ 10 MS/s max.

Table 2: test vehicle key features

Parameter	**Measured**
ENOB	12.9
SNR	79 dB
DNL	0.76
INL	4.9
THD	-72 dB
Power consumption @ 5Mhz	95 mW

Table 3: ADC measurements results

For column ADC we took the same test vehicle (160 x 120, 25 µm pixel pitch, focal plane array). We can see below in table 4, expected results for the column ADC.

Parameter	**Simulated**
ENOB	12.4 bits
SNR	76 dB
DNL	0.6 LSB
INL	6 LSB
THD	-70 dB
Power @ 5Mhz / ADC	200 µW

Table 4: 13 bits column ADC simulation results

5 CONCLUSION

In this paper, we demonstrated two ADC architectures dedicated to infrared focal plane array. We showed stand-alone converters are suitable for small to middle size arrays, while column-wise ADC are best suited for megapixel arrays. Started with 13 bits monolithic pipeline architecture in the ULIS standard products, this converter has been improved up to 14 bits to follow sensor NETD improvement up to 50 mK. In parallel a dual-ramp column ADC structure was developed to prepare the future for megapixel arrays.

REFERENCES

1. C. Trouilleau et al., "Uncooled amorphous silicon 160 x 120 IRFPA with 25-µm pixel-pitch for large volume applications", Infrared Technology and Applications XXXIII, Proceedings of SPIE Vol. 6542-60, 2007.
2. C. Vieider et al., "Low-cost far infrared bolometer camera for automotive use", Infrared Technology and Applications XXXIII, Proceedings of SPIE Vol. 6542-51, 2007.
3. M. Tchagaspanian et al., "Design of ADC in 25 \x{03BC}m pixels pitch dedicated for IRFPA image processing at LETI", Infrared Technology and Applications XXXIII, Proceedings of SPIE Vol. 6542-80, 2007.
4. B. Fieque, A. Crastes, JL. Tissot, JP. Chatard, S. Tinnes, "320 x 240 uncooled microbolometer 2D array for radiometric and process control applications", Proceeding of SPIE Vol. 5251, 2003
5. J. P. Knauth, "Method and apparatus for correction of microbolometer output", US Patent US2003/0146383
6. F. Niklaus et al., "Uncooled infrared bolometer arrays operating in a low to medium vacuum atmosphere: performance model and tradeoffs", Infrared Technology and Applications XXXIII, Proceedings of SPIE Vol. 6542-52, 2007.
7. B. Dupont, P. Robert et al., "Model based on-chip 13bits ADC design dedicated to uncooled infrared focal plane arrays", Infrared Technology and Applications XXXIV, Proceedings of SPIE Vol. 6941, 2008, this conference.
8. D. X. D. Yang, B. Fowler, A. El Gamal, "A Nyquist Rate Pixel Level ADC for CMOS Image Sensors", Proceedings of ISSCC, 1999
9. Y. Oike, M. Ikeda, K. Asada, " A CMOS Image Sensor for High-Speed Active Range Finding Using Column-Parallel Time-Domain ADC and Position Encoder", IEEE Transaction on Electron Devices, 2003
10. P. Fillon et al., "Digital output for high performances MCT staring arrays", Infrared Technology and Applications XXXII, Proceedings of SPIE Vol. 6206-30, 2006.
11. F. Guellec et al., "Sigma-delta column-wise A/D conversion for cooled ROIC", Infrared Technology and Applications XXXIII, Proceedings of SPIE Vol. 6542-121, 2007.
12. S. Elkind, A. Adin, I. Nevo, A.B. Marhasev, "Focal plane processor with digital video output for InSb Detectors", Infrared Technology and Applications XXVIII, Proceedings of SPIE Vol. 4820, 2003.
13. L. Lin, "Design Techniques for Parallel Pipelined ADC", Berkeley MS Thesis, 1996
14. P.C. Yu, HS Lee, "2.5V, 12b, 5 MSamples/s pipelined CMOS ADC", IEEE Journal of Solid-State Circuits, vol.31, pp 1854-1861, 1996
15. R. Van de Plasshe. « Integrated Analog-to-digital and digital-to-analog converters ». Kluwer Academic Publishers . 1994, p. 278-279.
16. H. Amemiya « Integrating Analog-to-digital converter with Digital Self-Calibration ». IEEE Transactions on Instrumentation and measurement, vo. 25, N°2, June 1976.