Journal of The Electrochemical Society, **157** (1) H13-H21 (2010)
0013-4651/2009/157(1)/H13/9/$28.00 © The Electrochemical Society

High Quality Ge Virtual Substrates on Si Wafers with Standard STI Patterning

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Further improving complementary metal oxide semiconductor performance beyond the 22 nm generation likely requires the use of high mobility channel materials, such as Ge for p-type metal oxide semiconductor (pMOS) and III/V for n-type metal oxide semiconductor devices. The complementary integration of both materials on Si substrates can be realized with selective epitaxial growth. We present two fabrication schemes for Ge virtual substrates using Si wafers with standard shallow trench isolation (STI). This reduces the fabrication cost of these virtual substrates as the complicated isolation scheme in blanket Ge can be omitted. The low topography enables integration of ultrathin high-k gate dielectrics. The fabrication schemes are also compatible with uniaxial stress techniques. Both modules include an annealing step at 850°C to reduce the threading dislocation densities down to 4×10^8 and 1×10^7 cm^{-2}, respectively. We are able to fabricate high quality Ge virtual substrates for pMOS devices as well as suitable starting surfaces for selective epitaxial III/V growth. The latter are illustrated by preliminary results of selective epitaxial InGaAs growth on virtual Ge substrates.
 [DOI: 10.1149/1.3244564]

Manuscript submitted August 3, 2009; revised manuscript received September 14, 2009. Published November 2, 2009. This was Paper 2386 presented at the Vienna, Austria, Meeting of the Society, October 4–9, 2009.

Downscaling of complementary metal oxide semiconductor (CMOS) devices beyond the 22 or 15 nm generation is expected to go together with the implementation of high mobility channel materials. Ge is being considered for pMOS devices, while III/V materials might be suitable for nMOS devices.[1,2] In both cases research is ongoing on both unstrained and strained layers (uniaxial and biaxial strains). A cost-effective implementation requires the fabrication of these materials on Si substrates and the compatibility with existing process modules like shallow trench isolation (STI) and state of the art fabrication modules for gate stacks. This sets limits on the fabrication schemes and material properties for the channel materials. For example, the material has to be proofed against a certain thermal budget during further processing steps. The cointegration of Ge with III/V materials as well as regular Si-based devices can be realized with selective epitaxial growth (SEG).[3-13] High quality Ge virtual substrates are grown by SEG. They are aimed for pMOS devices as well as acting as suitable starting surfaces for selective epitaxial III/V growth.[12]

A big obstacle for high quality Ge epitaxy on Si surfaces is the 4.2% lattice mismatch between the two materials. This results in two main challenges for Ge growth on Si. First, there is the possible high threading dislocation density (TDD) which might cause increased junction leakage and yield losses.[14] The second challenge is to obtain a smooth surface as Ge on Si growth normally occurs in the three-dimensional Stranski–Krastanow mode.[15,16] Several approaches have been used to reduce the TDDs in Ge epitaxial layers, such as graded SiGe buffer layers,[17,18] cyclic thermal anneal,[19,20] and threading dislocation (TD) trapping in submicrometer trenches (also known as necking effect).[3-5] Although these techniques are effective in reducing TDDs, each of them has drawbacks. Graded SiGe buffers require a few micrometers thick layers to reduce the TDD down to 1×10^7 cm^{-2}. This prevents its application in STI trenches because the STI depth is limited to a few hundred nanometers for the sake of scaling. Cyclic thermal anneal also reduces TDDs, but it only works for a layer of few micrometers. For thin Ge layers, cyclic anneal degrades the layer quality due to the fast intermixing at the Ge/Si interface.[21] The TD trapping by the oxide sidewalls in narrow trenches is compatible with advanced technologies because most of the TDs are trapped at the bottom part of a Ge layer when the aspect ratio, which is defined as the trench depth divided by the trench width, is greater than 2.[3,4] However, the TD trapping is only effective in submicrometer-size trenches but not in micrometer-size trenches. In real applications, both submicrometer and wider trenches may exist. Well behaving device performance and reliability requires a simultaneous reduction in the TDD in both wide and narrow trenches. A TDD below $<10^5$ cm^{-2} has been reported by Wistey et al. using a mixture of digermylmethane and digermane in a gas-source molecular beam epitaxy system.[22] Independent of the chosen fabrication scheme, surface roughness has to be optimized as it hinders Ge integration in metal-oxide-semiconductor flows because it directly affects the quality of the high-k gate/channel interface.[23]

In this work, we first give an overview of our recent work on the fabrication of Ge virtual substrates with low TDD.[8,11] This includes Ge SEG, followed by annealing at 850°C. The high temperature anneal allows an effective reduction in the TDD. Nonselective growth of Ge on the oxide mask, Ge facet formation, maintaining good material quality, surface roughening caused by three-dimensional growth, and high TDDs are important issues that are discussed in this paper. We compare two fabrication schemes to fabricate virtual Ge substrates. Both schemes have their own strengths and challenges. They both allow using standard Si STI wafers as a starting material. This enables a cost-effective implementation of these virtual substrates in regular CMOS process flows as the complicated STI fabrication in blanket Ge can be omitted. Our Ge on Si fabrication scheme provides high quality Ge virtual substrates for pMOS devices as well as suitable starting surfaces for III/V SEG, which are aimed to be used for nMOS devices. We present preliminary results for epitaxial III/V growth on Ge surfaces using Si STI wafers with 6° misalignment toward [110].

Fabrication Schemes of Virtual Ge Substrates on STI Patterned Wafers

Figure 1 shows the two fabrication schemes we studied to make virtual Ge substrates. Patterned Si(001) wafers with standard SiO_2 STI were used. The trench widths range from 0.15 to 10 μm. The depth of the STI trenches is 300 nm, and the active deposition area is about 58%. The wafers received an SC1 wet clean followed by an

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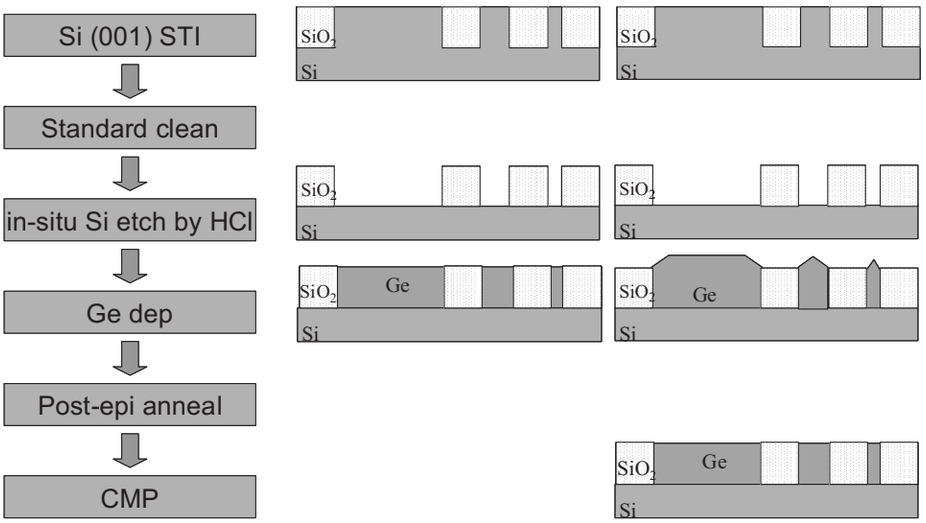

Figure 1. Fabrication schemes for Ge virtual substrates using Si wafers with standard STI. No CMP step is needed for the left scheme, where a facet-free Ge layer is grown and overgrowth above the oxide is prevented. In the other case, a much thicker layer is grown that results in a lower TDD but requires a CMP step after the post-epi anneal step.

HF dip to remove the native oxide on the active areas. Next, the wafers were loaded into our ASM Epsilon2000 epi-tool where they received an in situ pre-epi bake at 850°C. In the first scheme the pre-epi bake is followed by an ~300 nm Si recess of the STI wafers, using HCl vapor etching at 850°C,[24] immediately followed by SEG of a facet-free ~300 nm thick Ge epitaxial layer by chemical vapor deposition (CVD). The Ge deposition temperature was varied between 350 and 600°C, and the growth pressure was chosen to be either 80 Torr or atmospheric pressure. GeH_4 (1% in H_2) was used as a Ge precursor and either H_2 or N_2 was used as a carrier gas. The strength of this scheme is its simplicity as no further processing is required except for the post-epi thermal anneal for defect reduction. The postgrowth furnace anneal was done in N_2 ambient at 850°C for 3 min. The second scheme contains a combination of the above-mentioned epi step/thermal anneal and chemical mechanical polishing (CMP), as shown on the right side in Fig. 1. After the Si recess a much thicker Ge layer is grown, with some lateral overgrowth over the oxide. The quasi-equilibrium TDD of a given strain-relaxed Ge layer scales down with the inverse square of its thickness as discussed below. Growing a thicker layer therefore allows to reduce the TDD during the ex situ post-epi anneal. Except for the first ~50 nm above the Ge/Si interface, the TDD reduction occurs through the complete layer, as we discuss in this paper. After the anneal, Ge was polished back to the SiO_2 surface. CMP was done with a 200 mm polishing tool using a commercial Lam Teres belt polisher.

Ge Growth Challenges: Maintaining Selectivity, Material Quality, and Facet-Free Growth

The main challenges in selective epitaxial Ge growth on Si surfaces are loss of selectivity by polycrystalline Ge growth on the oxide mask, maintaining good material quality, Ge facet formation, surface roughening correlated with three-dimensional growth, loading effects, and high TDDs.[8] The growth temperature and the choice of the carrier gas have a major impact on the first three challenges. For the same GeH_4 partial pressure, using N_2 instead of H_2 as a carrier gas results in a significant increase in the low temperature growth rate (Fig. 2). In the lower temperature regime (below 450°C) the epitaxial growth is controlled by both surface kinetics and mass-transport effects. For H_2 as a carrier gas we obtained an activation energy of 1.47 eV, which is close to the expected value for hydrogen desorption from Ge surfaces (1.6 eV).[25] The linear correlation between growth rate and GeH_4 partial pressure (Fig. 2) indicates that the Ge growth is also influenced by mass-transport effects. Mass transport becomes even more dominant at higher temperatures, which is illustrated in Fig. 2 by the lower activation energy (lower slope of the curve). For N_2, an activation energy of ~0.9 eV has been extracted for the temperature regime of 350–400°C. This value is lower than the value obtained for H_2, showing that the mass transport is slightly more dominant. A much lower activation energy of 0.3 eV has been reported by Hartmann et al.[26] Their deposition process occurs in the mass-transport regime for the complete temperature regime they studied (400–725°C). This might be explained by the much lower growth pressure they use (20 Torr), as the same research team reports in Ref. 27 a much higher growth rate for Ge growth at 400°C and 100 Torr. In Fig. 2, the Ge growth rates as obtained for a GeH_4 partial pressure of 0.076 Torr and N_2 as a carrier gas are almost a prolongation of the Arrhenius curve as obtained for $p(GeH_4) = 0.30$ Torr in H_2. This illustrates the impact of the carrier gas on the Ge growth. Similar growth rates are obtained for both conditions despite the significant difference in GeH_4 partial pressures. However, the use of N_2 has a negative impact on the growth selectivity for growth temperatures of ≥375°C.[8] At 350°C, the Ge growth in N_2 is selective but for the Ge growth on Si surfaces, polycrystalline grains are identified by both X-ray diffraction (XRD) measurements and transmission electron microscopy (TEM).[8] The use of H_2 as a carrier gas allows SEG without Ge nuclei on the oxide at all temperatures studied in this work (400–600°C). However, depending on the GeH_4 flow, the facet formation occurs above a critical temperature, as discussed below. Again, a defective Ge layer is obtained for layers grown at low temperatures (≤400°C).

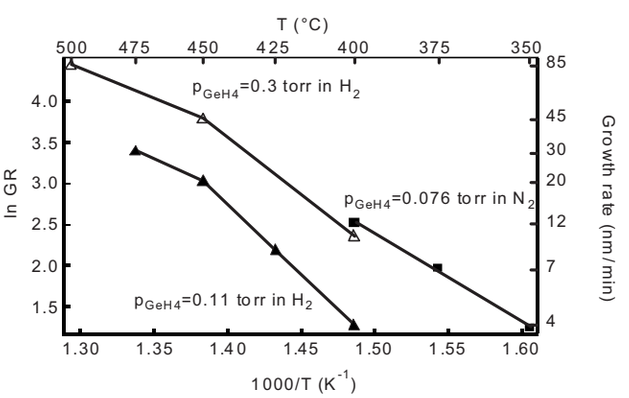

Figure 2. Arrhenius plot of the growth rate for Ge SEG at atmospheric pressure.

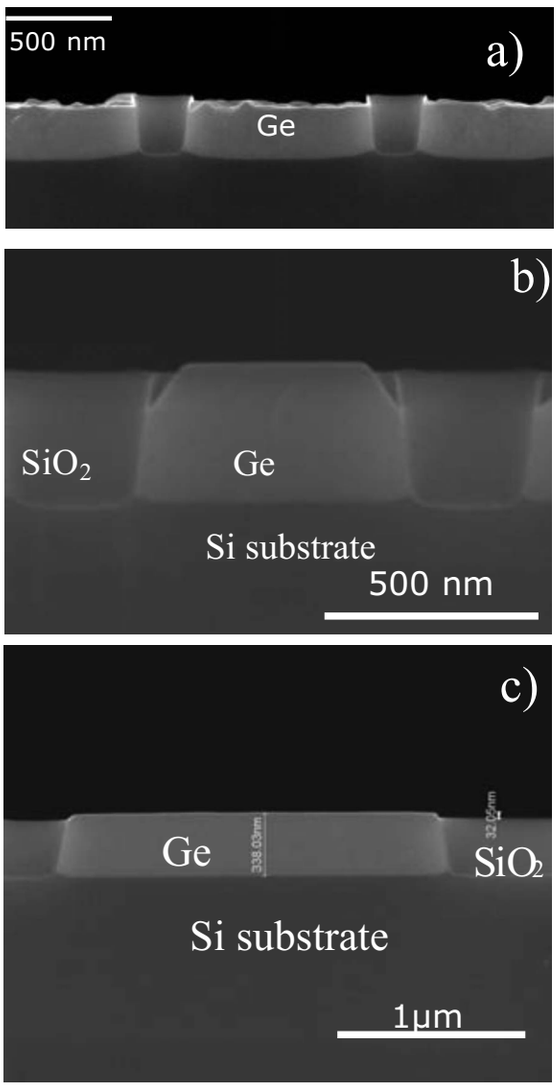

Figure 3. Impact of growth temperature and GeH_4 partial pressure on facet growth. All layers are grown with H_2 as a carrier gas and at atmospheric pressure. (a) 400°C, growth rate on the (001) surface: 4 nm/min; (b) 450°C, growth rate: 40 nm/min; and (c) 450°C, growth rate: 45 nm/min.

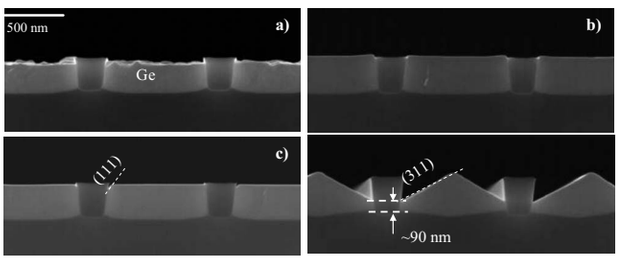

Figure 4. Impact of the growth temperature on facet growth as observed in 1 μm wide trenches. The Si recess, which precedes the Ge growth, was done at a pressure of 10 Torr. This results in a faceted starting surface for the Ge regrowth. All Ge layers are grown at atmospheric pressure with p_{GeH_4} = 0.15 Torr and with H_2 as a carrier gas. The growth temperatures are (a) 400, (b) 425, (c) 450, and (d) 500°C.

The facet formation is a well-known issue related to SEG. Facets are slower growing planes, which cause a thinning of the epitaxial layer near the pattern edge area. In our case, the facet formation needs to be avoided if the virtual substrates are fabricated following the first fabrication scheme, so without CMP (Fig. 1). In general, facet-free Ge growth requires low growth temperatures. But, it is also influenced by other growth parameters such as the total pressure during growth, the GeH_4 partial pressure, and the shape/slope (positive or negative) of the sidewalls of the open windows. The sloped mask geometry, with wider trenches at the top, leads to lateral overgrowth over the mask material. Consequently, {111} facets are generated, similar to the case of SEG of Si or SiGe.[28] Therefore, it is preferred to have a vertical side-wall geometry or a positive slope with narrower trench widths at the top (which is the case for our STI patterned wafers). For such an optimal side-wall geometry, the facet growth is primarily controlled by mass transport on the growing Ge surface. Recently, we reported a mass-transport model which enables to predict the facet formation.[8] In this model the mass transport on the facet plane consists of three components: (*i*) The mass flux from the masking oxide to the facet, (*ii*) the mass flux from the facet plane to the top (001) surface, and (*iii*) the mass flux from the gas phase to the facet. The net flux on the facet determines the Ge growth rate on the facet. The observed facet formation for different growth rates and different growth temperatures is shown in Fig. 3 and 4 and is well in line with the simulated predictions. With increasing growth temperature, the surface mobility of the adsorbed atoms increases. As a result, the ratio in growth rates $R^{(111)}/R^{(001)}$ and $R^{(311)}/R^{(001)}$ decreases. This explains the more pronounced faceting with increasing growth temperature. The same reasoning explains why the facet formation is less pronounced for higher GeH_4 partial pressures (Fig. 3). However, defects are observed in plan-view scanning electron microscopy (SEM) if the GeH_4 partial pressure (or equivalently the Ge growth rate) exceeds a critical value. This is the case for the growth conditions used for the samples of Fig. 3a and c and 4a. In general the facet formation is more pronounced if N_2 is used as a carrier gas. Again, replacement of the H_2 carrier gas by N_2 results in a higher surface mobility of the adsorbed atoms. For N_2, the facet-free Ge growth requires growth temperatures as low as 350°C.

In addition to the parameters listed above, the facet formation during Ge growth can also be influenced by the conditions as used for the preceding Si recess. Depending on the Si etch back conditions, the recessed Si surface can be faceted or flat, as shown in Fig. 5.[24] Si back-etching is done at 850°C, which gives an acceptable etching rate (9–14 nm/min). The reduced pressure reduces chemical loading effects. However, the process pressure during this in situ Si vapor etching affects the facet formation of the recessed surface. While no facets are observed at 40 Torr, {311} facets are observed if the etching is done at 10 Torr.[24] As soon as the Si recess reaches the bottom of the STI trench, lateral etching occurs and a {111} facet is generated. The pressure controlled facet formation of the recessed Si surface helps to suppress the facet formation during Ge regrowth. This becomes clear by comparing Fig. 3b with Fig. 4c. In both cases the Ge growth was done at 450°C using H_2 as a carrier gas. The facet formation is much less pronounced in Fig. 4c despite the lower GeH_4 partial pressure (0.15 Torr for Fig. 4c compared to 0.30 Torr for Fig. 3b). This is explained by the shape of the recessed Si surface, which contains {311} facets for the samples shown in Fig. 4. The Ge growth starts on a concaved shaped faceted Si surface, as shown in Fig. 5a. The faster growing (001) surface consumes the slower growing (311) surface. For a given Ge thickness, the facet is fully consumed and the Ge surface becomes flat. The Ge epi thickness for which flat surfaces are observed depends on (*i*) the facet width on the recessed Si surface, which in turn is given by the ratio of the different etching rates of the (001), (311), and eventually (111) surfaces and (*ii*) by the ratio of the Ge growth rates for the different surfaces. If the Ge growth proceeds further, the facet formation on the growing surface might occur, as discussed before and as shown in Fig. 4d.

The discussion of Fig. 3 and 4 illustrates how the facet formation

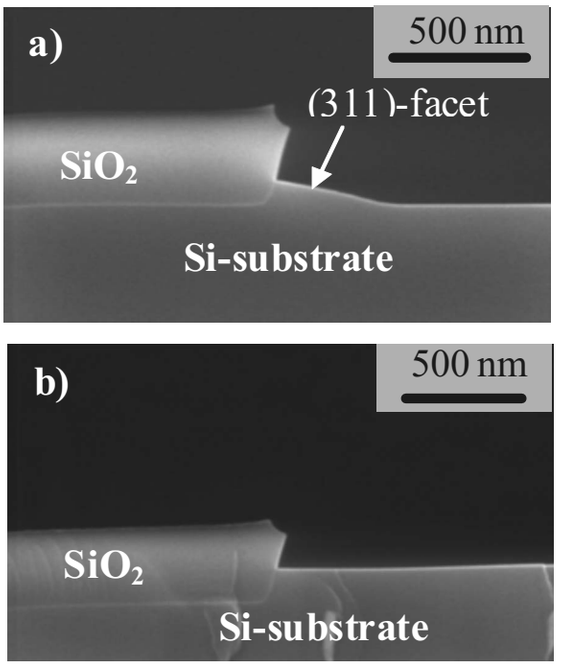

Figure 5. (a) In situ HCl etching at 10 Torr and 850°C leads to the formation of {311} facets. (b) No facet formation for HCl etching at 40 Torr and 850°C.

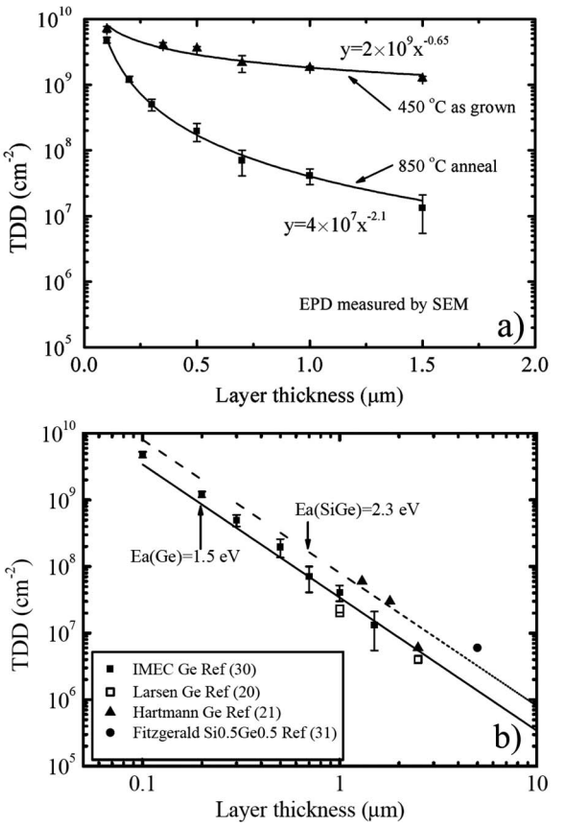

Figure 6. TDD dependence on film thickness for as-grown layers and after post-epi anneal. (a) Experimental TDDs as extracted by SEM analysis after etching in a diluted Schimmel solution by counting the etch pit density. (b) Comparison of experimental data with simulations. The solid and dashed lines are calculations for Ge and SiGe with activation energies for dislocation gliding of E_a = 1.5 and 2.3 eV, respectively.[30] Filled squares represent high temperature growth or single anneal and the open squares and filled triangles represent thermal cyclic anneal.

of the epitaxially grown Ge layer can be suppressed. However, the facet-free growth was only observed for relatively wide windows ($\geq$1 μm). For narrow windows, we always observed {111} facets. The dependency of the window size on the facet formation is still a research topic.

Reduction in TDD by Post-Epi Anneal

For SEG in wide trenches or on blanket wafers, the 4.2% lattice mismatch between Ge and Si results in a TDD that can be as high as (1–2) × 10^{10} cm^{-2} (Fig. 6a). A post-epi thermal anneal strongly reduces the TDD. After the anneal, a clear decrease in TDD with increasing Ge film thickness has been reported (Fig. 6a).[8,19-21,29,30] TD annihilation is facilitated by the increased TD glide speed with increasing temperature. This is a thermally activated process. The glide velocity follows an Arrhenius law with a given glide activation energy. When the annealing temperature is above 800°C, the TDDs do not decrease with temperature. This indicates that all unpinned TDs glide fast enough to react. Those TDs that do not glide are pinned by other dislocations or point defects.[29] Recently, we reported about a thermodynamics model of the TDD dependence on film thickness for the case that no physical blocking or trapping effect is involved.[30] In this model, the interaction energy between neighboring TDs is considered as the driving force for the dislocation migration in a strain-relaxed film. The separation between TDs in quasi-equilibrium determines the TDD. Our model gives a good prediction of the lowest obtainable TDD without the need for data fitting. The predicted equilibrium TDDs scales down inversely with thickness squared, and this was confirmed by experimental data (Fig. 6b). We also investigated the TD interaction and surface morphology changes initiated by the high temperature anneal.[11] After the anneal we observed a confined dislocation network (CDN) above the Ge/Si interface (Fig. 7). This CDN is the result of effective TD glide and reaction and is observed for both patterned and blanket Ge layers. The TD glide mechanism is schematically illustrated in Fig. 8. In strain-relaxed Ge epitaxial layers, a misfit dislocation network (MDN) is formed at the Ge/Si interface, and 60° TDs penetrate from the Ge/Si interface to the Ge surface. The 60° TDs have Burgers vector in ⟨110⟩ directions with ⟨110⟩/{111} glide systems. If two TDs in one glide plane are considered, as shown in Fig. 8a, they are either repulsive or attractive depending on the signs of their Burgers vectors. With repulsive force, they move away from each other until the interaction energy is smaller than the glide activation energy. This repulsive force drives them toward the TDs with opposite Burgers vectors and increases the annihilation probability. For attraction, they move toward each other and annihilate. For an illustration purpose, the latter case is considered in Fig. 8a. The two TDs glide freely on the top due to the traction-free surface. However, because both TDs are connected to the misfit dislocations (MDs) at the Ge/Si interface, they are repelled by the MDN. Based on theoretical considerations, it can be concluded that at a sufficiently high temperature, TD gliding is energetically favored if the Ge epi thicknesses exceed a value of 1.4 times the separation between TD (10 nm).[32] Based on TEM analysis we found that TD gliding occurs at a distance of ~50 nm above the Ge/Si interface (Fig. 7a). The average separation between the confined dislocations is 50–100 nm. This is significantly larger than the separation between MDs which are 10 nm away from each other.[26,33] A few cross nodes in the CDN were observed in Fig. 7b, which indicates the cross glide of TDs. The cross glide is driven by the enhanced TD interaction in a thick Ge layer. In contrast, for thin Ge layers on Si, such CDN was not observed.[33]

The CDN in the annealed thick Ge layer causes cross-hatch patterns during the high temperature anneal for Ge layers thicker than 1 μm.[11,34] Clear cross-hatch patterning was observed on atomic

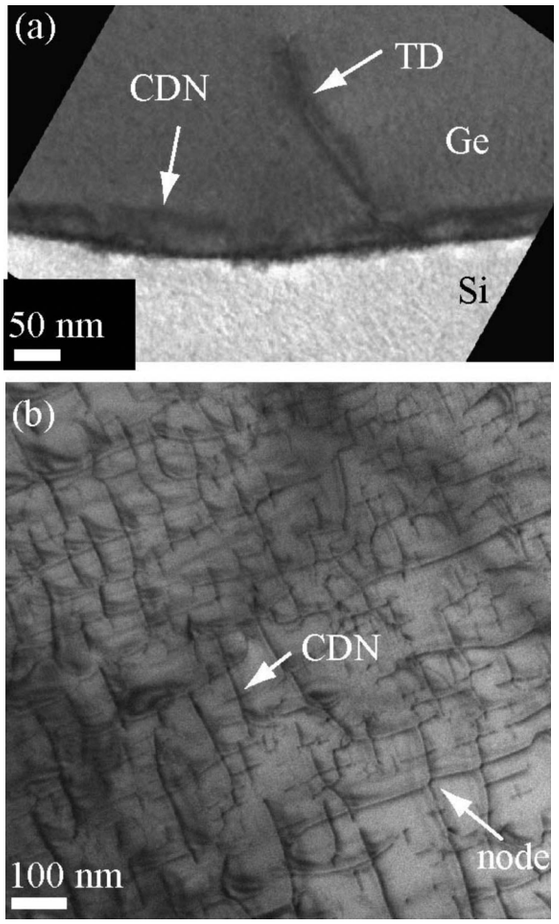

Figure 7. (a) Cross-sectional TEM image and (b) plan-view TEM image showing the confined dislocations at about 50 nm above the Ge/Si interface, in addition to the MDN at the interface with ~10 nm separation between two misfits. The epitaxial Ge layer received a 3 min anneal at 850°C. The separation between the dislocations is on the order of 100 nm. The cross node in (b) indicates a change in gliding planes.

force microscopy (AFM) images taken on 1.5 μm thick annealed Ge layers. On the as-grown layer no cross-hatch patterning was seen, although the as-grown layers are already fully relaxed. The root-mean-square (rms) roughness of the as-grown 1.5 μm thick Ge layer is 0.6 nm, excluding the possibility that a rough surface may obscure the cross-hatch patterns. In combination with the formation of the CDN (Fig. 7), it is believed that the Ge cross-hatch patterns

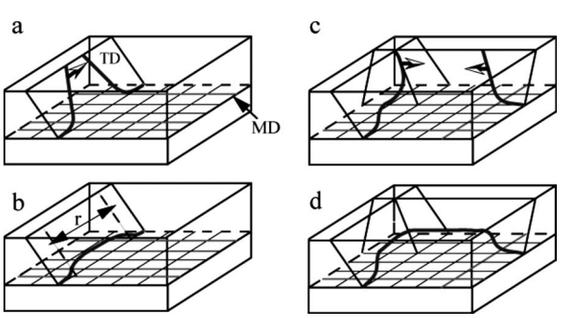

Figure 8. [(a) and (b)] Schematic of TD glide in one plane and [(c) and (d)] TD cross glide between two planes. After TD annihilation, a CDN is left above the MDN at the Ge/Si interface.

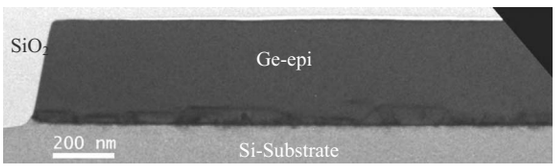

Figure 9. Cross-sectional TEM of a facet-free 320 nm thick Ge layer after the post-epi anneal.

after the anneal were caused by the strain field of the CDN. As mentioned before, the separation between the confined dislocations is much larger than the separation between the MDs. Consequently, the strain fields of the confined dislocations are also separated from each other and are distinct from the strain fields of the MDs. A simulation of the stress distribution on the Ge surface caused by a buried dislocation network shows an increased stress amplitude with increasing separation between two dislocations in the network.[11,32] This explains the observation that there is no cross-hatch pattern on the as-grown Ge surface where only the strain fields of MDs are present. During the anneal, the formation of the confined dislocations creates separated strain fields around each confined dislocation. The presence of the strain field causes Ge surface migration and forms cross-hatch patterns. Therefore, the formation of cross-hatch patterns on annealed Ge layers indicates a reduction in TDD. CMP enables a relatively easy removal of the cross-hatch patterns and a smooth surface is obtainable, as discussed in the next section.

SEG of Virtual Ge Substrates on STI Patterned Wafers

As mentioned before, we studied two different fabrication schemes for Ge virtual substrates (Fig. 1). An important difference between these schemes lies in the epitaxial Ge layer. The first scheme requires the epitaxial growth of ~300 nm thick facet-free Ge. The facet formation is no issue for the second scheme where a much thicker Ge layer is grown. The facet-free Ge growth can be obtained at 450°C if the GeH_4 partial pressure is sufficiently high. However, there is a risk for a nonperfect epitaxial deposition for such relatively thick epi layers. The degraded material quality above a critical thickness is correlated with the limited surface mobility of the adsorbed Ge atoms. For the first scheme, our process of record therefore contains a two-step approach for the Ge growth.[8] The Si recess is done at 10 Torr and results in a faceted Si surface (Fig. 5a). Next, a first 200 nm thick smooth and monocrystalline Ge layer is grown at 450°C, atmospheric pressure, a GeH_4 partial pressure of 0.30 Torr, and using H_2 as a carrier gas. These growth conditions result in a growth rate of ~40 nm/min (Fig. 2). The layer serves as a seed layer for the second growth step, where a 120 nm thick facet-free Ge layer is grown at a growth rate of ~3.5 nm/min at 350°C and atmospheric pressure using N_2 as a carrier gas. The presence of the underlying Ge seed layer enables smooth and monocrystalline growth despite the low growth temperature and in contrary to the case of direct Ge growth on Si (Fig. 3a and 4a). During the post-epi anneal at 850°C, the TDD reduces from $(1–2) \times 10^{10}$ down to $\sim 4 \times 10^8$ cm^{-2}, as extracted from plan-view and cross-sectional TEM (Fig. 9).[8] An rms surface roughness of ~1 nm has been measured by AFM for 10×10 μm large areas. The impact of the TDD on the relative contribution of various leakage components in short-channel Ge pMOS technologies has recently been studied.[14,35] The junctions show 5–10 times higher area leakage in comparison to similar junctions fabricated in thick Ge substrates with a lower TDD of 2×10^7 cm^{-2}. The presence of the STI leads to a factor of 10 lower perimeter leakage compared to a deposited oxide isolation. Leakage measurements at elevated temperatures reveal that the dominant generation mechanism is trap-assisted tunneling up to 1 V reverse bias both for the area- and perimeter-generated leakages.[14,35] Although the area leakage is 5–10 times higher than for thick Ge layers, it is not the most dominant leakage component. Ge pMOS with scalability down to gate lengths

of 70 nm require optimized halo implant conditions. This halo condition determines the extension leakage J_E, which is drain-to-bulk leakage generated under the transistor's spacer regions. J_E has a value of around 4×10^{-7} A/μm, and it is the dominant junction leakage component in a realistic transistor design.[14] It is band-to-band tunneling dominated up to 100°C. This indicates that J_E cannot be reduced by improving the substrate quality but rather by careful halo implant design and keeping supply voltage sufficiently low. Recently, we successfully demonstrated the integration of Ge pMOS technology with a standard STI module.[23] STI has a much lower topography than the previously used box isolation. This is a must to downscale the thickness of high-*k* gate dielectrics. The hole mobility of the fabricated devices is a factor of 2.4 higher as the Si universal mobility curve.[23]

Our second approach for making Ge virtual substrates in STI patterned Si wafers allows a simultaneous reduction in the TDD in both submicrometer and wider trenches.[11] Although the impact on the junction leakage is expected to be limited,[14] we do expect a beneficial impact on the device performance. For example, the yield values are directly affected by TDD, and above a critical TDD, the hole mobility might be influenced. After Si recess a much thicker Ge layer was grown. As the facet formation can be tolerated the growth temperature has been increased. The first 100 nm are grown at 450°C and atmospheric pressure to maintain a smooth surface. The remaining part of the Ge layer is grown at 600°C and reduced pressure (80 Torr). The higher temperature allows a higher throughput and likely an improved material quality as the number of point defects is probably lower. The growth pressure was reduced to 80 Torr to minimize loading effects and to avoid Ge coating on the reactor wall. Because of the facet formation, the total layer thickness varies as a function of window size. In the widest trenches the grown Ge layer reaches a thickness of 1.5 μm. In narrow windows, facets meet each other, and the (001) surface disappears after growing a certain thickness, which depends on the trench width. As a result, the Ge thickness reduces with decreasing window size. Despite the thinner layer, a lower TDD is found in the narrowest windows of the as-grown layer, thanks to the TD necking effect (aspect ratio trapping) at the STI walls. The thermal treatment results in a strong reduction in TDD for all window dimensions. Plan-view TEM images were taken at different vertical positions of the Ge layers. Besides the direct Si/Ge interface, a very uniform TDD was found through the whole Ge layer.[11] This is attributed to our short annealing time which sufficiently suppresses the intermixing at the Ge/Si interface. Together with cross-sectional TEM, we estimated the TDD to be around 1×10^7 cm^{-2} for wide windows (≥1 μm). For the narrowest trenches 150 nm wide and with an aspect ratio of 2 we did not find any TDs penetrating the topmost 150 nm (Fig. 10a). This indicates a TDD below 1×10^7 cm^{-2}. The estimated TDD as obtained for large windows is well in line with the data as observed for a 1.5 μm thick layer grown on blanket wafers (Fig. 6). The high temperature anneal is the dominant factor in TDD reduction, and the final TDD for a given Ge layer thickness is determined by the annealing conditions rather than the conditions during Ge growth.[11] Our approach allows a uniform TDD through the Ge layer, which is a main benefit compared to cyclic annealed layers. In the latter case, a higher TDD was found in the bottom region. In this region, which can be a few hundred nanometers thick, a strong Ge/Si intermixing occurs during the thermal cycling.[36] The uniform and low TDD demonstrates the feasibility of fabricating high quality virtual Ge substrates with a thickness of 250–300 nm. Because these layers are obtained for both wide and narrow (submicrometer) trenches, the fabrication approach is not mask-dependent and hence compatible with integrated circuit manufacturing for different applications. Figure 10b shows a cross-sectional SEM image of an epitaxial Ge layer after CMP. The resultant rms roughness after CMP is about 1.5 Å, which is significantly lower compared to the obtained roughness of the first fabrication scheme.

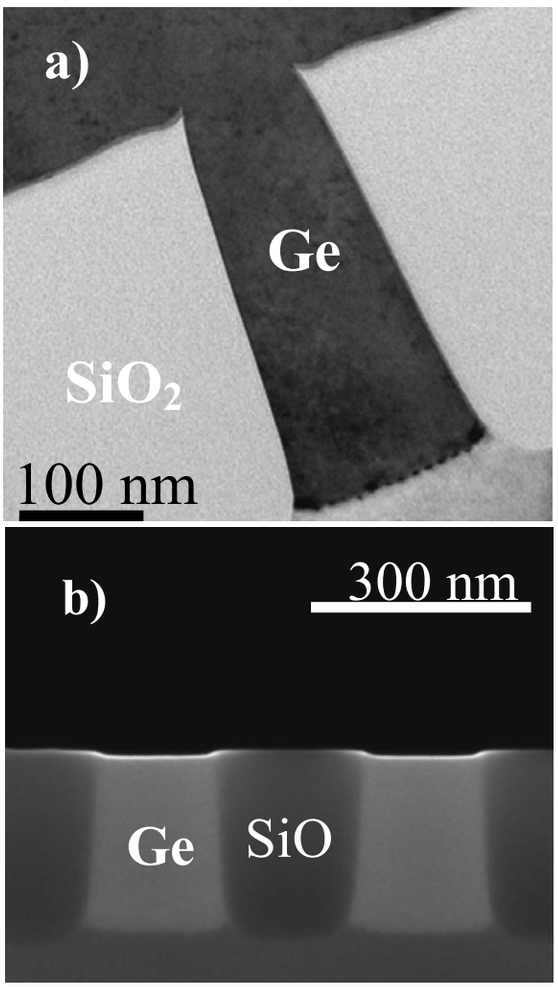

Figure 10. (a) Cross-sectional TEM of a ~1.5 μm thick epitaxial Ge layer grown on a recessed STI Si wafer and after thermal treatment. (b) cross-section SEM of epitaxial Ge after CMP. The roughness after CMP is about 1.5 Å, which is significantly lower compared to the obtained roughness of the first fabrication scheme.

Compatibility with Uniaxial Stress

We achieved promising pMOS device results using our Ge virtual substrates selectively grown on STI patterned wafers.[23] However, it has to be taken into account that a device material has to outperform uniaxially compressively strained Si pMOS devices rather than conventional unstrained Si pMOS. According to Antoniadis and Khakifirooz, short-channel Ge pMOSs require uniaxially strained Ge channels because the ballistic hole velocity of relaxed Ge does not offer a significant benefit over Si and is even lower compared to uniaxially strained Si. Considerably higher hole velocities are expected for uniaxially compressive strained Ge.[37] Similar to Si pMOS devices, uniaxially compressive strained Ge can be achieved by replacing the source/drain areas with a material with a larger lattice constant. For Ge channels the obvious choice is GeSn (Fig. 11).[38] To fabricate embedded GeSn, ion implantation followed by solid phase epitaxy has been suggested by Wang et al.,[38] but Ge recess by dry etching followed by GeSn regrowth using regular CVD can also be considered. In the latter case, challenging tasks are obtaining a high quality and contamination-free GeSn/Ge interface as well as avoid Sn precipitation as the required substitutional Sn content of at least 5% is far above the thermodynamics solubility limit (0.5%). Recently, the CVD growth of single-crystal $Ge_{1-y}Sn_y$ alloys with substitutional Sn concentrations above 10% has been

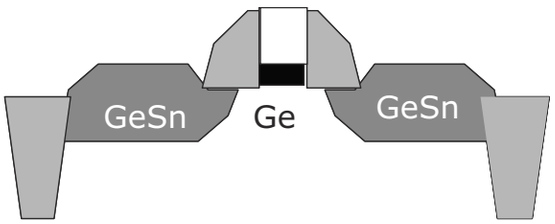

Figure 11. Schematic view of a Ge pMOS device with embedded GeSn to create a uniaxial compressive stress in the channel.

demonstrated.[39-41] So, it can be concluded that our fabrication schemes for Ge virtual substrates in STI are compatible with this uniaxial stress technique.

Selective Epitaxial III/V Growth on Ge Virtual Substrates

As mentioned above our Ge on Si fabrication scheme provides high quality Ge virtual substrates for pMOS devices as well as suitable starting surfaces for selective epitaxial III/V growth, which are aimed to be used for nMOS devices. In this section we briefly present preliminary results for epitaxial InGaAs growth on relaxed Ge surfaces. Si STI wafers with 6° misalignment have been used as a starting material to avoid issues with antiphase domains. The Ge growth was done following the first fabrication scheme, so without Ge overgrowth and without CMP. The purpose was to get a first impression about the selective III/V growth on Ge and to study the facet formation during STI trench filling (Fig. 12). Therefore, the Ge epitaxial thickness was limited to 75 nm, although the thin Ge thickness results in a TDD as high as $\sim 10^{10}$ cm^{-2}. The InGaAs growth was done in a metallorganic CVD tool from Thomas–Swan using tertiarybutylarsine (TBA), trimethylindium, and trimethylgallium as precursors.[12] No chemical treatment was done in between the Ge and the InGaAs growth. Before the III/V growth, the Ge surface received an in situ H_2 bake at 720°C. During this bake the native oxide is removed, and single atomic surface steps of the 6° misaligned (001) surface are merged into the more stable double surface steps.[42] SEG was done at 650°C using H_2 as a carrier gas. The details of our III/V SEG process development are described elsewhere.[12] A common practice is to first deposit a thin layer at 450 Torr followed by a second growth step at low pressure (30 Torr). This enables perfect selectivity, and it is a good compromise between reducing loading effects and inhibiting antiphase domains during the InGaAs growth.[12]

{111} facets are observed for both $In_{0.23}Ga_{0.77}As$ and $In_{0.49}Ga_{0.51}As$ growth in the STI trenches (Fig. 13 and 14). Due to the 6° misalignment, the facets are asymmetric. The overgrowth above the STI trenches followed by CMP is suggested to obtain a smooth InGaAs surface. On a blanket wafer a slight In surface segregation has been identified using energy dispersive X-ray measurements. On patterned wafers In segregation during growth does not occur. A uniform In content through the layer has been measured in the narrow trenches, except for the first 50 nm above the Ge surface. In this area In is depleted, which is correlated with the high TBA flow and the higher growth pressure during the initial stage of the growth. At this point we would like to mention that a slight increase

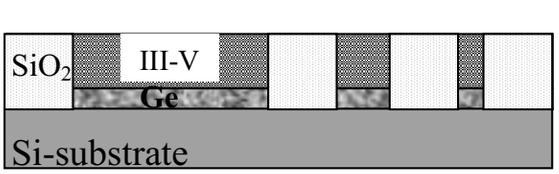

Figure 12. Schematic drawing of the epitaxial III/V layers grown on Ge virtual substrates. The thickness of the Ge layers is limited to 75 nm to enable SEG of the III/V within the STI trenches.

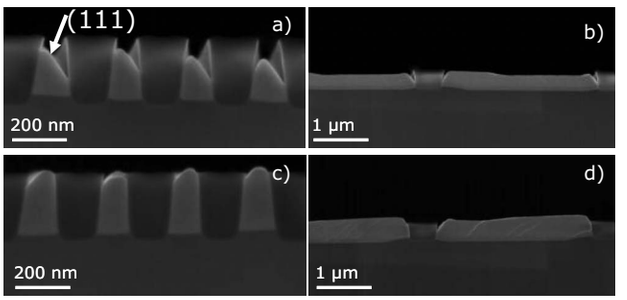

Figure 13. Facet formation as observed for $In_{0.23}Ga_{0.77}As$ growth on 75 nm relaxed Ge. [(a) and (b)] ~230 nm $In_{0.23}Ga_{0.77}As$. [(c) and (d)] ~400 nm $In_{0.23}Ga_{0.77}As$. The trench widths are [(a) and (c)] 150 nm and [(b) and (d)] 3 µm, respectively.

in layer roughness has been observed with increasing In content. The lattice mismatch between InGaAs and Ge is 1.6 and 3.4% for In concentrations of 23 and 49%, respectively. As a result, the InGaAs layer relaxes and for narrow windows, TDs are trapped at the STI sidewalls (Fig. 15a and b). This is very similar to the Ge on Si growth and has also been reported for GaAs growth on Si.[13,43] For 400 nm thick $In_{0.49}Ga_{0.51}As$, we measured a relaxation degree of 80% using XRD reciprocal space maps (Fig. 15d). A slightly lower relaxation of 70% has been measured for 400 nm thick $In_{0.23}Ga_{0.77}As$ (Fig. 15c). Grading the In content during layer growth has no major impact on relaxation. In addition to the (trapped) TD, we observed some unwanted twinning defects if TEM images are taken under the right conditions (Fig. 15a and b).

The presented InGaAs growth data are our first results, as mentioned in the beginning of this section. It illustrates the suitability of SEG for cointegration of Ge and III/V materials with regular Si. However, more process development is required to improve the material quality, especially the III/V layers.

Conclusions

Two modules to fabricate Ge virtual substrates on STI patterned wafers have been discussed. Starting from standard Si STI wafers, the Si active area is 300 nm recessed by in situ vapor etching. This is followed by Ge SEG and a simple ex situ thermal anneal. Growing a thick Ge layer above the STI-oxide surfaces enables to reduce

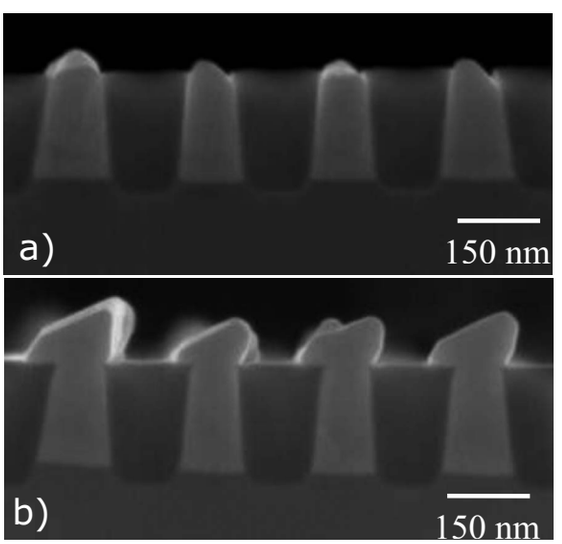

Figure 14. Facet formation as observed for $In_{0.49}Ga_{0.51}As$ growth on 75 nm relaxed Ge. The layers are (a) 360 and (b) 490 nm thick.

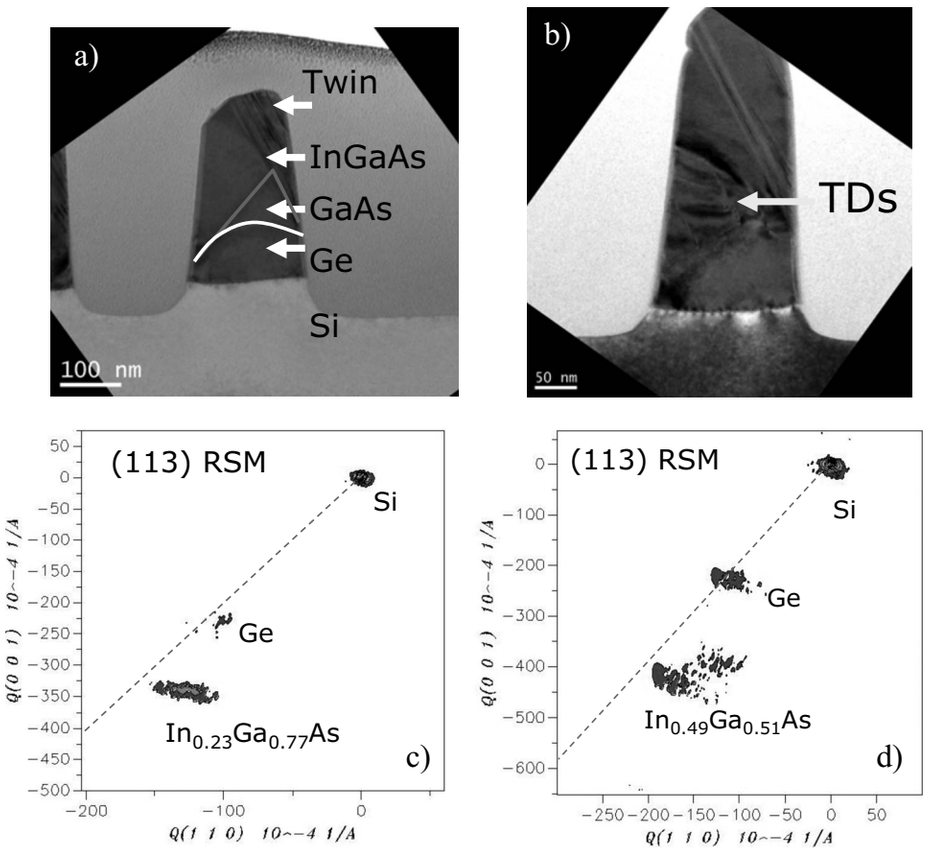

Figure 15. Cross-sectional TEM (a) for an $In_{0.23}Ga_{0.77}As$ layer and (b) an $In_{0.49}Ga_{0.51}As$ layer grown by SEG on top of a Si STI wafer with 75 nm relaxed Ge in between the Si substrate and the InGaAs layer. [(c) and (d)] XRD-RSM plots as measured for 400 nm thick. (c) $In_{0.23}Ga_{0.77}As$ and (d) $In_{0.49}Ga_{0.51}As$ selectively grown on relaxed Ge. The dashed lines in (c) and (d) are the full relaxation lines. Ge is fully relaxed despite the low thickness. The degree of relaxation as measured for the $In_{0.23}Ga_{0.77}As$ and $In_{0.49}Ga_{0.51}As$ layers is 70 and 80%, respectively.

TDD down to 1×10^7 cm^{-2}. In this module, CMP is used to polish the Ge back to the SiO_2 surface. This results in high quality virtual substrates with an rms surface roughness as low as 1.5 Å, as measured for 10×10 μm large areas. In the other fabrication scheme a much thinner Ge layer is grown. In this case, no CMP is needed but it requires facet-free Ge growth and therefore a careful choice of growth conditions. In this case, the TDD is higher (4×10^8 cm^{-2}) but still low enough in terms of junction leakage. Despite the higher surface roughness (rms of ~1 nm), successful integration of Ge pMOS technology with a standard STI module has been demonstrated, as reported in Ref. 23. The hole mobility of the fabricated Ge pMOS devices lies a factor of 2.4 above the Si universal mobility curve. From the device point of view, these fabrication schemes have several advantages: (*i*) High quality isolation at low cost, (*ii*) a cointegration of Si, Ge, and eventually III/V based devices, and (*iii*) low surface topography allowing integration of ultrathin high-*k* gate dielectrics. Finally, we presented first results of InGaAs SEG on thin (75 nm) Ge virtual substrates on STI patterned wafers. This illustrates the suitability of SEG for cointegration Ge and III/V materials.

Acknowledgments

We are indebted to the European Commission for financial support in the frame of the DualLogic project no. 214579. Further, we thank the IMEC core partners for financial support within the frame of IMEC's Industrial Affiliation Program on Ge-III/V. We appreciate the help from Dr. Chih-Mou Huang (from TSMC) who performed a part of the TEM analysis.

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