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# Side Wall Wet Etching Improves the Efficiency of Gallium Nitride Light Emitting Diodes

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This paper describes a method for introducing side wall etching (SWE) into the process flow for the fabrication of light emitting diodes. We investigated the effect of the deposition conditions for the $SiO_2$ protection layer on the surface damage of devices during the wet etching process and, thereby, the electrical characteristics of the device performance. More importantly, we found that recording X-ray diffraction spectra prior to SWE processing allowed us to categorize the quality of the GaN epiwafers [in terms of the full width at half maximum of the signal for the (102) facet], thereby allowing optimization of the etching time to avoid both over- and under-etching and potentially increasing the production yield and the reliability of the device performance. From a comparison of the electrical and photonic characteristics of devices prepared with and without SWE processing, we found that the former exhibited superior performance, with no degradation of the electrostatic tolerance or reliability, relative to the latter.
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To fulfill the potential of using solid state devices to replace current general lighting, there is a need for low-cost, high-yield technologies for the industrial mass production of light emitting devices exhibiting high luminescence efficiencies. The luminescence efficiency of a light emitting diode (LED) is defined primarily by three loss factors: the absorption loss of the LED itself; the Fresnel loss, which depends on the relative refractive index of the two adjacent materials; and the total reflection loss. The absorption loss originates from the absorption factor of the materials in the light output path, such as the active region and the cladding layers. The Fresnel loss is related to the efficiency of light emission from the active region, where the carriers undergo radiative recombination; it depends on the difference in refractive index between the active region and its cladding layer, both of which are related to the material properties of the LED and its structural configuration. Therefore, methods for reducing Fresnel loss are limited; as a result, the most feasible approach for improving the light extraction efficiency (LEE) of an LED is to minimize the total reflection loss.

To alter the critical angle of total reflection, the most logical method is to change the device's features. A conventional LED chip has a rectangular shape; because the difference in refractive index between semiconductors and the atmosphere is relatively large, the critical angle of total reflection is very small. For example, the critical angle of a GaAs device is limited to $\pm 16^\circ$; for nitride-based devices, it is $\pm 23.5^\circ$. Moreover, the parallel facets of standard rectangular devices result in a majority of photons being reabsorbed in the device, due to total reflection.

Most of today's commercial LED devices exhibiting high luminance possess altered device features to improve their LEEs. In conjunction with optimization of device features, methods such as side wall etching (SWE) have become critical for improving the performance of LEDs. Multiple etching sequences are very common in the industrial production of LEDs, with wet etching methods adopted widely. Because its low cost and simplicity make it suitable for mass production, manufacturing technologies using patterned sapphire substrates (PSSs) have also gradually shifted away from dry etching toward wet etching, thereby avoiding damage to the substrate surface upon bombardment with high-speed ions during dry etching processes.[1]

The wet etching methods involved in the manufacture of LEDs are typically followed by plasma etching to remove the exposed area. This process sequence would, however, impose a high risk of plasma damage to the active region, degrading not only the emission efficiency of the devices but also their performance reliability. In this study, we employed a process flow adopting plasma etching prior to wet etching. With this sequence, the area exposed to the plasma impact is minimized, thereby minimizing the risk of encountering reliability problems. The luminance of devices prepared with our SWE process was significantly greater than that of the corresponding devices prepared without SWE processing; more importantly, we did not observe any degradation of the electrostatic damage (ESD) tolerance or reliability for the device prepared with SWE processing. Herein, we also discuss the possibility of introducing SWE processing into the process flow for the mass production of LEDs with high production yield. In particular, we propose that, by measuring the full width at half maximum (fwhm) of the signal in the X-ray diffraction (XRD) spectrum of the (102) facet of GaN LED structures, device chips grown in the same batch can be categorized to determine the optimal etching time. Such an approach should vastly improve the production yield and the repeatability of device performance, because the adverse effects arising from fluctuations in crystalline quality during the epitaxial process would be mitigated.

## Experimental

GaN LEDs were grown, using a metallorganic chemical vapor deposition (MOCVD) system, on a PSS, with the structure comprising 2-μm undoped GaN, 2.5-μm Si-doped n-GaN, eight pairs of InGaN/GaN multiple quantum wells (MQWs) as the emission layer (overall thickness of each pair: 11 nm), capped with 0.8-μm p-GaN. The surface of the epi-structure featured a micro-pits structure with a depth of approximately 0.2–0.5 μm to decrease the effect of the surface total reflection. The LED chip size in this study was $10\times18$ mil ($250\times450$ $\mu m^2$); the width of the metal electrode was 70 μm.

The side wall wet etching method was adopted to alter the shapes of the side walls of the LEDs. Fig. 1 illustrates the full process flow, which is described as follows. The laser scribing streets were approximately 6 μm wide and 26 μm deep.

(1) Plasma-enhanced chemical deposition (PECVD) was used to grow a protection layer of 1.4-μm $SiO_2$ that defined the removal region. Inductively coupled plasma (ICP) was then employed to etch off part of the p-GaN and the action region to reveal the n-GaN mesa. The $SiO_2$ layer was then removed using a buffered oxide etch solution (40% $NH_4F$:49% HF, 6:1).
(2) A 2-μm-thick layer of $SiO_2$ was deposited to protect the epilayer surface during etching.
(3) The sample featuring the $SiO_2$ protection layer was scribed with a laser through the front side to define the chip size and reveal the side walls of the chips.

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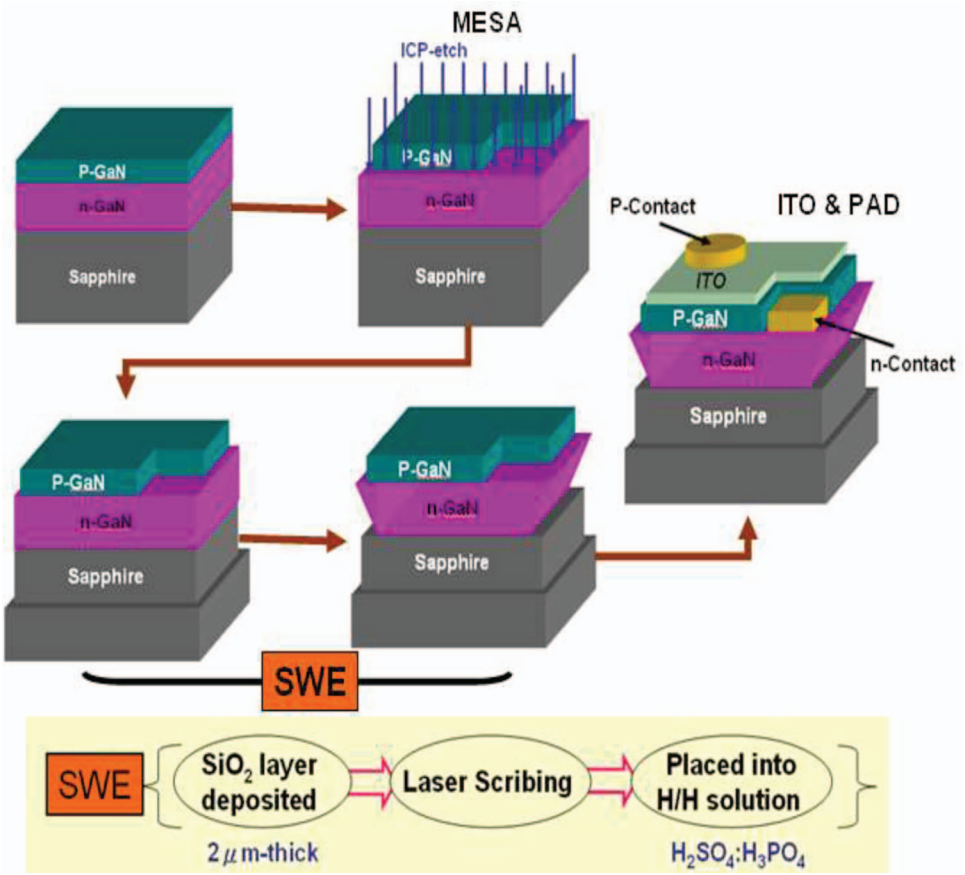



**Figure 1.** Full process flow for the fabrication of LEDs using the side wall wet etch method.

(4) SWE was performed by dipping the chips into heated (260 °C) $H_2SO_4$ and $H_3PO_4$ for etching times of 10 and 18 min, respectively.
(5) Indium tin oxide (ITO) was deposited as the metal electrode.
(6) Chip-on-wafer (COW) probing was employed to measure the electrical and photonic characteristics, followed by lapping and cleaving processes.
(7) The chips were placed into the To-can package for integral sphere measurement.

## Results and Discussion

As it is well known, the incomplete covering of the $SiO_2$ protection layer during wet etching will damage the pitted surface of p-contact epilayer and resulted in higher serial resistances for our devices—in turn, increasing the forward bias of the chips. We have also noticed that with our slight alteration of the convention processing flow with the (H/H) etching after the laser scribing, that would provide another advantage, that is in the previous process flow, there would be some melting residue from the laser scribbling, those residue could act as the detrimental absorption area, but with our alteration, those residue would be etched off and would not induced any adversary effect on the device performance.

Radouane et al.[2] reported that decreasing the $N_2O/SiH_4$ flow ratio can improve the density, grain size, and refractive index of $SiO_2$ deposits; therefore, to ensure that the $SiO_2$ protection layer could indeed resist the wet etching process, we deposited 2-μm-thick $SiO_2$ layers on the p-GaN cap layer at $N_2O/SiH_4$ flow ratios of 50 and 15 and used SEM to compare the resulting surface features.

The $SiO_2$ grain size (diameter) in the SEM image of the sample surface deposited at a $N_2O/SiH_4$ flow ratio of 50 [Fig. 2a] was approximately 2–2.5 μm, considerably larger than that obtained at a $N_2O/SiH_4$ flow ratio of 15 [Fig. 2b; diameter: 1–1.5 μm), with no apparent gaps between grains. In addition, from the easement of the elliptical sphere, the refractive index of the $SiO_2$ deposits increased from 1.44 to 1.51 upon decreasing the $N_2O/SiH_4$ flow ratio from 50 to 15.

Figs. 3a and 3b display SEM images of the GaN LED obtained after laser scribing and after SWE, respectively. The $SiO_2$ protection layer near the periphery of the laser-scribed streets had become translucent, with the width of the translucent part being quite uniform. Fig. 3d presents the relative position of the sample after wet etching. In this image, the S mark indicates the residue of the $SiO_2$ protection layer; clearly, this layer was not removed during the high-temperature etching process. Apparently, the $SiO_2$ protection layer was more effective after adjusting the deposition parameters; furthermore, the translucent parts of the $SiO_2$ protection layer represented areas in which GaN had been etched off beneath the protection layer. Therefore, this approach allows the etching width to be estimated prior to removal of the $SiO_2$ protection layer, thereby facilitating quality control during the manufacturing process to determine whether a sample is over-etched or whether additional make-up etching is required. In contrast, Fig. 3c reveals that the peripheral areas of the LED chips could display irregular features after SWE processing; in addition, the scribing street was also expanded slightly. Furthermore, in Fig. 4d we observe that over-etching of the interface between GaN and PSS caused corner cracking during the flip chip process used to form the metal electrode, potentially seriously affecting the yield of LED chips. Together with the large increase in the ratio of the forward bias to the leakage

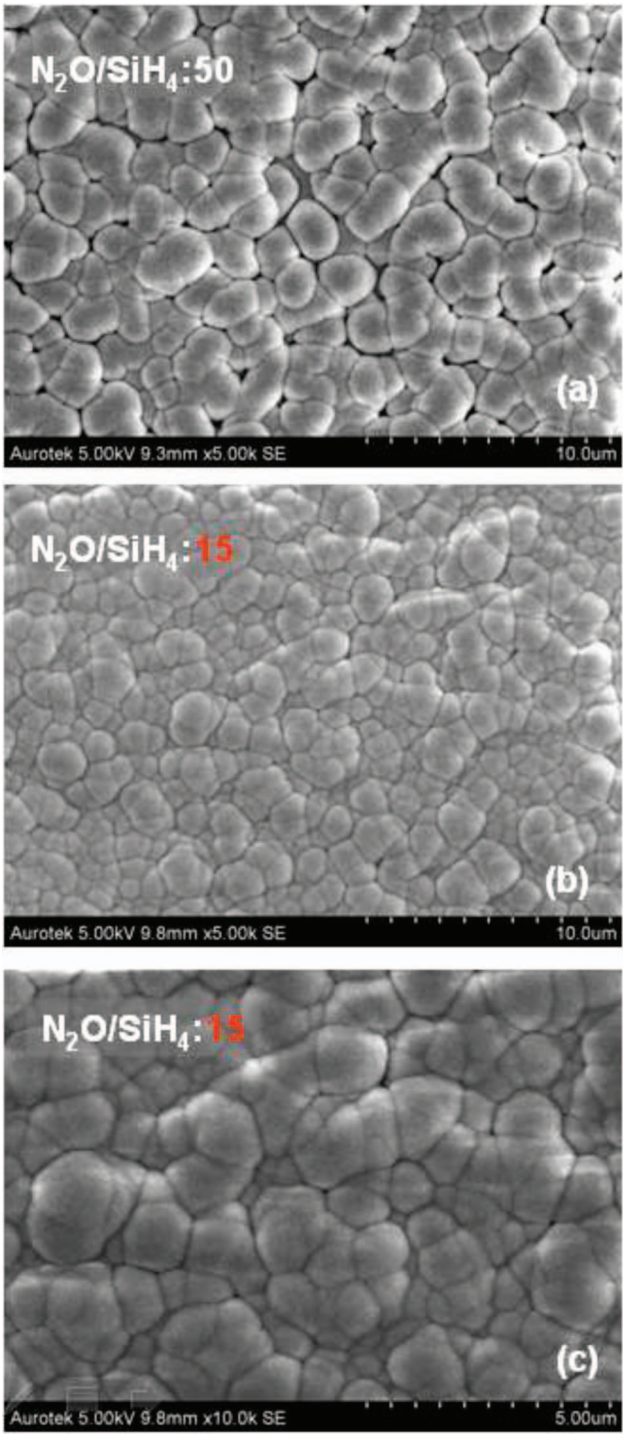



**Figure 2.** SEM images of surfaces obtained at $N_2O/SiH_4$ flow ratios of (a) 50 (5000x), (b) 15 (5000x), and (c) 15 (10,000x).

current, over-etching during the wet etching process would have a major negative impact on the production process.

Weyher et al.[3,4] reported that the conditions used for etching GaN are affected by the material properties, defect density, and the polarity of the etching protection layer; moreover, the etching rate would be a function of the defect density. Youtsey et al.[5] concluded that the density of defects and the dislocation of the etch protection layer determined the resistance of the etch protection layer against etching, with a higher density of dislocations indicating poorer crystallization of the material and, therefore, a higher etching rate. Thus, controlling the density of defects and dislocation should lead to stable and uniform etching during the side wall wet etching process.

XRD analysis is an efficient and precise method for characterizing the quality of GaN materials. In this study, because we grew GaN epilayers on c-axis (0002) $Al_2O_3$ PSS, we used the rocking curve of XRD to scan the (102) facet of the sample; this method is a common one for evaluating material quality and defect density.[6,7] In particular, we used a Bruker D8 high-resolution XRD analyzer for full-angle rocking curve scanning on the full structures of the (102) facets of GaN LED structures grown for different lengths of time; we also estimated the fwhm of the rocking curves. For this characterization, we set the reference etching width at 12 μm (as determined from the translucent area of the unetched $SiO_2$ protection layer). Fig. 5 displays the estimated relative etching times for a 12-μm etching width. The required etching time of each sample was inversely proportional to its fwhm; for example, when the fwhm of the (102) facet increased from 360 to 460 arcsec, the required etching time decreased from 16 to 5 min. A linear relationship between the fwhm and the etching time is not unexpected, because a wider fwhm signifies a poorer material quality with higher densities of defects and dislocations. Therefore, mass production will require the quality of the epilayers to be categorized so that different etching times can be adopted to prevent the wet etching process from over- or under-etching the same batch.

For further confirmation, we etched four epiwafers with various (102) FWHMs (353, 370, 402, and 436 arcsec) in H/H solution for 9 min. The etching profiles, examined with SEM and OM revealed (Fig. 6) that the etching width increased upon increasing the (102) fwhm. Furthermore, for a constant etching time, the sample having an fwhm of 353 arcsec underwent only slight side etching, whereas that having an fwhm of 436 arcsec underwent over-etching. Therefore, prior to wet etching, the (102) fwhm of the epiwafers is a reference value for categorization of the batch production. In addition, Fig. 6g reveals that the inclination angle in the etching was approximately 55°. Because the GaN epilayers were grown on the c-axis (0001) $Al_2O_3$ substrates, they would form {10-1-1} hexagonal structures; therefore, the etching profile would be along the ⟨1–100⟩ crystal orientation, which has a inclination angle of approximately 58°; this result is consistent with previous reports.[8,9]

Fig. 7a displays the electrical luminescence (EL) data from two LEDs, one that had been prepared with the SWE process (SWE LED) and one that had been prepared without (standard LED), at an injection current of 20 mA. Because the epilayers were grown in the same batch, both samples exhibited the same peak wavelength and fwhm in the emission spectrum. The values of the luminance of the SWE LED and the standard LED were 18.02 and 16.17 mW, respectively; thus, the SWE processing of the LED increased its luminance by approximately 11.4%. Fig. 7b presents the luminescence intensities (LIs) of the two samples at injection currents varying from 0 to 100 mA; the LI of sample prepared with SWE was always higher than that prepared without SWE, with the difference becoming more pronounced at higher injection currents.

Fig. 8 displays the emission patterns of both samples at an injection current of 20 mA; the peripheral regions of the laser scribing streets of the SWE LED chip had a brighter emission area than those of the standard LED, possibly indicating that the etched oblique facets had effectively altered the total reflection angle of the LED, thereby increasing the reflection or light scattering ratio of the side and front emissions of the active region. This phenomenon is consistent with the EL spectral data.

Figs. 9a and 9b present the current–voltage (*I*–*V*) curves of the SWE and the standard LED at a forward (from 0 to 4 V) and reverse (0 to −25 V) bias, respectively. The forward voltage of the SWE and the standard LED at 20 mA were 3.3 and 3.1 V, respectively; we attribute the greater forward voltage in the SWE LED to two factors. (i) Although we had improved the deposition parameters for the $SiO_2$ protection layer, the epiwafer sample featured a pitted surface

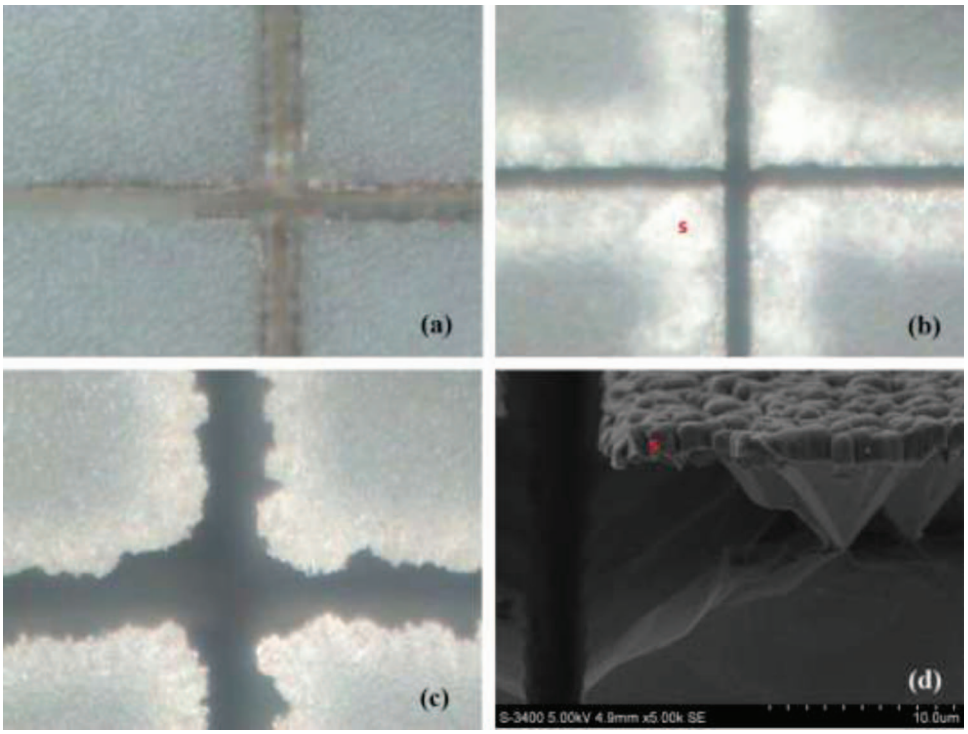



**Figure 3.** (a, b) SEM images of the LEDs samples obtained after (a) laser scribing and (b) SWE. (c) OM image of the LEDs samples after removal of the $SiO_2$ protection layer. (d) Side-view SEM image of the LEDs samples after wet etching.

that could still induce incomplete or partially non-uniform surface covering, leading to surface damage of the epiwafer during the wet etching process. (ii) Because our samples were grown on PSS with a conical surface having a diameter of 2 μm and a height of 1.2 μm, during the growth of undoped GaN buffer, voids could form at the interface between the epilayer and the conical surface;[10,11] it is possible that the etching solution could flow through these voids and etch inward, resulting in the greater forward voltage of the SWE LED.

In Fig. 9b, the leakage currents of the SWE LED and the standard LED at a reverse bias of –25 V were $9.8 \times 10^{-7}$ and $4.2 \times 10^{-6}$ A,

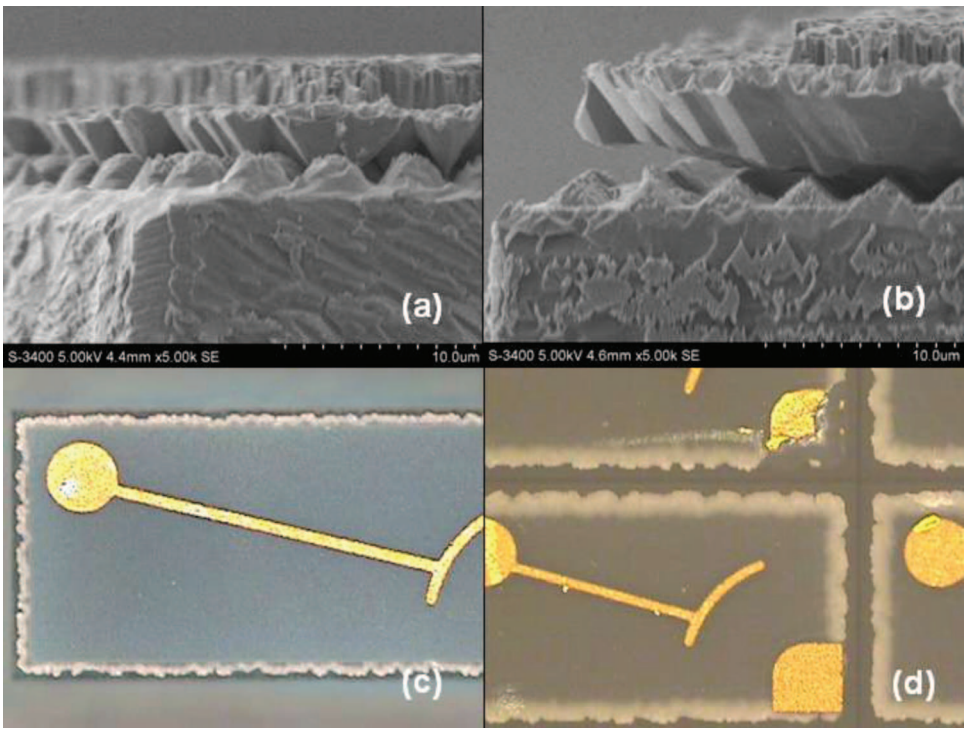



**Figure 4.** (a, b) Side-view SEM and (c, d) front-view OM images of GaN LED chips subjected to wet etching for (a, c) 10 and (b, d) 18 min.

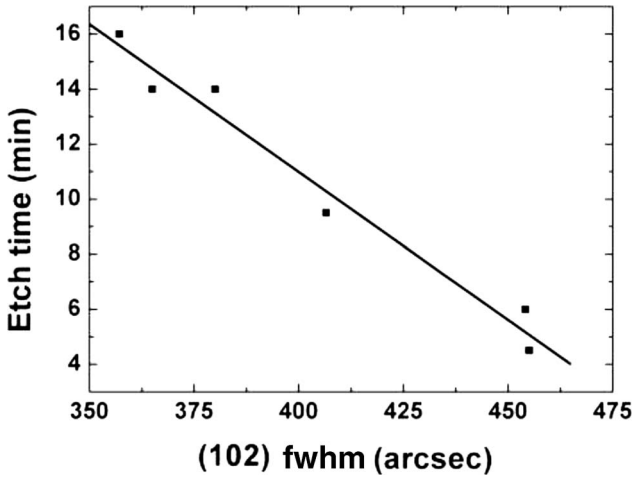



**Figure 5.** Plot of the fwhm of the (102) signal in the XRD pattern with respect to the etching time.

respectively. The lower leakage current of the SWE LED relative to that of the standard LED might be due to the SWE process mitigating the surface damage from the ICP system during the general fabrication process of the etching platform. Therefore, the SWE process proposed herein not only increased the luminance of the LED but also decreased the leakage current.

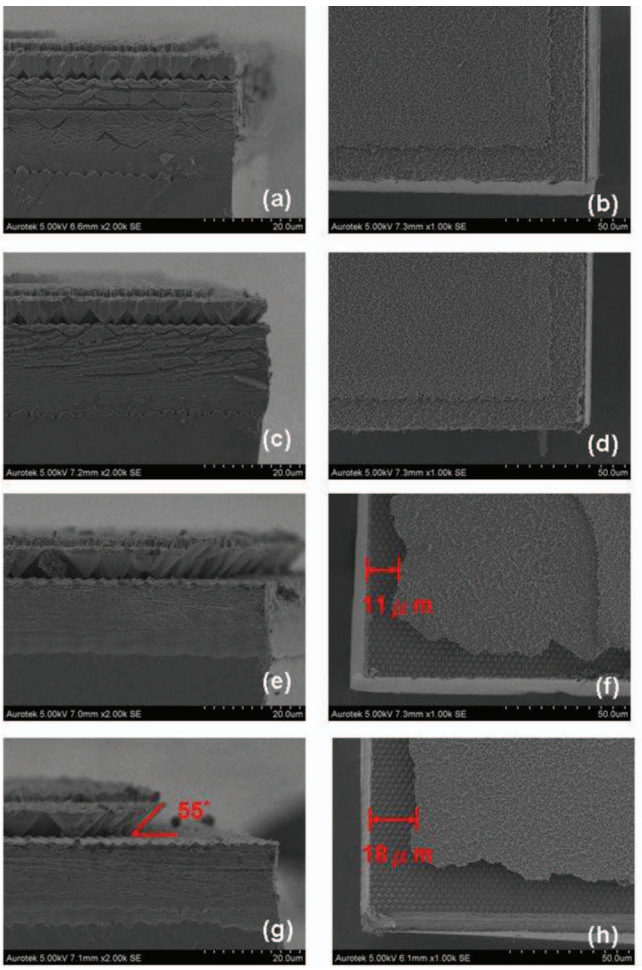
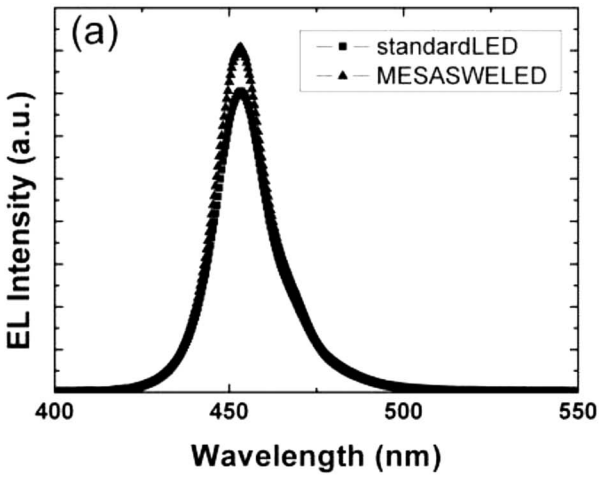



**Figure 6.** SEM images of the samples obtained after etching for 9 min; FWHMs of XRD (102) signal: (a, b) 353, (c, d) 370, (e, f) 402, and (g, h) 436 arcsec.



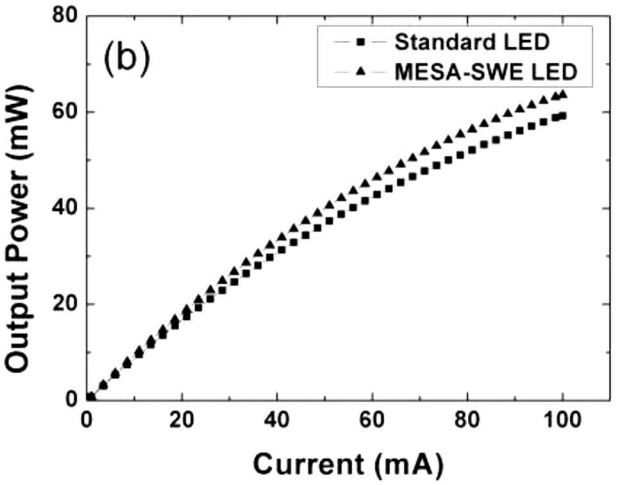




**Figure 7.** (a) EL (injection current: 20 mA) and (b) LIs (injection current: from 0 to 100 mA) of the SWE LED and standard LED.

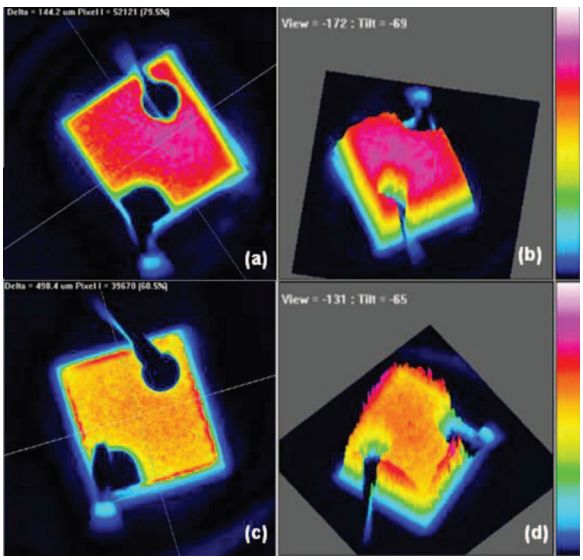



**Figure 8.** (a, c) Front emission patterns and (b, d) 3D emission patterns with the angle of 45° for (a, b) the 13-mil LED without SWE (injection current: 20 mA) and (c, d) the 13-mil LED with MESA-SWE.

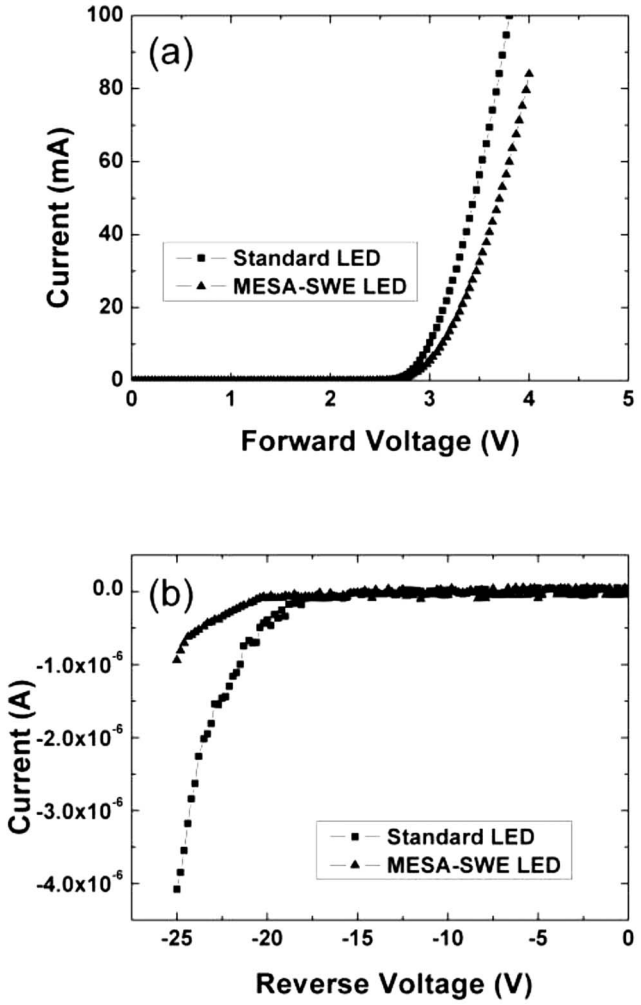



**Figure 9.** *I–V* curves of the SWE LED and standard LED at a (a) forward bias (0–4 V) and (b) reverse bias (0–25 V).

Next, we tested the ESD tolerance of both samples, including tests in the human body static mode (HBM) at 2000 and 4000 V and in the mechanic static mode (MM) at 200 and 400 V. Table I reveals that, regardless of the testing mode, both samples exhibited good yields (>90%); therefore, the SWE processing did not affect the ESD endurance of the devices. In further reliability tests, we packaged both samples into a 3020 surface mount diode (SMD), at room temperature, and observed the brightness variation at a constant injection current (20 mA) for 960 hr. After this period of time, the luminance of each sample remained greater than 95% (Fig. 10); because the attenuation of the output light was less than 5% for both samples, the SWE process does not appear to affect the reliability of the devices.

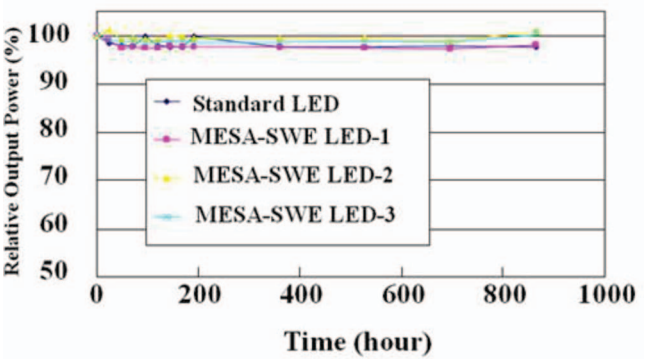



**Figure 10.** Reliability test data for various LEDs, packaged into 3020 surface mount diode (SMD), at room temperature for up to 960 h.

## Conclusions

We have developed a simple low-cost process involving SWE in heated acid solutions for improving the efficiency of LEDs. This approach, which alters the total reflection angles of the side walls, increases the external LEE of GaN LEDs; for example, at an injection current of 20 mA, the output luminance of our GaN LED increased by 11.4%. The ESD endurance and reliability of the devices did not deteriorate when applying the SWE process; in addition, we noted an increase in the protection capability of the sample surface after wet etching, implying that the deposition conditions of the $SiO_2$ protection layer should be optimized in each case. Furthermore, from a study of the effect of the etching conditions on the fwhm of the XRD signal for the (102) facet of the epiwafers on the grown LED wafers, we propose that this feature can be used as a reference for sample categorization, allowing the optimized etching conditions (e.g., etching time) to be determined, thereby improving the efficiency of the devices and the production yield.

## Acknowledgments

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**Table I. ESD tolerances of the SWE LED and standard LED tested in the HBM and MM modes.**

| Wafer No | Photo mask (mil) | M/M Test value (V) | M/M Observation point | M/M Acceptance number | M/M Yield (%) | HB/M Test value (V) | HB/M Observation point | HB/M Acceptance number | HB/M HB/M Yield (%) |
|---|---|---|---|---|---|---|---|---|---|
| CAIV19F02 | 10*18 Reference | 400 | 115 | 111 | 96.5 | | | | |
| | | | | | | 4000 | 115 | 112 | 97.4 |
| | | 200 | 112 | 110 | 98.2 | | | | |
| | | | | | | 2000 | 113 | 112 | 99.1 |
| CAIV19F04 | 10*18 SWE | 200 | 107 | 104 | 97.2 | | | | |
| | | | | | | 2000 | 109 | 105 | 96.3 |
| | | 400 | 109 | 98 | 89.9 | | | | |
| | | | | | | 4000 | 98 | 98 | 100 |

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