

Contents

<i>Preface</i>	<i>page</i> vii
<i>Abbreviations</i>	ix
1 An introduction to domino logic	1
1.1 CMOS and NMOS	1
1.2 Domino logic circuits	5
1.3 Clocking domino logic	12
1.4 Summary	15
2 High-speed digital design	18
2.1 Microprocessors since 1989	18
2.2 Microarchitectures for high speed	22
2.3 Designing and using high-speed memories	31
2.4 What to remember if applying domino logic	35
3 Domino logic library design	37
3.1 High-speed digital circuit design	37
3.2 An introduction to standard cells	42
3.3 Designing a high-performance standard cell library	45
3.4 Circuit design of domino logic cells: a qualitative approach	48
3.5 Circuit design of domino logic cells: a quantitative approach	51
3.6 Characterizing domino logic-compatible registers	63
3.7 Layout of domino logic standard cells	65
3.8 Timing models for domino logic cells	66
4 Domino logic synthesis	70
4.1 Introduction to domino logic synthesis	70
4.2 Unate transform	73
4.3 Phase assignment	75
4.4 Phase-assignment rules	77
4.5 An example domino synthesis flow	86
4.6 Schematic capture of domino designs	106

5	Circuits designed with domino logic in an ASIC flow	108
5.1	Introduction	108
5.2	Domino integer execution unit	108
5.3	A synthesized domino logic DSP core	119
5.4	A synthesizable domino logic Viterbi add–compare–select (ACS) test chip	121
5.5	Intel’s published domino logic synthesis flow	124
5.6	Conclusions	126
6	Evolution of domino logic synthesis	127
6.1	The state of digital ASIC design methodologies	127
6.2	Process trends and domino logic	128
6.3	Clocking methodology for domino circuits	130
6.4	Synthesizing other dynamic logic families	132
6.5	Flow improvements for domino synthesis	137
6.6	The case for domino logic synthesis	141
	<i>Index</i>	143