High Performance InGaAsSb TPV Cells via Multi-Wafer OMVPE Growth

Zane A. Shellenbarger, Gordon C. Taylor, Ronald K. Smeltzer, Jizhong Li, Ramon U. Martinelli, and Kalipada Palit

Sarnoff Corporation
Princeton, New Jersey 08543

Abstract. The fabrication and performance of InGaAsSb thermophotovoltaic cells are described. The InGaAsSb layers, grown by organometallic vapor-phase epitaxy in a multi-wafer reactor, with a 0.53 eV bandgap are lattice-matched to a GaSb substrate. Growth series with up to thirty 50 mm wafers have been done with good control of material composition and carrier transport properties. With improved materials and metallization and with a modification to the cell edges, fill factors near 70% and a greater than 60% peak external quantum efficiency are obtained. A two order-of-magnitude increase in shunt resistance with a consequent 15% improvement in fill factor was achieved with the improved edge structure. Series resistance, about 20 mΩ, is the remaining limitation to cell performance and is closely correlated with fill factor.

INTRODUCTION

Continued development of thermophotovoltaic (TPV) systems to exploit available thermal sources offers the potential for high conversion efficiency systems in a variety of applications. To achieve high efficiencies with many available sources, devices in low bandgap semiconductors are required. One low bandgap material system, the quaternary InGaAsSb, has the advantage of being lattice matched to available GaSb wafers, thus offering the possibility of a low concentration of crystalline defects with consequently good carrier lifetimes [1, 2]. In this paper, we report the recent advances in preparation of the quaternary material, the improvements in cell fabrication methods, and the cell performance characteristics achieved.

MATERIAL DEVELOPMENT

The active material, InGaAsSb, of the p-on-n cells is prepared by organometallic vapor-phase epitaxy (OMVPE) on a GaSb substrate. The target composition is $In_{0.16}Ga_{0.84}As_{0.14}Sb_{0.86}$ with a 0.53 eV bandgap. A low-pressure, vertical rotating-disk reactor with a capacity of three two-inch wafers is used. The system has a vertical gas flow, high-speed rotation, and a turbo-pumped low-pressure load-lock. Precursors used are triethylgallium (TEG), trimethylindium (TMI), trimethylantimony (TMSb), and 1000-ppm arsine (AsH_3) in hydrogen. Doping is done with 1000-ppm dimethylzinc (DMZ) in hydrogen for p-type material and 100 ppm hydrogen selenide

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(H_2Se) in hydrogen for n-type material. Typical growth conditions are 60 torr pressure, 100 rpm wafer rotation, and 19 slpm H_2 carrier gas flow. Achievement of high material quality for this low bandgap composition depends on temperature and substrate orientation. The typical growth temperature is 500°C and typically a (100) substrate misoriented 6° towards the (111)B direction is used. The structure of the cells is schematically illustrated in Figure 1.

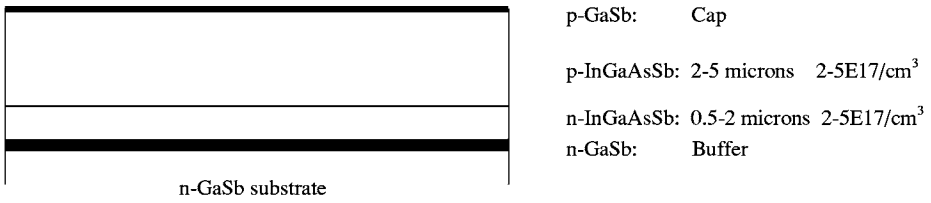

FIGURE 1. Schematic device layer structure.

Material uniformity is essential for a good yield of high efficiency cells. Properties of the layers are assessed with double-crystal X-ray diffraction, photoluminescence (PL), and Hall measurements. Photoluminescence, which is the key measure of uniformity, is recorded at the center of the wafer and at four points 5 mm from the edge of the wafer. Typically the variation of the PL peak had been ± 50 nm, but is now typically ± 5 nm. For three wafers from a single growth run, variation in the peak PL from the center of the wafers is typically within ± 3 nm. Variation in the peak PL from the center of the wafers from run to run is typically within ± 6 nm.

The improved uniformity in PL was achieved with a low, 100 rpm, susceptor rotation speed and with TEG instead of trimethylgallium (TMG) as the gallium source. Figure 2 shows the effect of rotation speed on peak PL across a wafer. It is speculated that the higher rotation speeds disturb the gas source profile, especially near the outer edge of the susceptor. With the lower rotation speed, improved surface morphology is obtained and the surface morphology is less sensitive to the V/III ratio. The use of TEG ensures more complete pyrolization at the growth temperature, thus reducing nonuniformity effects due to temperature variations across the susceptor. A third factor that may be important is adoption of a consistent surface preparation procedure to remove native oxide on the substrate prior to loading into the growth system.

Achievement of the target composition, with the 0.53 eV bandgap, increased the cutoff wavelength, defined at one-half of the peak value of the spectral quantum efficiency (SQE) characteristic, from an initial value of about 2125 nm to 2300 nm and reduced the variation among wafers from ± 45 nm to ± 5 nm. Thus, more of the input radiant energy can be utilized and cell-to-cell variability in performance is reduced.

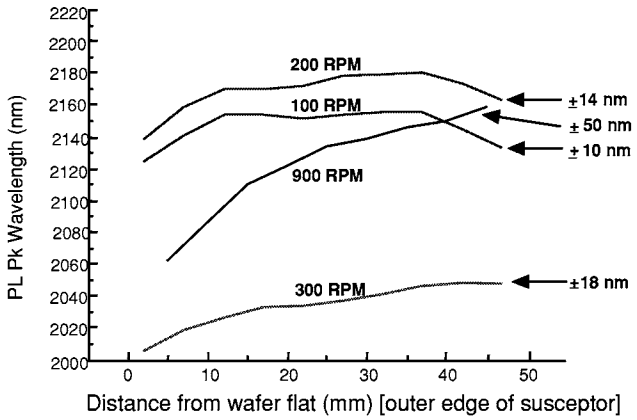

FIGURE 2. Peak PL across the wafer for various rotation speeds.

Data indicate almost identical properties for the three wafers from a growth run, not surprising since the wafers are symmetrically located. To demonstrate reproducibility, a growth series of 30 wafers was done. It was found important to keep the V/III ratio slightly higher than its lowest value, 3.4, to minimize run-to-run variations and formation of metal droplets. With the V/III ratio slightly higher, 3.6, a very small area at the edge of wafers was adversely affected, but a much larger area of good morphology was consistently obtained. Among the 30 wafers, the average peak PL at the center of the wafer was 2351 nm with a standard deviation of 9 nm and the average lattice mismatch was 0.074% with a standard deviation of 0.03%. These observations suggest that material can be prepared in reasonable volume for the fabrication of TPV cells.

Following fabrication of cells from the wafers, a standard set of measurements is taken from 5 mm x 10 mm cells, as many as 24, to assess uniformity and yield. The data indicate that good uniformity and yield from multiple wafers are achievable. Standard deviations less than about 3% for peak SQE and open circuit voltage are typical. Fill factor, which can be affected by cell processing, typically has a slightly larger variation. In a later section, fundamental cell characteristics related to the process improvements, which are discussed in the next section, are described in detail.

PROCESS OVERVIEW

Fabrication of the p-on-n cells begins with steps to remove contaminants and surface oxide. The p-contact, Ti/Au/Pt/Au (10nm/100nm/100nm/50nm), for the current collection grid is prepared by a lift-off process. Contact resistance and adhesion are improved by a 2 min sinter at 300 °C. The grid conductivity is increased with 5 μm thick plated gold, formed with a two layer photoresist process. The first resist layer is patterned with lines slightly narrower than the grid, and a seed layer of Ti/Au/Ti (150nm/100nm/60nm) is deposited. A second photoresist layer is patterned to etch off the top titanium and expose the gold layer in the grid area. After plating

and resist removal, the titanium and gold layers are removed. Finally, the photoresist that protected the semiconductor during plating and etching is removed with acetone and a plasma clean-up.

Contact to the n-GaSb substrate is made with Ni/Au/Ge/Ni/Au (5nm/45nm/20nm/15nm /200nm). A 60 sec sinter at 250 °C is done. A diffusion barrier of Ti/Pt/Au (50nm/100nm/ 200nm) with a gold overcoat is added to facilitate solder mounting of the cells for testing.

The process is completed by dicing the wafer with a protective layer of photoresist on the surface. The mechanical damage from sawing is removed by etching the diced wafer in a 10:1 mixture of 50 wt % citric acid and hydrogen peroxide. Removal of approximately 1 μm of material from the device edges is adequate to obtain a high shunt resistance, as described later.

The specific contact resistances were evaluated with GaSb wafers metallized with a Cox and Strack [3] pattern. Contact resistances for the sintered Ti/Au/Pt/Au p-type contact are in the low 10^{-7} Ωcm^2 range. For the n-type contact, $2.5x10^{-5}$ Ωcm^2 was measured. A metal system for p-type contacts composed of Ti/Pt/Ag/Pt/Au (30nm/100nm/ 5000nm/100nm/200nm) and patterned by lift-off yielded $6x10^{-6}$ Ωcm^2 without sintering. Higher conductivity and lower cost with respect to gold are advantages of the silver-based p contact.

Two sizes of cells, 4 mm x 4 mm and 5 mm x 10 mm, are produced with one photomask. Although the layouts for the current collection grids are slightly different, basically the grids of the two cells consist of 10 μm wide lines on a 100 μm spacing with one bus bar.

CELL PERFORMANCE

A variety of measurements are done to assess material and process variants. Dark current-voltage characteristics are used to extract the zero-bias slope as the shunt resistance. As noted later, this definition of shunt resistance yields a good fit to a model calculation. Dark forward-bias, current-voltage characteristics are employed to extract the diode ideality factor, n, and the dark current density, Jo. Short circuit current versus open circuit voltage plots for different light intensities also yield the diode ideality factor and the dark current density. Output characteristics with illumination to a short circuit current density 2 A/cm^2 are used to determine fill factor and to monitor open circuit voltage. For series resistance, output characteristics are taken at different light intensities and the method described by Handy [4, 5] is used. The merit of the Handy method is that series resistance is determined from operating characteristics with no need to assume a value for any device parameter, to assume an ideal characteristic, or to have a high shunt resistance. The Handy method yields physically reasonable values of series resistance that correlate well with fill factor. Finally, SQE of the cells is determined from an absolute measurement at 1.55 μm and from the relative SQE in the range from 1.0 to 2.6 μm.

For the measurements discussed here, the cells were packaged by soldering them onto a brass pallet with a lead attached along the main bus bar to minimize external series resistance. The pallet serves as a heat sink and is attached to a water-cooled

copper block for measurements. Open circuit voltage measurements indicate that there is no appreciable temperature rise during the measurements. In the remainder of this section, the important test results are described.

Low shunt resistance had been a substantial limitation to cell performance until addition of the edge etch to the process flow. To illustrate, Figure 3 shows diode characteristics before and after etching the edges of a cell. As measured by the zero-bias slope, edge etching increased shunt resistance from 13 to 860 Ω, with a resulting fill factor of 70% obtained from the operating characteristic. The fill factor prior to etching the edges of this cell was not measured, but fill factors near 60% were typical prior to addition of the edge etch to the process.

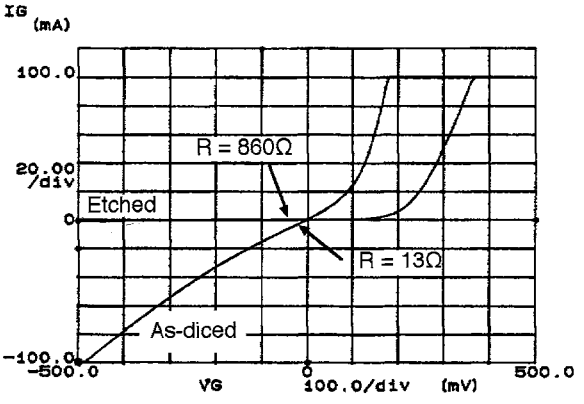

FIGURE 3. Pre- and post-edge-etch diode characteristics.

To illustrate more clearly the shunt resistance measurement and its effect on device characteristics, cells were characterized pre- and post-edge-etch. For the same cell, Figure 4 illustrates dark forward current-voltage characteristics measured pre- and post-edge-etch and calculated from the post-etch characteristic shunted by the initial measured shunt resistance. The effect of the edge etch on this cell was to increase the shunt resistance from 10.4 Ω to 350 Ω. The calculation of the shunted device characteristic agrees very closely with the pre-etch measurement, thus validating the zero-bias slope as a useful method to determine shunt resistance. The ideality factor of the diode after etching is close to one over a wide range of voltages, as indicated by the line for n=1 in Figure 4. The as-diced characteristic has very large excess currents over much of the voltage range, indicating that conduction through the shunt resistance path dominated the device behavior before the edge was etched. The fill factor for this particular cell increased from 61 to 68% after the edges were etched. Elimination of the large excess shunt current is also evident in the plot of short circuit current versus open circuit voltage, Figure 5, which yields a diode ideality factor near one and a dark current density of 3.6E-5 A/cm^2.

Under very low illumination conditions shunt resistance can be approximated [6] as the quotient of open circuit voltage to short circuit current. One comparison yielded a shunt resistance value from the low-illumination approximation within a few percent

of that from the slope measurement, which however is a much more convenient procedure.

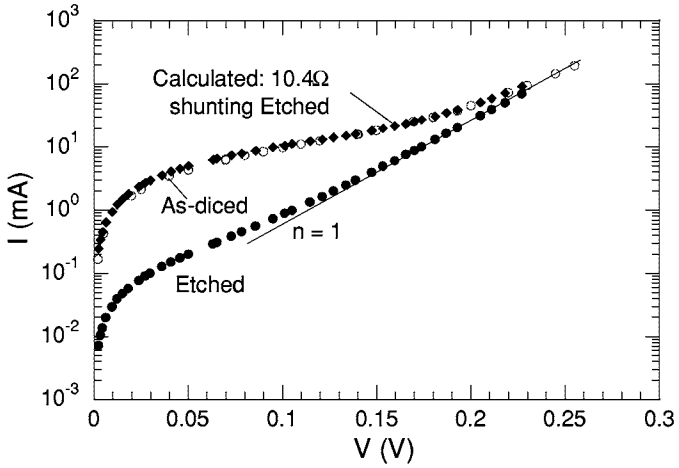

FIGURE 4. Dark forward characteristics: as-diced (open circles), after edge etching (filled circles), and calculated from etched characteristic shunted by the measured shunt resistance (filled diamonds) to illustrate the validity of the shunt resistance model.

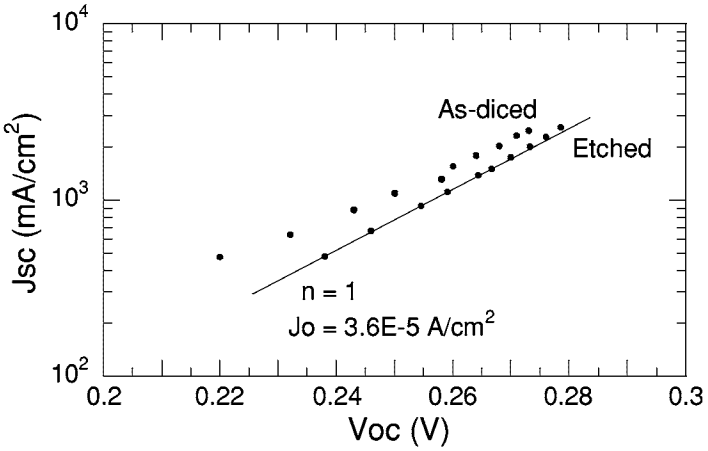

FIGURE 5. Short circuit current density versus open circuit voltage before and after edge etch.

To quantify the effect of shunt resistance and to determine the range of shunt resistance values for which the fill factor is independent of shunt resistance, the basic diode equation was solved, Figure 6, without series resistance for typical values of dark current. Converting from Ωcm^2 for the two cell sizes, one finds about 190 Ω for the small cells and about 60 Ω for the large cells yield fill factors independent of shunt resistance. Most cells now meet the respective criterion for shunt resistance. Presumably, series resistance is the remaining limitation to fill factor, now typically close to 70%, which is about three units from the theoretical limit shown in Figure 6.

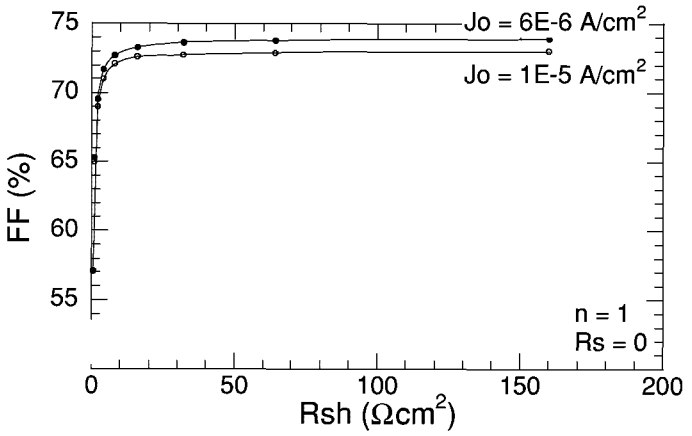

FIGURE 6. Calculated fill factors for ideal diodes with no series resistance.

The measurement of series resistance in a photovoltaic device is not trivial. The method of Handy was adopted because it uses only measured cell characteristics. In the Handy method, output characteristics are taken at various illumination levels, and an increment of current from the short circuit value is marked-off on each characteristic. Were there no series resistance, a line drawn through the points would be parallel to the current axis; in the real case, there is a voltage drop due to the series resistance, and the slope of the line is the series conductance. Because packaged devices are used for the measurement, a large database for series resistance is not available. However, with a sufficiently large shunt resistance and a correlation between fill factor and series resistance, fill factor serves as a measure of series resistance for a fixed cell structure.

An example of the use of the Handy method to determine series resistance is shown in Figure 7. Various current increments yield a series resistance of about 18 mΩ. A value for series resistance on the order of a few tens of milli-Ohms is consistent with an estimate of 10 mΩ for the series resistance of the current collection grid. Measured fill factor and series resistance for cells are plotted in Figure 8 to illustrate that the relationship is consistent with the best expected fill factor, about 73% from Figure 6, in the absence of series resistance. Another operational definition [7] of series resistance also yielded values of a few tens of milli-Ohms.

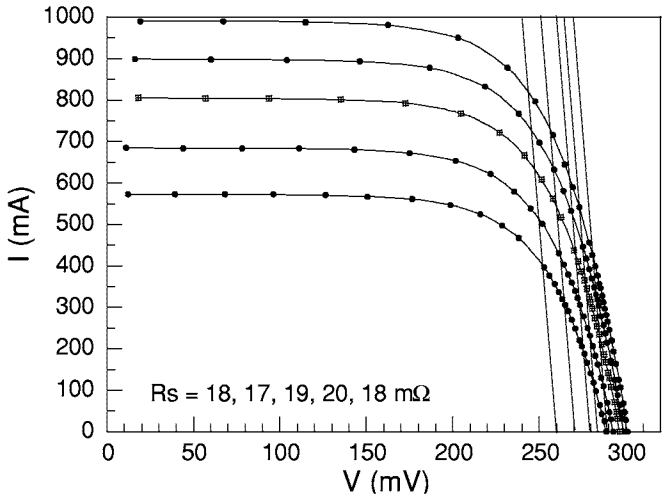

FIGURE 7. Series resistance determination from a family of operating characteristics for a large cell.

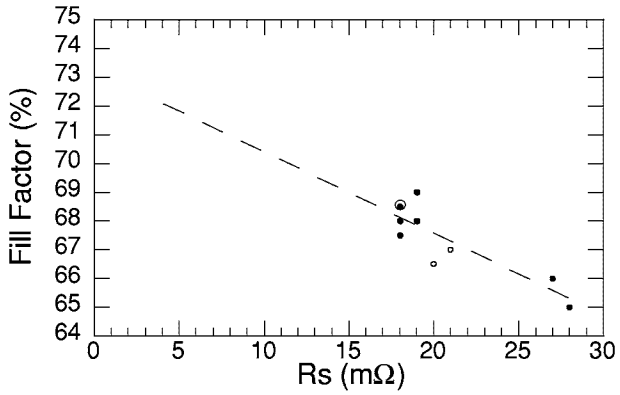

FIGURE 8. Fill factor vs. series resistance from Handy method measurements.

The fundamental optical performance of the cells is assessed by the measurement of external SQE. Figure 9 shows the measured SQE over the wavelength interval from 1 to 2.6 μm of four cells from two different wafers. The solid and the open data points identify data associated with each wafer. The data were taken at very low illumination levels, under short-circuit-current conditions of less than 1 μA.

The four cells have similar spectral responses. The long-wavelength cut-off is about 2.4 μm, indicating good control and uniformity of the composition both within a wafer and wafer-to-wafer. The SQE curves show peak values of 61-65% at 2 μm. Since the reflectivity of the cells is about 33% at 2 μm, the internal quantum efficiency is about 94%. The decrease in the SQE curves to 50% at 1 μm has two causes. First and most importantly, an increase in the reflectivity to 37% at 1 μm decreases the

fraction of absorbed light. Second, the optical absorption constant increases with decreasing wavelength, thus decreasing the number of photo-generated electrons collected at the junction. Because the electron diffusion length is much longer than the p-emitter width, only a slight decrease in the internal quantum efficiency results. A one-dimensional minority-carrier diffusion model accurately describes these effects [8]. With a broad-band, 1-2.4 μm, anti-reflection coating, the cells would be efficient converters of radiant energy.

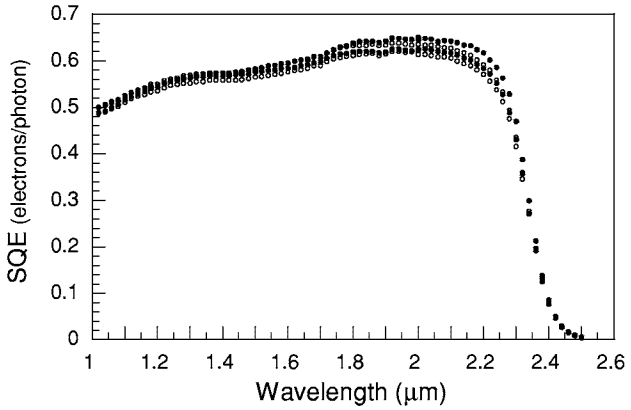

FIGURE 9. Typical external spectral quantum efficiency characteristics.

SUMMARY

InGaAsSb TPV cells with layers grown by OMVPE in a multi-wafer reactor are produced with fill factors near 70% and with a peak external quantum efficiency greater than 60%. Growth series with as many as 30 wafers show good control of material composition and carrier transport properties. Key to good cell performance is the two order-of-magnitude increase in shunt resistance achieved with an improved process. Dark forward diode characteristics without the process improvement are modeled closely as the improved diode characteristic shunted by a measured value for initial shunt resistance. Series resistance, typically about 20 mΩ, is the remaining limitation to cell performance for the current device architecture and is closely correlated with fill factor. Sarnoff TPV diode technology when combined with module technology by Sarnoff [9] and spectral control technologies provided by other organizations has led to TPV conversion efficiencies in excess of 17% [10].

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