Low Cost and Highly Manufacturability 10Gb/s Mini-Flat Transmitter for Ethernet Applications

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ABSTRACT

The key issues of local-area-network (LAN) and storage-area-network (SAN) applications are to improve cost, manufacturability and reliability of optoelectronic devices in high speed transmission. The authors have demonstrated highly manufacturability, reliability and thermal stability mini-transmitter for 10Gb/s Ethernet applications in this paper. Passive alignment technology is a way to improve manufacturability of optoelectronic devices in the future. However, the assembly yield rate of conventional LD chip on silicon optical bench to fiber is quite limited due to restricted optical alignment tolerance (< 1um). In this study, a novel two lens structure of 10Gb/s LC receptacle type optical mini-flat transmitter is designed and demonstrated to exhibit above 20% coupling efficiency with less than ±6um aligned deviation. Moreover, a high resistivity silicon optical bench (1kΩ/cm) and pressure-free bonding technique using the electroplated AuSn solder are also adopted to guarantee the transmitted performance in high frequency operation. The eye diagram of 10Gb/s mini-flat transmitter developed in this study showing the excellent quality obtained passing 10Gb/s Ethernet mask test with 20% margin. And the extinction ratio of transmitter is also proved to above 6dB at room temperature. The response of monitor PD is also examined up to 80% by mirror coating on silicon V-groove. Thermal stability of 10Gb/s mini-flat transmitter is another critical issue in high speed transmission. The performance of temperature stabilized transmitter over wide case temperature range is also evaluated in this study. The optical eye diagram of 10Gb/s transmitter developed in this paper showing excellent eye quality passing 10Gb/s Ethernet mask test between 0℃ to 80℃. Finally, the reliability of transmitter is also performed. The reliability data indicate that the optical alignment of these modules are stable and observed essentially low variations in optical coupling as results of 1000 hours damp heat and 1000 temperature cycling durations.

1. INTRODUCTION

The recent increase in the amount of data traffic requires optical communication systems operating at 10Gb/s and above even in LAN and MAN such as 10Gigabit Ethernet (10GE) and 10Gigabit Fiber-Channel (10GFC). One of the most key issue is reducing the cost, size and power consumption of optical components in these applications. There have been many studies on improving the performance of 10Gb/s 1310nm DFB chip with box type packages, especially the high frequency performance at high temperature [1-2]. Passive aligned technique is a way to improve manufacturability of optoelectronic devices in high speed transmission [3-5]. However, it can be achieved without high accuracy flip chip bonder、perfect process of SiOB, and accuracy packaging flow to keep the total alignment tolerance below ±1μm. In this paper, the authors demonstrated a novel two lenses semi-passive alignment structure not only to loose the tolerance but also improve the coupling efficiency up to 35% with general semiconductor process and optoelectronic packaging equipments. Moreover, the 10Gb/s 1310nm uncooled direct modulation mini-flat transmitter developed in this paper is also proven to follow the requirements of 10Gb/s Ethernet transceiver modules. The remaining of this paper is organized as follows: section 2 will describe the electrical design and analysis of SiOB for 10Gb/s applications. Optical design and analysis of the two lenses structure are discussed in section 3. The process of SiOB and following packaging and evaluations are points in sequential sections, respectively. Finally, the conclusions of this study are given in last section.

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2. ELECTRICAL DESIGN AND ANALYSIS

The core factors of designing the SiOB in 10Gb/s operations are including the electrical characteristics of material and the parameters of process. The electrical parameters of silicon, such like the dielectric constant, loss-tangent and dielectric conductivity will mainly determine the transmission performance of signal. On the other hand, the skin effect, thickness and effective conductivity of compound metal will also deeply influence the transmission loss of signal. Therefore, all the electrical parameters mentioned will be calculated by the simulation tool to predict and specify the requirement and the probable tolerance of process before the actual implementation of SiOB.
Fig. 1 depicts the simulation model of SiOB, and the simulation conditions are listed in Table 1. Table 1 lists the electrical characteristics of dielectric layers and metal layers. The thickness of the silicon, SiNx, and metal will also affect the impedance design. The surface resistance and skin effect of the metal layer is an effective value that represents synthetic conductivity of three different metals. As operating at high frequency, it is supposed that the most signal is transmitted along the Au-layer.

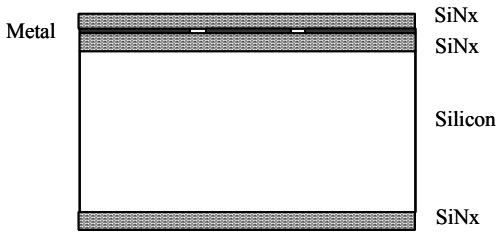

Fig. 1 Simulation model of SiOB

The propagation loss between different resistivity of silicon wafer is also analyzed in this study. Fig. 2 shows that 500Ω/cm resistivity silicon wafer causes the transmission loss more serious than silicon wafer with 1kΩ/cm resistivity. However, if effective surface resistance R_{DC} of the compound metal is changed from 0.067 to 0.075, that means more signal transmit in the Ti/Pi-layer in the low frequency range, the transmission loss will become more significant.
From the simulation results, the dimension of the RF transmission line is determined. Besides, the reasonable thickness of silicon, SiNx and metal are specified for following SiOB processing.

Material	Electrical Parameters			
Silicon	Dielectric Constant	Loss Tangent	Resistivity	Thickness
	12	0.0004	1kΩ/cm	660 μm
Metal	Surface Resistance R_{DC}	Skin Effect Coefficient R_{RF}	Thickness of Ti / Pt / Au	
	0.067Ω/sq	9.81e-7	500Å/500Å/3500Å	
SiNx	Dielectric Constant	Loss Tangent	Thickness	
	7	0.00001	Above metal: 3000Å Below metal: 5000Å	

Table 1 Simulation conditions of SiOB.

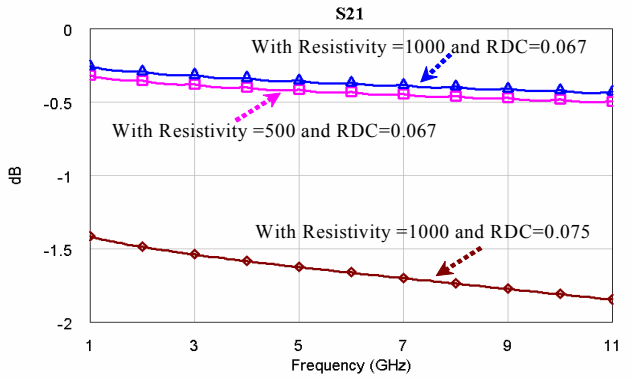

Fig. 2 The simulation results with different resistivity of silicon wafer

The comparison of measurement data and simulation results are displayed in Fig. 3. The line with mark represents the simulation data and the measurement data is described in solid line without mark. The results of S21 depicts that the exactly transmission loss is around 0.5~0.6dB. The difference between simulation and measurement results is about 0.3dB.

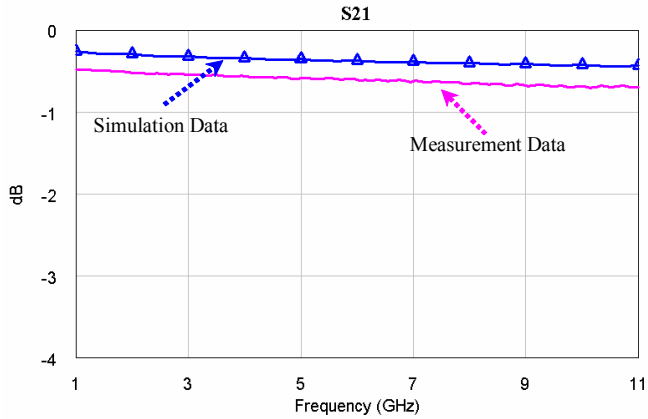

Fig. 3 The comparison between measurement data and simulation result of SiOB

3. OPTICAL DESIGN AND ANALYSIS

The high coupling efficiency(>20%)、receptacle type、low cost optical transmitter are some key issues to meet the requirements for 10Gb/s Ethernet applications. However, the traditional butt coupling optical system used in SiOB requires a high accuracy flip chip bonder、perfect process of SiOB, and accuracy packaging flow to keep the total alignment tolerance below ±1μm, the tolerance is too tight for mass production. Therefore, the semi-passive double-lenses optical system including a ball lens and an aspheric lens is designed not only to loose the system tolerance but to improve the coupling efficiency of 10Gb/s mini-flat transmitter. Figure 4 shows the schematic structure of double-lenses optical system, where C.E. is the coupling efficiency, Lx, Ly, Lz are LD axis shifted in x、y、z directions, respectively, By is the radius 800um BK7 ball lens axis shifted in y direction, Sx, Sy, Tz represent the axis shift of the aspherical lens in x, y, z direction relative to the ball lens, and C is the distance between single-mode fiber (SMF) and aspheric lens.

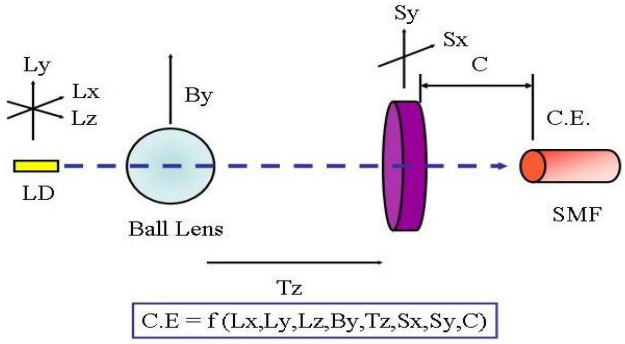

Fig. 4 Schematic structure of 10Gb/s mini-flat transmitter optical system

According to the schematic structure of 10Gb/s mini-flat transmitter optical system shown in Fig. 4, the coupling efficiency of system can be described as the assembly function as Eq. (1)

$$C.E. = f(Lx, Ly, Lz, By, Sx, Sy, Tz, C) \quad (1)$$

And the coupling efficiency can simplify as Eq. (2) due to cylinder symmetrical of SiOB.

$$C.E. = f(\vec{R}_B, Lz, Sx, Sy, Tz, C) \quad (2)$$

where $\vec{R}_B = \sqrt{(\vec{L}x)^2 + (\vec{L}y + \vec{B}y)^2}$.

Let the axis shifted of aspheric lens as $\vec{R}_L = \sqrt{Sx^2 + Sy^2}$, where (Sx, Sy) are the shift of aspheric lens on x, y axis. Then the coupling efficiency can be further defined as Eq. (3)

$$C.E. = f(\vec{R}_B, \vec{R}_L, Lz, Tz, C) \quad (3)$$

Two cases are studied in this paper, one is the case with high accuracy flip chip bonder、perfect process of SiOB, and accuracy packaging flow. And the following are the assembling conditions of case 1: $\vec{R}_B = 5\mu m$, $\vec{R}_L = 10\mu m$, Lz = 1μm and Tz = 100μm. Fig. 5 shows the simulation results of case 1. The coupling efficiency of case 1 is calculated above 58.8%. Beside, the coupling efficiency of case 1 is also simulated to remain 50% with ±2μm deviation in final welding process.

The other is the case with ±5μm flip chip bonder、general process of SiOB, and packaging flow. And the following are the assembling conditions the authors suggested according to above situations in case 2: $\vec{R}_B = 20\mu m$, $\vec{R}_L = 150\mu m$, Lz =15μm and Tz = 1000μm. Fig. 6 shows the simulation results of case 2. The coupling efficiency of case 2 is simulated about 37.9%. Beside, the coupling efficiency of case 2 is also simulated to keep 36.1% with ±2μm deviation in final welding process.

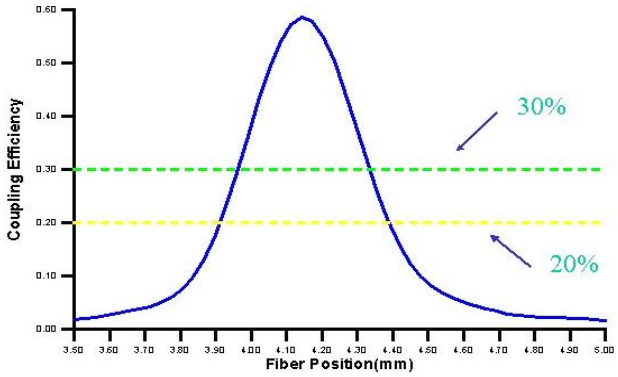

Fig. 5 The simulation result of coupling efficiency of case 1

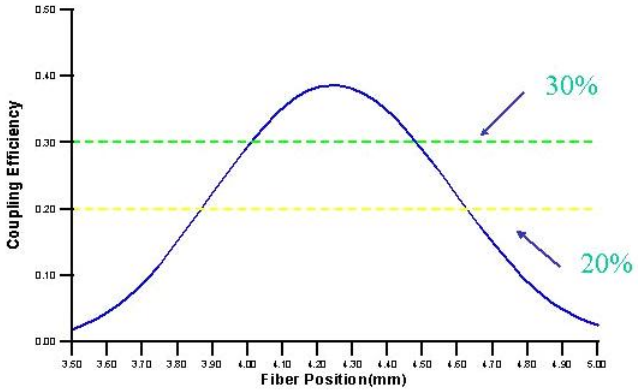

Fig. 6 The simulation result of coupling efficiency of case 2

4. SILICON OPTICAL BENCH FABRICATION

It's widely used for bulk micromachining of single crystal to fabricate the packaging platform for optical devices. The structure nature of silicon makes it possible to fabricate the precise three-dimensional shape. In general, silicon has high etching selectivity of (100) to (110) plane in anisotropic wet etching, and it offers a fascinate advantage to apply silicon on optoelectronic device packaging. In this paper we present a low-cost fabrication process of SiOB which contains two Silicon V-grooves, electrical circuit and eutectic gold-tin solder pad. A 964μm wide V-groove is created for holding the 800μm BK7 ball lens in place and the smaller one is coated with gold on the sidewalk acted as a mirror reflecting light to monitor photo diode. The main processing steps are described as following:
Step A. Start from a single polished p-type silicon wafer with orientation of (100). The wafer thickness is 680 um.

Step B. The first of making a SiOB is depositing a 5000Å thick silicon nitride (SiNx) layer on 1kΩ/cm resistivity silicon wafer by LPCVD(low pressure chemical vapor deposition). For protection from 45% KOH etchant, both sides of deposited silicon nitride layers are necessary.

Step C. Lithography and RIE (reactive ion etching) process are accomplished to remove the SiNx layer on V-groove area.

Step D. The silicon wafer is immersed into KOH solution. By controlling the etching time precisely and maintaining the temperature as 60℃, the width and depth of V-groove are 964±2μm and 400μm made to allow the passive alignment of ball lens, respectively.

Step E. E-beam evaporate the conductive layer (Ti/Pt/Au, 500Å/500Å/3500Å) on the silicon wafer after the V-grooves etchant have been created. With lithography process and commercial etchant, the conductive layer is selectively removed again and electrical circuit created.

Step F. To avoid short circuit on SiOB, the second SiNx layer (3000Å) is deposited on the surface of gold layer by PECVD.

Step G. Lithography and RIE (reactive ion etching) process are accomplished to remove the SiNx layer on plating area.

Step H. Thermal coating 3μm gold-tin to form solder plates, thick photoresist lithography to pattern gold-tin.

Fig. 7 represents the photography of the fabricated SiOB for 10Gb/s mini-flat transmitter. The width tolerances of both V-grooves etchant on SiOB are demonstrated in ±2μm.

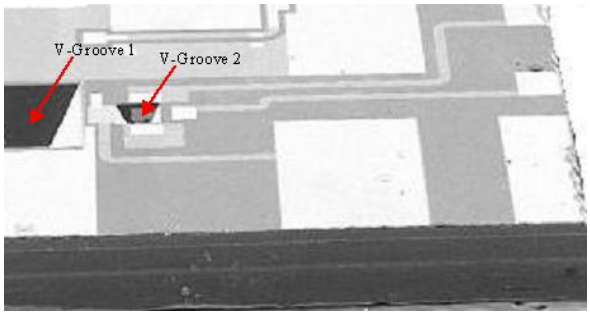

Fig. 7 The photography of fabricated SiOB.

5. PACKAGING

The fabricated SiOB provide a support and alignment platform for the LD chip, monitor PD chip, ball lens and other electrical passive devices (resistor, capacitor, thermistor, etc.). The LD chips are accurately bonded junction down on the SiOB according to the alignment features on LD and SiOB with a flip-chip bonder of ±5μm accuracy. The ball lens is passive-aligned on the V-groove and fixed with epoxy adhesive. After all the devices are assembled on the SiOB, the SiOB is wire bonded for electrically connection. The SiOB is then performed inside and bonded along with the 10Gb/s mini-flat package with the same system of the flip-chip bonder. One issue must be considered when the bench is aligned to the package, the LD chip is not exactly in the center of the bench due to the deviation of die sawing error of the SiOB. Therefore, the center of LD chip on SiOB (> 20μm) must be compensated as could as possible by measuring and shifting the center misalignment of bench and LD chip. After SiOB is fixed, an isolator is also bonded in similar process. The isolator is used for reducing optical feedback which causes the optical instability and increases relative intensity noise (RIN). A seam sealer is used to guarantee the hermetic of 10Gb/s mini-flat transmitter. A lid is attached to the Mini-Flat package by parallel seam welding with 1.5KW welding power. A leakage test is performed after sealing to evaluate the hermetic of the package, the leakage is below 1×10^{-11} Pam^3/s .
After the package is sealed, then the second aspherical lens and fiber ferrule are expected to attached to the sealed package for optical connection. The second aspherical lens is used for focusing the collimated light emitting from the window of the package, the 2nd lens is attached to the package via a lens holder, and the fiber ferrule is attached to the lens holder via a sleeve, all the fixation are done by laser welding method on a commercial laser welder system. The following are the welding parameters of lens holder、sleeve and fiber ferrule, respectively. The laser welding parameters are 1.5KW-5ms for lens holder and package, 1.8kW-5ms for sleeve and ferrule and 1.2kW-3ms for sleeve and lens holder. The maximum coupling efficiency is attained 35%, and the post laser welding shift loss is below 0.5dB. Fig. 8 shows the photography of LC receptacle type and pigtail type 10Gb/s mini-flat transmitter developed in this study. The dimension of the transmitter is 13.2 x 7.4 x 4.34mm, which is about 1/3 the volume of a traditional butterfly module.

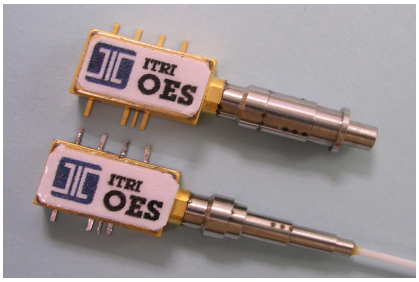

Fig. 8 The photography of LC receptacle type and pigtail type 10Gb/s mini-flat transmitter

6. PERFORMANCE AND RELIABILITY

Fig. 9 shows the measured frequency response of 10Gb/s mini-flat transmitter operated at 50mA biased current and permitted a modulated bandwidth over 10GHz at room temperature. The back to back eye diagram of 10Gb/s direct

modulation transmitter operated with 10.3125Gb/s Pseudo-Random-Binary-Sequence (PRBS) 2^{31}-1 pattern is also evaluated in Fig. 10. And exhibits an open and clear eye diagram complete accomplished the eye template of 10GE with 30% margin. The response of monitor PD is also examined up to 80% by mirror coating on silicon V-groove. The 10Gb/s 1310nm mini-flat transmitter developed in this paper has demonstrated excellent performance for future high speed applications.

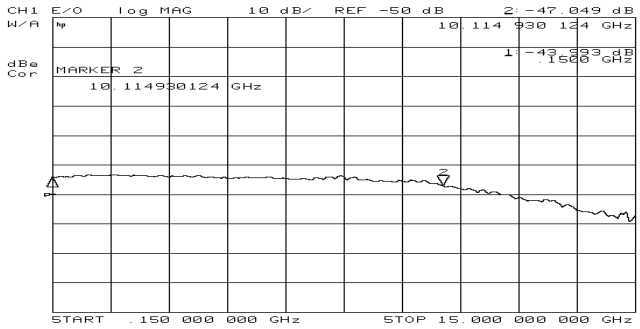

Fig. 9 Frequency response of 10Gb/s 1310nm mini-flat transmitter

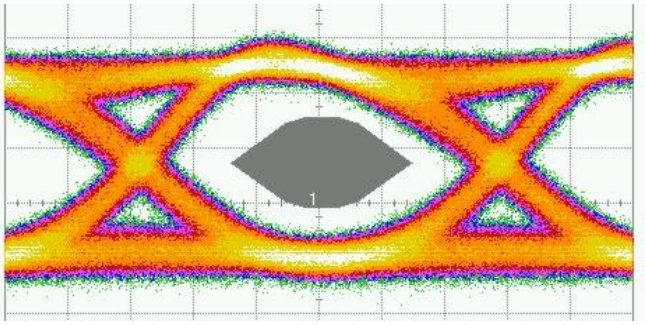
Fig. 10 Eye diagram of 10Gb/s 1310nm mini-flat transmitter with 30% mask margin at room temperature

The performance of the temperature stabilized transmitter over wide case temperature is also experimented. Thermal-electrical cooler (TEC) is a usual cooling element, but expensive one in box type transmitter for long haul or DWDM transport systems. However, it is quite difficult to combine a cooling element in a transmitter and to meet the low cost, compact size and low power consumption requirements of 10GE transceiver modules. The characteristic temperature of a laser diode determines the thermal stability. The high band-gap offset InGaAlAs laser diode is adopted to approach the uncooled aim with its high characteristic temperature. The 10Gb/s 1310nm InGaAlAs mini-flat transmitter is measured at 80℃ case temperature to verify thermal stability in high temperature. The eye diagram of 10Gb/s transmitter operated at 80℃ case temperature with 10.3125Gb/s PRBS 2^{31}-1 pattern is tested and accomplished the eye mask as shown in Fig. 11.

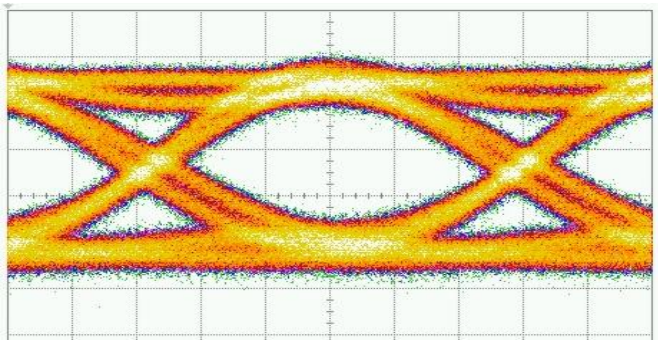

Fig. 11 Eye diagram of 10Gb/s 1310nm mini-flat transmitter at 80℃

Finally, the reliability issues of 10Gb/s mini-flat transmitter are also considered and performed according to Telcordia-GR468-CORE in this paper. In the bench level, die shear test of LD chip and wire bond strength test are performed, respectively. The die shear test is evaluated over 100gm, and the wire bond strength is over 4gm, and all meet the requirements of MIL-STD-883 standard. The mechanical integrity issues including mechanical shock, vibration and fiber pull are performed, and also demonstrated qualified. The endurance test of damp heat and temperature cycling are chosen to test. The test condition of damp heat test is 85%/85°C, 1000hrs, and the condition of temperature cycling test is -40°C to 85°C, 1000 cycles. The launch power variation of 10Gb/s mini-flat transmitter is evaluated during the tests, and the launch power deviation is both below ±0.5dB after the damp heat and temperature cycling test.

7. CONCLUSIONS

Passive alignment technique is a way to promote manufacturability of optoelectronic devices in the future. However, the assembly yield rate of conventional LD chip on SiOB to fiber is quite limited due to restricted optical alignment tolerance. In this study, the novel two lenses semi-passive structure of 10Gb/s LC receptacle type and pigtail type optical 1310nm mini-flat transmitter is designed and demonstrated to exhibit about 35% coupling efficiency with ±5μm accuracy flip chip bonder、general process of SiOB and packaging flow. Moreover, a high resistivity SiOB and pressure-free bonding technique using the electroplated AuSn solder are also adopted to guarantee the transmitted performance in high speed operation. The eye diagram of 10Gb/s mini-flat transmitter developed in this study showed the excellent quality obtained passing 10GE mask test with 30% margin. And the extinction ratio of transmitter is also proved to above 6dB at room temperature.

The performance of temperature stabilized transmitter over wide case temperature range is also experimented and pass 10Gb/s Ethernet mask test at 80℃. Finally, the reliability tests of 10Gb/s mini-flat transmitter are performed. The reliability data indicate that the optical alignment of these modules are stable and observed essentially low variations in optical coupling as a result of 1000 hours and 1000 cycles damp heat and temperature cycling durations, respectively.

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