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Research on High-power Power Factor Corrector of Power Electronic Transformer

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Abstract: Power electronic transformer (PET) which has a big potential application value in smart grid is an electrical power transformer device adopting power electronic converter and high frequency switch transformer. A new PET with power factor correctors (PFC) is proposed in this paper. Due to high power level of PET, PFC should have a high power level as well. Therefore, the multi-phase interleaved PFC is employed. The paper describes the one cycle control principle, proposes a current synthesis method based on IGBT current, and then analyses the relationship between ripple current and duty cycle of IGBT. In addition, the whole PFC system is simulated completely by means of Matlab/Simulink. In order to verify the theoretical analysis and simulation analysis, a four-phase interleaved PFC with a rated output power of 8.0kW is designed and implemented based on the an analog control chip. The obtained results show that the interleaved PFC by means of one cycle control and current synthesis is feasible, capable of reaching a good suppression effect of ripple current.

Introduction

As the smart grid develops, intelligent power electronic transformer (PET) which has a great superiority on volume and cost will replace the traditional electrical transformer. At present many application and control methods of PET in electric power distribution system are developing fast [1, 2]. In order to satisfy the requirements of low-frequency electromagnetic compatibility [3], power factor corrector (PFC) is very suitable for PET application. The high frequency noises generated by PFC converter can be eliminated by electro-magnetic interference (EMI) filter [4,5,6]. According to the continuity of inductor current, PFC has three operation states: continuous conduction mode (CCM), discontinuous conduction mode (DCM) and critical mode (CRM). CCM is more suitable for high power application due to its advantages of high power density, low conduction loss and low ripple current [6]. Compared with traditional PFC, multi-phase interleaved PFC can reduce the volume, electromagnetic loss, switch device current stress and raise efficiency, power factor [6,7,8,9]. This paper does a comprehensive research on the system of four-phase interleaved PFC applied in PET. Section 2 describes the system structure of PET, PFC and one cycle control principle. Section 3 analyses the relationship between input ripple current and duty cycle of IGBT, proposes an inductor current synthesis method based on IGBT current, line voltage and output voltage. Section 4 gives the simulation and experiment of 8.0kW four-phase interleaved PFC. The experiment shows the proposed scheme is feasible.

Circuit topology and control principle

Topology of PET. The proposed PET topology proposed shown in Fig.1 is consist of buck converter and PFC. The buck converter includes high voltage side LC filter, AC push-pull converter, high frequency transformer and low voltage LC filter. PFC topology employs boost converter.

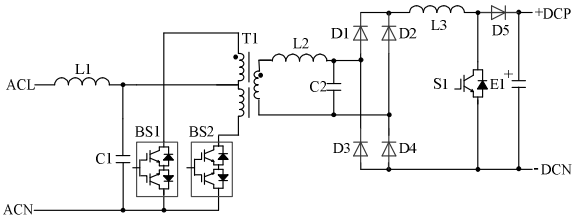

Fig.1 PET topology

This kind of PET can acquire unit power factor in main side. The advantages are: simple high voltage side topology and control method, safe commutation procedure and the power factor correction part set at the low voltage side. In order to raise the power level of PFC, the four-phase interleaved topology is employed.

Circuit topology and operating principle of paralleled interleaved PFC. As is shown in Fig.2, four-phase paralleled interleaved PFC is consist of four parts: EMI filter in main side, two paralleled diode rectifiers, four paralleled boost circuits and analog control circuit. L1, L2, L3 and L4 are boost inductors. S1, S2, S3 and S4 are IGBTs. FRD1, FRD2, FRD3 and FRD4 are fast recovery diodes. Due to the high output power, several electrolytic capacitors are paralleled connected in the DC output side. R2A20104 is employed as the analog control chip to realize the four-phase interleaved function.

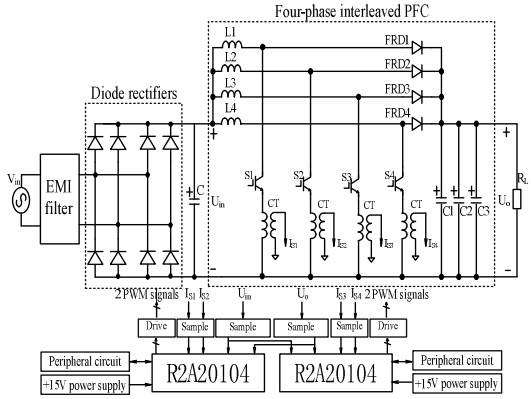

Fig.2 System structure of interleaved PFC

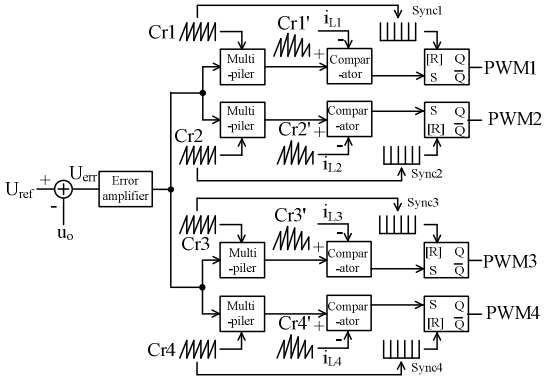

Fig.3 Block diagram of one cycle control

The control chip of interleaved PFC is adopting one cycle control principle, whose block diagram is shown in Fig.3.The control target of PFC is to make the input current vary in phase with input voltage, namely the displacement factor $\cos\phi_1=1$. As a result, the whole converter can be seen as a pure resistor R_e. Suppose the rectifier output voltage is u_{in}, inductor current is i_L. $u_{in}=i_L\times R_e$. For boost circuit, the relationship between input voltage and output voltage is $u_{in}=U_o\times(1-D(t))$. Use above equations and the current sensing resistor R_s to get:

$$i_L\times R_s=\frac{U_o\times R_s}{R_e}(1-D(t)) \tag{1}$$

Let switch period equals to T_s. The math model of one cycle controlled PFC is described as follows:

$$\begin{cases} U_1=-i_L\times R_s \\ U_2=-\dfrac{U_o\times R_s}{R_e}+\dfrac{1}{T_s}\displaystyle\int_0^{DT_s}\frac{U_o\times R_s}{R_e}dt \end{cases} \tag{2}$$

If the duty cycle meets equation (4), input current is ensured to keep in phase with input voltage, so that PFC function is accomplished.

Analysis of ripple current and the principle of current synthesis

Analysis of inductor ripple current. While four-phase interleaved PFC is working in CCM, there are 16 different operating states. Considering the relationship between every single inductor current and the total input current, these 16 states can be divided into the following four conditions in accordance with the duty cycle of IGBT. When 0<d<0.25, d_i=4d. When 0.25<d<0.5, d_i=4d-1. When 0.50<d<0.75, d_i=4d-2. When 0.75<d<1, d_i=4d-3. Where d is the duty cycle of IGBE; d_i is the duty cycle of total current.

The total current, exactly the output current of diode rectifier, can be obtained by adding the four inductor currents which are interleaved 90° with each other. The frequency of ripple current is three times higher than inductor ripple current, but the amplitude is much smaller. Obviously four-phase interleaved PFC can restrain the input ripple current better.

The increased value of L1 ripple current is the sum of decreased value of L2, L3, L4 ripple currents. Suppose that the inductance of L1, L2, L3 and L4 are equal to L. Switching period is T_s.

$$\Delta i_{L1} = u_{in}(t) \times 4d \times T_s / 4L \tag{3}$$

$$\Delta i_{L2} = \Delta i_{L3} = \Delta i_{L4} = (u_{in}(t) - U_o) \times 4d \times T_s / 4L \tag{4}$$

According to the equations (3) and (4), when 0<d<0.25, 0.25<d<0.5, 0.5<d<0.75, 0.75<d<1.0, total ripple current peak-peak values Δi_{total} are $T_s U_o(-4d^2 + d)/L$, $T_s U_o(-8d^2 + 6d - 1)/2L$, $T_s U_o(-8d^2 + 10d - 3)/2L$, $T_s U_o(-4d^2 + 7d - 3)/L$ respectively. Obviously, the ripple current of interleaved PFC is less than single-phase PFC. When d＝0.25, 0.5 or 0.75, the ripple current is reduced to zero. When d＝0.125, 0.375 or 0.625, the ripple current reaches the maximum value.

Current synthesis. In the traditional PFC scheme, PWM signals are generated by the calculation of current loop which can sampling current directly. In the interleaved PFC scheme, due to the components parameters' differences and layout diversity, using the traditional method may cause current unbalance. Therefore, the signal used by current loop should be sampled from every single inductor current not the total current. Meanwhile, it increases the complexity of current sensing circuit. This paper uses the calculation method to construct the inductor current according to the sensed IGBT current.

Inductor current can be seen as the sum of IGBT current and FRD current. When IGBT is turned on, inductor current is equal to IGBT current which can be sensed by current transformer. When IGBT is turned off, inductor current is equal to FRD current which can be calculated by equation: $di_L/dt=(u_{in}-U_o)/L$, where u_{in} and U_o are diode rectifier output voltage and output voltage respectively. Since the switch frequency is very high, diode rectifier output voltage and output voltage can be seen as constants in a switching period. The slope of FRD current can be described as $(u_{in}-U_o)/L$. According to sampled IGBT current at the falling edge of PWM, FRD current can be calculated. As a result, inductor current can be obtained too.

Simulation analysis and experimental result

Simulation analysis. In the simulation, the parameters' values are listed as follows: input voltage U_{in} is 220V AC, Output voltage U_o is 390V DC, switch frequency f_s is 40kHz, inductance is 0.5mH.The simulation fully realizes the function of four-phase interleaved PFC and has a good effect on current balance. The average value of output voltage is 390V, and the peak-peak value of output ripple voltage is 25V. The curves in Fig.4 show the input voltage and current. Obviously they have almost the same shape. Point A, B and C represent the working point when the duty cycle is 0.75, 0.5 and 0.25. They prove that the ripple current is reaching zero at these times mentioned above.

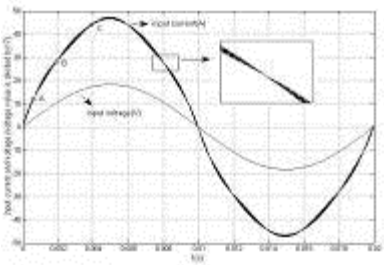

Fig.4 Simulated waveforms of voltage and current at main side

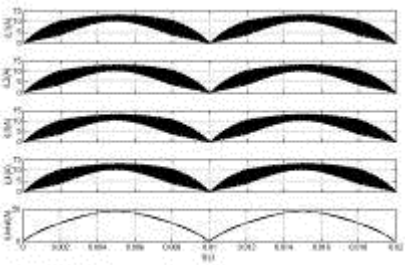

Fig.5 Inductor currents and total current

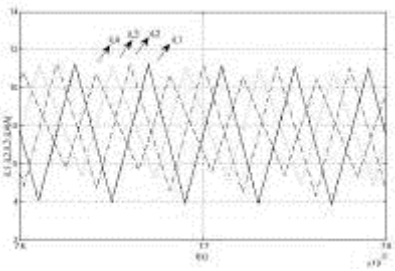

Fig. 6 Inductor currents with parameters mismatched

As is shown in Fig.5, the total ripple current is much less than every single inductor current which proves that the four-phase interleaved topology can reduce the input ripple current greatly and simplify the design of inductor. However, in a real system it is not possible to ensure the parameters' values are always the same. Therefore, to test the robustness of the proposed scheme, the next results considering parametric variation as follow: L_1, L_2, L_3, L_4 are 0.3mH, 0.5mH, 0.6mH, 0.7mH respectively. As is shown in Fig.6, the simulation result shows the control method employed by this paper has a good current sharing effect.

Experimental results. In order to verify the simulation analysis, a four-phase interleaved PFC experiment is implemented by means of using two analogy control chips, every one of which can control two-phase interleaved PFC. The rated input voltage of system is 220VAC. The range of input voltage is from 170VAC to 265VAC (mono phase 47~63Hz). The rated output voltage is 390V without load. The output power is 8.0kW. Ferrite material inductors whose inductance is 350μH are designed by using JMAG and integrated magnetic technology. IGBTs are RJH60F7ADPK: 50A/100°C/600V. FRDs are SiC CSD20060D: 20A/150°C/600V.

After testing, the overall efficiency of PFC is more than 0.95 with a wide range of load and can reach 0.98 when load is rated. Fig.7 and Fig.8 show the waveforms of input current with the different load. Both the curves have the same shape with input voltage, and the power factor can reach 0.98. The curve in Fig.7 is input current with load of 3.5kW. The curve in Fig.8 is input current with load of 8.0kW. When the single phase current is less than 16A, the harmonic current limitation standard is IEC61000-3-2[3]. Using FLUKE43 to analysis the harmonics, the 17th and 19th harmonic current is a little higher due to de distortion of input voltage. When the single phase current is more than 16A and less than 75A, the harmonic current limitation standard is IEC61000-3-12. Harmonic contents have a relationship with minimum Rsce and the THD, PWHD requirements is looser relatively. As a result, it is easily to satisfy the IEC61000-3-12 standard.

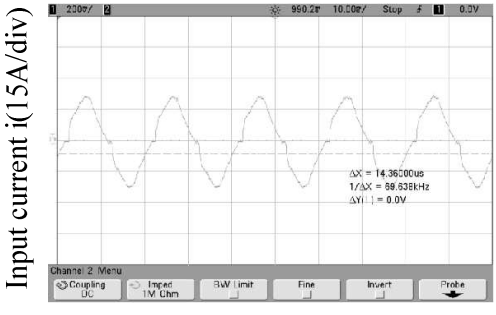

Fig.7 Input current with load of 3.5kW

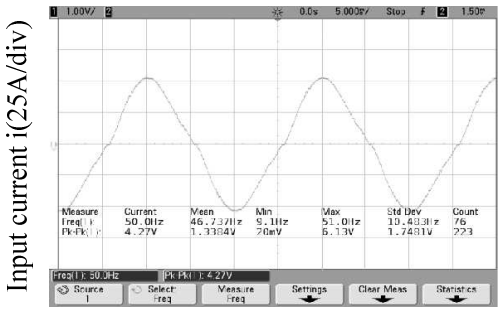

Fig.8 Input current with load of 8.0kW

Conclusions

This paper describes the one cycle control principle, current synthesis method and the relationship between ripple current and duty cycle of IGBT. Simulation by using MATLAB/SIMULINK and experiment based on R2A20104 are implemented to prove the validity of proposed scheme. The result shows interleaved PFC employing control method mentioned above can support the high

output power, simplify the design of inductor and reduce the ripple current of electrolytic capacitor. Although, the harmonic current can meet the requirements of IEC6100-3-2 and IEC6100-3-12, in the condition of light load, three times harmonic current takes a great proportion. Selection of electrolytic capacitor has no relationship with switch frequency. However, when the power loss is to be calculated, the ESR and switch frequency should be considered. The scheme is applicable for not only the power electronic transformer in smart grid but also the high power air conditioning installations.

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References

[1] M． Kang, P.N. Enjeti and I.J. Pitel． IEEE Trans on Power Electronics, 1999, 14(6): 1133～1141．
[2] M．Kang．Analysis and design of electronic transformers for electric power distribution and utility interface of power electronic systems．TEXAS A&M University,2000．
[3] Electromagnetic Compatibility. Part 3: Limits—Sect. 2: Limits for Harmonic Current Emission (Equipment Input Current @ 16 A Per Phase), IEC 1000-3-2, 1995.
[4] Shuo Wang, F. C. Lee and W.G. Applied Power Electronics Conference and Exposition, 2003, pp.368 - 374.
[5] Leopoldo Rossetto, Simone Buso and Giorgio Spiazzi. IEEE Trans, power electron, vol.36, no.2, pp. 578 – 585,Aug.2002.
[6] Thomas Nussbaumer, Johann W. Kolar. IEEE Trans, power electron, vol.56, no.7, pp. 2559 – 2573, July 2009.
[7] Fernando Beltrame, Leandro Roggia, Luciano Schuch, José Renes Pinheiro. 2010 IEEE International Conference on Industrial Technology, pp. 625 – 630.
[8] José R. Pinheiro, Hilton A.Gründling, Dalton L.R.Vidor and José E Baggio. Power Electronics Specialists Conference, 1999. PESC 99. 30th Annual IEEE, pp. 137 – 142.
[9] Daniel Kübrich, Markus Schmid, Thomas Dürbaum. The 31st Annual Conference of IEEE Industrial Electronics Society, Nov. 2005, pp.900-905.

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