Down to 2 nm Ultra Shallow Junctions : Fabrication by IBS Plasma Immersion Ion Implantation Prototype PULSION®

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Abstract. Classical beam line implantation is limited in low energies and cannot achieve P+/N junctions requirements for <45nm node. Compared to conventional beam line ion implantation, limited to a minimum of about 200 eV, the efficiency of Plasma Immersion Ion Implantation (PIII) is no more to prove for the realization of Ultra Shallow Junctions (USJ) in semiconductor applications: this technique allows to get ultimate shallow profiles (as implanted) thanks to no lower limitation of energy and offers high dose rate. In the field of the European consortium NANOCMOS, Ultra Shallow Junctions implanted on a semi-industrial PIII prototype (PULSION®) designed by the French company IBS, have been studied. Ultra shallow junctions implanted with BF_3 at acceleration voltages down to 20V were realized. Contamination level, homogeneity and depth profile are studied. The SIMS profiles obtained show the capability to make ultra shallow profiles (as implanted) down to 2nm.

Keywords: Plasma Immersion Ion Implantation (PIII), Ultra Shallow Junctions (USJ).
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INTRODUCTION

Due to constant shrinking of sizes in CMOS fabrication, junction depth requirements for Source / drain extension doping is more and more difficult to achieve. For bulk MPU ASICS, ITRS roadmap 2005 [1] imposes junction depth as low as 6.5nm for 45 nm node and 4.5 nm for 36 nm node. As Classical beam line implanters are reaching there limits for these specifications, Plasma Immersion Ion Implantation (PIII) or Plasma Doping (PLAD) has been proved as a possible solution for some years now [2-18]. The French Company IBS has developed its own PIII machine, named PULSION®, based on a original, simple and robust working mode. This machine has been tested for 45 nm CMOS application within the European project NANOCMOS. Metallic Contamination, homogeneity and demonstration of extremely shallow doped layers are presented bellow.

MACHINE DESCRIPTION

The structure of PULSION® is described in figure 1. The pulsed plasma is created thanks to a self designed ICP source located above a vacuum chamber.

Wafer is located on a chuck at the bottom of the chamber. The chuck is polarized through a capacitor and thanks to a current source (High voltage capacitor charging system). To improve uniformity on large substrates, the substrate holder rotates under the non centered plasma source. To avoid metallic contamination, the chamber is in aluminum alloy, plasma source in quartz with an external antenna and substrate holder is coated with a thick silicon coating.

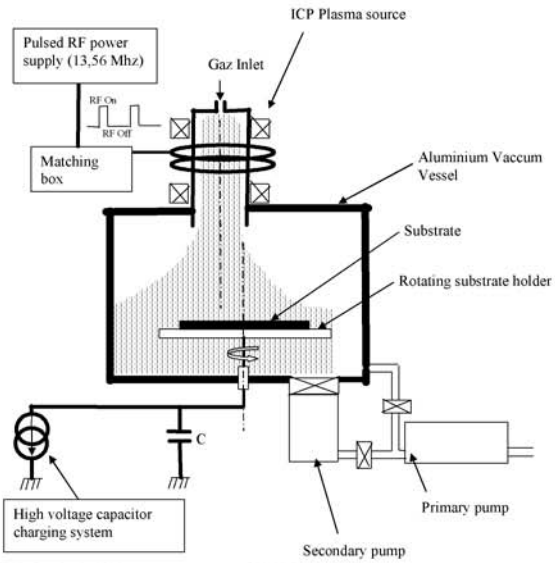

FIGURE 1. Machine structure of PULSION®

CP866, *Ion Implantation Technology*,
edited by K. J. Kirkby, R. Gwilliam, A. Smith, and D. Chivers

Polarization modes

PULSION® can work under two polarisation modes:

- **Mode 1**: pulsed plasma & constant polarisation voltage. This polarisation mode is very robust and easy to control. Acceleration voltage is kept constant thanks to the use of a big capacitor (> 1µF). Pulsed plasma offers the possibility to reduce thermal budget, etching and contamination. The efficiency of this mode has been proved on blank wafer [19]. Nevertheless, when an insulating layer is deposited on the wafer, charging problems occur. To avoid this drawback a new polarisation mode has been developed and patented.
- **Mode 2**: pulsed plasma and "self pulsed" acceleration voltage. The principle of this mode is the following:

  1 – phase 1: plasma is off and the power supply charges the capacitor up to the desired acceleration voltage.

  2 –phase 2: the power supply is inhibited when the plasma is ON. As the capacitor discharges, an implantation "pulse" occurs and the substrate voltage drops to 0V at the end of plasma pulse. Then plasma electrons are attracted towards the substrate and then can neutralize the positive charges accumulated on the substrate surface.

  3 – Then, plasma is off again, and power supply inhibition is switched off to allow a new capacitor charging cycle….etc.

The capacitor value must be small to allow a rapid drop of the voltage and no irremediable charging problems.

The mode 2 has been proved to be compatible with real patterned wafers containing resists and oxides. It is used in all the following experiments.

CONTAMINATION STUDIES

Metallic contamination was checked by ToF SIMS on 200mm implanted wafers (PULSION® BF_3, 500V) and compared with the ITRS 2005 specification values. Results are presented on Figure 2. Except from Cu and Ni, the levels are all under the ITRS specifications. These results are good considering that the machine has no liner yet, and should be considerably improved soon by the setting up of a liner. Moreover, it appears that contamination at the center of the wafer is less important than at the edge, which indicates that major source of contamination may come from the substrate holder. For this reason, a new substrate holder is also under development to cope with this problem.

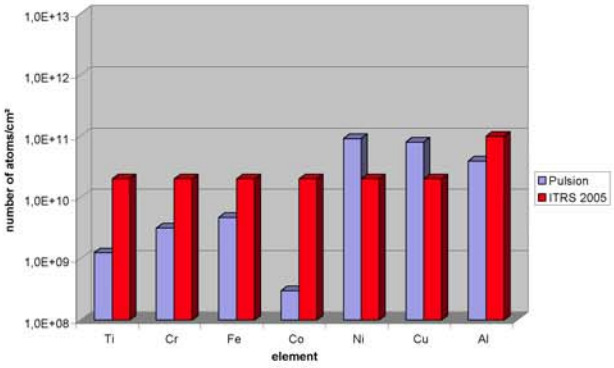

FIGURE 2. Metallic contamination level: ToF Sims analysis of a BF_3 500V implanted sample. Values (in atome/cm²) are measured at the center of the sample.

HOMOGENEITY

A non homogeneity of 3.5% on 200mm wafers implanted with PULSION® (BF_3, 500V, 1E15/cm²), activated using spike anneal (1050°C) and measured using four point probe has already been presented [20]. In the present paper, we have chosen to study non homogeneity on 200mm wafers (PULSION®, 500V, 5E15/cm²) using CAMECA LEXES tool, which allows measurement on as-implanted wafers, in such a way that we suppress possible non homogeneity due to the annealing process. Figure 3 presents the mapping obtained. As we can see on this figure, the non homogeneity looks good except from the wafer edge. Then, when we compare the implanted wafer mapping to a blank wafer mapping (see figure 4), we notice that this effect is mainly due to native oxide masking.

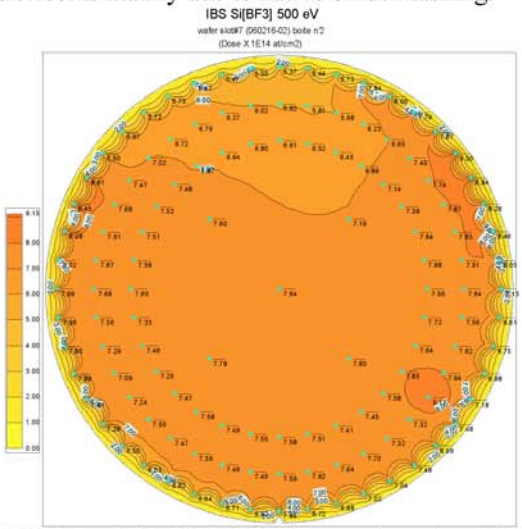

FIGURE 3. CAMECA LEXES mapping of a 200 mm wafer implanted with PULSION® using 500V polarisation voltage. Measured non homogeneity: 5%, but LEXES non reproducibility : 3.7%.

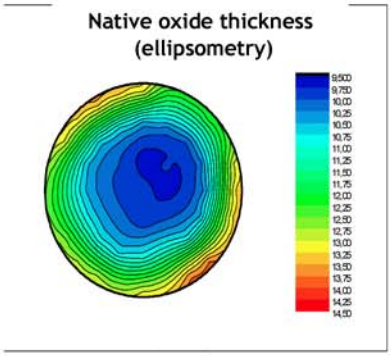

FIGURE 4. Mapping of a 200mm blank wafer measured by ellispometry at SEMILAB.

DOPING PROFILES

The measurement of implantation profile using dynamic SIMS has to be considered carefully when the ion used for the analysis (Oxygen or Cesium) has an incident energy higher than the one used to accelerate the studied specie (Boron) in the ion implanter. Indeed, due to recoil effect during SIMS analysis, the implantation depth can be bigger after analysis than the initial one.

We have started collaboration with CAMECA to use their last generation of dynamic SIMS (7F version) to characterize USJ implanted down to extremely low energies (PULSION® BF_3 from 2kV to 20V). The interest of this tool is its ability to work down to 300eV in positive mode with O_2^+ duoplasmatron source and down to 500eV in positive mode with Cs microbeam source using Cesium clusters (MCs^+ and MCs_2^+). Boron and Aluminium profiles were analysed using Oxygen beam, Fluorine profile was analysed using Cesium.

Boron profiles

The Boron profiles obtained are presented on figure 5: from 2kV to 500V, the implantation depth at 1E18/cm3 is proportional to the acceleration voltage (see figure 6). When the acceleration voltage is lower than 100V, there is no difference between the profiles due to the lack of sensitivity of SIMS at very low energy, as explained before. Recently, ToF SIMS has succeeded in separating these profiles.

Nevertheless, the possibility to implant Boron in extremely shallow layers (down to 2 nm at 1E18/cm^3) using PULSION® has been demonstrated.

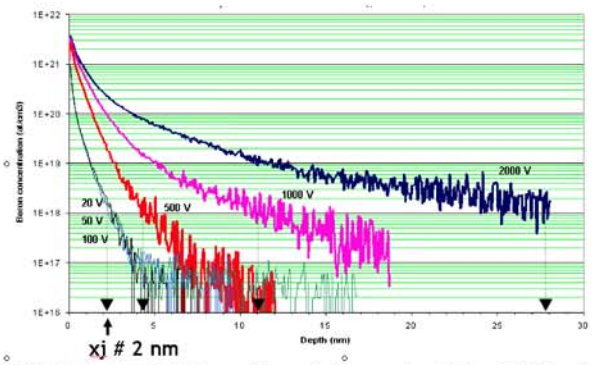

FIGURE 5. SIMS profiles of Boron for BF_3, 1E15/cm² PULSION® implantations from 20V to 2000V acceleration voltage.

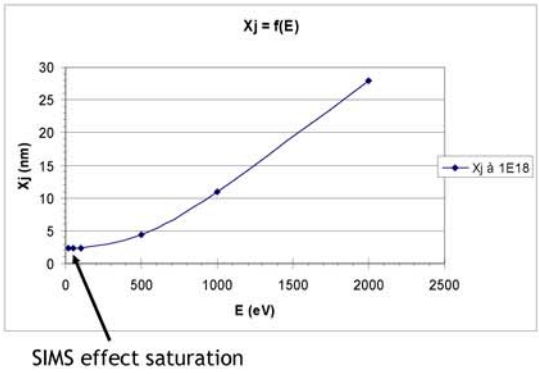

FIGURE 6. Implantation depth (at 1E18/cm3) as a function of acceleration voltage for BF_3, 1E15/cm² PULSION® implantations.

Fluorine profile

SIMS profiles of Fluorine were obtained using Cs at 400eV and 700eV depending on implantation depth.

An example of Fluorine profile compared with Boron one is showed in figure 7. As expected with a plasma which contains mainly BF_2^+ ions, Fluorine profile is almost superposed with Boron one. Figure 7 also shows Aluminium contamination profile, confirming the contamination level of 0.7% measured by ToF SIMS .

F/B ratio has been calculated from SIMS profiles integration. It varies from 2.5 to 3.5 for acceleration voltages higher than 500 V and is around 8 for lower voltages (see fig 8). F/B ratio was also measured on a sample after a thermal treatment of 750°C during 20s: exodiffusion of Fluorine is observed with a reduction of F/B ratio from 3.5 as implanted to 2 after annealing.

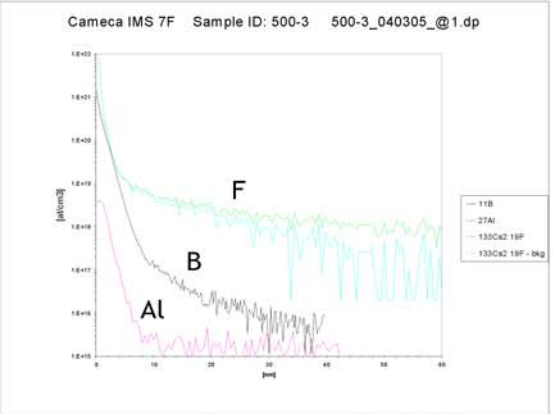

FIGURE 7. Fluorine, Boron and Aluminium profiles obtained by SIMS for BF_3, 1E15/cm², 500V PULSION® implantation

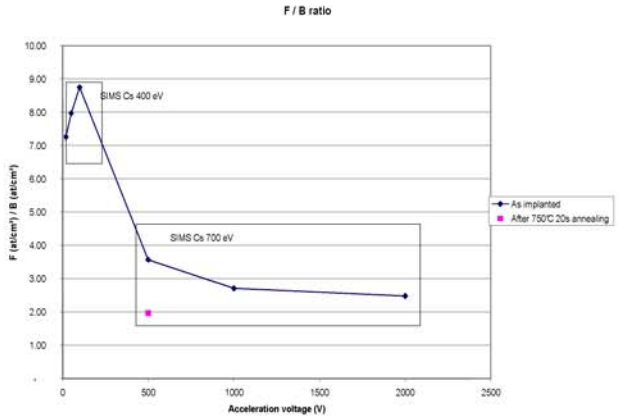

FIGURE 8. F/B ratio as a function of acceleration voltage for a sample as implanted and after thermal treatment samples.

IMPLANTATION DEFECTS

Implantation defects were studied using TEM observation on a PULSION® BF_3, 500V, 1E15/cm² as implanted sample. The TEM picture is presented in figure 9. As one can see no defect is observed under the native oxide layer (about 2 nm) even if the SIMS analysis gives an implantation depth of 5 nm for 1E18/cm^3 and 10 nm for 1E16/cm^3. It seems that for this sample, that was not etched before implantation to suppress native oxide, most of the energy was deposited within the native oxide, thus the amorphous layer is in the native oxide layer. And even if there are some Boron atoms under the native oxide layer, we can notice the absence of end of range defect, which is likely to be of great interest for the post activation process and for the final device electrical characteristics.

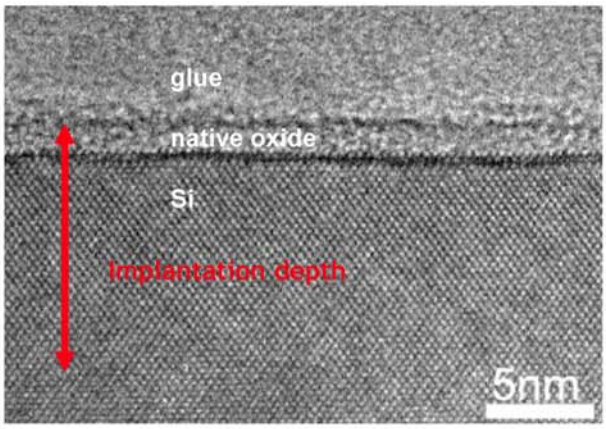

FIGURE 9. TEM picture of a PULSION® BF_3 500V 1E15/cm^2 as implanted sample.

CONCLUSION

The possibility to make PIII with a simple polarisation system avoiding any high voltage switching system has been demonstrated. A prototype named PULSION®, which allows implantation on wafers up to 300mm wafers was built. We have demonstrated that this machine was able to make Boron Ultra Shallow Junctions down to 2 nm using BF_3 and acceleration voltages down to 20V. Despite the fact that we are reaching the limits of all characterization systems, non uniformity on 200mm and 300mm has been measured on very shallow implanted layers and arises native oxide masking and edge effects, but it could be acceptable, if we take into account the high non reproducibility of the measurement and the improvements that have to be made. Then, metallic contamination is going to be improved by the setting up of a liner in the chamber and the development of a new substrate holder in order to decrease Ni and Cu levels and to be CMOS compatible. Finally, even if Boron and Fluorine concentrations at the surface of the silicium are important, no crystal defect was observed by TEM under the native oxide layer.

The next step of this study is the fabrication of a real alpha test machine scheduled to be located at LETI in 2007 thanks to the European integrated project SEA-NET.

ACKNOWLEDGMENTS

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