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Oxidation process by RTP for 4H-SiC MOSFET gate fabrication

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Keywords: MOSFET, oxidation, nitridation, RTP, N_2O, H_2 surface pre-treatment.

Abstract. Rapid Thermal Processing (RTP) has been evaluated as an alternative to the conventional furnace process for the gate oxide formation of SiC lateral MOSFETs. We show that this innovative oxidation method has not only the advantage to significantly reduce the thermal budget compared to classical oxidation, but also produces a significant improvement of MOSFET performance when using N_2O as oxidizing gas. Studying different surface preparation before gate oxidation, we demonstrate that *in-situ* surface preparation by H_2 annealing increases considerably the channel mobility and also the electrical stability with respect to constant bias stress at low-field.

Introduction

The 4H-SiC power MOSFET is one of the most promising candidates for high power electric device applications in the next generation. However, inversion channel mobility in 4H-SiC MOSFETs is still far below the value of its bulk electron mobility. The main reason is that the high density of defects encountered at the SiO_2/SiC interface results in charge trapping and Coulomb scattering. Therefore, a suitable oxidation processing technology is a critical issue for the reduction of the specific on-state resistance (R_{on}) in SiC power MOSFETs.

Toward this end, different passivation methods have been studied. The most effective one involves nitridation processes, using either nitric oxide (NO) or nitrous oxide (N_2O) gases. Indeed, MOS devices with oxides grown in N_2O exhibit superior performance and reliability compared to those with oxides grown in O_2 [1] with respect to constant current stress [2, 3]. But the threshold voltage stability of MOSFET with these kinds of oxides is influenced by low-field bias, even at room temperature, for lateral channels [4] as well as vertical channels [5]. Moreover, the main drawback of such nitridation techniques is that applied to SiC thermal oxidation, require a huge thermal budget in conventional furnaces [6]. Instead by rapid thermal processing (RTP) when using high energetic photons as the source of thermal and optical energies, we have already shown that the oxide growth is one or two orders of magnitude faster [7]. Also, the resulting dielectrics exhibit a reduced effective charge and a less defective interface compared to oxides grown by classical N_2O oxidation [7, 8].

In this paper, we have evaluated the use of a RTP furnace for gate oxide formation in N_2O of SiC lateral MOSFETs, and also the electrical stability of the processed devices.

Experiment

The n-MOSFET devices were fabricated on 10 µm p-type epitaxial layers with a doping concentration of 5×10^{16} cm^{-3} grown on 8° off-axis Si-face n-type 4H-SiC substrates. The source and drain n^+-regions were formed by selectively nitrogen implantation and subsequently annealed at 1600°C in Ar atmosphere for 30 min. For all the processed wafers, the RTP thermal oxidation was done in 100% N_2O at 1050°C for 10 min, resulting in an average oxide thickness of 45 nm. Then, a rapid post-oxidation annealing (RTA) step was performed under Ar during 3 min *in-situ* when cooling the system down to 800 C.

Two types of MOSFET's have bee
gate-oxidation:
- Wafer #1 was treated by O_2 plasma
- Wafer #2 was *in-situ* pre-annealed
oxidation in a RTP chamber.
The total processing time for the MO
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drain contact windows, nickel and a

Results and discussion

Fig. 1 shows typical $I_{ds}(V_{gs})$ and I_{ds}
W = 150 µm fabricated on the 2 wa
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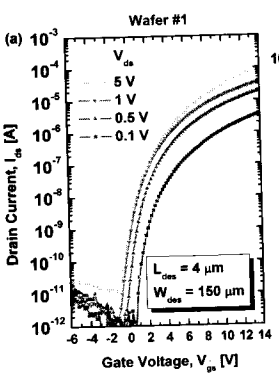

Fig. 1. Electrical characteristics of 4
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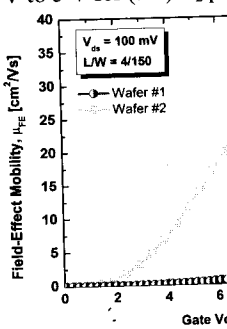

Fig. 2. Field-effect mobility of 4H
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From these results, it appe
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Two types of MOSFET's have been fabricated with varying surface preparation just before the gate-oxidation:
- Wafer #1 was treated by O_2 plasma in a Reactive Ion Etching chamber.
- Wafer #2 was *in-situ* pre-annealed (passivated/etched) under H_2 at 800 °C for 3 min before gate-oxidation in a RTP chamber.

The total processing time for the MOSFET gate fabrication was only about 30 min when combining *in-situ* a rapid hydrogen annealing as pre-cleaning (wafer #2). Finally, after definition of source and drain contact windows, nickel and aluminium were deposited by sputtering and patterned by lift-off.

Results and discussion

Fig. 1 shows typical $I_{ds}(V_{gs})$ and $I_{ds}(V_{ds})$ characteristics of 4H-SiC MOSFETs with L_{des} = 4 µm and W = 150 µm fabricated on the 2 wafers. It can be seen that MOSFET devices with H_2 surface pre-treatment (wafer #2) exhibit better performance compared to devices with surface prepared using O_2 plasma cleaning (wafer #1). The extracted field-effect mobility (μ_{FE}) from the transfer curves is shown in Fig. 2 for the two wafers. High channel mobility ~ 32 $cm^2/V.s$ was obtained when using H_2 surface pre-treatment (wafer #2), which is much higher than for the MOSFETs on wafers pre-cleaned by O_2 plasma (wafer #1), and comparable to the best devices found in the literature [9, 10].

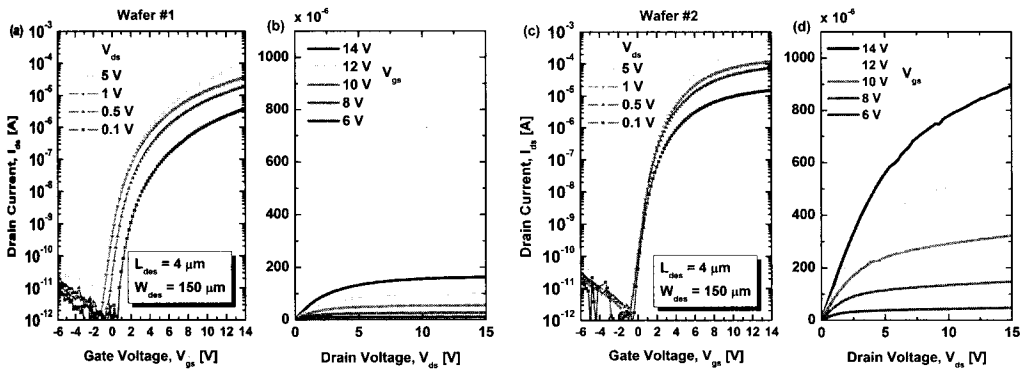

Fig. 1. Electrical characteristics of 4H-SiC MOSFETs with L_{des} = 4 µm and W = 150 µm at V_{ds} varied from 0.1 V to 5 V for (a-b) O_2 plasma treatment before oxidation and (c-d) H_2 RTA treatment prior to oxidation.

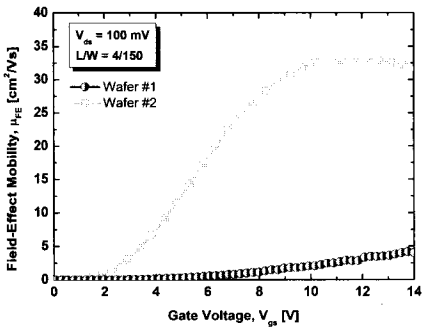

Fig. 2. Field-effect mobility of 4H-SiC MOSFETs with L_{des} = 4 µm and W = 150 µm for O_2 plasma treatment and H_2 annealing before oxidation.

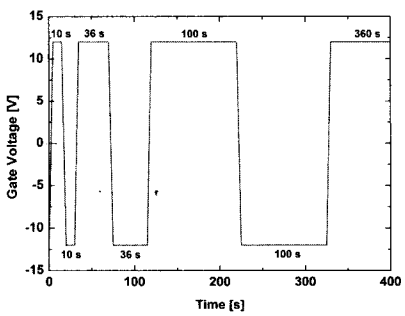

Fig. 3. Measurement sequence for the threshold-voltage instability measurement for a bias stress of ± 12 V.

From these results, it appears that the native oxide as well as metal contaminants on SiC surface are reduced more efficiently by *in situ* cleaning in H_2 ambient compared to O_2 plasma cleaning. Then, once the 4H-SiC surface has been properly hydrogenated, there are less initial defects for the oxidation process to take place. The oxidation proceeds through a reasonably clean

interface layer. As a result, the traps coming from the interface layer are more efficiently passivated by the creation of deep C-N and Si-N bonds.

In order to examine the electrical stability of the MOSFET devices integrating gate oxide grown by RTP, the influence of a prolonged gate bias of ± 12 V on the threshold voltage and drain current was investigated for MOSFETs with gate dimension of L/W = 12/150 μm. A typical cycle used for the bias-stress induced instability measurements is shown in Fig. 3 [4]. It consists in four different gate biasing steps for each stress time. The gate bias was interrupted at fixed times to record the transfer characteristics of the transistor at a drain bias of 100 mV by sweeping the gate bias, while the source electrode was grounded.

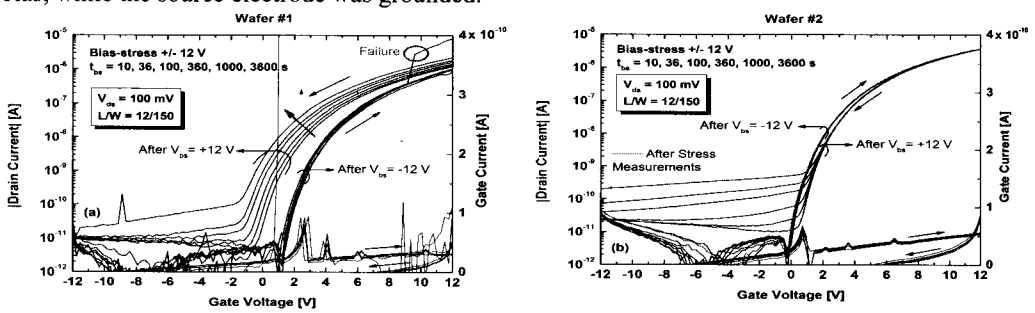

Fig. 4. $I_{ds}(V_{gs})$ curves of a 4H-SiC lateral MOSFET with L_{des} = 12 μm and W = 150 μm, as a function of stress time (t_{bs}) for (a) O_2 plasma treatment before oxidation (wafer #1) and (b) H_2 annealing treatment prior to oxidation (wafer #2).

Fig. 4 illustrates the transfer characteristics variation of 4H-SiC MOSFETs fabricated on the 2 wafers, as a function of the stress time, for a constant bias stress of ±12 V. For wafer #1, the $I_{ds}(V_{gs})$ characteristics obtained after positive bias-stress (the sweep-down step) exhibit higher drain currents than those obtained after the corresponding negative bias-stress (the sweep-up step). Then, by increasing positive bias-stress time, the drain current shift increases significantly leading to the failure of the device. Instead, by increasing negative bias-stress time, no larger increase of the drain current is observed and, the negative bias-stress always restores the drain current close to its original value. For wafer #1, the $I_{ds}(V_{gs})$ curves shifted in the opposite direction to that expected in response to the applied bias stress as the bias stress increases: a positive bias stress causes a negative shift and a negative bias stress causes a low positive shift. This was likely due to mobile ions being present [4].

In contrast, for wafer #2 the positive bias-stress yields lower drain currents compared to those obtained after the corresponding negative bias-stress. A positive bias stress causes a positive shift in the $I_{ds}(V_{gs})$ curves with an almost constant shape (but also, an increase of the leakage current), while for a negative bias stress, the curves hardly move from the initial one. Moreover, the sub-threshold slope of the curves does not show a large variation during the applied bias stresses, which indicates that the shift can be mainly described by the threshold voltage shift ΔV_{th} without mobility degradation. This demonstrates that for wafer #2, the creation of electron trapping states in the interface of active and dielectric layers by gate bias stressing is negligible (contrary to wafer #1) and, that ΔV_{th} is primarily due to trapping of electrons in the traps located in the interface or bulk dielectric layer and, results in a significant enhancement of the gate induced drain leakage current.

Typical threshold voltage shift (ΔV_{th}) values measured on the 4H-SiC MOSFETs as a function of stress time under different gate bias stress are shown in Fig. 5 for the 2 wafers. It shows that for MOSFETs on wafers pre-cleaned by O_2 plasma (wafer #1), by increasing positive bias-stress duration, threshold voltage shift (ΔV_{th}) increases and its magnitude becomes more negative. Instead, MOSFET devices with H_2 surface pre-treatment (wafer #2) exhibit low positive ΔV_{th}'s comparable to the best state of the art [4]. Based on these results, it demonstrates the benefit action of the *in-situ* surface preparation by hydrogen annealing before oxidation with respect to constant bias stress at low-field.

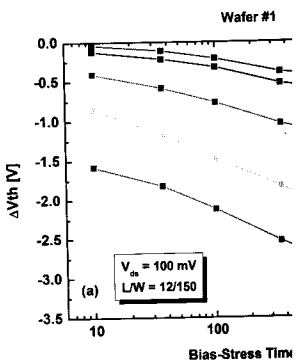

Fig. 5. Time dependence of ΔV
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Summary

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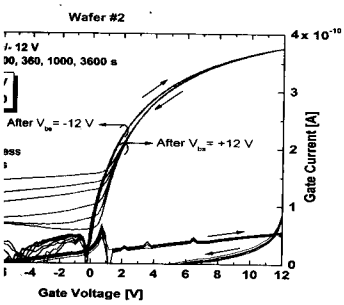

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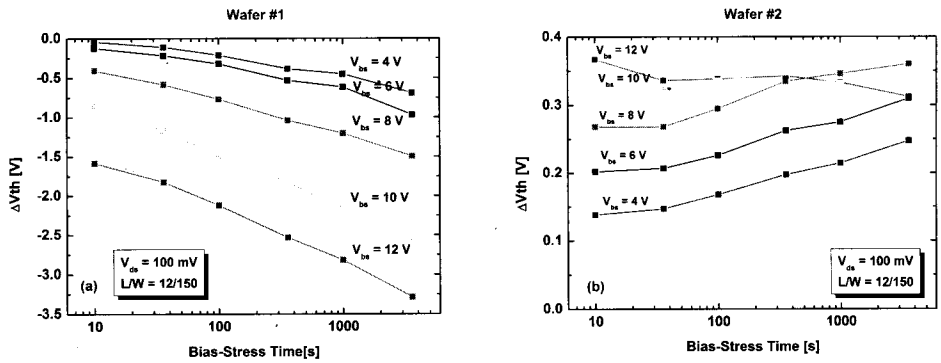

Fig. 5. Time dependence of ΔVth under different gate bias stress for (a) O_2 plasma treatment before oxidation (wafer #1) and (b) H_2 annealing treatment prior to oxidation (wafer #2).

Summary

N-channel enhancement MOSFETs have been fabricated on 4H-SiC using a gate oxide process based on oxynitridation in 100% N_2O by RTP. This process has not only the advantage to reduce the thermal budget compared to classical oxidation, but also produces a significant improvement of MOSFET performance, especially when *in-situ* surface preparation by H_2 annealing is performed. Indeed, a considerable increase of the electron channel mobility is observed as well as a significant reduction of the threshold voltage and drain current instability. All together this makes our SiC MOSFETs in the state of the art when taking into account all the critical parameters for MOSFET power electronics industry: mobility and reliability.

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