Journal of The Electrochemical Society, **157** (2) H174-H177 (2010)
0013-4651/2009/157(2)/H174/4/$28.00 © The Electrochemical Society

Fabrication of Nanometer-Scale Si Field Emitters Using Self-Assembled Ge Nanomasks

Sheng-Wei Lee,[*,z] Bo-Lun Wu, and Hung-Tai Chang

Institute of Materials Science and Engineering, National Central University, Jhong-Li 32001, Taiwan

Large-area, nanometer-scale Si field emitters have been fabricated by selective chemical etching of self-assembled Ge islands on Si. Taking advantage of the relatively low etching rate, uniform Ge islands act as virtual nanomasks for the underlying Si substrate. During selective chemical etching, Ge nanomasks shrink into small Ge-core islands, which determine the apex sharpness of the resulting Si pyramidal tips. The results demonstrate that Si pyramidal tips exhibited improved antireflective and electron field emission characteristics compared to as-grown Ge islands. The high field enhancement factor can be attributed to high tip density, nanoscale apex, and well-controlled spacing between Si pyramidal tips. This work offers a low cost alternative for designing and fabricating high efficiency Si-based field emitters or nanodevices.
© 2009 The Electrochemical Society. [DOI: 10.1149/1.3267512] All rights reserved.

Manuscript submitted May 19, 2009; revised manuscript received November 2, 2009. Published December 9, 2009.

In recent years, intensive research efforts have been devoted to the design and fabrication of Si-based field emitters in pursuit of a new generation of flat panel displays and vacuum microelectronic devices.[1-3] Sharp field emitters are highly desirable because an electron emission strongly depends on the electric field, and the electric field scales with emitter sharpness.[4] Processes typically use wet chemical etching with an oxide pattern mask to control the shape of the Si tips or pyramids, but in micrometer sizes.[5,6] Several approaches have been used to fabricate nanometer-scale Si tips or pyramids. An electron-beam lithography combined with etching can define features down to sub-10 nm,[7] but the cost is high and the throughput is low. A nanoimprint lithography is a possible choice, but it requires a reliable mold which has a low fabrication cost and a long lifetime.[8] A nanosphere lithography, which exploits a self-organized, order, and close-packed sphere array as a deposition or etching mask, is an effective method for the fabrication of periodic nanostructures.[9] Nevertheless, it usually requires a combination of other techniques, such as reactive ion etching[10] or metal deposition[11] to realize the fabrication of the designed structures.

With a moderate lattice mismatch (4.2%), Ge/Si has emerged as a model system for the fabrication and investigation of nanometer-scale heteroepitaxy.[12-14] Recently, Tondare et al. reported the feasibility of using the self-assembled Ge islands on Si(111)-7 × 7 as field emitters.[15] In the previous study, we also demonstrated the improved field emission properties in Si-capped Ge islands.[16] This work, taking advantage of the relatively low etching rate and uniform size of self-assembled Ge islands, proposes a low cost method to fabricate nanoscale Si field emitters over a large area. The self-assembled Ge islands act as virtual nanomasks for the underlying Si substrate during selective chemical etching. The resulting Si pyramidal tips have an average height and base width of 47 and 95 nm, respectively. The density of Si pyramidal tips is as high as 8 × 10^9 cm^{-2}. Furthermore, these Si pyramidal tips exhibit improved antireflective and field emission characteristics. The fabrication process is compatible with the existing Si/SiGe-based device technology.

Experimental

p-Type (001)-oriented Si wafers (10–25 Ω cm, 150 mm diameter) were used in the present study. All Ge-island samples were grown at 600°C in a multiwafer ultrahigh vacuum chemical vapor deposition (UHV/CVD) system under a base pressure of 5 × 10^{-9} Torr. Pure SiH_4 and GeH_4 were used as precursors. Both gas flow rates were kept at 100 sccm. The growth rates for Si and Ge are 0.03 nm/s and 0.8 eq-ML/s, respectively. Note that the amount of Ge deposition is expressed in the unit of equivalent-monolayers (eq-ML, 1 eq-ML = 6.27 × 10^{14} Ge atom/cm^2). The Si wafers were dipped in a 10% HF solution to achieve the hydrogen-passivated surface, and then transferred into a UHV/CVD system. A 50 nm thick Si buffer layer was first grown to cover the wafer surface. After depositing the Si buffer, a Ge layer of 12 eq-ML was then deposited to form the self-assembled Ge islands via the Stranski-Krastanow (SK) mode.[17] Finally, the selective wet etching process was performed by dipping the as-grown samples in 50% aqueous tetramethylammonium hydroxide (TMAH) solutions at 50°C for various periods of time.

The surface topographies of the etched samples were analyzed ex situ by the atomic force microscopy (AFM) in a tapping mode. The transmission electron microscopy (TEM) was carried out with a JEOL 2100 TEM operating at 200 kV to reveal more detailed information about the microstructures of the etched samples. We also measured the total hemispherical reflectance spectra in air on a spectrophotometer with an integrating sphere (Hitachi U-4100, 350–850 nm) to characterize the surface morphologies after etching. The electron field emission properties were measured under a pressure of 1 × 10^{-7} Torr in a scanning-probe field emission system. A platinum sphere with a diameter of 1 mm was used as an anode to collect electrons from the samples. The measurement distances between the anode and the emitting surface were fixed at 30 μm. The measurements were repeated several times to obtain the stable and reproducible current-density–electric-field characteristics.

Results and Discussion

For the as-grown sample, Fig. 1a and b shows the well-known bimodal islands, pyramids with shallow {105} facets and domes with multiple steeper facets, which are commonly observed in high temperature depositions.[18] The island density is about 9 × 10^9 cm^{-2} and roughly 88% of the Ge islands are highly uniform domes. The Ge domes have an average diameter of 72 nm. Figure 1b-f illustrates the topographic evolution of the Ge islands during the selective chemical etching. When immersed in a 50% TMAH solution for 20 s, the morphology of the Ge islands remains almost unchanged (not shown here). The self-assembly of Ge islands on Si is known to develop in the SK growth mode, in which heteroepitaxial growth starts with the formation of a two-dimensional wetting layer followed by the nucleation of three-dimensional islands.[19] Therefore, a wetting layer of several monolayers is thought to exist on the Si surface. Such a thin wetting layer may act as a protective layer for the underlying Si substrate during the initial etching process. However, after etching for 30 s, the wetting layer surrounding the Ge islands started to be attacked by the etchant (see arrows in Fig. 1c). With 40 s immersion in 50% TMAH solution, the surface heights of the Ge islands increased significantly (Fig. 1d). The average diameter of the etched nanostructures increased slightly to 86 nm. As marked by a dotted line, it is evident that the apexes of etched structures exhibit a similar geometry to the as-grown Ge domes. At

* Electrochemical Society Active Member.
[z] E-mail: swlee@ncu.edu.tw

Downloaded 07 Feb 2010 to 159.226.100.225. Redistribution subject to ECS license or copyright; see http://www.ecsdl.org/terms_use.jsp

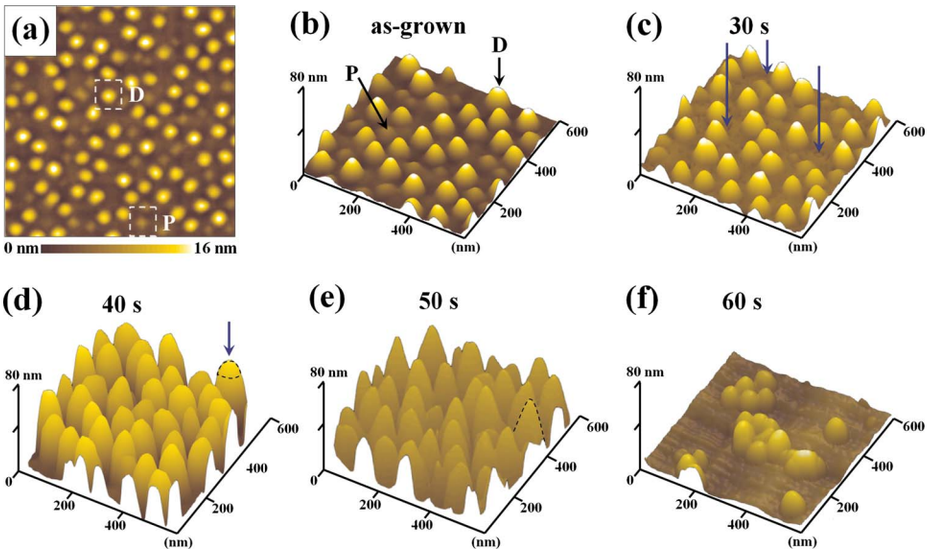

Figure 1. (Color online) AFM images (1×1 μm) of (a) as-grown Ge islands and three-dimensional view of Ge-island samples after etching for (b) 0, (c) 30, (d) 40, (e) 50, and (f) 60 s, respectively. Pyramid-like and domelike Ge islands in (a) and (b) are marked as P and D, respectively.

this stage, the monodisperse Ge islands act as nanomasks to prevent the underlying Si substrate from being etched. In the meantime, anisotropic etching proceeds quickly on the unmasked Si regions located in between the islands. After etching for 50 s, the etched nanostructures became sharper. It was speculated that the upper Ge islands were removed, leaving the Si pyramid-shaped nanostructures (pyramidal tips) on the surface, as shown in Fig. 1e. By the AFM cross-sectional analysis, the pyramidal tips are primarily bounded by {111} facets. The tip density is estimated to be about 8×10^9 cm^{-2}, very close to that of the as-grown Ge domes. These Si pyramidal tips have an average height and base diameter of 47 and 95 nm, respectively. The Si pyramidal tips are expected to exhibit improved field emission characteristics because they have a much higher aspect ratio compared to self-assembled Ge nanodots.[16] However, after further etching for 60 s, the Si pyramidal tips tended to shrink or even disappear, as shown in Fig. 1f.

Optical reflectance is a sensitive nondestructive method to examine the etched surface morphology. Figure 2 shows the optical reflection spectra with wavelengths from 300 to 850 nm for the as-grown and etched samples. The inset of Fig. 2 is a plot showing the variation in reflectance at 400 nm as a function of etching time. The reflectance decreased with the etching time and reached a minimum

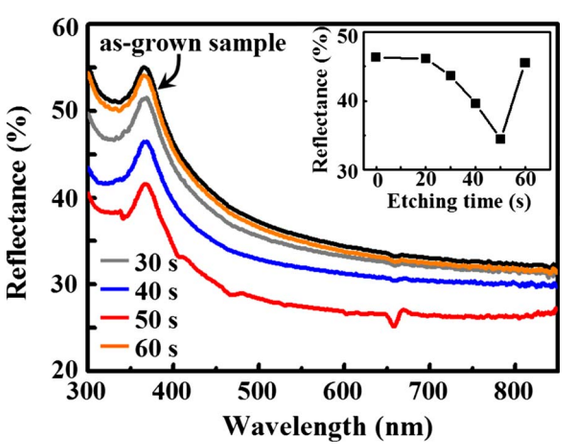

Figure 2. (Color online) Optical reflection spectra with wavelengths from 300 to 850 nm for the as-grown and etched samples measured at an incident angle of 5°. The inset shows the variation in reflectance at 400 nm as a function of etching time.

value as the Si pyramid tips formed (50 s in this case). The lower reflectance of the Si pyramid tips can be attributed to the highly roughened surface. However, after etching the sample for 60 s, the reflectance increases significantly. This result is consistent with the AFM observation that Si pyramidal tips disappear or smooth out with an overetching time. Recently, many techniques including laser-chemical[20] and metal-assisted chemical etching[21] have been reported to fabricate "black silicon" with an ultralow reflectance. Compared with black silicon, the reflectance of the Si pyramidal tips is still too high for photovoltaic applications. Nevertheless, this surface nanoroughening process could be an approach applied to other Si-based nanodevices, such as metal-oxide-Si tunneling diodes[22] or light-emitting diodes.[23]

The cross-sectional transmission electron microscopy (XTEM) images in Fig. 3 show the representative microstructures of the as-grown and etched samples. As shown in Fig. 3a, a typical multifaceted Ge island with a very thin wetting layer was observed in the as-grown sample. After etching for 40 s, the wetting layer was completely destroyed and anisotropic etching of the Si substrate occurred, resulting in a mushroomlike shape in Fig. 3b. The mushroomlike structure consists of an upper Ge island and an underlying sigma (Σ)-shaped Si pedestal. The Σ-shaped Si pedestal was produced by the anisotropic etching of Si sidewalls.[24] With further etching for 45 s, as seen in Fig. 3c, the heights of mushroomlike structures continue to increase. Meanwhile, the upper Ge islands apparently shrink. As reported previously, Ge islands usually suffer from serious Si–Ge intermixing during island growth. The Ge-rich area in the Ge islands exists as a core of the islands encapsulated by the intermixed phase.[25] Therefore, the outer parts of Ge islands are easily etched out during the process, leaving the smaller Ge-rich cores of islands on Si. As seen in the XTEM image, the dimension of Ge-core islands is an important parameter for determining the apex sharpness of the resulting structures. After etching the sample for 50 s, the Ge-core islands were removed, leaving the Si pyramidal tips on the Si substrate. As shown in Fig. 3d, the diameter of the apex of Si pyramidal tips is less than 20 nm. Eventually, after further etching for 60 s (Fig. 3e), the Si pyramids tended to smooth out, leading to an increase in reflectance. We also find that Ge-core islands are highly resistant to a TMAH etchant. Figure 4 gives an example of a freestanding Ge-core island, which was left on Si after 2 min of etching. It also indicates that Ge-core islands were not eroded away but lifted off from the Si pyramidal tips. In the present study, we use the AFM tips with a typical tip radius of less than 7 nm and a conical angle better than 25°, which is much smaller than the apex angle of the Si pyramidal tips. Therefore, tip-sample

Downloaded 07 Feb 2010 to 159.226.100.225. Redistribution subject to ECS license or copyright; see http://www.ecsdl.org/terms_use.jsp

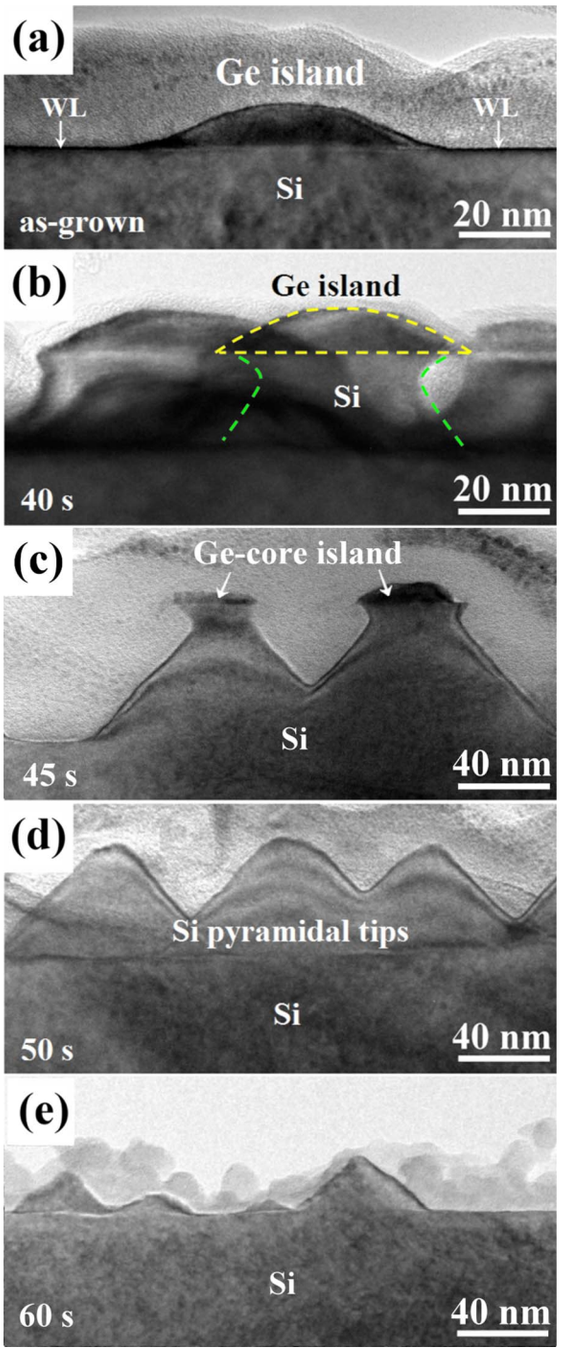

Figure 3. (Color online) XTEM images of (a) as-grown Ge islands on Si after etching for (b) 40, (c) 45, (d) 50, and (e) 60 s, respectively. Note that WL in (a) refers to the wetting layer and (c) and (d) were taken along ⟨010⟩ directions.

convolution effects can be largely neglected. Here, the inconsistency between AFM and XTEM images mainly occurs in those etched samples with a Σ-shaped Si pedestal, where AFM tips cannot access the re-entrant surface and thus display a distorted facet in imaging. Nevertheless, for the Si pyramidal tips, the AFM results, including pyramidal shape, facet, and base diameter, are very consistent with those obtained from XTEM observations because the Σ-shaped pedestal has disappeared.

Based on these experimental observations, the formation procedures for the Si pyramidal tips with Ge nanomasks are summarized

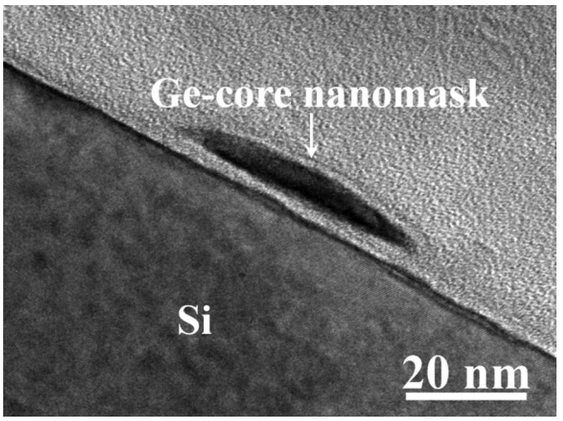

Figure 4. XTEM image of a Ge-core island remaining after 2 min immersion in a 50% TMAH solution.

in Fig. 5. First, the thin wetting layer was removed (Fig. 5a and b). Subsequently, Ge islands act as nanomasks to prevent the underlying Si substrate from being etched, resulting in a Σ-shaped Si pedestal (Fig. 5c). With a longer etching time, the height of the Σ-shaped Si pedestal continues to increase (Fig. 5d). Meanwhile, Ge islands shrink into Ge-rich cores, thus reducing the lateral size of the upper Si pedestal. Underetching is a well-known problem in the Si etching technology.[26,27] This is not observed experimentally in this work, possibly because Ge nanomasks shrink at the same time. Nevertheless, we speculate that, with further etching, underetching of the upper Si pedestal may occur and shrink the dimension of the upper Si pedestal because Ge-rich cores do not shrink anymore. Eventually, Ge-core islands were lifted off and Si pyramidal tips form on the Si substrate (Fig. 5e). We expect that the pyramid structures can be further optimized. The size uniformity of Ge nanomasks is an important parameter for the fabrication of pyramid structures. Postgrowth annealing can be performed to obtain more uniform Ge islands as nanomasks[28] and thus yield more uniform Si pyramidal tips. In addition, the aspect ratios of the resulting structures in the present study are limited to the formation of Si pyramids. Recently,

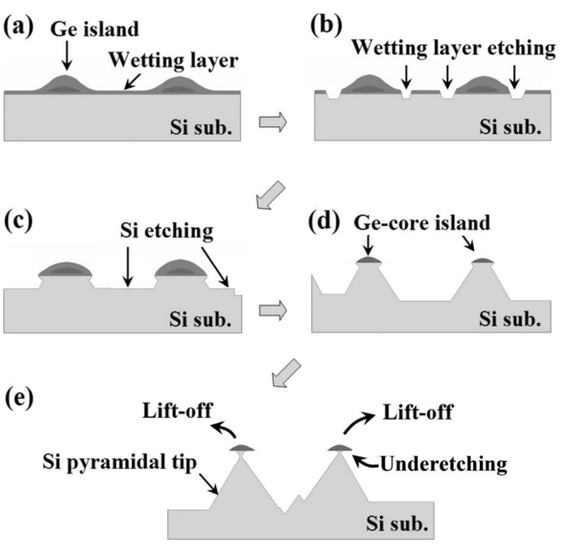

Figure 5. Schematic depiction of the formation of Si pyramidal tips with Ge nanomasks: (a) as-grown Ge islands, (b) etching on wetting layer, (c) anisotropic etching to produce a mushroomlike structure, (d) Ge nanomask shrink, and (e) underetching and final structure with Si pyramidal tips.

Downloaded 07 Feb 2010 to 159.226.100.225. Redistribution subject to ECS license or copyright; see http://www.ecsdl.org/terms_use.jsp

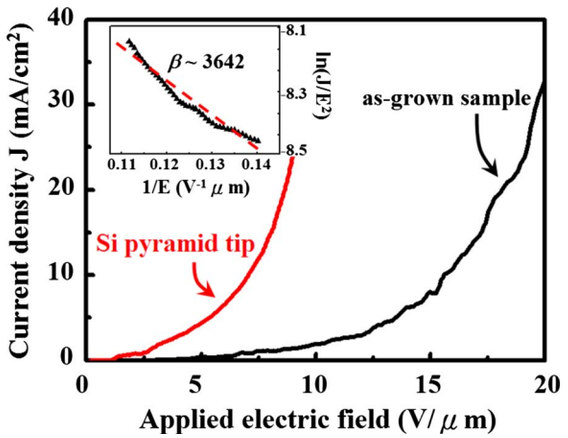

Figure 6. (Color online) Plots of field emission current density J (mA/cm^2) against local applied field E (V/μm) curves for Si pyramidal tips and as-grown Ge islands. The inset presents the emission current data plotted with the FN relationship for the Si pyramidal tips.

the tensile-strained Si regions located below the Ge islands have a slower etching rate of Si.[29] Therefore, by increasing the amount of deposited Ge or by using the Ge/Si multilayers, a higher tensile strain may be introduced into the Si regions located directly below the Ge islands, thus slowing down the underetching rate of the upper Si pedestal. Higher aspect ratios or a sharper apex may be obtained. Related work is in progress.

Figure 6 also shows the field emission characteristics for the Si pyramidal tips and as-grown Ge islands, respectively. The turn-on field (defined to be the electric field required to generate a current density of 1 mA/cm^2) for the Si pyramidal tips was measured to be about 2.6 V μm^{-1}, which is much lower than that of as-grown Ge nanodots (7.5 V μm^{-1}). In addition, by normalizing the turn-on field of the similar reference samples (as-grown Ge islands), the Si pyramidal tips also exhibit a lower turn-on field than that of Si-capped Ge islands in the previous study (6.5 V μm^{-1}).[16] The turn-on voltage highly depends on the sharpness of the field emitters. A higher aspect ratio of the Si pyramidal tips, compared with the as-grown Ge islands, accounts for the improved turn-on field. The field emission current originates from the electrons that jump over an energy barrier from the tip to the vacuum. The Fowler–Nordheim (FN) equation can be expressed as

$$J = (A\beta^2E^2/\Phi)\exp(-B\Phi^{3/2}/\beta E)$$

where J is the current density, E is the applied electric field, and Φ is the work function. A and B are constants, corresponding to 1.56×10^{-10} A eV V^{-2} and 6.83×10^3 eV$^{-3/2}$ μm^{-1}, respectively.[30] The inset of Fig. 6 shows the FN plot for the Si pyramidal tips. The $\ln(J/E^2) - 1/E$ plot gives a straight line at a high field, suggesting an FN tunneling process. The field enhancement factor β, which depends on the geometry, crystal structure, and density of the emitting point, can be calculated based on the FN equation.[31] The Si pyramidal tips possess a β value of 3642, much higher than that of as-grown Ge islands, which is 1043. The high β value of Si pyramidal tips can be attributed to high tip density (8×10^9 cm^{-2}), nanoscale apex (less than 20 nm), and well-controlled spacing between Si pyramidal tips so that the antenna effect is minimized. The present work, although still needing optimization, has demonstrated the feasibility of using self-assembled Ge islands as nanomasks to fabricate high efficiency Si field emitters.

Conclusion

In summary, large-area, nanometer-scale Si field emitters have been successfully fabricated using self-assembled Ge islands as nanomasks. During the etching process, Ge nanomasks shrink into small Ge-core islands that determine the apex sharpness of the Si pyramidal tips. These Si pyramidal tips have an average height and base width of 47 and 95 nm, respectively. The results also demonstrate that Si pyramidal tips exhibited improved antireflective and field emission properties compared to as-grown Ge islands. The high field enhancement factor can be attributed to high tip density, nanoscale apex, and well-controlled spacing between Si pyramidal tips. This process promises to be applicable for fabricating future high efficiency Si-based field emitters.

Acknowledgment

The research was supported by the National Nano Device Laboratories and the National Science Council of Taiwan under contract no. NSC 97-2221-E-008-091-MY3 and no. NSC 98-2623-E-008-007-NU.

National Central University assisted in meeting the publication costs of this article.

References

1. F. C. K. Au, K. W. Wong, Y. H. Tang, Y. F. Zhang, I. Bello, and S. T. Lee, *Appl. Phys. Lett.*, **75**, 1700 (1999).
2. H. C. Lo, D. Das, J. S. Hwang, K. H. Chen, C. H. Hsu, C. F. Chen, and L. C. Chen, *Appl. Phys. Lett.*, **83**, 1420 (2003).
3. Y. L. Chueh, L. J. Chou, S. L. Cheng, J. H. He, W. W. Wu, and L. J. Chen, *Appl. Phys. Lett.*, **86**, 133112 (2005).
4. M. R. Rakhshandehroo and S. W. Pang, *J. Vac. Sci. Technol. B*, **14**, 612 (1996).
5. I. J. Chung, D. B. Murfett, A. Hariz, and M. R. Haskard, *J. Mater. Sci.*, **32**, 4999 (1997).
6. D. Resnik, D. Vrtacnik, U. Aljancic, M. Mozek, and S. Amon, *Microelectron. J.*, **34**, 591 (2003).
7. P. B. Fischer, K. Dai, E. Chen, and S. Y. Chou, *J. Vac. Sci. Technol. B*, **11**, 2524 (1993).
8. G. Zhang, J. Zhang, G. Xie, Z. Liu, and H. Shao, *Small*, **2**, 1440 (2006).
9. W. Li, J. Zhou, X. Zhang, J. Xu, L. Xu, W. Zhao, P. Sun, F. Song, J. Wan, and K. Chen, *Nanotechnology*, **19**, 135308 (2008).
10. C.-M. Hsu, S. T. Connor, M. X. Tang, and Y. Cui, *Appl. Phys. Lett.*, **93**, 133109 (2008).
11. H. Y. Hsieh, S. H. Huang, K. F. Liao, S. K. Su, C. H. Lai, and L. J. Chen, *Nanotechnology*, **18**, 505305 (2007).
12. G. Medeiros-Ribeiro and R. S. Williams, *Nano Lett.*, **7**, 223 (2007).
13. H. C. Chen, S. W. Lee, and L. J. Chen, *Adv. Mater. (Weinheim, Ger.)*, **19**, 222 (2007).
14. J. T. Robinson, A. Rastelli, O. Schmidt, and O. D. Dubon, *Nanotechnology*, **20**, 085708 (2009).
15. V. N. Tondare, B. I. Birajdar, N. Pradeep, D. S. Joag, A. Lobo, and S. K. Kulkarni, *Appl. Phys. Lett.*, **77**, 2394 (2000).
16. S. W. Lee, Y. L. Chueh, H. C. Chen, L. J. Chen, P. S. Chen, L. J. Chou, and C. W. Liu, *Thin Solid Films*, **508**, 218 (2006).
17. G. Medeiros-Ribeiro, A. M. Brathovski, T. I. Kamins, D. A. A. Ohlberg, and R. S. Williams, *Science*, **279**, 353 (1998).
18. S. W. Lee, L. J. Chen, P. S. Chen, M.-J. Tsai, C. W. Liu, T. Y. Chien, and C. T. Chia, *Appl. Phys. Lett.*, **83**, 5283 (2003).
19. V. L. Thanh, P. Boucaud, D. Débarre, Y. Zheng, D. Bouchier, and J.-M. Lourtioz, *Phys. Rev. B*, **58**, 13115 (1998).
20. C. Wu, C. H. Crouch, L. Zhao, J. E. Carey, R. Younkin, J. A. Levinson, E. Mazur, R. M. Farrell, P. Gothoskar, and A. Karger, *Appl. Phys. Lett.*, **78**, 1850 (2001).
21. S. Koynov, M. S. Brandt, and M. Stutzmann, *Appl. Phys. Lett.*, **88**, 203107 (2006).
22. B.-C. Hsu, K.-F. Chen, C.-C. Lai, S. W. Lee, and C. W. Liu, *IEEE Trans. Electron Devices*, **49**, 2204 (2002).
23. G.-R. Lin, C.-J. Lin, and C.-K. Lin, *Opt. Express*, **15**, 2555 (2007).
24. N. Tamura and Y. Shimamune, *Appl. Surf. Sci.*, **254**, 6067 (2008).
25. A. V. Kolobov, K. Morita, K. M. Itoh, and E. E. Haller, *Appl. Phys. Lett.*, **81**, 3855 (2002).
26. N. Wilke, A. Mulcahy, S.-R. Ye, and A. Morrissey, *Microelectron. J.*, **36**, 650 (2005).
27. V. B. Svetovoy, J. W. Berenschot, and M. C. Elwenspoek, *J. Electrochem. Soc.*, **153**, C641 (2006).
28. T. I. Kamins, G. Medeiros-Ribeiro, D. A. A. Ohlberg, and R. S. Williams, *J. Appl. Phys.*, **85**, 1159 (1999).
29. Z. Zhong, G. Katsaros, M. Stoffel, G. Costantini, K. Kern, O. G. Schmidt, N. Y. Jin-Phillipp, and G. Bauer, *Appl. Phys. Lett.*, **87**, 263102 (2005).
30. R. H. Fowler and L. Nordheim, *Proc. R. Soc. London, Ser. A*, **119**, 683 (1928).
31. S. M. Yoon, J. Chae, and J. S. Suh, *Appl. Phys. Lett.*, **84**, 825 (2004).

Downloaded 07 Feb 2010 to 159.226.100.225. Redistribution subject to ECS license or copyright; see http://www.ecsdl.org/terms_use.jsp