Low-Power Switching of Phase-Change Materials with Carbon Nanotube Electrodes

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Low-Power Switching of Phase-Change Materials with Carbon Nanotube Electrodes

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Phase-change materials (PCMs) are promising candidates for nonvolatile data storage and reconfigurable electronics, but high programming currents have presented a challenge to realize low-power operation. We controlled PCM bits with single-wall and small-diameter multi-wall carbon nanotubes. This configuration achieves programming currents of 0.5 microampere (set) and 5 microamperes (reset), two orders of magnitude lower than present state-of-the-art devices. Pulsed measurements enable memory switching with very low energy consumption. Analysis of over 100 devices finds that the programming voltage and energy are highly scalable and could be below 1 volt and single femtojoules per bit, respectively.

Phase-change materials (PCMs) such as chalcogenides like $Ge_2Sb_2Te_5$ (GST), have amorphous (a) and crystalline (c) phases with contrasting electrical and optical properties. PCMs are the active material in rewritable digital video discs (DVDs), where phase transformations are induced and read by a pulsed laser (*1*, *2*). The data in electrically programmable PCMs are stored as changes in bit resistivity (*3*–*6*), which can be reversibly switched with short voltage pulses and localized Joule heating. In this sense, PCMs are appealing compared to other semiconductor memories where data are stored as charge and are susceptible to leakage and volatile behavior. Electrically programmable PCMs have captured wide interest for applications in nonvolatile memory (*7*, *8*) and reprogrammable circuits (*5*, *6*) with low voltage operation, fast access times, and high endurance (*3*, *4*). These attributes make them contenders for a "universal" nonvolatile memory, which could replace all data storage from random-access memory to hard disks. However, a drawback of PCMs is their high programming current (>0.1 mA), because Joule heat must be coupled to a finite bit volume, previously achieved with 30- to 100-nm-diameter nanowires (*9*–*11*) or metal interconnects (*12*–*14*).

We used carbon nanotubes (CNTs) with diameters of ~1 to 6 nm as electrodes (*15*, *16*) to reversibly induce phase change in nanoscale GST bits. Our findings address the potential size and power reduction that are possible for programmable bits of PCM. We demonstrate reversible switching with programming currents from 0.5 to 8 μA, two orders of magnitude lower than state-of-the-art PCM devices. We also present a device-scaling study that suggests memory switching is possible with voltages below 1 V and energy less than femtojoules per bit.

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The CNTs used in this work were grown by chemical vapor deposition (CVD) with Fe catalyst particles on SiO_2/Si substrates (*17*, *18*) [also see (*19*)]. We obtained single-wall and small diameter multi-wall CNTs, and we found that both can be used to switch GST bits. The as-grown CNTs span Ti/Pd (0.5/40 nm) metal contacts with 1 to 5 μm of separation (fig. S1). We then created nanoscale gaps in the CNTs through electrical breakdown (*20*) in air or under Ar flow, as illustrated in Figs. 1 and 2A, left inset. This simple approach yielded a wide range of nanogaps (from ~20 to 300 nm) in more than 100 devices, which was essential for our subsequent scaling study. The nanogap is typically near the middle of the CNT, consistent with the electrical breakdown location and with negligible Pd contact resistance (*20*, *21*). Then, a ~10-nm GST film was sputtered over the device surface (fig. S2), with settings previously found to preserve the good electrical characteristics of CNTs (*18, 19*). This deposition fills the CNT nanogaps, creating self-aligned lateral PCM bits (Fig. 1). Such devices can be readily switched and examined by atomic force microscopy (AFM) (Fig. 2); however, a ~5-nm SiO_2 capping layer deposited after the GST without breaking vacuum (*12*) is used to prolong the switching lifetimes.

Devices are initially in the off state (Fig. 1C) because the as-deposited GST films are amorphous (a-GST) and highly resistive, with resistance R_{OFF} ~ 50 Mohm (*22*). A voltage applied at the CNT contacts creates a sizable electric field (*E*-field) across the nanogap and switches the GST bit to the crystalline phase (c-GST), which lowers the device resistance by about two orders of magnitude to R_{ON} ~ 0.5 Mohm. Although a-GST covers the entire device, the switching occurs only in the nanogap, which is the location of highest *E*-field and Joule heating.

To test initial memory switching, we sourced current and measured voltage across the devices (Fig. 2). The amorphous bits displayed switching at a threshold voltage, V_T, as is typical with GST (*7*, *8*), and a sharp transformation to a conductive phase under high *E*-field. Importantly, we note that little voltage is dropped across the CNT electrodes, which are always more conductive than the GST bit, as confirmed with finite-element (FE) simulations (*19*). Transport in the a-GST material is temperature-activated (*23*) even in the ~10-nm-thin films, as shown in Fig. 2A, right inset, and discussed in (*19*). Once threshold switching occurs, the bit crystallizes from Joule heating, and this marks the set transition. The set current was of the order ~1 μA in more than 100 devices tested (*19*), two orders of magnitude lower than set currents in conventional PCM devices. However, the V_T scaled linearly with the nanogap size (see below). This linear relationship provides strong

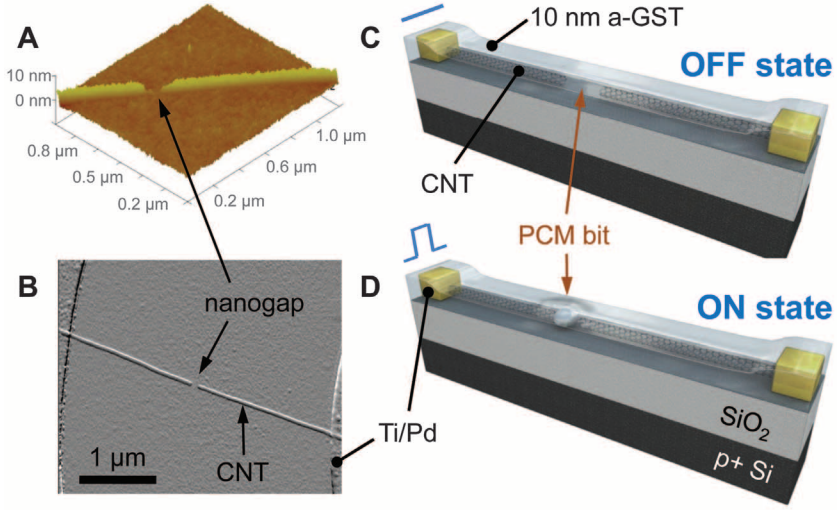

Fig. 1. Schematics of CNT-PCM device. (**A**) AFM imaging of nanogap created after CNT breakdown under electrical stress (*20*). (**B**) AFM image of an as-fabricated device. (**C** and **D**) Schematic of device obtained after deposition of GST thin film. The device is in its off state immediately after fabrication, with highly resistive a-GST in the nanogap. (D) The device is switched to its on state after an electric field in the nanogap transforms the bit to its conductive c-GST phase.

evidence that threshold switching in a-GST is driven by *E*-field (*24*, *25*) even at the minimal bit sizes explored here.

We examined reversible switching of our devices through pulsed measurements. In Fig. 3A, we plotted the resistance after a series of pulses with the same duration (150 ns) and increasing amplitude, starting from the resistive off state. The resistance decreases abruptly when the current exceeds ~1 μA, marking the set transition. As in Fig. 2, this signals the transformation of GST in the nanogap to the c-phase, thus "reconnecting" the two CNT electrodes. The resistance increases again when the current exceeds ~5 μA, which is the reset transition. This behavior is consistent with fast melting and quenching of the bit (*7*), returning the material to the a-GST phase. Repeated cell switching (Fig. 3B) exhibited good stability after several hundred cycles in devices capped with SiO_2, as described above.

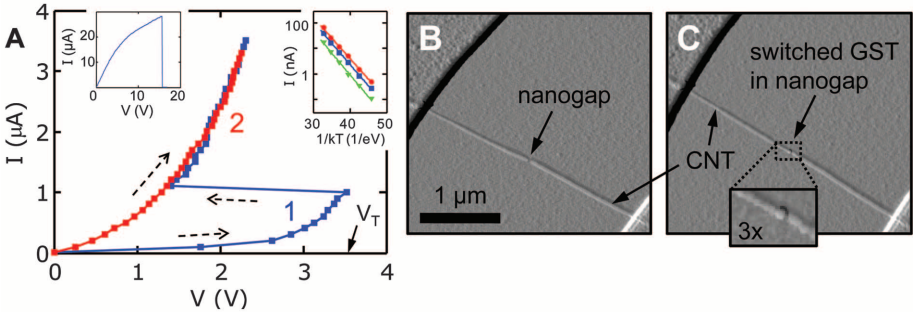

Fig. 2. Initial antifuse-like switching. (**A**) Current-voltage of a device with CNT diameter ~3 nm, nanogap ~35 nm, and GST film thickness ~10 nm. The initial sweep (no. 1) turns the bit on (a→c) at ~1 μA and V_T = 3.5 V. The c-GST bit phase is subsequently preserved (no. 2). The left inset shows the current-voltage of the CNT as used to create the nanogap before GST deposition (*20*). The right inset shows temperature-activated transport in the subthreshold regime after a-GST deposition [also see fig. S9 (*19*)]. The activation energy ~0.38 eV decreases slightly with voltage (*19*), consistent with trap-assisted transport in disordered a-GST (*23*). (**B** and **C**) AFM images of the same device before and after switching. Small changes of GST volume in the gap can be seen after switching here without a capping layer (*18*). Also see fig. S6 in (*19*).

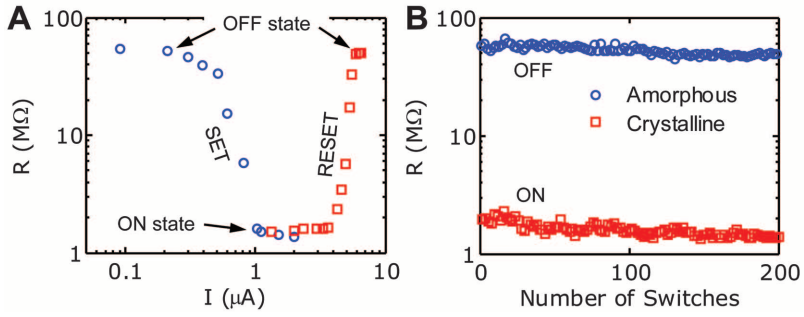

Fig. 3. Reversible memory operation using pulsed measurements. (**A**) Device resistance versus current pulse magnitude. The width of the set and reset pulses are 150 ns (20-ns falling edge) and 50 ns (8-ns falling edge), respectively, as limited by our experimental setup. Sharp transitions are seen at 1 μA (set) and 5 μA (reset) current, two orders of magnitude lower than the present state of the art (*9*–*14*). (**B**) Memory endurance test showing excellent separation between on and off states, with no degradation after hundreds of cycles (set pulse, 1.5 μA and 150 ns; reset pulse, 6.0 μA and 50 ns). The device shown here is covered by the ~5-nm SiO_2 capping layer.

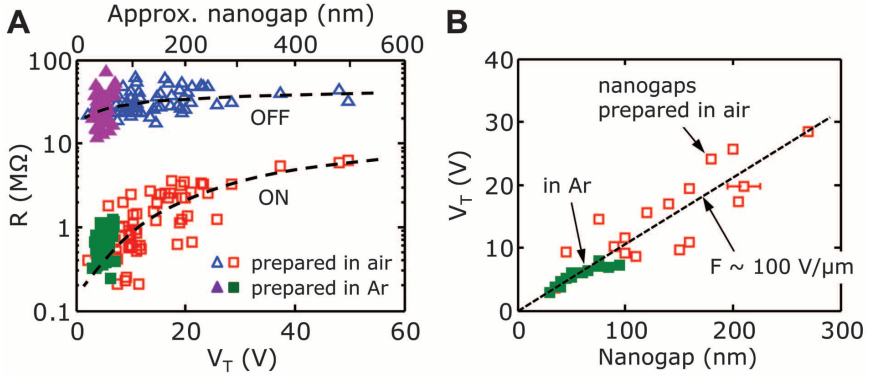

Fig. 4. Scaling trends of memory devices. (**A**) On- and off-state resistance for 105 devices shown versus V_T. As marked, 61 nanogaps were created in air ambient (open symbols); the other 44 devices were formed under Ar flow (solid symbols). Ar-formed nanogaps are consistently smaller (<100 nm) and yield lower-power devices. Dashed lines are trends to guide the eye. (**B**) Threshold voltages scale proportionally to size of nanogap, at an average field of ~100 V/μm. The dashed line is a linear fit, indicating excellent device scalability. Lateral error bar is estimated uncertainty from nanogap measurement under AFM.

We comment on the ultimate scaling limits of such materials and technology. For our "best" results, switching occurred at <1 μA (set), ~5 μA (reset), and ~3 V across 20- to 30-nm nanogaps, with only a few microwatts of programming power. The programming current and power are two orders of magnitude lower than present state of the art (*12*–*14*), enabled by the very small volume of PCM addressed with a single CNT.

The dimensions of the bits examined here are in general defined by the small nanogaps (down to ~20 nm), the thin (~10 nm) GST film, and the CNT electrode diameters (~1 to 6 nm). The low thermal conductivity of GST (*19*) appears to play a role in laterally confining the bit to a scale not much greater than the CNT diameter. The small lateral extent of the bits can be seen in Fig. 2C and fig. S6 and also confirmed with simulations (*19*, *26*). We estimate the effective bit volumes addressed here are as small as a few hundred cubic nanometers.

We present a statistical study of more than 100 devices in Fig. 4. First, we plot R_{ON} and R_{OFF} versus their respective threshold voltage V_T in Fig. 4A, showing two distinct memory states for every device studied. During fabrication, 61 of the CNT nanogaps were created in air and 44 were created under Ar flow, the latter producing smaller gaps because of reduced oxygen (*15*, *19*). We note R_{OFF} values are fairly constant (*22*). However, R_{ON} scales proportionally with V_T, as seen in Fig. 4A, because both R_{ON} and V_T are related to the nanogap size. R_{ON} is dominated by the resistance of the c-GST and proportional to the nanogap size, because the CNT electrodes are much more conductive. The nanogap size also determines V_T, because threshold switching in a-GST is driven by the *E*-field in the nanogap. The linear scaling trend between V_T and nanogap size in Fig. 4B supports this observation, with an average threshold field of ~100 V/μm. This value is comparable to ~56-V/μm threshold field measured in 30-nm GST films (*27*) and an order of magnitude lower than the breakdown field of SiO_2 (*28*), indicating the switching indeed occurs in the GST bit. The mean set currents across all nanogaps fabricated in air and Ar were nearly identical at ~2 μA, with a range of 0.5 to 4 μA (fig. S7C). Reset currents were typically four times higher, ranging from 5 to 8.5 μA as shown in Fig. 3 and fig. S7D.

The minimum energy per bit obtained with our sharpest (~20 ns) pulses is of the order ~100 fJ. However, the linear trend of V_T with nanogap size (Fig. 4B) reveals that such devices are highly scalable and suggests that ~5-nm GST bits with CNT electrodes could operate at ~0.5 V and <1 μA, such that nanosecond switching times (*29*, *30*) would lead to sub-femtojoule per bit energy consumption [for additional estimates see section 6 of (*19*)]. Low-voltage operation could also be achieved by using materials with lower threshold fields, such as GeSb (*27*). These results are encouraging for ultralow-power electronics and memory based on programmable PCM with nanoscale carbon interconnects.

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Supporting Online Material

www.sciencemag.org/cgi/content/full/science.1201938/DC1
Materials and Methods
SOM Text
Figs. S1 to S9
References

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Low-Voltage, Low-Power, Organic Light-Emitting Transistors for Active Matrix Displays

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Intrinsic nonuniformity in the polycrystalline-silicon backplane transistors of active matrix organic light-emitting diode displays severely limits display size. Organic semiconductors might provide an alternative, but their mobility remains too low to be useful in the conventional thin-film transistor design. Here we demonstrate an organic channel light-emitting transistor operating at low voltage, with low power dissipation, and high aperture ratio, in the three primary colors. The high level of performance is enabled by a single-wall carbon nanotube network source electrode that permits integration of the drive transistor and the light emitter into an efficient single stacked device. The performance demonstrated is comparable to that of polycrystalline-silicon backplane transistor-driven display pixels.

Organic light-emitting diode (OLED) displays have well-recognized advantages in power consumption, pixel brightness, viewing angle, response time, and contrast ratio over liquid crystal displays (LCDs) (*1*). The primary technical challenge preventing wider commercial implementation remains the drive transistor in the active matrix (AM) backplane. Amorphous silicon (a-Si), the transistor channel material that sources the voltage to switch AM-LCD pixels, has a low mobility (~1 $cm^2 V^{-1} s^{-1}$) (*2*). To drive the currents necessary for OLEDs would require higher drive voltages, consuming power; moreover, its stability is unacceptable for AMOLED pixels (*3*, *4*). For small AMOLED displays now in some handheld devices, the solution has been to use low-temperature polycrystalline silicon (poly-Si). However, poly-Si adds processing steps, time, and expense to the device fabrication (*5*, *6*). Poly-Si also suffers from a more fundamental limitation: variation in the size, orientation, and number of the large polycrystalline grains (important to its high mobility for sourcing the high drive currents) leads to pixel-to-pixel inhomogeneity (*7*). This limits the production yield and becomes an increasingly severe problem with increasing display size.

Organic semiconductor channel materials are attractive for their homogeneity, low cost, and the variety of means by which they can be deposited, but their best mobilities are similar to that of a-Si. In the typical thin-film transistor (TFT) architecture, low-mobility channel layers would require a large source-drain voltage to drive the necessary current. This consumes power in the transistor (as opposed to light production in the OLED), compromising the power savings. In one all-organic AMOLED demonstration, more power was dissipated in the drive transistor than in the OLED it was powering (*8*). Mitigating this by increasing the channel width of the drive transistor to source more current is not viable; to do so would reduce the fraction of pixel area available to the OLED, requiring a higher current density through the electroluminescent emitter to maintain the display brightness, reducing OLED lifetime (*9*). Alternatively, the low mobility of the organics could be compensated by making the channel length short, placing the source and drain terminals very close to each other; but that incurs the expense of high-resolution patterning.

We recently demonstrated a carbon nanotube enabled vertical field effect transistor (CN-VFET) that, intrinsic to its architecture, permits short channel lengths without high-resolution patterning and gave on-currents sufficient to drive OLED pixels at low operating voltages (*10*). Here, to realize the full benefit of the architecture, we integrate the OLED into the CN-VFET stack. We call such a device a carbon nanotube enabled vertical organic light-emitting transistor (CN-VOLET)

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