

Precision Wafer Thinning and Its Surface Conditioning Technique

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Abstract. Experimental observations were conducted to investigate the effects of various parameters on the surface finish and subsurface damage (SSD) of ground silicon wafers. A novel design in wet chemical etching was proposed and implemented to provide wafers a means of strength enhancement while allowing the user to control the backside wafer surface finish. The results indicate that no propagating crystalline defect was accompanied, but leaving the wafer in a rather good surface integrity for back metal adhesion purposes.

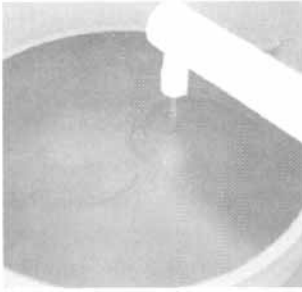
Introduction

Silicon wafers are most extensively used materials for integrated circuit (IC) substrates. As the demand of miniaturization with higher performance standards for electronic devices such as memory cards, smart cards, portable communication devices, and portable computers becomes a clear trend. IC package as a whole makes it a requirement to reduce both feature sizes and chip thickness. These requirements render the chip and packaging designers to develop high-speed, ultra-thin chips that utilize less individual area and overall package height to accommodate multiple layers of dense interconnects. The chips that are required to fit into these so-called intelligent devices have to be remarkably thin, which indicates that silicon chip thinning and stress relief considerations have been turned into significant issues in the backend treatment and assembly of semiconductor component manufacturing.

There are four primary methods for wafer thinning (Manfred and Gerald 2003): mechanical grinding, chemical mechanical polishing (CMP), wet etching and atmospheric downstream plasma (ADP) dry chemical etching (DCE). Because of its high thinning rate, mechanical grinding currently is the most common technique for wafer thinning. However, there is a remaining defect band near the surface. The remaining defect layer and surface roughness are the reasons for an additional thinning process after mechanical grinding. This can be done either by CMP, dry etching or wet chemical etching. Wet chemical etching is one of the most common thinning techniques. One of the commercial wet chemical etching equipments was shown in Fig. 1.

Besides substrate thinning, there are still back surface roughness requirements for different back metal adhesion. The chemical wet etching process can be chemically roughened to provide the optimal conditions increased surface area for improved back metal adhesion.

In this paper, the ductile grinding technique was introduced experimentally with its benefit on minimum micro-fracture and limitation on ultra thin wafer thickness. And then, wet chemical etching technology was conducted to meet advanced wafer thinning requirement. A new type wet chemical etching equipment was designed and setup for this research, and three different chemical solutions were developed and experimental parameters and results were discussed.



(a) Rotating wafer with simultaneous etchant delivery (b) Overview
Figure 1 Commercial wet chemical etching equipment
(Solid State Equipment Corporation, 2004)

Ductile grinding and subsurface damage layer

Because the properties of single crystalline silicon are hard and brittle, surface and subsurface damage are easily induced during the machining processes including sawing, grinding, and lapping. To achieve a better surface and subsurface performance, ductile regime grinding has been proposed (Bifano et al. 1991). With ductile regime grinding, the chip removal mechanism will induce minimum micro-fracture and micro-crack shown in Fig. 2 and Fig. 3.

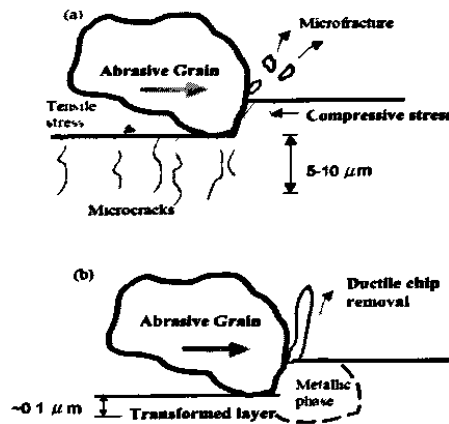


Figure 2 Chip removal mechanism (a) brittle (b) ductile. (Puttick et al. 1996)



Figure 3 Chip removal mechanism (a) brittle (b) ductile. (Zhong 2003)

An important condition for ductile regime grinding is that the grain depth of cut (d_g) of every grits on the wheel should be less than the critical depth of cut (d_c) of silicon wafer. We had proposed an effective means to investigate d_c of silicon wafer grinding in previous paper (Young 2005). It was shown that the value of the critical depth (d_c) is within the range of 20~40 nm and the grain depth of cut (d_g) would change with different grinding conditions. From the definition of ductile regime grinding $d_g < d_c$, it means to achieve ductile regime grinding, d_g must be less than all the critical depth of cut of ground silicon wafer (about 20 nm in the experiment). The grinding condition for ductile regime grinding is shown in Eq. 1.

$$d_g = 7.37R \left(\frac{f' r_1 \omega_1}{L w_2 F_v \omega_2^2} \right)^{0.4} < 20nm \quad (1)$$

Where f is the infeed per revolution of the grinding wheel, r_1 is the distance from silicon wafer centre to the sample location, ω_1 is the chuck rotational speed in rpm, ω_2 is the wheel rotational speed in rpm, F_v is the grain volume fraction in the binder, L is the mean circumference of the grinding wheel and w_2 is the diamond cup wheel thickness.

Ductile regime grinding can get good result while wafer thickness is above 250 μ m. In this research, the G&N Nanogrinder MPS NO 940 grinding equipment was use to try the extreme thickness that grinding could achieve. The results shown in Fig. 4 and Table 1 indicated that mechanical grinding process would meet the limit with the requirement of ultra thin wafer thinning. Thus wet chemical etching technology was introduced below.

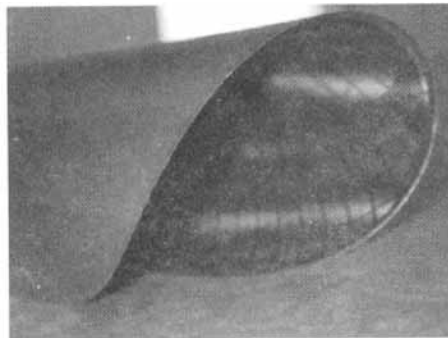


Figure 4 Warped wafer after ground

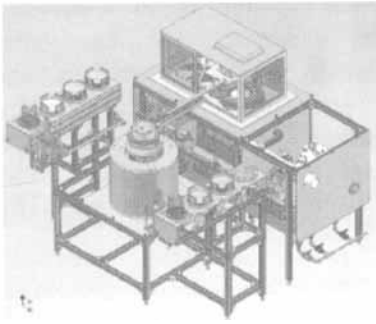
Table 1 Results of different Grinding thickness

	Initial Thickness [μ m]	Final Thickness [μ m]	Results
Rum 1	725	200	Warped
Rum 2	725	175	Warped
Rum 3	725	150	Warped
Rum 4	725	140	broken
Rum 5	725	125	broken

Wet etching process in wafer thinning

The strength of wet chemical etching includes simple process, low cost, high etching selectivity and high yielding rate. The etchants for silicon wafer backside etching are mostly mixtures of HF, H_3PO_4 , CH_3COOH and HNO_3 , etc. The different mixtures conduct different etching rates and are characterized by different selectivities. Also various degrees of backside wafer surface finish can be achieved.

In this research, a novel type wet chemical etching equipment was designed and setup as shown in Fig. 5.



(a) 3D CAD Model



(b) Prototype photograph

Figure 5 Wet chemical etching equipment designed and fabricated prototype

The difference between this technology and the traditional wet chemical etching is the use of surface tension of etchant, as the schema shown in Fig. 6.

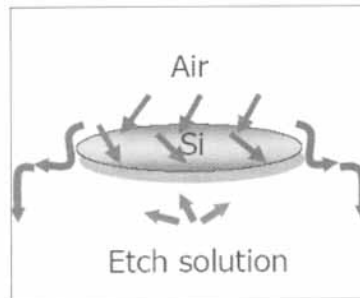


Figure 6 Wet chemical etching schema

The wafer is floating on the surface of chemical etching solution with backside down and chemical solution flows are conducted from bottom of the reaction chamfer. At the same time, the wafer is spun and protected by the action of airflows from the upper side.

In this research, silicon wafers were thinned with floating etching process in this equipment. And three aqueous chemical etchants (Solution A (HF, CH_3COOH , HNO_3), Solution B (HF, NH_4F , HNO_3), Solution C (HF, HNO_3 , buffer acid)) were developed and used in the experiments. The results were discussed below.

Results and discussion

TTV and etching rate. To study the Total Thickness Variation (TTV) and etching rate of the floating etching process, experiment had been down in the wet chemical etching equipment developed in this research with fifty pieces of 200 mm silicon wafers. At first, all wafers were thinned to 250 μm by mechanical grinding. In the 300 sec etching processing with Solution A, Thickness of each wafer was measured per 30 sec, and TTV was measured at the end of etching process.

The results were shown in Fig. 7 and Fig. 8. The etching rate 11.6 $\mu\text{m}/\text{min}$ and the TTV 18.8 μm can be reached in average.

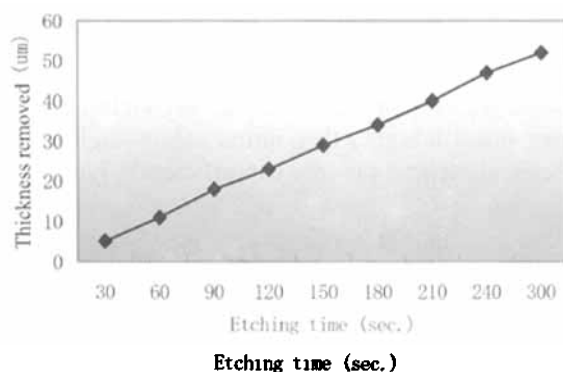


Figure 7 Wet etching rate

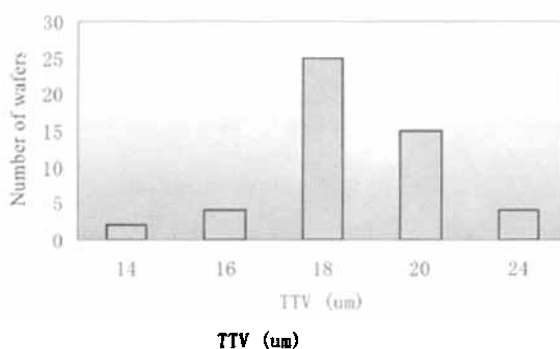


Figure 8 TTV measured for 50 wafers

Subsurface damages removed. The experimental results indicated that wet chemical etching process can fine remove damages produced while grinding by using either solution A, B or C as shown in Fig. 9, with: (a) surface ground with #2000 grind abrasives; (b) surface etched with Solution C after ground; (c) cross-sectional view of sample (a); (d) cross-sectional view of sample (b).

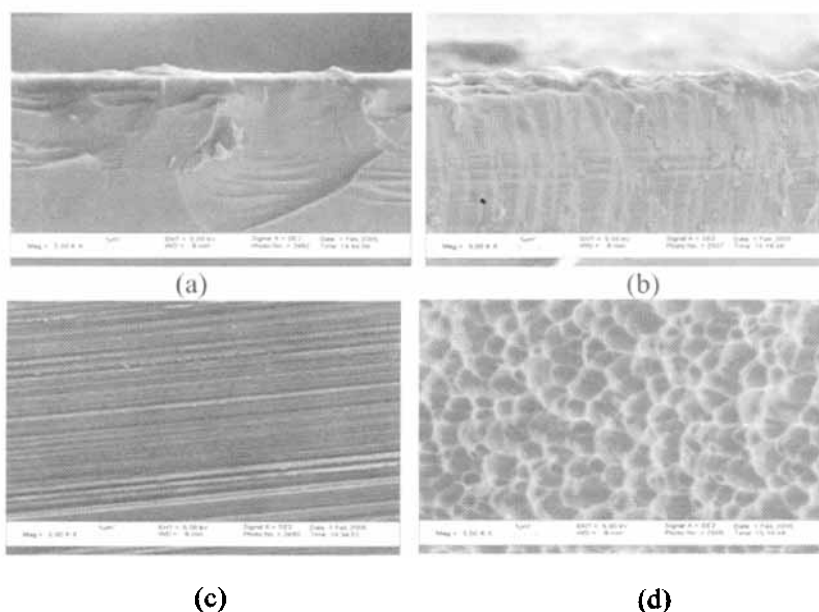


Figure 9 Ground damage removed by etching

Surface conditioning with different etchants. The chemical etchants utilized are optimized in this research for various back metal schemes and provide the optimal conditions for adhesion purposes. Fig. 11 shows the surfaces etched by solution A, B and C. The surface roughness etched by Solution C was ten times rougher than Solution A and Solution B.

In this research, Peva-900E Evaporator (Advanced System Technology Co. Ltd.) was used to adhesion titanium, nickel and silver membrane on silicon wafer. And followed with the peeling test by 2-0300 with 3M Scotch® Brand Tape Core Series, as shown in Fig. 12.

The results are conclusive and could be seen that either Solution A, B or C can effectively remove SSD and residual stress on wafers, but only wafers etched with Solution C can pass through the peeling test.

Breakage while handling. With the process of this research, 200 mm wafers could be thinned to 100-125 μ m in thickness. When the wafers were further thinned to 75 μ m and below, breakage always accompanied during handling by robotic arm or in detaping process, as shown in Fig. 13.

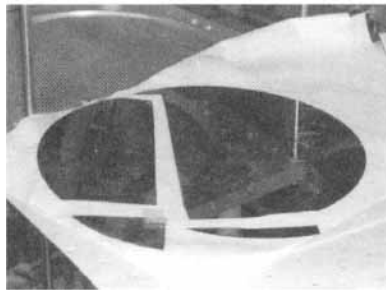


Figure 13 Wafer broken while in handling

Summary

In this paper, a minimum thickness of 150 μ m (accompanied with large bow) for 200 mm wafers with precision grinding process was observed experimentally. A wet chemical etching equipment was developed and applied to thin the 200 mm silicon wafer to 100-125 μ m in thickness by the process with precision grinding followed by wet chemical etching. Also in this study the capability of wet chemical etching process in SSD and residual stress removing, and surface conditioning was verified.

When the wafer was thinning to 75 μ m and below, breakage is always accompanied in robot arm handling and detaping process. It is suggested that an innovated wafer handling method will be required to handling the ultra thin wafers as the diameter increases.

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