

# BARRIER OHMIC CONTACTS TO INDIUM GALLIUM ARSENIDE

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## ABSTRACT

The addition of a barrier layer to Ni-Au-Ge Ohmic contacts on n-InGaAs were investigated over a range of alloying/sintering temperatures and surface pre-treatments. A 20% HCl dip followed by deposition of Ni-Au-Ge-ZrB<sub>2</sub>-Au produced good ohmic contacts, electrically and physically. These had contact resistance values of 0.33  $\Omega$ .mm as deposited and a minimum of 0.05  $\Omega$ .mm for a peak sinter temperature of 260°C. Specific contact resistivity was in the  $10^{-7}$   $\Omega$ .cm<sup>2</sup> range. Contact stability and morphology were shown to be enhanced by use of the barrier layer. Using a barrier layer there was no significant rise in contact resistance after 100 h at 300°C; without a barrier layer the resistance increased by 73%. J-FETs fabricated in InGaAs on InP with a ZrB<sub>2</sub> barrier have been fabricated successfully. The measured contact resistance was < 0.03  $\Omega$ .mm which has contributed to the good current and transconductance characteristics.

## 1. INTRODUCTION

Owing to the low barrier height of metals on n-InGaAs (0.2eV) the production of ohmic contacts to this material is not difficult. Ni-Au-Ge is a common ohmic system for use in III-V devices and has been used successfully on InGaAs [1,2]. These metals deposited directly on the surface can have contact resistances well below 1  $\Omega$ .mm with no heat treatment if the surface is properly cleaned prior to metal deposition. However such contacts are not necessarily stable during subsequent thermal treatment in processing or throughout life.

Most contact systems for n-InGaAs have been transferred directly from GaAs systems with little change in annealing temperatures, however a Ni-Au-Ge contact can be further optimised for use with InGaAs.

The requirements of the contact for use in high performance opto-electronic components are:

- 1 Good morphology to allow fine line lithography on subsequent process steps;
- 2 Contact resistance < 0.4  $\Omega$ .mm for < 10% degradation of the transconductance;
- 3 Stability throughout optical (PIN) and electronic (J-FET) processing;
- 4 Good long term stability.

### 1.1 Background

There was a wealth of information about Ni-Au-Ge contacts to GaAs, also including the use of a barrier layer to limit the amount of gold in contact with the

semiconductor [3]. Initial work on ohmic contacts to n-InGaAs had indicated a number of requirements for successful ohmic contacts using Ni-Au-Ge:

- a A surface pre-treatment is essential for good adhesion, improved morphology, and uniform electrical characteristics;
- b The benefit of including Ni in Au-Ge systems to promote good adhesion and morphology;
- c Separate layers of Au and Ge can be deposited, thus allowing the use of electron beam evaporation.

## 2. EXPERIMENTAL

### 2.1 Material

Assessment material for this work was a 50 mm semi-insulating InP wafer onto which was grown a buffer layer of p-InP (0.3  $\mu\text{m}$ ) and a n-InGaAs (0.3  $\mu\text{m}$ ) active layer. The doping concentrations, measured with a Polaron plotter, were  $5 \times 10^{15} \text{ cm}^{-3}$  for the InP buffer layer and  $1.5 \times 10^{17} \text{ cm}^{-3}$  for the InGaAs. The p-InP and n-InGaAs layers were grown by Molecular Beam Epitaxy (MBE). The layer structure is illustrated in Fig. 1.

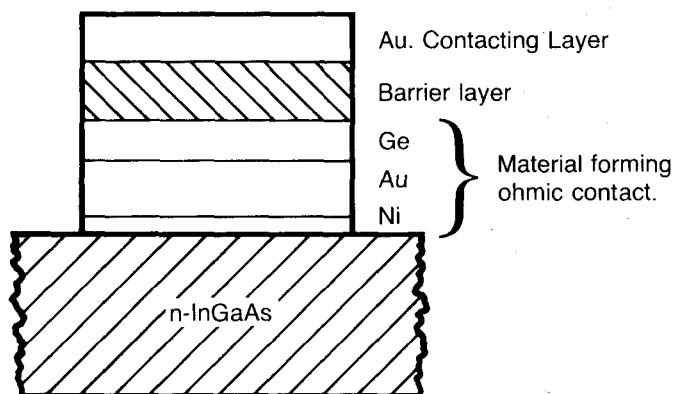


Fig. 1 Contact structure

### 2.2 Sample Preparation

Contact test patterns were mesa isolated using a photo-resist mask to define the test area and a selective etch used to remove all the n-InGaAs and approximately 50 nm of the InP buffer layer.

Contact windows over the whole wafer were defined with a further layer of photo-resist before the sample was cleaved into 8 mm square chips. Each chip contained 16 test patterns suitable for Transmission Line Model (TLM) [4,5] contact resistance measurements. The test pattern, consisted of 100  $\mu\text{m}$  by 150  $\mu\text{m}$  pads with separations of 5  $\mu\text{m}$  to 20  $\mu\text{m}$  (Fig. 2).

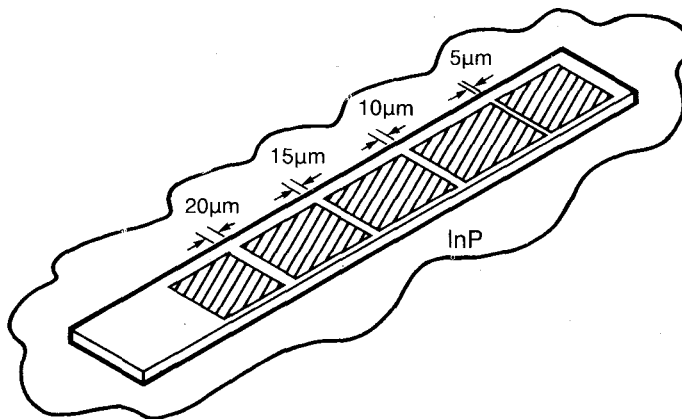


Fig. 2 Contact resistance pattern

### 2.3 Contacts

Immediately prior to deposition, some chips were cleaned in either 20% HCl solution or  $\text{H}_2\text{O}_2:\text{H}_2\text{SO}_4:\text{H}_2\text{O}$  at 1:1:50. Contact layers were sequentially deposited in a single run in a load-lock chamber e-beam evaporator, followed by lift off, inspection and resistance measurement. Three contact structures were assessed:

- a) 5 nm Ni + 45 nm Au + 20 nm Ge
- b) 5 nm Ni + 45 nm Au + 20 nm Ge + 50 nm  $\text{ZrB}_2$  + 20 nm Au
- c) 5 nm Ni + 45 nm Au + 20 nm Ge + 50 nm  $\text{ZrB}_2$  + 200 nm Au

### 2.4 Resistance measurements

A programmable dc parametric tester and an automatic stepping probe were used to measure each of the 16 test elements on the 8mm square chips. Two probes were placed onto each large contact pad to give approximately Kelvin connections for every resistance measurement (Fig. 4a).

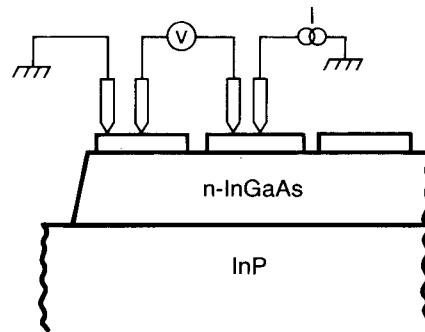


Fig. 4a Four-probe resistance measurement

The contact resistance ( $R_c$ ) was determined by extrapolation to zero spacing between the four differently spaced pads (Fig. 4b). These graphs were consistently linear because the contact areas were large compared to that required by the TLM model. The normalised contact resistance ( $\Omega\cdot\text{mm}$ ) is a good measure of contact quality, giving a simple parameter that is directly related to the parasitic contact resistance in a FET. A measure of sheet resistivity of the semiconductor can also be obtained from the slope of the same graph.

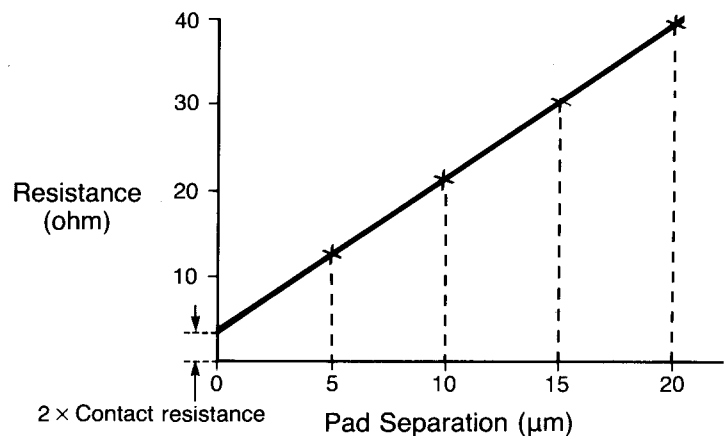


Fig. 4b Resistance at 4 contact spacings

### 2.5 Alloying/sintering

Using a carbon strip heater, samples were heated in the range  $100^\circ\text{C}$  to  $400^\circ\text{C}$  in a forming gas ambient. The current was switched off at the peak temperature and the specimen and graphite allowed to cool. Samples would reach  $300^\circ\text{C}$  in 25 s and fall to less than  $150^\circ\text{C}$  in 60 s.

### 2.6 Temperature stress tests

After sintering the contacts at  $260^\circ\text{C}$ , their stability was assessed by thermal overstress tests at  $300^\circ\text{C}$  for up to 100 h in a furnace flushed with dry nitrogen.

## 2.7 Adhesion tests

Ohmic metallisation was similarly deposited and processed onto identical 8 mm square chips of unpatterned InGaAs on InP. Contact adhesion was assessed with a Sebastian puller or by visual examination after repeated probing.

## 3. RESULTS AND DISCUSSION

### 3.1 Dependence of contact quality on surface pre-treatment

The morphology and adhesion of contacts are summarised in Table 1 below.

CONTACT STRUCTURE	SURFACE PRE-TREATMENT	LIMIT OF GOOD MORPHOLOGY (°C)	CONTACT ADHESION
NiAu/Ge eutectic	none	250	poor <sup>+</sup>
NiAuGe	none	250	poor <sup>+</sup>
NiAuGe	20% HCl	400	good
NiAuGe	H <sub>2</sub> O <sub>2</sub> :H <sub>2</sub> SO <sub>4</sub> :H <sub>2</sub> O = 1:1:50	300	very good*
NiAuGeZrB <sub>2</sub> Au	20% HCl	400	very good*
NiGeAu	20% HCl	300	poor <sup>+</sup>

<sup>+</sup> Poor adhesion is defined as significant loss of contact area at each measurement stage after heat treatment at over 200°C.

<sup>\*</sup> In both these cases the substrates failed before the metallisation when using the Sebastian puller.

Generally, the 260°C sintered contact morphology and adhesion were good with both forms of pre-clean and very poor with none. However, the morphology of contacts after 100 h at 300°C clearly depended on whether they included a barrier (Fig. 3).

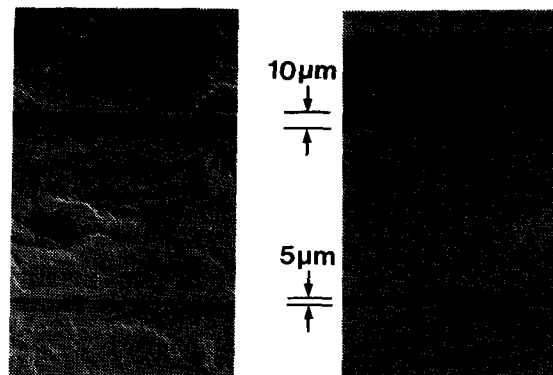


Fig. 3 Contacts without and with a barrier

The contact resistance of the samples also depended on the type of pre-treatment. The resistances of those which were pre-dipped in  $\text{H}_2\text{O}_2:\text{H}_2\text{SO}_4:\text{H}_2\text{O}$  were 160% higher "as deposited" and 70% higher after 260°C peak thermal treatment, than the samples which were pre-dipped in 20% HCl.

### 3.2 Dependence of contact resistance on sinter/alloy temperature

For all three metallisation schemes listed in section 2.3 the contact resistance varied with peak sinter/alloy temperature, as shown in Fig. 5. All contact structures experienced a dramatic increase in contact resistance at 150°C, making the good "as deposited" resistances irrelevant after further wafer processing. In each case a resistance minimum occurs at about 260°C with values between 0.05 and 0.2  $\Omega\cdot\text{mm}$ . Samples without a barrier layer then degraded when sintered at higher peak temperatures. The resistance of the barrier contacts with thin gold above the  $\text{ZrB}_2$  also increased after treatment at the higher peak temperatures. Samples with thick gold above the  $\text{ZrB}_2$  showed no significant change.

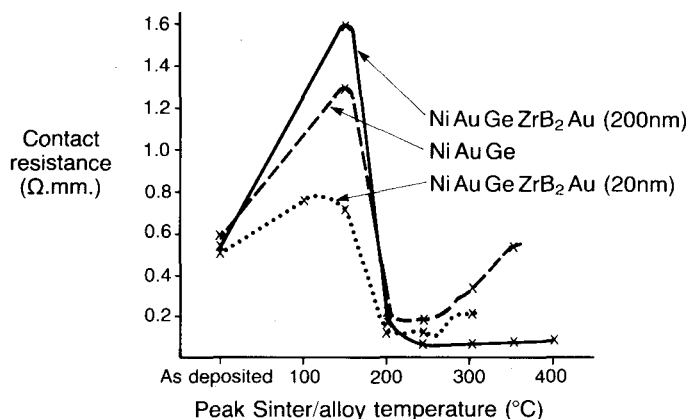


Fig. 5 Dependence of contact resistance on sinter/alloy temperature

### 3.3 Stability of contact resistance with thermal overstress

The average resistances of contacts subjected to extended periods at 300°C are shown in Fig. 6. Specimens without a barrier layer first increased by 108% and then decreased. After 100 h the resistance was still 73% above the initial value. The resistance of barrier ohmic contacts with thin gold above the  $\text{ZrB}_2$  were more stable, with a maximum change of only 28%. No degradation was observed for barrier contacts with thick gold above the  $\text{ZrB}_2$ . Indeed, the resistance values on these samples were always low and reproducible, partly due to better probe contact on the thicker gold, during measurement.

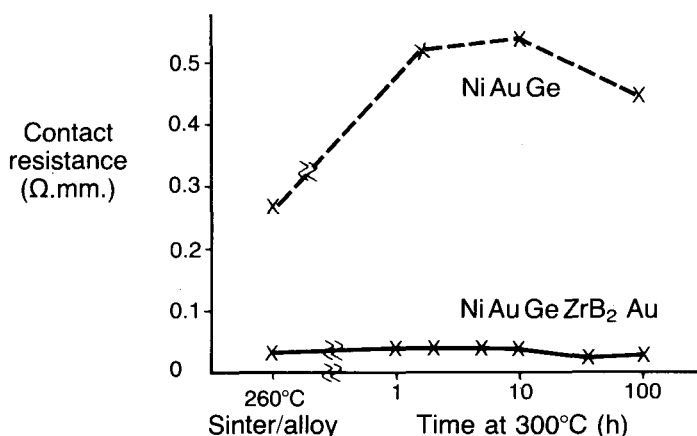


Fig. 6 Thermal stability of contacts

Thus, the use of a barrier layer gives much improved stability with thin or thick gold above it. The barrier also allows the use of thick gold metallisation, which may be required for probing or for direct bonding. Thin gold above the  $\text{ZrB}_2$  is entirely satisfactory in devices where additional metal is subsequently deposited over the ohmic contacts. This has been confirmed repeatedly and is illustrated by the J-FET characteristics shown in Figs. 7 & 8.

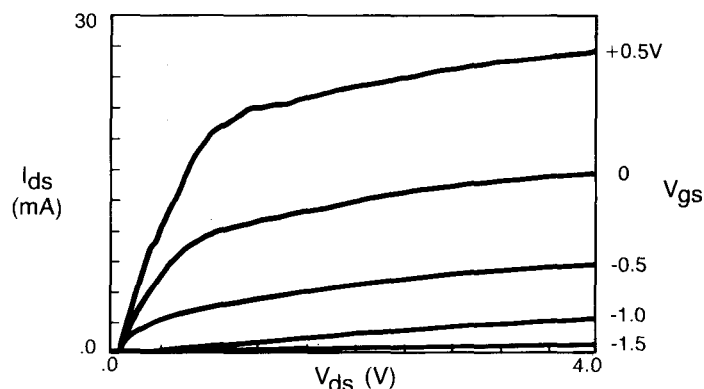


Fig. 7 J-FET Output characteristics

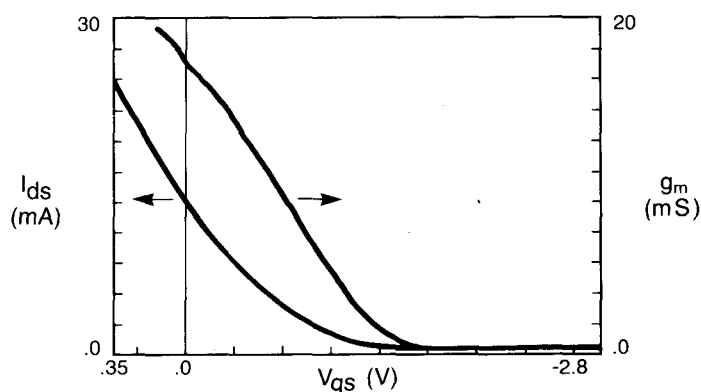


Fig. 8 J-FET drain transfer characteristics

### 3.4 Semiconductor and specific contact resistivities

The sheet resistivity ( $R_s$ ), of the semiconductor between the contacts, was calculated from the slope of the resistance measurements versus contact spacing (Fig. 3). This was then used, together with the measured thickness ( $t$ ) of the grown layer, to determine the bulk resistivity of the InGaAs:

$$\begin{aligned} \text{layer resistivity} &= R_s * t \\ &= 240 \, \Omega/\square * 0.3 \, \mu\text{m} \\ &= 7.2 * 10^{-3} \, \text{ohm.cm} \end{aligned}$$

For comparison, the resistivity of the InGaAs layer, measured on a Polaron plotter, was  $5.5 * 10^{-3} \, \text{ohm.cm}$ . Thus, the resistivity of the channel used in TLM is very close to that of the n-InGaAs and the assumptions of using just the InGaAs thickness to calculate specific contact resistivity are valid. The calculated value of the contact resistivity, using the TLM technique, was  $\approx 10^{-7} \, \Omega.\text{cm}^2$  [5,6].

#### 4. CONCLUSIONS

The best contacts, both morphologically and electrically, resulted from a 20% HCl dip followed immediately by deposition of Ni-Au-Ge-ZrB<sub>2</sub>-Au. These had contact resistance values of 0.33 ohm.mm as deposited and a minimum of 0.05  $\Omega$ .mm for a peak sinter/anneal temperature of 260°C. Contact stability and morphology were shown to be enhanced by use of the barrier layer. Samples with a barrier layer showed no significant change in contact resistance after 100 h at 300°C. The barrier contacts have been successfully used in fabricating J-FETs.

#### 5. ACKNOWLEDGEMENT

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#### 6. REFERENCES

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