Journal of
Nanoscience and Nanotechnology
Vol. 12, 3552–3554, 2012

# Top-Down Processed Silicon Nanowires for Thermoelectric Applications

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50 nm wide *n*-type silicon nanowires have been manufactured by using a top-down process in order to investigate the thermoelectric properties of silicon nanowire. Nanowire test structures with platinum heaters and temperature sensors were fabricated. The extracted temperature coefficient of resistance (TCR) of the temperature sensors was 786.6 PPM/K. Also, the extracted Seebeck coefficient and power factor of the 50 nm wide phosphorus doped *n*-type silicon nanowires were $-118\ \mu$V/K and 2.16 mW·K$^{-2}$·m$^{-1}$.

**Keywords:** Silicon Nanowire, Top-Down Process, Thermoelectricity, Seebeck Coefficient.

RESEARCH ARTICLE

## 1. INTRODUCTION

$Bi_2Te_3$ material has been widely used for thermoelectric generators operating at room temperature due to its high thermoelectric performance. Even though bulk silicon is a poor thermoelectric material, the feasibility of nanostructured silicon as thermoelectric material has been reported.

A thermoelectric generator creates an electric potential difference when there is a temperature gradient. The conversion efficiency of thermoelectricity can be expressed by the dimensionless figure of merit ZT, which is governed by material properties. ZT is defined as $ZT = \alpha^2\sigma T/\kappa$, where $\alpha$, $\sigma$, $\kappa$ and $T$ represent the Seebeck coefficient, electrical conductivity, thermal conductivity and absolute temperature, respectively.[1,2]

Until now, the widely used thermoelectric materials have been $Bi_2Te_3$ compounds for which ZT = 0.9 at 300 K.[3–5] The ZT of $Bi_2Te_3$ has been the upper limit for more than 40 years. However, due to the recent tendency for the development of products using $Bi_2Te_3$ thermoelectric devices, supplies of $Bi_2Te_3$ are predicted to face shortage, soon.

By contrast, silicon is the most abundant semiconductor material, and it enjoys a mature fabrication infrastructure. One drawback in the consideration of silicon as thermoelectric material is the low ZT value due to its high $\kappa$ value at room temperature.[6,7] Thus, silicon has been considered an inappropriate material for thermoelectric applications. However, low-dimensional materials such as thin film and nanowires have become attractive because of their potential application for thermoelectric and electronic devices. Hicks and Dresselhaus proposed a possible way to raise the ZT value higher than 1 using nanostructured materials.[8,9]

In this work, a top-down process is adopted to implement a silicon thermoelectric device. By using a conventional top-down process, we have manufactured 50 nm wide phosphorus doped *n*-type silicon nanowires. The electrical conductivities are evaluated using a 4-point probing method. Also, the Seebeck coefficient and power factor are evaluated from the manufactured silicon nanowires.

## 2. EXPERIMENTAL DETAILS

A ⟨100⟩ *p*-type 8 inch silicon-on-insulator (SOI) wafer was used to fabricate silicon nanowire thermoelectric devices. The SOI wafer was boron doped with a resistivity of 13.5~22.5 Ω·cm and the corresponding doping concentration was about $1.0 \times 10^{15}$ cm$^{-3}$. The thicknesses of the SOI and the buried oxide (BOX) layer are 100 nm and 2,000 nm, respectively. The SOI layer is thinned down to 40 nm using the thermal oxidation method. Phosphorus atoms are doped for *n*-leg formation using the ion implantation method. 160 nm wire patterns are defined by using the KrF lithography technique. After the photo lithography step, the $O_2$ plasma ashing technique is adopted to reduce the wire width down to 50 nm, as shown in Figure 1.

After the patterning of silicon nanowires using dry etching technique, 10 nm thick titanium and 50 nm thick

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1533-4880/2012/12/3552/003 doi:10.1166/jnn.2012.5580

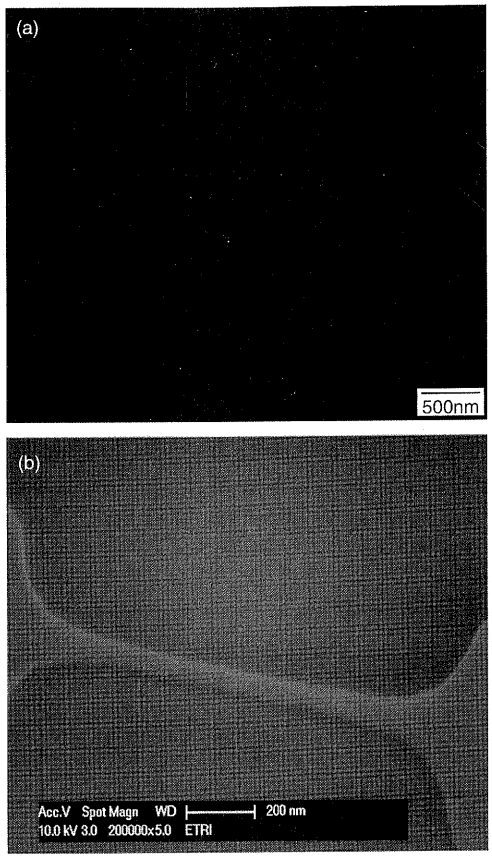


**Fig. 1.** (a) Optical microscope image of 50 nm wide and 40 nm thick silicon nanowire and (b) SEM image of 50 nm wide silicon nanowire manufactured by top-down process.

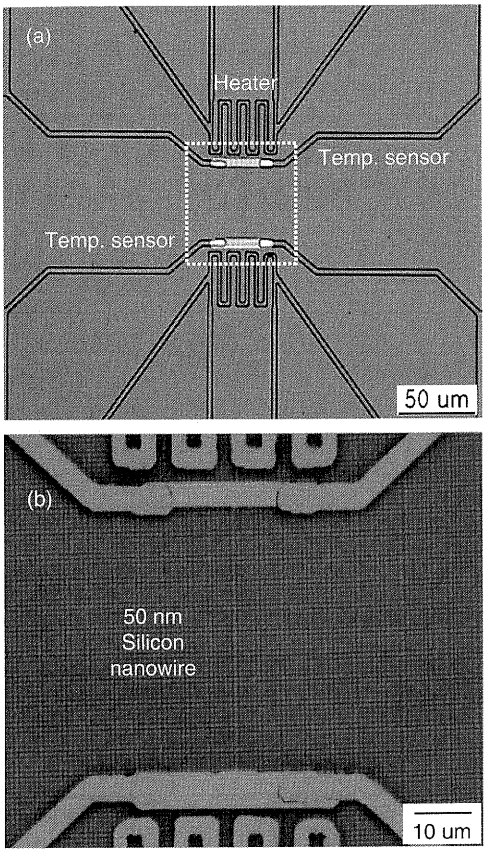


**Fig. 2.** Optical microscope images of the Seebeck voltage measurement pattern. (b) shows the enlarged image of the dotted square in (a).

platinum (Pt) layers are sputtered and patterned using the lift-off method. Titanium is used as an adhesion layer between the $SiO_2$ and Pt. The Pt layer is used as a heating source and temperature senor.

A semiconductor parameter analyzer (Model HP4156, Agilent Systems) was used for accurate resistance measurement. To decrease heat loss and thermal noise caused by air heat conduction, the measurement was performed in a vacuum of $10^{-5}$ Torr.

## 3. RESULTS AND DISCUSSION

Figure 2 shows the optical microscope image of the test pattern manufactured for Seebeck coefficient measurement of the 50 nm $n$-type silicon nanowire. The upper Pt line is used as a heating source. The designed width of the Pt line is 2 $\mu$m. The Pt lines in the middle regions are used as temperature sensors for the measurements of hot and cold temperature, respectively, as shown in Figure 2. Also, Seebeck voltage is measured across the silicon nanowire.

To determine the temperatures of the hot ($T_H$) and cold ($T_C$) sides, the temperature coefficient of resistance (TCR) values of upper and lower temperature sensors were measured, respectively. TCR is defined as in the following equation.

$$R = R_0 \cdot [1 + \mathrm{TCR} \cdot (T - T_0)] \quad (1)$$

In Eq. (1), $R$ and $T$ represent resistance and substrate temperature, respectively. $R_0$ and $T_0$ represent reference resistance and temperature, respectively. Thus, by measuring the variation of resistance as a function of temperature, TCR could be easily extracted. In Figure 2, the width of the Pt temperature sensor is 2 $\mu$m and the silicon nanowire length is 40 $\mu$m. Thus, we expect there would be no big error in the measurement of temperature.

Figure 3 shows the variation of resistance of the upper and lower temperature sensors as a function of substrate temperature. The closed circle and solid line represent measured data and linear extrapolation, respectively. The resistance value at a substrate temperature of 20 °C is about 2 kΩ. As shown in Figure 3, resistance increases linearly from 20 °C to 55 °C. From Figure 3, the extracted TCR value is 786.6 PPM/K.

Figure 4 shows the temperature difference between the hot ($T_H$) and cold ($T_C$) regions as a function of input current to the Pt heater. To make 1 K difference between the hot and cold regions through the silicon nanowire, an 8.8 mA input current to the Pt heater is necessary.

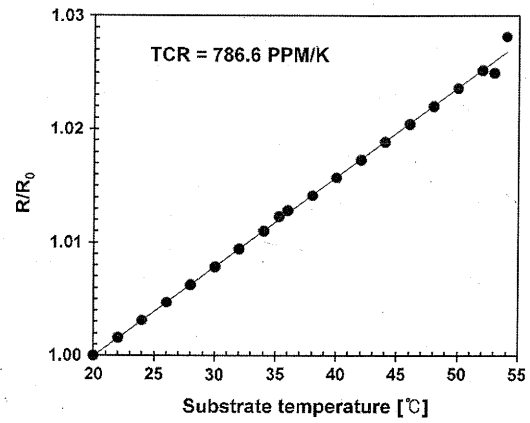


**Fig. 3.** The variation of resistance as a function of substrate temperature. The extracted TCR value is 786.6 PPM/K.

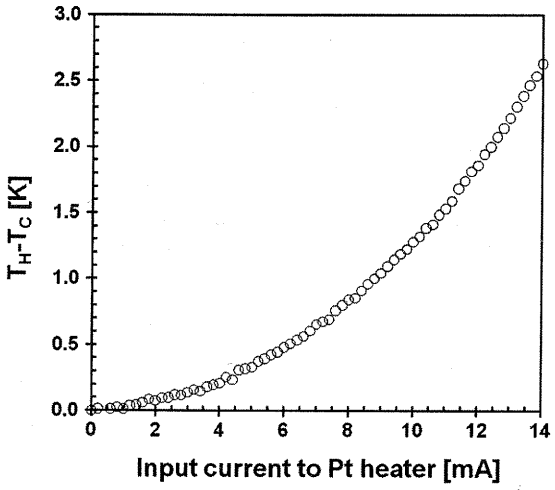


**Fig. 4.** Temperature difference between hot and cold region ($T_H$–$T_C$) with the variation of input current to Pt heater.

Figure 5 shows the output Seebeck voltage as a function of temperature difference between the hot and cold regions. The open circle and solid line represent the measured data and the linear extrapolation result, respectively. The extracted Seebeck coefficient ($S$) is $-118$ $\mu$V/K. From the electrical 4-point measurement, the extracted electrical conductivity ($\sigma$) is 1,553 $\Omega^{-1} \cdot cm^{-1}$. Thus, the power factor ($S^2 \cdot \sigma$) of 50 nm $n$-type silicon nanowire is 2.16 $mW \cdot K^{-2} \cdot m^{-1}$. The maximum power factor of $Bi_2Te_3$ is about 5 $mW \cdot K^{-2} \cdot m^{-1}$.[2] Silicon nanowire has a power factor value comparable with $Bi_2Te_3$. Thus, silicon nanowire could be considered as a possible candidate for thermoelectric applications.

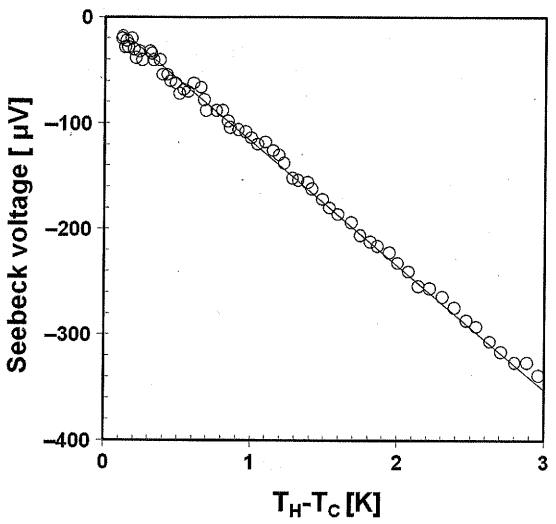


**Fig. 5.** Seebeck voltage as a function of temperature difference between hot and cold region ($T_H$–$T_C$). The extracted Seebeck coefficient is $-118$ $\mu$V/K.

## 4. CONCLUSIONS

Silicon nanowires were fabricated by using KrF photo lithography and $O_2$ plasma ashing techniques in order to investigate the thermoelectric properties of silicon nanowire. 50 nm wide $n$-type silicon nanowire test structures with platinum heaters and temperature sensors were fabricated. The extracted TCR value of the manufactured temperature sensor was 786.6 PPM/K. Also, the extracted Seebeck coefficient and power factor of the 50 nm wide phosphorus doped $n$-type silicon nanowire were $-118$ $\mu$V/K and 2.16 $mW \cdot K^{-2} \cdot m^{-1}$ By optimizing the power factor as the function of doping concentration and nanowire width, further enhancement of the power factor could be expected.

## References and Notes

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Received: 29 October 2010. Accepted: 21 January 2011.