EFFECT OF H_2 ANNEALING ON OXIDE INTEGRITY IMPROVEMENT

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ABSTRACT

H_2 annealing at 1150°C for 30min prior to oxidation improves the TDDB of 190A° gate oxides by achieving a low interstitial oxygen concentration region near the surface. However, a subsequent 2μm surface polishing completely eliminates the oxide integrity improvement. H_2 annealing also improves the BV_{ox} of 1000A° oxides, but retains ≈ 30% of B-mode type oxide breakdown failures, presumably due to the presence of D-defects. A subsequent 2μm surface polishing also completely removes the H_2 annealing BV_{ox} improvement. Finally, H_2 annealing dissolves oxygen precipitates, thereby, it improves oxygen precipitate induced oxide integrity degradation. Once again the effect is limited to a depth of ≈ 2μm.

INTRODUCTION

In VLSI/ULSI fabrication, the thin gate oxide integrity(GOI) is a key factor in achieving high yield and reliability of devices. There are many sources for GOI degradation such as grown-in defects[1-3], metallic impurities[4], and micro-roughness[5]. Recently, much effort has been made to eliminate micro-defects in the denuded zone, thereby improving GOI. One method often utilized for reducing micro-defects near the surface is hydrogen annealing above 950°C, which induces GOI improvement[6,7]. In addition, hydrogen annealing is expected to increase the activation energy for micro-defect nucleation by reducing the denuded zone interstitial oxygen concentration, which is particularly useful with MeV implantation and flash memory devices[8]. On the negative side, it has been reported that samples hydrogen-annealed at 1150°C exhibit micro-pitting which roughens the surface, causing GOI degradation[9,10]. In this study, the effect of hydrogen annealing on the micro-defect reduction is discussed, and the depth limit of the hydrogen annealing effect is investigated in detail.

EXPERIMENTAL

The wafers used were primarily p-type, 5 ohm-cm, 150mm diameter CZ Si with carbon concentrations below the instrument sensitivity limit. They were grown with a crystal pull rate of ≈1.5mm/min, yielding a D-defect density from 1 to $7x10^5 cm^{-3}$. Two

different initial oxygen concentrations, ≈11.5 and ≈15.6 ppma (ASTM 1986), were chosen in order to observe the effect of hydrogen annealing on interstitial oxygen diffusion. The detailed experimental flow is shown in Fig.1. A pre-annealing at 750°C for 20hrs was done in a horizontal furnace, followed by annealing at 1000°C for 10hrs in N_2 ambient. For removing the denuded zone completely, ≈ 50μm of the surface was etched off in $HF/HNO_3/CH_3COOH$, followed by polishing. Hydrogen annealing at 1150°C for 30min was done in an Epi-reactor. After hydrogen annealing, ≈2μm was polished from the surface of some wafers in order to investigate the depth limit of the hydrogen annealing effect. Two wafers for each condition in Fig.1 were oxidized. 200Å oxides were grown at 820°C in a dry O_2 ambient, while 1000Å oxides were done at 1000°C in a wet O_2 ambient. MOS capacitors with an area of $0.4cm^2$ were fabricated using aluminum electrodes. The BV_{ox} (time zero dielectric oxide breakdown) was defined as the applied voltage at which the leakage current reached $-25\mu A/cm^2$, and 66 capacitors per wafer were measured. It should be noted that the breakdown voltage for 1000Å oxides is very sensitive to the presence of D-defects while that for 200Å oxides is more sensitive to the presence of oxygen related defects[11]. The bulk oxygen precipitate density was measured by laser scattering tomography(LST), Model MO-411(Mitsui Mining & Smelting Co., Ltd). For wafers without a pre-annealing, the LST sampling volume was 500μm(depth)x2000μm(lateral scan)x6μm(laser beam dia.); whereas, for wafers with a pre-annealing, it was 200μmx200μmx6μm. The surface oxygen precipitate density was evaluated by bevel polishing at 1° 9' and Wright etching for 1min. The D-defect density(etch pits with a wedge-shaped flow pattern) and Secco etch pit density(etch pit without a wedge-shaped flow pattern) were measured following a non-agitated Secco etching for 5min at room temperature. The D-defect sampling volume was 2.5mm(x-axis

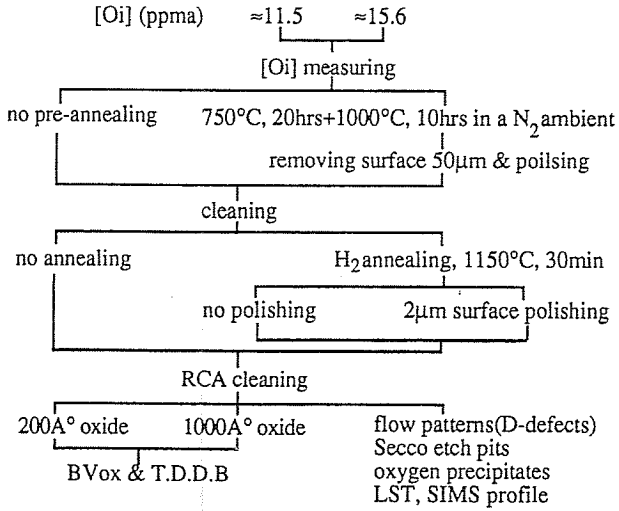

Fig.1. Experimental flow of present study

scan)x60mm(y-axis scan)x4μm(etched depth), while the Secco etch pit sampling was 250μm(y-axis scan)x4μm(etched depth). Interstitial oxygen concentration SIMS depth profiles across the denuded zone were obtained for three samples representing annealing at 1150 and 1200°C for in an H_2 and at 1200°C in an O_2 ambient for 1hr.

EXPERIMENTAL RESULTS

Oxide Integrity

A. Without a pre-annealing

Figures 2 (a) and (b) present 190Å BV_{ox} on low and high initial interstitial oxygen concentration [Oi] substrates as a function of H_2 annealing and subsequent 2μm surface polishing. Higher [Oi] leads to slightly lower BV_{ox}, which is almost independent of H_2 annealing and subsequent 2μm surface polishing. However, the TDDB of 190Å thick oxides depends strongly on [Oi], H_2 annealing, and subsequent 2μm surface polishing, as shown in Fig.3. Higher [Oi] leads to worse TDDB, while H_2 annealing at 1150°C for 30min improves TDDB. Note that the TDDB for wafers with subsequent 2μm surface polishing following H_2 annealing returns to the distribution observed for wafers without H_2 annealing.

Figures 4(a) and (b) present 1000Å BV_{ox} data as a function of [Oi], H_2 annealing and subsequent 2μm surface polishing. Recall that B-mode type oxide breakdown failures(3-8MV/cm) for 1000Å oxides have been attributed to the presence of substrate D-defects[11]. H_2 annealing significantly improves the 1000Å BV_{ox} between 2.5 and 3.3MV/cm(average ≈2.9MV/cm) which is attributed to the dissolution or shrinkage of D-defects by H_2. However, a B-mode type oxide breakdown failure of ≈ 30% still remains. Once again, the BV_{ox} for wafers with 2μm surface polishing following H_2 annealing recovers to that for wafers without H_2 annealing.

B. With a pre-annealing plus 50μm polishing

A pre-annealing at 750°C for 20hrs plus 1000°C for 10hrs in an N_2 ambient followed by 50μm surface removal produces an oxygen precipitate density in the 10^9 to 10^{10} cm^{-3} range. Figures 2(c) and (d) present the 190Å BV_{ox} for pre-annealed wafers as a function of [Oi], H_2 annealing and subsequent 2μm surface polishing. A pre-annealing drastically decreases the 190Å BV_{ox} between 6.1 and 6.5MV/cm(average ≈ 6.3MV/cm), compare Figs.2(c) and (d) with Figs.2(a) and (b); whereas, H_2 annealing greatly improves the 190Å BV_{ox} between 5.85 and 6.05MV/cm(average ≈ 5.9MV/cm), as shown in Figs.2(c) and (d). Again, 190Å BV_{ox} for wafers with 2μm surface polishing following H_2 annealing returns to that for wafers without H_2 annealing.

Figures 4(c) and (d) presents 1000Å BV_{ox} for pre-annealed wafers as a function of H_2 annealing and subsequent 2μm surface polishing. A pre-annealing significantly decreases the 1000Å BV_{ox} between 2.6 and 2.8MV/cm(≈ 2.7MV/cm), compare Figs.4(c) and (d) with Fig.4(a) and (b). H_2 annealing significantly improves the 1000Å BV_{ox} between 4.1 and 4.5MV/cm(average ≈ 4.3MV/cm), due to the dissolution of D-defects and oxygen precipitates. As before, the 1000Å BV_{ox} for wafers with 2μm surface polishing following H_2 annealing returns to that for wafers without H_2 annealing.

Micro-defects Distributions

Table 1 presents the bulk oxygen precipitate(O/P) density, determined via laser scattering tomograph as a function of [Oi], pre-annealing, H_2 annealing, and subsequent 2μm surface polishing. As expected, higher [Oi] leads to higher bulk O/P density, and a pre-annealing drastically increases the bulk O/P density. Note that H_2 annealing does not change the bulk O/P density. Table 2 presents the D-defect density within ≈ 4μm from the surface. Both pre-annealing and H_2 annealing do not change the D-defect density. Table 3 presents the Secco etch pit, i.e., etch pits without wedge shaped flow pattern, density near the surface. For wafers without pre-annealing, the Secco etch pit density is less than the detection limit of $<1.2x10^6 cm^{-3}$. Otherwise, for wafers with pre-annealing, higher [Oi] leads to higher Secco etch pit density, indicating that Secco etch pits are O/Ps within ≈ 4μm from the surface. H_2 annealing reduces the Secco etch pit density by an order of magnitude, while Secco etch pit density for wafers with subsequent 2μm surface polishing following H_2 annealing recovers to that for wafers without H_2 annealing. Figures 5(a), (b), and (c) present optical micrographs of the surface O/P distribution as a function

Table 1. Bulk oxygen precipitate density [cm^{-3}] as a function of annealing and polishing

annealing condition \ [Oi]	≈11.5 ppma	≈15.5 ppma
as-grown	$1.4x10^6$	$3.0x10^6$
H_2 ann.	$1.5x10^6$	$3.9x10^6$
H_2 ann. + 2μm pol.	$1.6x10^6$	$3.2x10^6$
pre-ann.	$5.1x10^8$	$2.1x10^{10}$
pre-ann.+H_2 ann.	$5.4x10^8$	$2.2x10^{10}$
pre-ann.+H_2 ann.+2μm pol	$8.9x10^8$	$2.1x10^{10}$

Table 2. D-defect(Flow Pattern) density [cm^{-3}] as a function of annealing and polishing

annealing condition \ [Oi]	≈11.5 ppma	≈15.5 ppma
as-grown	$2.5x10^5$	$6.5x10^5$
H_2 ann.	$2.3x10^5$	$7.2x10^5$
H_2 ann. + 2μm pol.	$3.2x10^5$	$6.6x10^5$
pre-ann.	$1.5x10^5$	rough surface
pre-ann.+H_2 ann.	$2.6x10^5$	$5.6x10^5$
pre-ann.+H_2 ann.+2μm pol	$2.6x10^5$	$6.8x10^5$

*Non-agitated Secco etching for 5 min.

Table 3. Secco etch pit density [cm^{-3}] as a function of annealing and polishing

annealing condition	≈11.5 ppma	≈15.5 ppma
as-grown	N.D($< 2x10^6$)	N.D
H_2 ann.	N.D	N.D
H_2 ann. + 2μm pol.	N.D	N.D
pre-ann.	$2.9x10^8$	$5.0x10^{10}$
pre-ann.+H_2 ann.	$1.7x10^7$	$7.9x10^9$
pre-ann.+H_2 ann.+2μm pol	$2.1x10^8$	$1.1x10^{10}$

of H_2 annealing and subsequent 2μm surface polishing for samples bevel polished and Secco etched. A pre-annealing followed by 50μm surface removal completely eliminates the denuded zone, resulting in the uniform distribution of O/Ps shown in Fig.5(a). H_2 annealing dissolves O/Ps within ≈2μm of the surface, see Fig.5(b); therefore, a subsequent 2μm surface polishing eliminates the region in which O/Ps were dissolved, as shown in Fig.5(c). Figure 6 presents the O/P depth profile from the surface, measured from Fig.5. For the pre-annealed wafer, O/Ps are uniformly distributed. For the hydrogen annealed wafer, the O/P density drastically decreases toward the surface. However, the subsequent 2μm surface polishing eliminates the low O/P region near the surface, thus, the O/P density slightly increases with depth. It should be noted that the O/P density for the hydrogen annealed wafer is less than that for wafers with subsequent 2μm surface polishing following H_2 annealing.

Interstitial Oxygen Concentration[Oi] Profile

Figure 7 presents [Oi] profiles as a function of annealing gas ambient and temperature. For annealing at 1200°C, near-surface [Oi] for wafers annealed in an H_2 ambient is lower than that for wafers annealed in an O_2 ambient. For the H_2 ambient, higher annealing temperature leads to lower near-surface [Oi] . The out-diffusion of interstitial oxygen from the bulk to the surface can be expressed by [12]

$$C(x,t) = Cs + (Cb - Cs)erf[\frac{x}{2\sqrt{Do * t}}] \quad (1)$$

where C_s is the interstitial oxygen concentration at the surface, C_b is the concentration in the bulk, and D_o is the oxygen diffusivity. Fitting the SIMS interstitial oxygen concentration profiles with Eqn.(1) yields C_s for each annealing ambient, as shown in Table.4. C_s for wafers annealed in a H_2 ambient is much lower than that for wafers annealed in an O_2 ambient. In addition, the diffusivity of interstitial oxygen, D_o, for H_2 annealed wafers obtained for this work was 17.58exp(-2.97eV/kT).

Table.4. C_s and C_b depending on annealing ambient

annealing condition	C_s(cm^{-3})	C_b(cm^{-3})
H_2, 1200°C, 1hr	< 1x10^{10}	≈ 1.53x10^{18}
O_2, 1200°C, 1hr	≈ 1x10^{17}	≈ 1.23x10^{18}

DISCUSSION

Investigating the BV_{ox} dependence on oxide thickness(Tox) is a convenient mechanism for separating the origin of oxide breakdown failures, since D-defects and oxygen precipitates exhibit a different BV_{ox} dependence on Tox[11]. As shown in Fig.8, for Tox from 200 to 2000Å, BV_{ox} due to the presence of D-defects decreases with increasing Tox up to ≈ 1000Å, and then increases with further increase in Tox. On the other hand, the oxide breakdown degradation due to the presence of oxygen precipitates attenuates with increasing Tox above 200Å, see Fig.9. Thus, the 200 or 1000Å BV_{ox} distribution will differentiate oxide breakdown failures due to the presence of D-defects from those due to oxygen precipitates. For wafers without pre-annealing, H_2 annealing improves both the

190Å TDDB and the 1000Å BV_{ox} by dissolving both oxygen precipitates and D-defects, but is only effective to a depth of ≈ 2μm. It must be emphasized that H_2 annealing for as-grown wafers improves 1000Å BV_{ox} ≈ 2.9MV/cm by mainly dissolving or shrinking D-defects near the surface. A pre-annealing followed by removing the denuded zone drastically degrades oxide integrity, which is a function of oxide thickness; i.e. the oxygen precipitate induced BV_{ox} degradation is ≈ 6.3 and ≈ 2.7MV/cm for 190 and 1000Å, respectively, which is very consistent with our previous studies, as shown in Fig.9. Also, for wafers with pre-annealing, H_2 annealing improves 190 and 1000Å BV_{ox}, but subsequent 2μm surface polishing eliminates the H_2 annealing effect. In addition, it is evident that H_2 annealing for pre-annealed wafers increases 190Å BV_{ox} ≈ 5.9MV/cm, mainly by dissolving oxygen precipitates, while it increases 1000Å BV_{ox} ≈ 4.3MV/cm by dissolving oxygen precipitates and dissolving or shrinking D-defects near the surface.

The detailed [Oi] profile in Fig.7 for H_2 annealed wafers enables us to understand the H_2 effect on 190Å TDDB. Recall that 190Å oxide growth consumes ≈ 84Å of Si. There are two possibilities for achieving low[Oi] within ≈ 84Å of the surface during H_2 annealing; i.e., hydrogen enhanced interstitial oxygen diffusivity and a high concentration gradient driving force for interstitial oxygen out-diffusion due to a very low C_s. A number of interstitial oxygen diffusivities[13-19] have been reported. Zhong et al noted that H_2 annealing enhances the interstitial oxygen diffusivity in Si[20]. Figure 10 presents the simulated surface [Oi] profile with various interstitial oxygen diffusivities for wafers annealed at 1150°C for 30min in an H_2 ambient, where C_s and C_b were assumed to be ≈ 1.0x10^{10} and 1.2x10^{18}cm^{-3}, respectively. The hydrogen enhanced interstitial oxygen diffusivity does not significantly change [Oi] within ≈ 84Å of the surface compared to interstitial oxygen diffusivity in an O_2 ambient (Mikkelson's diffusivity[15]). However, a low [Oi] within ≈ 84Å of the surface can be obtained by achieving very low C_s during H_2 annealing. First of all, H_2 annealing results in very low C_s, explained by considering chemical interaction of H_2 with SiO_2. The etching rate of SiO_2 at 1150°C in an Epi reactor is ≈ 4.5Åmin, see Fig.11 while the measured native oxide thickness for as-grown wafers was ≈ 11A°. Thus, H_2 annealing at 1100°C removes the native oxide within ≈ 3min allowing C_s to approach zero, similar to inert gas ambient, see Fig.12(a). On the other hand, O_2 annealing under 1 atm of pressure grows an oxide from the Si/SiO_2 interface, which pins C_s to the solubility of interstitial oxygen in bulk Si, i.e. ≈ 1x10^{17}cm^{-3}, see Fig.12(b). Since C_s for H_2 annealed wafers is very low, a higher driving force for near-surface interstitial oxygen out-diffusion exists compared to O_2 annealed wafers. As a result, H_2 annealed wafers produces an interstitial oxygen concentration of < 6x10^{14}cm^{-3} within ≈ 84Å of the surface, as shown in Fig.13, which is ≈ two orders of magnitude lower than that for O_2 annealing. However, the [Oi] at a depth of ≈ 2μm for H_2 annealed wafers approaches ≈ 1x10^{17}cm^{-3}, as shown in Fig.14, explaining why a subsequent 2μm surface polishing following a H_2 annealing eliminates the H_2 annealing improvement on 190Å TDDB.

Oxygen precipitate dissolution during H_2 annealing enables us to understand the beneficial H_2 annealing effects on 190 and 1000Å BV_{ox} for pre-annealed wafers. Oxygen precipitates in the denuded zone degrade GOI due to the presence of oxygen precipitate induced stresses[11]. Since H_2 reacts chemically with bulk oxygen precipitates at 1150°C, precipitate dissolution occurs via the out diffusion of H_2O gas, see Fig.5; thus, H_2 annealing improves oxide integrity for pre-annealed wafers, see Figs 2 and 4. However, since H_2 diffusion into the bulk follows complementary error function, the dissolution rate of oxygen precipitates decreases deeper into Si bulk, allowing an oxygen precipitate density increase with depth, as shown in Figs.5(b) and 6. A subsequent 2μm surface polishing

removes the region with a low oxygen precipitate density, see Fig.5(c), resulting in eliminating the H_2 annealing effect on oxide integrity improvement.

D-defects are cavities[21,22] which exhibit a minimum BV_{ox} for Tox of ≈ 1000Å due to the presence of local oxide thinning and oxidation induced stresses at the defect site[11]. H_2 annealing significantly improves 1000Å BV_{ox} for those wafers without pre-annealing, but still retains a D-defect induced B-mode type BV_{ox} failure rate of ≈ 30%. As before, the H_2 annealing benefits on 1000Å BV_{ox} is limited to the depth of ≈ 2μm. Two possible ways for H_2 annealing to improve 1000Å BV_{ox} are either dissolution or shrinkage of D-defect near the surface. The shrinkage of D-defects increases the capping Si layer above the defect, reducing local oxide thinning at the defect site during oxidation and improving 1000Å BV_{ox}, which is similar to wafers grown with slow pull rate[23]. Since H_2 annealing in an Epi-reactor doesn't reduce the D-defect density ≈ 4μm from the surface, see Table 2, the D-defect shrinkage might be the dominant effect on 1000Å BV_{ox} improvement. Generally, H_2 annealing etches the native oxide on the Si surface and induces surface roughening by complexing with surface Si atoms. Thus, it can be hypothesized that interstitial silicon near the surface tends to diffuse into the surface via Frankel defect formation to reduce the surface energy allowing an increase in the equilibrium vacancy concentration in the matrix during H_2 annealing; then, diffusing interstitial into the surface may shrink D-defects. However, the D-defect shrinkage within ≈ 2μm is very difficult to observe using conventional techniques, requiring development of a new technique.

CONCLUSION

H_2 annealing produces a surface region containing reduced interstitial oxygen concentration by achieving a low C_s, yielding an oxide integrity improvement. However, the H_2 annealing effect on oxide integrity is limited to a depth of ≈ 2μm, since [Oi] beyond ≈ 2μm in H_2 annealing approaches [Oi] during O_2 annealng. H_2 annealing dissolves oxygen precipitates and shrinks D-defects, but the H_2 annealing effect on as-grown defect dissolution is also limited to the depth of ≈ 2μm. Therefore, H_2 annealing will be useful in devices with shallow junction and high energy implantation, since it gives a low [Oi] region which can release oxygen precipitates pile up[8] and suppress defect formation in a high energy implantation. However, a strong intrinsic gettering effect by a H_2 annealing itself can not be expected, since the H_2 annealing effect is limited to the depth of ≈ 2μm, which requires an optimization of initial [Oi] and thermal treatments in device fabrication.

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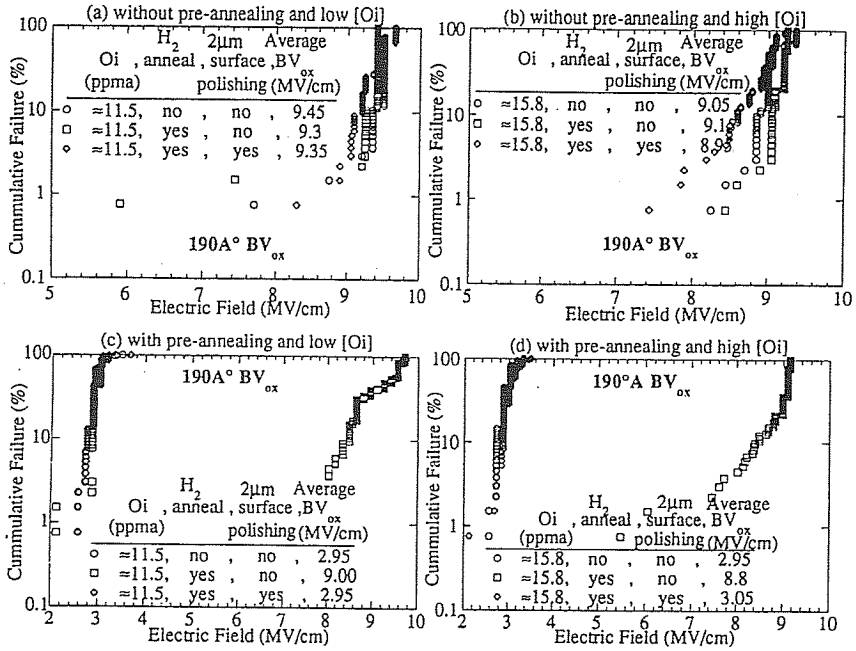

Fig.2. 190Å BVox as a function of [Oi], pre-annealing, H_2 annealing, and subsequent 2μm polishing.

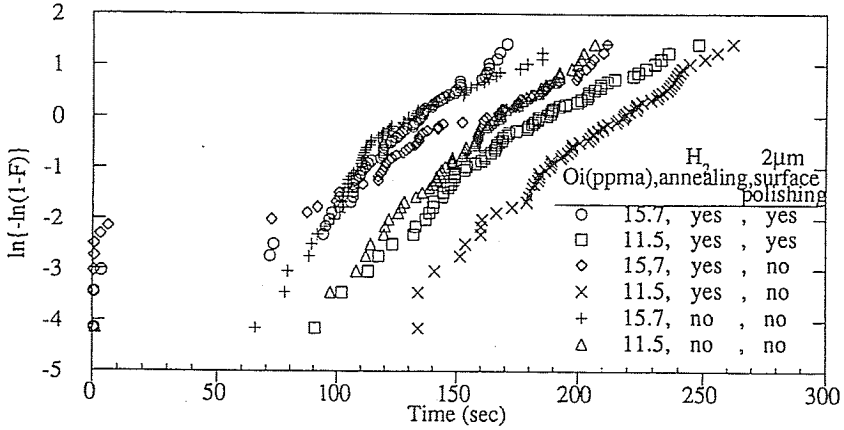

Fig.3. 190Å TDDB as a function of [Oi], H_2 annealing, and subsequent 2μm polishing.

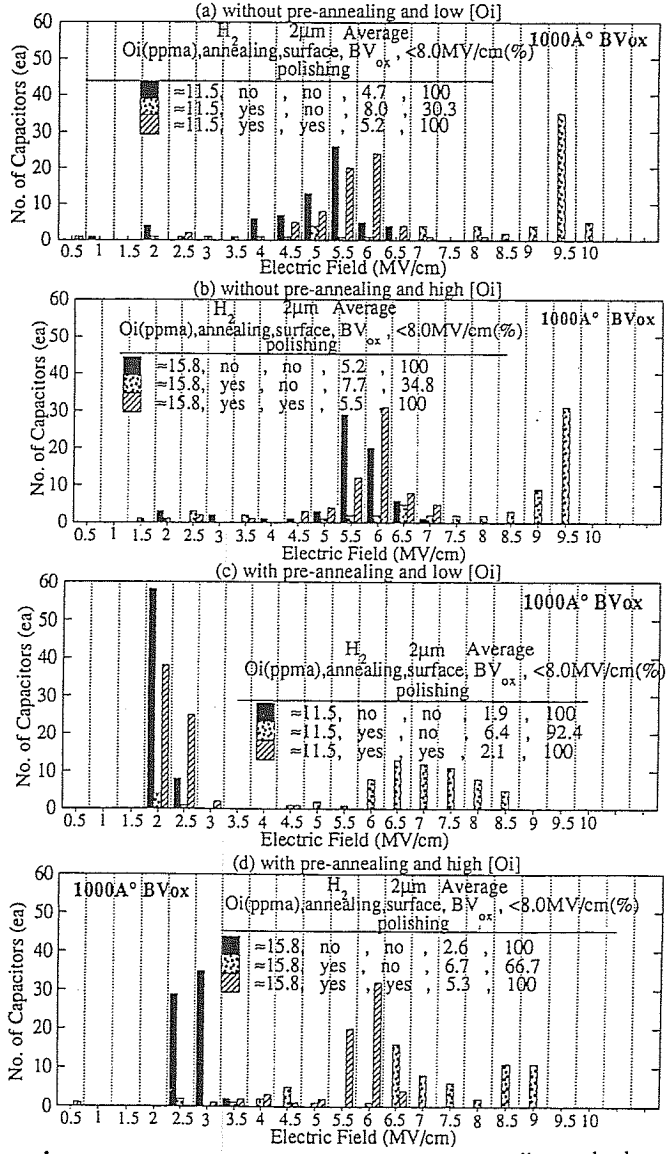

Fig.4. 1000Å BVox as a function of [Oi], pre-annealing, H_2 annealing, and subsequent 2μm polishing

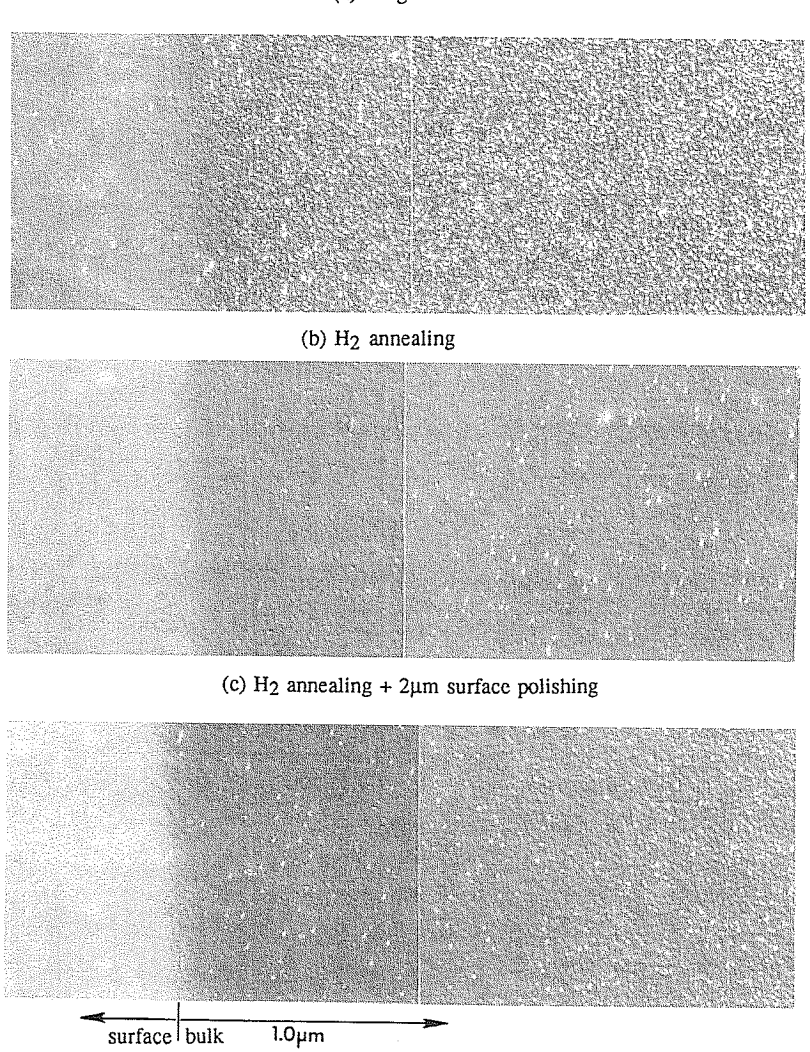

Fig.5. Surface oxygen precipitate distribution on bevel polished and Secco etched samples as a function of H_2 annealing and subsequent 2μm polishing. [Oi] for used wafers were ≈15.8 ppma.

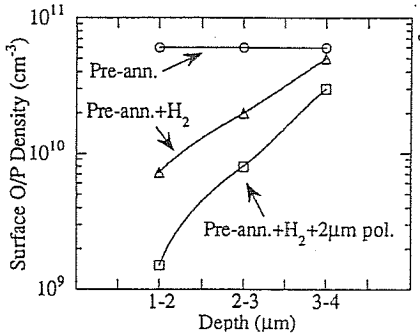

Fig.6. O/P profile as a function of H_2 annealing and 2μm polishing.

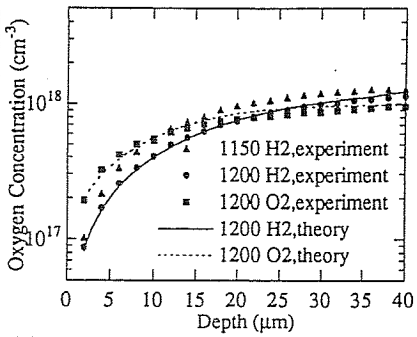

Fig.7. [Oi] SIMS profile as a function of annealing ambient and temperature.

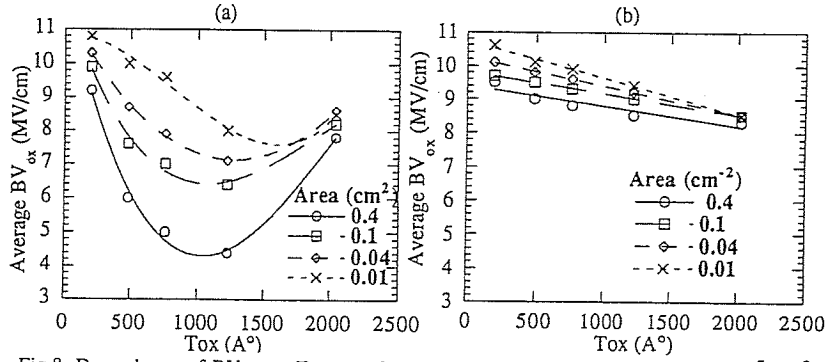

Fig.8. Dependence of BV_{ox} on Tox as a function of the D-defect density. (a) ≈ $2x10^5 cm^{-3}$ and(b) ≈$1x10^3 cm^{-3}$.

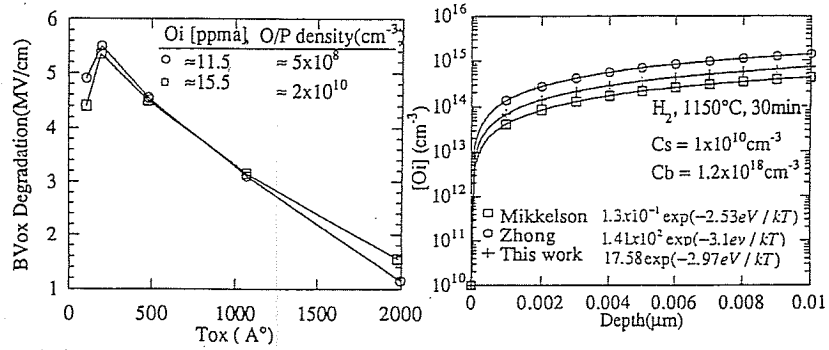

Fig.9. BV_{ox} degradation due to the presence of O/Ps as a function of Tox.

Fig.10. Simulation of oxygen diffusivity dependence on [Oi].

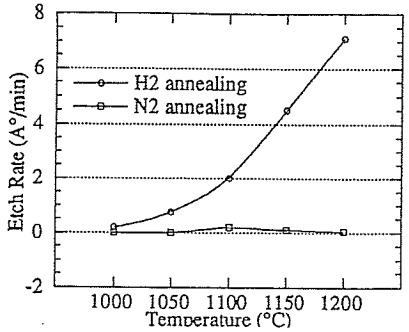

Fig.11. SiO_2 etch rate in an Epi-reactor.

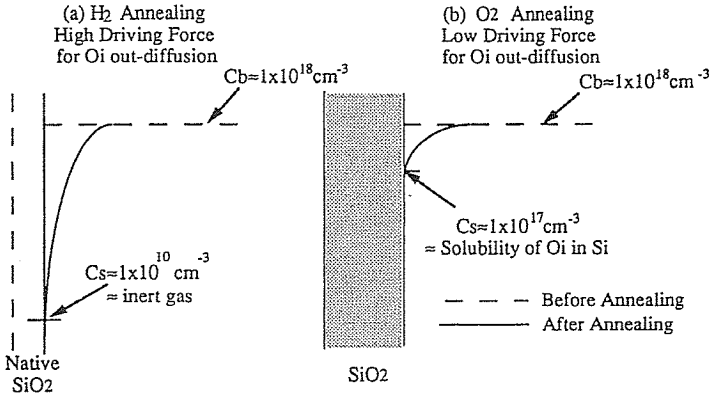

Fig.12. Schematic illustration showing the oxygen out-diffusion.

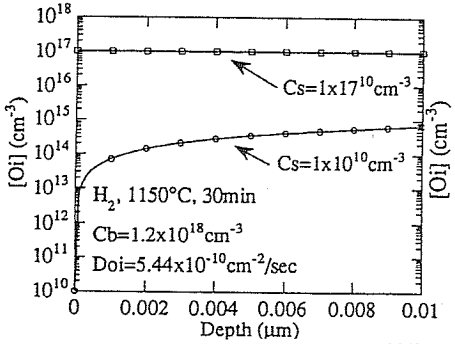

Fig.13. Simulation of Cs dependence on [Oi] near the surface.

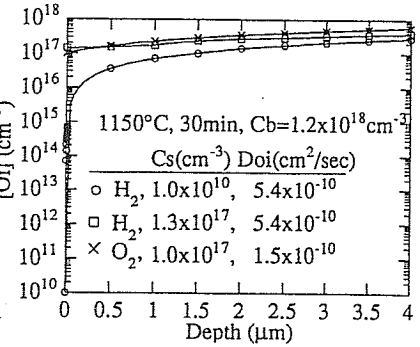

Fig.14. Simulation of Cs dependence on [Oi] in the bulk.

GATE OXIDE INTEGRITY IN DRAM DEVICES : THE INFLUENCE OF SUBSTRATE D-DEFECTS

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ABSTRACT

The presence of D-defects in as-grown CZ Si directly affects the gate oxide integrity in D-RAM devices. D-defects have been identified as cavities in as-grown wafers and subsequently appear as shallow etch pits during DRAM process. These D-defect induced etch pits degrade the gate oxide integrity by causing oxide thinning and roughening of the Si/SiO_2 interface. Defect engineering via interstitial silicon injection using dry oxidation at 1200°C for 2hr improves the gate oxide integrity by dissolving the D-defects near the surface. Also, a dry/wet oxidation mixture improves the gate oxide integrity by alleviating the oxide thinning at the convex edge of the D-defect induced etch pits.

INTRODUCTION

Recently, much effort has been made in characterizing the effect of as-grown defects on gate oxide integrity (GOI), particularly D-defects(etch pits with wedge shaped flow patterns in non-agitated Secco etching), oxygen precipitates, and Laser Scattering Tomography defects(LSTDs)[1-3]. In addition, separation of surface particles from as-grown defects after SC1 cleaning has been extensively researched[4-6]. We have presented[7-9] detailed X-TEM data on the nature of D-defects in CZ Si via a one-to-one correlation of MOS/EBIC breakdown sites which revealed the D-defects to be cavities of 0.25 to 0.5μm in diameter. These defects induce large variations in oxide thickness(Tox) around the defect site, as shown in Fig.1. The D-defect related oxide breakdown (BV_{ox}) depends strongly on oxide thickness, peaking at ≈ 1000Å, see Fig.2. When the oxide collapses into the D-defect, shallow etch pits form prior to gate oxide growth in DRAM devices. An illustration from a completed D-RAM process is shown in Fig.3. Because of the difficulties inherent in examining low volume density micro-defects, it has been debated[3,6] which as-grown defect, D-defects or LSTDs, is the dominant source for gate oxide integrity degradation. Both defect densities are known to be bulk related since they each increase with crystal pull rate which leads to higher GOI failures[1,10]. However, the D-defect induced BV_{ox} dependence on Tox can be used to distinguish it from LSTDs. As shown in Fig.2, the D-defects exhibit the lowest average BV_{ox} for Tox of ≈ 1000Å. In addition, the D-defect density is significantly reduced by interstitial silicon injection[1]. On the other hand, interstitial injection does not change the LSTD density[10]. We confirmed the different nature between D-defects and LSTDs using a mask to prevent interstitial silicon injection on half of a wafer, as shown in Fig.4. It is evident that interstitial injection via oxidation significantly reduces the D-defect density(solid circles), improving the BV_{ox} for Tox of ≈