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Chapter 15

SILICON FOR SOLAR CELLS

T.F. CISZEK

Solar Energy Research Institute, Golden, Colorado USA 80401

Contents

1. Introduction

Crystalline silicon has a number of qualities that make it one of the most desirable materials for terrestrial photovoltaic applications. Some of the main ones are its (1) abundance, (2) established technology base, (3) favorable electrical transport properties, (4) relative salubrity, (5) unique oxidation characteristics, and (6) demonstrated high photovoltaic energy conversion efficiencies. Silicon is obtained from quartzite, the most plentiful mineral in the earth's crust. Table 1 shows the relative abundance of silicon and other materials that could have relevance as components of active photovoltaic materials.

The worldwide industrial production capacity of metallic silicon for all uses exceeds 2 million tons per year. Most of it is used in the steel and aluminum industries, and only about 1% is converted to high-purity semiconductor-grade silicon. It is important that a solar cell material be abundant, because replacing even 10% of conventional electrical power generation with photovoltaic power generation requires about 40 million tons of crude silicon — 20 times the current total metallic silicon capacity, and about 80 times the current crude or elemental metallurgical-grade silicon production capacity. (About 75% of the

Table 1
Abundance in the earth's crust of some photovoltaic materials.

Element	Weight (%)
Si	27.7
Al	8.1
Mg	2.1
P	0.1
S	0.05
Zn	0.01
Cu	0.007
Ga	0.002
Ge	0.0007
As	0.0005
Sb	0.0001
Cd	0.00002
In	0.00001
Se	0.000009
Te	0.0000002

total metallic silicon capacity consists of alloys with iron and other metals.)

The technology base for semiconductor silicon has evolved over the past 35 years. Therefore, a large body of knowledge now exists on materials preparation and handling, materials compatibility, crystal growth, materials properties, defect characteristics, device fabrication, and reliability. The compatibility of silicon dioxide films with crystalline silicon has been an important part of this evolution, because of the device processing functions they serve and also because of their surface passivation characteristics. Generally, other semiconductor systems lack this feature. Another factor that has contributed to the fast development and widespread use of semiconductor silicon is its extremely low toxicity compared with components of other semiconductors.

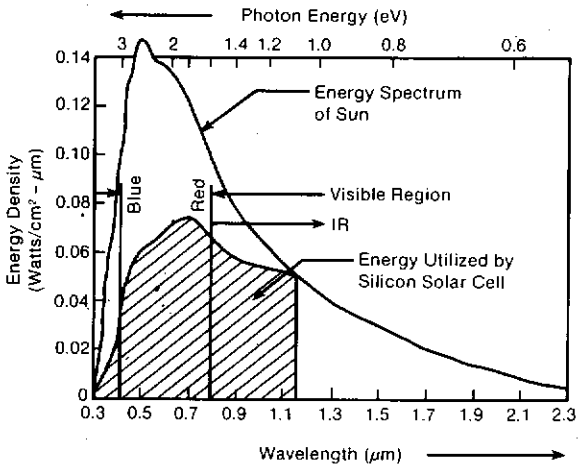

Fig. 1. Portion of the solar spectrum utilized by a silicon cell.

In a solar cell, sunlight is converted directly into electricity. The full solar spectrum cannot be utilized because photons possessing an energy less than the semiconductor's bandgap cannot excite conduction electrons. On the other hand, photons with energy greater than the bandgap create thermal energy and thus are not utilized to their fullest capacity. These considerations indicate that a semiconductor having a bandgap near 1.5 eV is the most efficient one for solar energy conversion. The gap for silicon is 1.1 eV, and the portion of the solar spectrum that it can utilize is shown in fig. 1. We can see that about 44% of available solar energy is utilized by a silicon solar cell. Because of fundamental limitations in the mechanism of cell operation, theoretically only about half of this energy can be realized at the output terminals of a working device. Thus, the theoretical conversion efficiency of a silicon solar

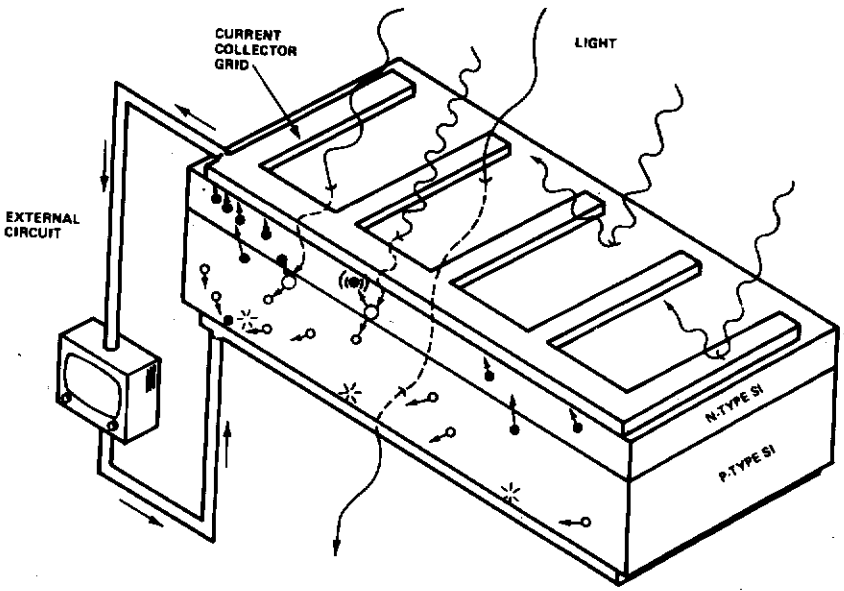

Fig. 2. Schematic of silicon solar cell operation.

cell is about 22%. To date, efficiencies of 19% have been obtained on actual 4 cm^2 experimental cells operating at air mass 1. In principle materials like InP, CdTe, and GaAs should have greater efficiencies since their bandgaps are in the 1.3–1.5 eV range. Somewhat higher efficiencies have been obtained for GaAs.

The functioning of a solar cell is illustrated schematically in fig. 2. The device shown is a large-area diode of n on p design. Junction depths of 0.2–0.5 μm are usually used, and the top of the cell is contacted by an ohmic grid with about 5% area coverage. The back of the cell has a large area ohmic contact. Photon-generated carriers are propelled toward the surfaces by the drift field at the p/n junction. If excessive defects or impurities are present in the crystal, some of these carriers will be trapped and this will detract from the cell's output current. This is one loss mechanism. A few of the others are schematically indicated in the figure (surface reflection, grid reflection, thermal energy loss due to short wavelength photons, and transmission of long wavelength photons). The cell voltage is typically between 0.5 and 0.7.

2. Conventional silicon technology

The main steps that precede and follow crystal growth in current silicon technology are shown in fig. 3. It can be seen that the silicon is transformed from a rather crude low-cost material to high-purity, high-perfection polished wafers that sell at a substantially higher price. The high cost is not a major concern for most device applications. However, for large-scale photovoltaic use, cost is a significant factor. The silicon process steps shown in fig. 3 are reviewed here to gain insight into conventional procedures. Then, possible alterations in keeping with solar cell requirements are discussed.

The steps shown in fig. 3 are applied to extract, purify, crystallize, and shape silicon into a material with useful electronic properties for semiconductor devices. The first step is reduction of silicon dioxide with carbon in an arc furnace. A schematic of the arc furnace process is shown in fig. 4. Commercial furnaces use about 10–30 MW of electrical energy to power carbon electrodes 1 m in diameter. They can produce on the order of 20 000 tons of silicon per year. Coke, coal, wood chips, and other forms of carbon are used as carbothermic reductants. In simple terms, the reduction reaction can be expressed as

$$SiO_2 + 2C = Si + 2CO. \quad (1)$$

However, a complex series of reactions actually takes place in the different temperature regions of the furnace. Some of these are

$$SiO_2 + C = SiO + CO, \quad (2)$$

$$SiO + 2C = SiC + CO, \quad (3)$$

$$SiC + SiO_2 = Si + SiO + CO. \quad (4)$$

The arc furnace process produces metallurgical silicon 98–99% pure. Typical impurities and levels are Fe, 0.3–1%; Al, 0.1–0.5%; Ca, 0.01–0.4%; C, Mn, Cr, Ni, V, Ti, and Mg, 0.01–0.04%; and B, P, Cu, and Zr, < 0.004%. Semiconductor-grade silicon requires purity levels at least in the low ppma range, and many impurities must even be in the ppba range. Therefore, purification of the silicon is necessary. To purify it, the metallurgical-grade silicon is first converted to trichlorosilane ($SiHCl_3$) by reacting it with HCl in a fluidized bed at a temperature of about 300°C:

$$Si + 3HCl = SiHCl_3 + H_2. \quad (5)$$

The liquid trichlorosilane has a boiling point of 33°C and can be purified by distillation. After purification, the major impurity becomes silicon tetrachloride at < 0.01%. Hydrocarbon levels are less than 5 ppmw.

The purified liquid trichlorosilane must now be converted back to high-purity elemental silicon. This is done by passing it and hydrogen over the surface of hot silicon rods where decomposition and chemical vapor deposition take place according to

$$SiHCl_3 + H_2 = Si + 3HCl. \quad (6)$$

This process is shown schematically in fig. 5 and is carried out at temperatures in the 900–1100°C range. The silicon forms in a cylindrical shape at a rather slow deposition rate (< 1 mm/h). Major

residual impurities in such "poly rods" are carbon and oxygen at $< 10^{16}$ atoms/cm^3. Dopants such as boron and phosphorus are present in concentrations of less than 5×10^{12} atoms/cm^3 in a well-controlled deposition process. Long rods of this type are used as feed material for float-zone crystal growth, while large-diameter pieces and broken chunks are used in Czochralski growth.

Crystal growth is necessary to convert the high-purity, small-grain-size polycrystalline material into dislocation-free single crystals. The Czochralski growth method is the most widely used and best-known technique. Hence, only a brief description, along with its current status, is presented here. Silicon is melted in a quartz crucible at temperatures slightly above 1412°C, the silicon melting point. Current technology generally employs graphite resistance heaters operating at input power levels up to 150 kVA, crucible diameters ranging from 30–40 cm, and silicon charge sizes of 20–60 kg. The crucible rotates and is moved upward during growth. Crystal growth is initiated at the free melt surface, on the crucible axis, by inserting a small diameter seed crystal into the liquid and then moving it upward to solidify silicon on the seed. Temperature and pulling speed are adjusted to first neck the crystal diameter down to several millimeters (to eliminate dis-

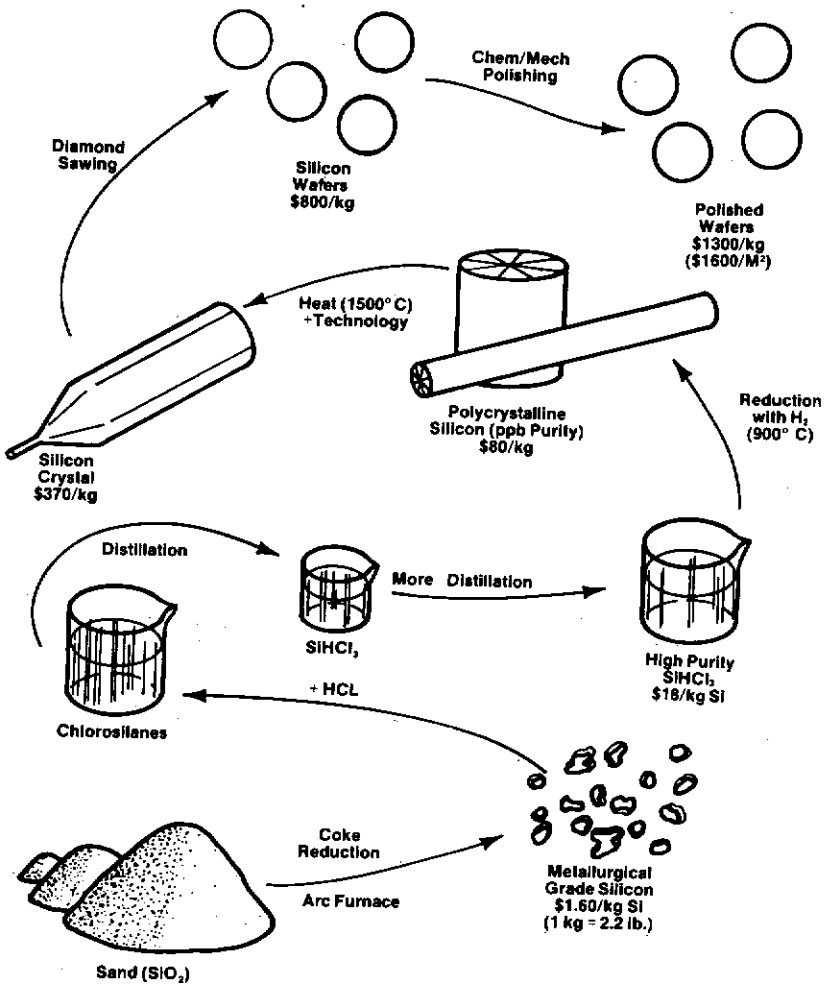

Fig. 3. Process steps for semiconductor grade silicon.

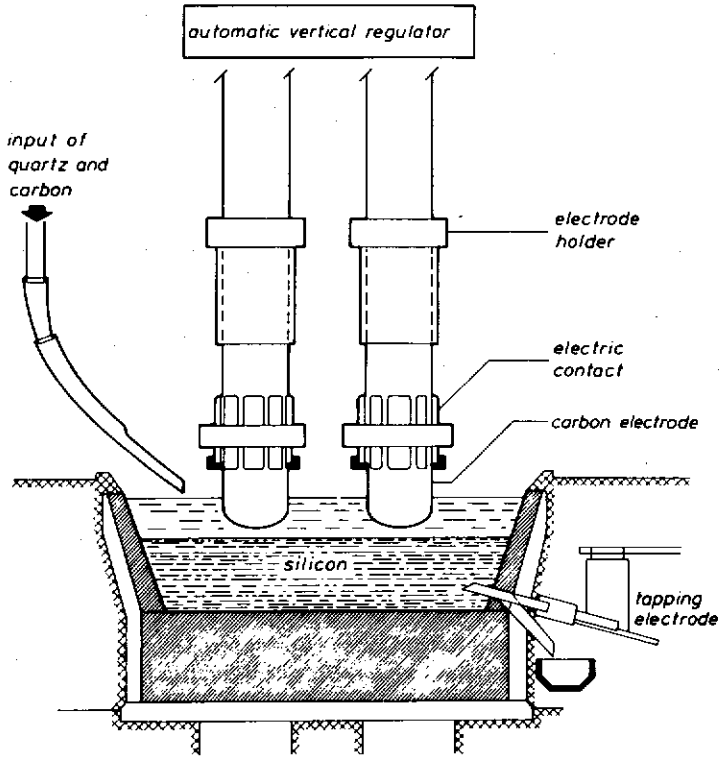

Fig. 4. Schematic of an arc furnace (after Sirtl [1]).

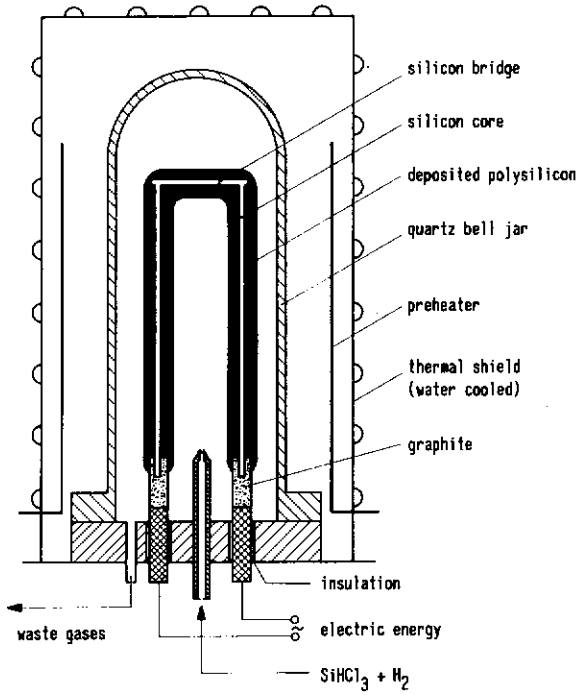

Fig. 5. Schematic of silicon CVD process (after Dietze et al. [2]).

locations from the seed/melt contact shock) and then to widen the crystal rapidly to full diameter. Crystal lengths of 1 m and diameters up to 15 cm are attainable with current commercial growth systems.

The usual configuration for float-zoning (FZ) silicon is shown in fig. 6. Induction heating at frequencies in the 1–3 MHz range is used, and the liquid does not come in contact with any foreign material. Therefore, very pure crystals can be obtained. Whereas Czochralski-grown crystals typically contain 10^{16} atoms/cm^3 of carbon and up to 10^{18} atoms/cm^3 of oxygen, conventional FZ crystals contain two orders of magnitude less of these impurities. With care, it is possible to achieve 100 kΩ-cm resistivities and corresponding boron dopant contents of about 1×10^{11} atoms/cm^3 (3 parts per trillion) using float-zoning. The FZ method tends to be more technologically complex than CZ growth for a number of reasons. First, there are the instabilities associated with a liquid zone suspended between silicon rods. Because of gravity effects on zone shape, the growing crystal must

be below the melt, and there is a consequent unstable equilibrium of the crystal resting on a necked seed 2–3 mm in diameter. Harsh thermal gradients are necessary to melt through large-diameter rods without exceeding maximum stable zone heights (25–30 mm). Skilled operators are required for balancing the zone through the transition from neck size to full diameter. Complex morphological, ridge-like bulges occur on the surface of dislocation-free crystals and cause a deviation from cylindrical geometry. Enhanced hydrodynamic flow effects occur because of the zone geometry and the sharp thermal gradients. It is remarkable that commercial FZ crystals are grown dislocation-free in lengths over 1 m and with diameters over 10 cm.

Sawing of ingots results in a 45–50% material loss as silicon sawdust. A typical material yield is 1 m^2 of surface area per kg of silicon. Internal diameter saws of the type used in the semiconductor industry can produce 2000 wafers/m of 10 cm diameter ingot at an area rate of about 0.15 m^2/h. The sawed wafers are polished with a colloidal silica slurry to remove abrasive sawing damage and produce a flat surface ready for device fabrication.

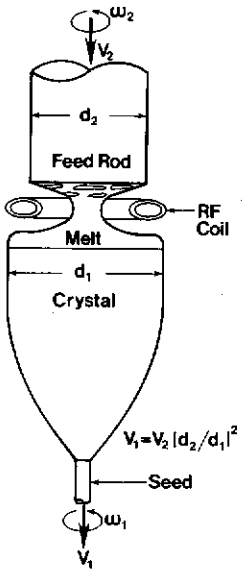

Fig. 6. Schematic of FZ silicon growth.

3. Silicon requirements for solar cells

Silicon selling prices escalate in the conventional semiconductor silicon process we have just examined from \$ 1.60/kg at the metallurgical silicon phase to \$ 1300/kg or \$ 1600/m^2 for polished wafers (fig. 3). Hence, the material cost for 15% efficient solar cells made from this type of silicon is of the order of \$ 10/W_p. To be considered in large-scale power generation, the silicon substrate cost should be about 1/50th of this amount. Much effort has been directed at all phases of the process shown in fig. 3 to eliminate, substitute, or simplify as many of the steps as possible. Only the efforts related to crystal growth will be discussed in detail here. A number of methods for producing polycrystalline feed stock material show promise of attaining selling prices of less than \$ 10/kg. In most cases, compromises in purity are necessary to achieve this.

The purity requirement for silicon used in solar cells is not as stringent as that for many other semiconductor devices, but it is still high. Table 2 lists some approximate levels at which a detectable degradation in solar cell performance can be noted for an impurity present at the concentration

Table 2
Approximate solar cell degradation thresholds and segregation coefficients for some impurities in silicon (after Davis et al. [3]).

Impurity	Threshold level (atoms/cm^3)	Segregation coefficient
Zr	10^{11}	10^{-7}
Mo	10^{12}	10^{-7}
Ta	10^{12}	10^{-7}
V	10^{12}	10^{-5}
Ti	10^{12}	10^{-5}
Au	10^{14}	10^{-5}
Cr	10^{14}	10^{-5}
Mn	10^{14}	10^{-5}
Fe	10^{14}	10^{-5}
Al	10^{16}	10^{-3}
Ni	10^{16}	10^{-5}
Cu	10^{17}	10^{-4}
C	10^{18}	10^{-1}
P	10^{18}	10^{-1}
B	10^{18}	1

listed. The table also lists approximate equilibrium segregation coefficients k_0 for each impurity. It can be seen that metallic impurities have $k_0 \ll 1$; thus, they are readily removed in the ingot growth methods. For some sheet growth processes, the effective segregation coefficient k_e is near one and no purification occurs during growth. Other sheet growth methods have $k_0 < k_e < 1$ and some purification occurs. Boron is by far the most bothersome impurity in metallurgical-grade silicon, since it does not segregate appreciably in any melt-growth process.

In ingot crystal growth, the trends for photovoltaic applications are toward methods that are low-cost, simple, and capable of producing large sizes. The main reason that sheet crystal growth has received considerable attention is that the cost and material waste of the sawing or wafering operation associated with ingot growth are eliminated. Sheet growth, in principle, allows one to go directly from polycrystalline feed stock to the equivalent of a polished wafer. In addition, high linear growth speeds are attainable relative to ingot speeds. However, this does not necessarily imply a higher throughput for sheet growth.

4. Crystal growth of silicon for solar cells

Many methods have been applied to the growth of silicon crystals; Table 3 lists 19 of them. The ingot growth methods are the oldest, dating back to 1950. Czochralski growth (CZ), float-zoning (FZ), and pedestal growth produce single crystals, while casting and directional solidification generally result in multicrystalline ingots because of grain nucleation at the container walls. Despite this, the latter have recently been of interest for photovoltaics because the growth processes are simple, low in cost, and require little technical skill to conduct. Pedestal growth has not been extensively developed for photovoltaics.

4.1. Ingot growth methods

Figure 7 shows the progress in ingot diameter as a function of time for FZ, CZ, and casting growth methods. The slope of these curves is indicative of the relative complexity of the three growth methods.

Crucible costs and slow growth rates are the main economic problems associated with CZ growth. Work has been done to implement crucible recharging and enhance growth speeds. Growth of 150 kg of crystals from a single crucible at pulling speeds of 1.5 mm/min has been

Table 3
Crystal growth methods for silicon.

Si ingot growth methods

- Czochralski pulling (CZ, 1950)
- Float zoning (FZ, 1952)
- Casting (1959)
- Pedestal growth (1972)
- Directional solidification (1976)

Si sheet growth methods

- Dendritic web (WEB, 1963)
- Stepanov (S, 1967)
- Edge-defined, film-fed growth (EFG, 1972)
- Horizontal ribbon growth (HRG, 1975/LASS, (1980)
- Ribbon-against-drop (RAD, 1976)
- Ribbon-to-ribbon zoning (RTR, 1976)
- Silicon-on-ceramic (SOC, 1976)
- Capillary action shaping technique (CAST, 1977)
- Continuous capillary coating (CCC, 1977/S-WEB, 1982)
- Inverted Stepanov (IS, 1977)
- Roller quenching (RQ, 1979)
- Edge-supported pulling (ESP, 1980)
- Interface-controlled crystallization (ICC, 1981)
- Melt spinning (spinning, 1982)

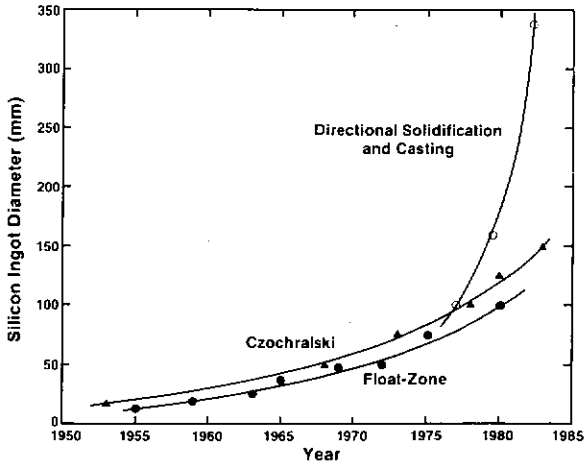

Fig. 7. Progress of ingot size with time.

Table 4
Ingot growth characteristics.

	Float zoning	Czochralski growth	Bridgman growth	Ingot casting
Growth rate (mm/min)	2–4	1–2	0.1–5	1–2
Diameter (mm)	100	150	340	210
Throughput (kg/h)	4	4	1–6	5
Crystal structure	dislocation-free	dislocation-free	multi-grain	multi-grain
Technology/skill	very high	high	low	low
Solar cell efficiency (%)	16–19	15–17	9–15	9–13
Comments	no crucible	recharge possible	crucible adheres	independent melting

achieved. Table 4 lists some of the characteristics of CZ and other ingot growth techniques.

FZ growth eliminates the crucible cost problem and allows higher growth speeds (about twice those of CZ crystals). It is technologically complex, however, and produces smaller ingots. Induction heating is less efficient than the resistance heating used in CZ growth, and float-zoning requires a somewhat more selective geometry for the polycrystalline starting material. An area where FZ crystals may attain increasing importance is for high-efficiency silicon cells. Cells of 19% efficiency have been made on FZ crystals.

Some progress has been made recently in using impure silicon for both CZ and FZ ingot growth. For example, when a 125 mm diameter seed and 0.6 mm/min growth speeds were used, very large-grained CZ crystals could be grown from 98.5% pure silicon. Epilayer solar cells of 11% average AM1 efficiency were made from these crystals.

Although it was used quite early for other applications, casting was not applied to ingot growth for photovoltaics until 1975. Casting and Bridgman-type directional solidification are relatively simple processes, but they generally produce multicrystalline ingots. An exception is the heat exchanger method (HEM), which can yield nearly single-crystal material. Recent advances in these processes have resulted in block-shaped ingots a third of a meter in size. The distinguishing feature between casting and other directional solidification techniques is that the former is conducted by pouring molten silicon into a mold where it solidifies, whereas the latter methods melt and resolidify the silicon in the same container. One of several possible configurations for conducting directional solidification is shown in fig. 8, and a casting apparatus is shown in fig. 9. Directional solidification and casting produce ingots with similar grain structures. Figure 10 illustrates this structure for small-diameter ingots. Grains continually nucleate at the crucible walls, and surviving grains align approximately parallel with the normal to the advancing solid/liquid interface. Larger ingots tend to have a larger average grain size.

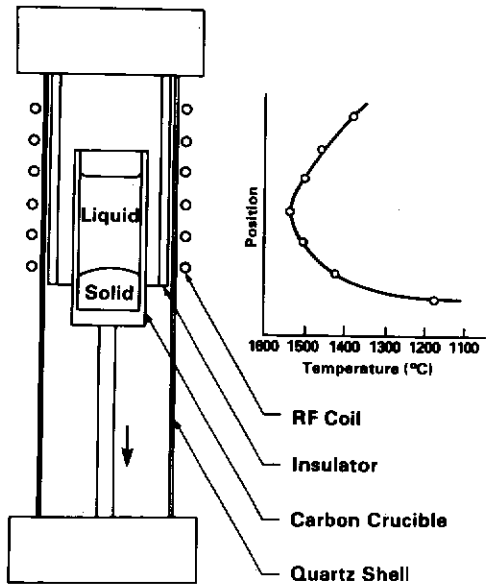

Fig. 8. Schematic of one type of directional solidification method.

Thermal expansion coefficient mismatch between silicon and the crucible container at temperatures near and below the silicon plastic deformation temperature can be an important consideration, particularly for directional solidification. Figure 11 depicts the thermal expansion coefficients of silicon and several materials in the temperature range of interest. The container used for directional solidification should be inert, and the material to be grown should contract upon freezing, or at least not stick to the crucible walls. In traditional fused quartz crucibles, silicon does neither. The silicon adheres to the container walls and both the container and the silicon crack due to differential thermal expansion during cooldown. Some progress has been made in eliminating the silicon cracking, at the expense of the container, by altering the structure of the inner quartz crucible wall: the wall is effectively weakened so that it cracks instead of the silicon. Graphites are available with a wide range of thermal expansion coefficients (1.1 to 8.3 $\times$ 10^{-6} $°C^{-1}$), some isotropic and some anisotropic. To avoid cracking of the silicon charge and/or the crucible, the graphite or carbon crucible should have a coefficient of thermal expansion (CTE) in the range of 20 to 650°C which either matches that of silicon or else, on the average, produces about the same dimensional change.

For casting, these considerations are not as important since the mold can be at a low enough temperature during pouring to prevent the solid silicon from sticking to the mold. In fact, two-piece molds can be separated after growth and

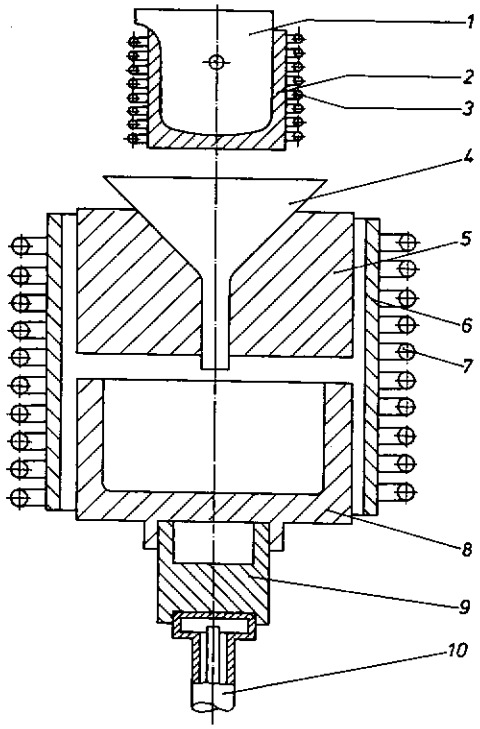

Fig. 9. Schematic of casting apparatus (after Helmreich [4]).

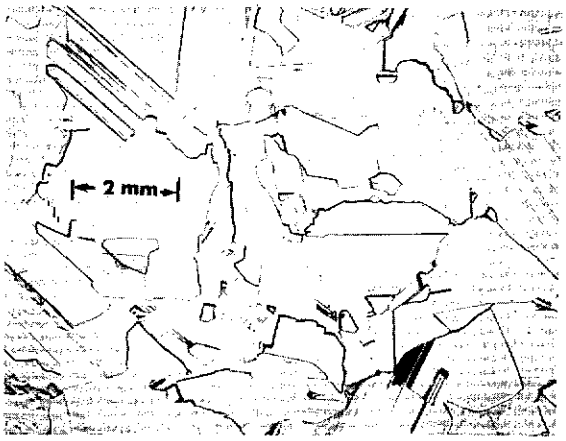

Fig. 10. Grain structure for directionally solidified ingots.

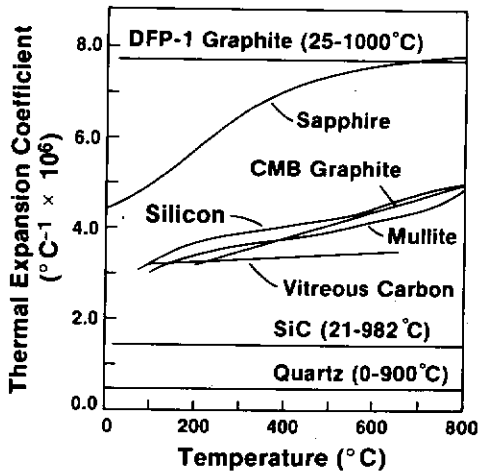

Fig. 11. Thermal expansion coefficients for silicon and some container materials.

reused many times over. Table 4 compares the characteristics of casting and directional solidification with those of the single-crystal ingot growth techniques.

A common requirement of all ingot growth methods is wafering. In addition to the material waste associated with wafering, the rate of the wafering process is a concern. Hence, efforts are being made to enhance the ID saw process (e.g., by rotating the ingot during sawing). Also, work is being done to scale up the multiblade slurry (MBS) and related sawing methods (multiwire slurry and fixed abrasive slicing technique, FAST). On a pilot scale, these methods can produce 2500 wafers/m from 10 cm diameter ingots at an area rate up to about 0.007 m^2/h/blade (e.g., for MBS). Thus, the area production rate of a MBS 22-blade pack is approximately equivalent to that of an ID saw. Higher cutting rates are achieved at faster blade travel velocities with MBS sawing. The depth of abrasive damage associated with these newer cutting techniques is typically 5–6 μm.

4.2. Silicon sheet growth

Classification of silicon sheet growth methods by meniscus geometry permits them to be discussed in three groups: short meniscus techniques, high meniscus techniques, and extended meniscus or large solid/liquid interface area techniques. A second parameter, meniscus shaper interaction with the liquid silicon, is also instrumental in determining the characteristics of the various sheet processes. The current status of each process is discussed in the context of meniscus geometry and shaper/melt interaction.

Each of the silicon sheet growth methods listed in table 3 can be assigned one of the three general meniscus shapes depicted in fig. 12. The height of the M_1 meniscus is on the order of the sheet thickness t. The M_2 meniscus rises from a broad base (at the crucible melt level, for example) to the sheet interface and typically has a height on the order of 6–7 mm. The M_3 meniscus is characterized by a large solid/liquid interface area compared to Wt, where W is the ribbon width.

Figures 13 to 17 are schematic representations of the five ribbon processes having the M_1 meniscus: edge-defined, film-fed growth (EFG), capillary action shaping technique (CAST), Stepanov technique (S), inverted Stepanov technique (IS), and ribbon-to-ribbon zoning (RTR). In these processes, there is close physical proximity between the melt shaping device (or feed stock ribbon in the case of RTR) and the solid/liquid interface of the growing ribbon. This suggests potential thermal and mechanical control difficulties. Furthermore, if the shaper is a foreign material (all cases except RTR), its close proximity can lead to significant impurities in the Si sheet.

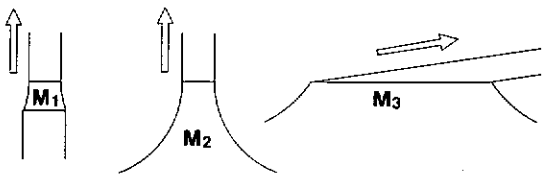

Fig. 12. Three types of meniscus encountered in Si sheet growth.

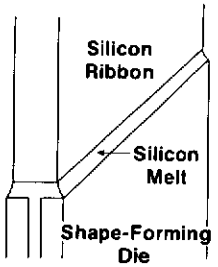

Fig. 13. Schematic of Dow Corning and Mobil/Tyco EFG Process.

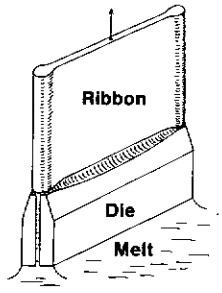

Fig. 14. Schematic of the IBM CAST process.

In the EFG method, the liquid silicon rises up capillaries in the shaping die and spreads across the die top. The outer edges of the die top pin the base of the meniscus from which the shaped crystal solidifies. The method was first applied to sapphire growth and later, in 1972, extended to silicon ribbon growth. This was the first silicon sheet method directed primarily at photovoltaic applications, with the rationale that the lower purity and crystal perfection imposed by the interaction of the shaping die with the melt might be offset by the relatively greater tolerance of solar cells to such problems (as compared with integrated circuit devices).

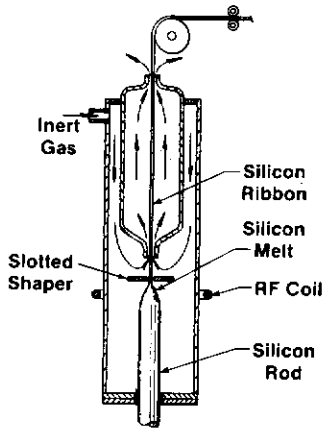

Fig. 15. Schematic of Texas Instruments Stepanov process.

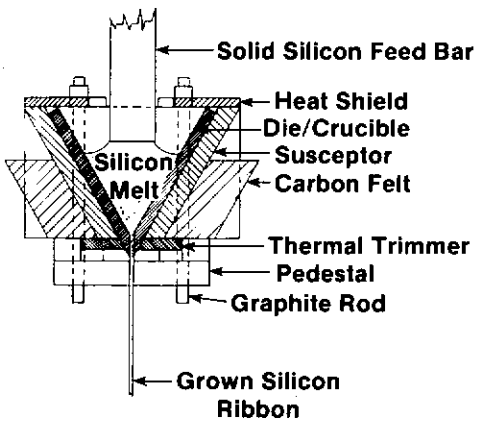

Fig. 16. Schematic of the RCA inverted Stepanov process.

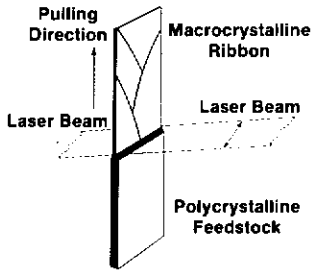

Fig. 17. Schematic of Motorola RTR process.

The height to which liquid will rise in a capillary is governed by Laplace's equation, which relates the pressure difference ΔP across a liquid surface to the two principal radii of curvature of the surface R_1 and R_2, and to the surface tension γ:

$$\Delta P = \gamma \left(\frac{1}{R_1} + \frac{1}{R_2} \right) . \tag{7}$$

If liquid rises up a vertical capillary to a height h above the ambient liquid surface, then

$$\Delta P = \varrho g h, \tag{8}$$

where ϱ is the liquid density (the density of the gas phase surrounding the liquid is assumed to be negligible) and g is the acceleration due to gravity. The capillary channel geometry and the wetting angle θ of the liquid have an influence on R_1 and R_2. For a cylindrical capillary channel of radius r containing liquid which meets the wall at angle θ, it is typically assumed that the liquid surface is spherical so that $R_1 = R_2 = r/\cos\theta$. In this case, the height of liquid rise is

$$h = \frac{2\gamma}{\varrho g r} \cos\theta. \tag{9}$$

For a capillary formed between two vertical infinite plates separated by a distance s, it is usually assumed that the liquid surface is a segment of a cylinder. If the liquid meets the plates at angle θ, then $R_1 = s/2 \cos\theta$ and $R_2 \to \infty$ so that

$$h = \frac{2\gamma}{\varrho g s} \cos\theta. \tag{10}$$

In fig. 18, eq. (10) is plotted as h versus s using the relevant parameters for silicon and an assumed contact angle θ of 60°. This approximates the condition for graphite dies, which are widely used for silicon EFG. Plate separations of 0.03–

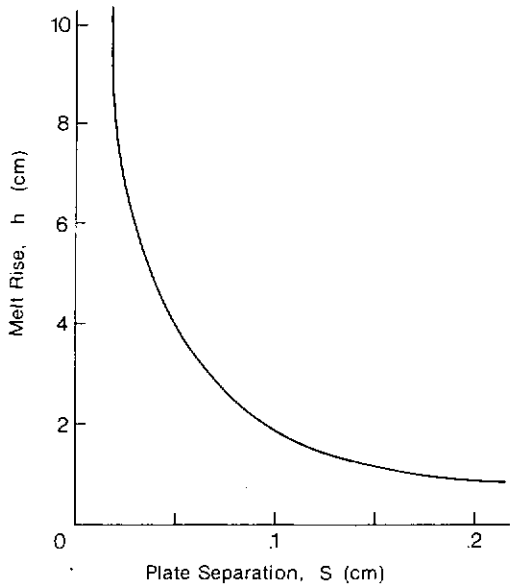

Fig. 18. Silicon capillary rise, h, between plates of spacing s and contact angle 60°.

0.05 cm are typical for silicon ribbon growth from graphite dies.

The die configuration of course must be such that the distance from the crucible melt level to the die-top, h_d, is less than the value of h given by eqs. (9) or (10). The advantage of making h_d large is that it is easier to separate thermal control at the die-top from thermal control in the crucible. The advantage to making the distance small is that a higher meniscus h_m between the die-top and the freezing interface is attainable. This decoupling between the die-top and the solid/liquid interface is an important feature of the capillary action shaping technique (fig. 14). The reason that smaller values of h_d allow larger values of h_m is that the radius of curvature R_m of the meniscus surface in a vertical plane perpendicular to the crystal surface is, to a good approximation, given by

$$R_m = \gamma/\varrho g h_d. \tag{11}$$

Thus, R_m increases as h_d decreases. Since the meniscus base is pinned at the die edge (which has finite curvature on a microscopic scale), and the top of the meniscus must meet the crystal surface at a characteristic constant angle (11° for [111] silicon), a larger value of R_m allows a larger value of h_m. Of course, this argument also implies that h_m increases as the die-top thickness increases. The maximum meniscus height occurs for infinitely thick dies not elevated above the melt surface; i.e., for no die at all. This condition is approximated in the "web" region of the dendritic web and ESP growth processes and is discussed later.

Maintaining a high meniscus reduces the detrimental effects of close die-top proximity to the solid/liquid interface. Freeze-outs to the die-top become less likely, and the pick-up of SiC particles (which grow from the carbon supersaturated melt at the die-top) is reduced. Thus, the process becomes more stable and the surface smoothness and crystal structure of the ribbon are enhanced.

A reasonable compromise between the extremes of a short meniscus remote from the crucible melt surface and a high meniscus with small h_d is provided by the CAST die design of fig. 19 with h_d ranging from 2–3 cm. In this one-piece design, the melt rises up side channels and then flows across the top channel to feed the entire die-top. The die-top surface is curved so that it is higher at the edges than in the middle. In this way, if the ribbon's solid–liquid interface is maintained approximately planar, then the interface is farther from the die, at least in the central region. The central region is the most critical one for generating defects in the ribbon. However, if the thickness of the die-top is kept constant while the

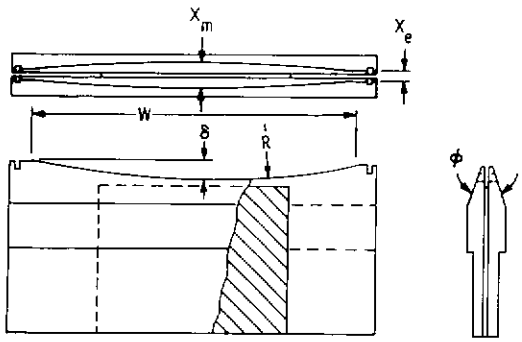

Fig. 19. Capillary action shaping technique (CAST) die design.

die-top surface is curved, then a higher meniscus in the central region necessarily implies that the top of the meniscus is thinner there. This would cause the ribbon to be very non-uniform in thickness from one edge to the other (i.e., much thinner in the middle than at the ends). Thus, not only should the die top curve downward from the ends toward the central region, but it must also become thicker in the central region than at the ends, as shown in fig. 19. The meniscus, then, has a wider base in the central region. The wider base, combined with the greater meniscus height in the central region, results in a more uniform ribbon thickness at the solid/liquid interface.

In summary, there are two things that are important to the design of the die: the curvature of the top surface and the thickening of the die top in the central region. If the curvature of the die top and the taper angle of the sides of the die are correctly chosen, an optimum value for this variation in the thickness of the die top with position along the die can be obtained. R and ϕ (see fig. 19) are chosen to optimize the values of $x_m - x_e$ and δ for successful ribbon growth. These parameters are given by

$$\delta = R - \frac{W}{2\tan\left(\sin^{-1}\frac{W}{2R}\right)}, \tag{12}$$

$$x_m - x_e = 2\delta \tan \phi/2. \tag{13}$$

Table 5 lists CAST die-top dimensions that have been successfully used for various silicon ribbon widths. In general, edge thickness, middle thickness, and deviation from flatness all increase with ribbon width. For a given die-top geometry, ribbons of different thickness can be grown. This is accomplished by varying the pulling speed and the thermal profile over the width of the ribbon growth front. Faster pull rates and hotter middle-versus-edge temperatures tend to decrease the thickness and vice versa.

Table 5
CAST die-top parameters (in mm) for ribbon widths of 25–100 mm.

Ribbon width	x_e	x_m	δ
25	0.4–0.8	1.0–1.3	0.6–0.7
38	0.4–0.8	1.1–1.5	0.9–1.1
50	0.8–1.2	1.8–2.1	1.6–2.0
100	1.5	2.5	1.8

The improvement in ribbon surface quality that is achieved with a higher meniscus is evident in fig. 20, in which the surface of a ribbon grown from a flat-top die and the surface of a ribbon grown from a CAST die are compared. Figure 21 depicts a simple experimental arrangement that can be used for both EFG and CAST growth, and fig. 22 shows a growing 50 mm wide CAST ribbon.

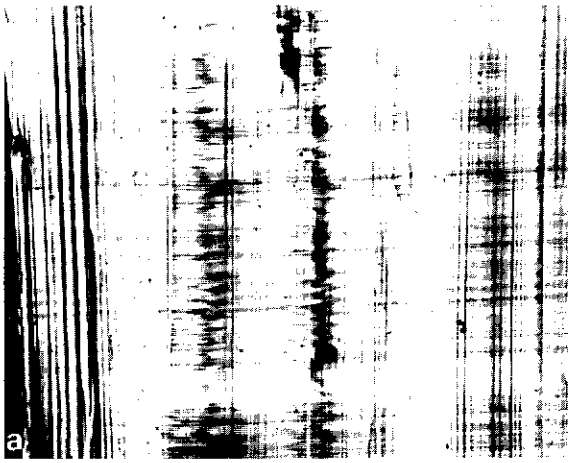

Fig. 20a. 11× micrograph of ribbon surface, flat-top die.

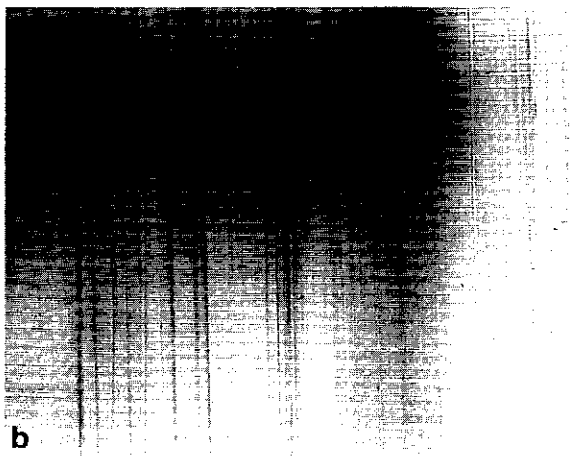

Fig. 20b. 11× micrograph of ribbon surface, CAST die.

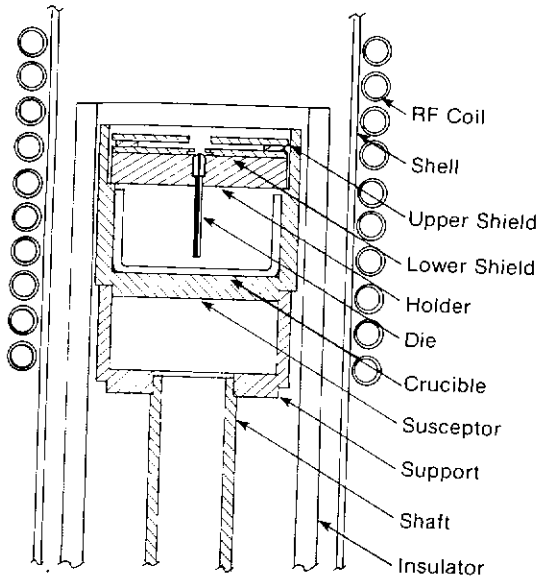

Fig. 21. Furnace hot-zone for capillary die sheet growth.

An interesting extension of capillary die growth is the solidification of silicon tubes using a cylindrical die. Since no edges are present, in contrast to sheet growth, thermal control is more flexible. A recent commercial application of this concept is the growth of nine-sided polygonal tubes where each side is a sheet 5 cm wide. Thus, nearly 0.5 m of ribbon width is produced in one pull.

The Stepanov process is shown in fig. 15. The melt is held on the top of a silicon pedestal rod and is heated inductively. Ribbons are solidified from a meniscus shaped by a nonwetting slot (SiO_2, BN, and others) at the top of the melt. Dislocation-free, 12 mm wide ribbons have been grown by this method, but further scale-up has not been done.

An inverted Stepanov (IS) geometry (fig. 16) has also been investigated. The Stepanov methods potentially exhibit fewer problems with shaper interaction than do the capillary die

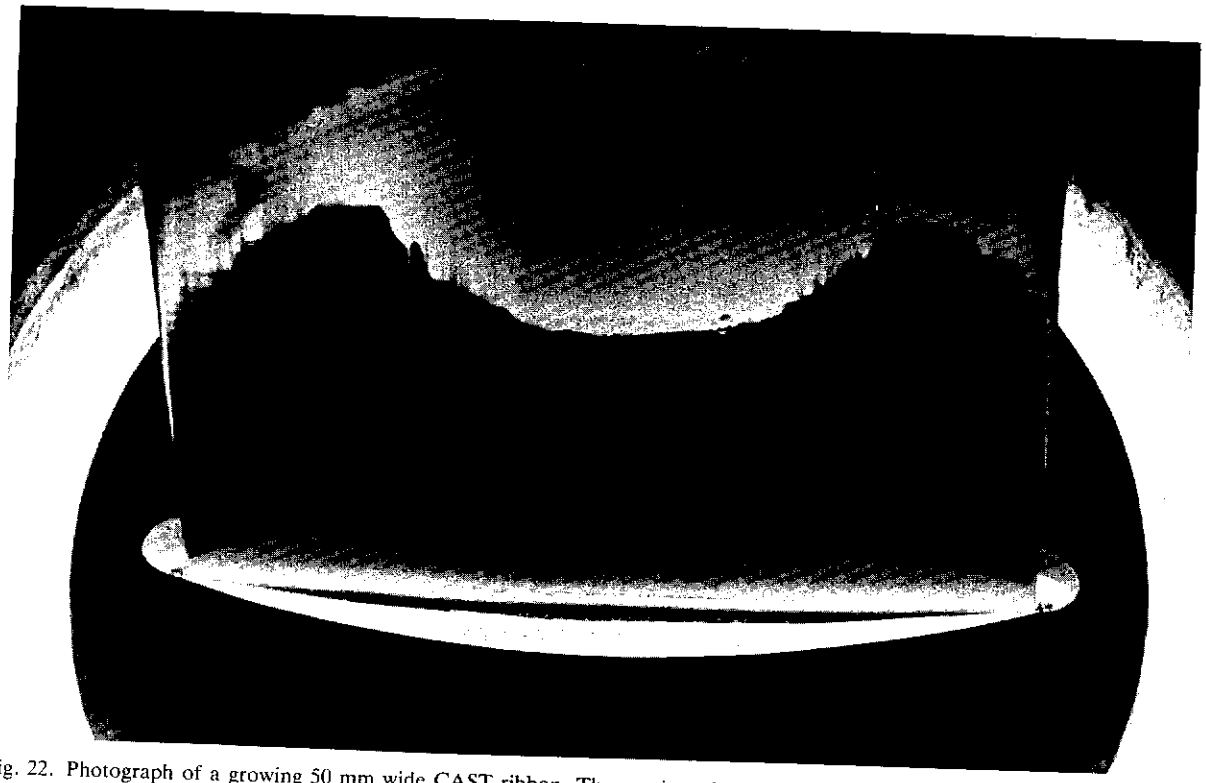

Fig. 22. Photograph of a growing 50 mm wide CAST ribbon. The meniscus is the dark thin crescent. The shiny ribbon surface reflects the front heat shield.

techniques, if a nonwettable shaper is used. Thermal control problems were experienced with nonwettable shapers in the IS method, but ribbons 20 mm in width were grown using wettable shapers.

Since the RTR method uses no foreign shaper, the purity associated with it can be high if the feed ribbon is sufficiently pure. Feed ribbons are made by CVD coating Si on a Mo substrate and using thermal shear stress separation to isolate the polycrystalline Si feed ribbon. Molybdenum silicides are of concern. The meniscus height is of the order of 1 mm and good thermal control is required. Interface profiling is possible and beneficial. This and leaving the edges of the feed ribbon rigid or unmelted have led to enhanced process stability and attainment of large-grained sheets. Electron beam heating is being explored to overcome the low efficiency of laser heating.

In tables 6 and 7, some of the characteristics and factors affecting the stability and purity of the short meniscus growth methods are listed.

Figures 23 to 27 depict the ribbon processes characterized by the free-rising M_2 meniscus: dendritic web (WEB), ribbon-against-drop technique (RAD), silicon-on-ceramic technique (SOC), continuous capillary coating (CCC and S-WEB), and the edge-supported pulling technique (ESP). From Laplace's equation, the meniscus height for liquid attached to a perfectly wetted plate immersed in the liquid is

$$a = (2\gamma/\varrho g)^{1/2}. \tag{19}$$

Table 6
Some characteristics of short-meniscus sheet growth methods.

	EFG	CAST	Stepanov	Inverted Stepanov	RTR
Growth rate (mm/min)	10–50	10–50	30	10	30–90
Maximum width (mm)	100	125	~ 12	20	75
Minimum thickness (microns)	150	~200	~500	500	100
Maximum length (cm)	3000	130	–	15	~ 60
Crystal structure	mm grain size	mm grain size	single	mm grain size	mm grain size
Solar cell efficiency (%)	7–14	10–12	–	8 (epilayer)	10–13
Technology/skill	high	high	high	high	high

Table 7
Factors affecting stability and purity of short-meniscus methods.

	EFG	CAST	Stepanov	Inverted Stepanov	RTR
Meniscus height (mm)	0.3	0.7	~1	~1	~1
Thermal control (°C)	<2 in crucible	<2 in crucible	<1	<1	–
Surface morphology	SiC particles rippled	SiC particles smooth	smooth	rippled	smooth
Impurity sources	die, crucible furnace	die, crucible	die, crucible	die, crucible	feed ribbon
Impurity segregation	$k_e \sim 1$	$k_e \sim 1$	$k_e \sim 1$	$k_e \sim 1$	$k_e \sim 1$
Use of impure silicon	no	no	no	no	no
Areas of concern	freezes, stresses	stresses, seeding	control, die	control, die	feed stock, laser heating

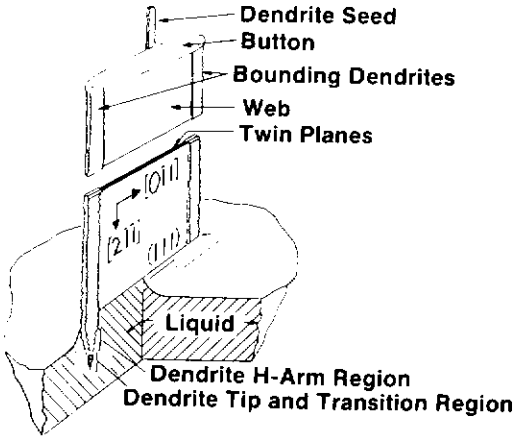

Fig. 23. Schematic of Westinghouse WEB process.

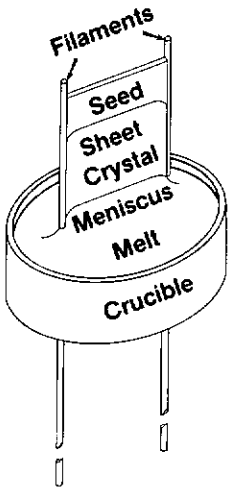

Fig. 24. Schematic of SERI ESP process.

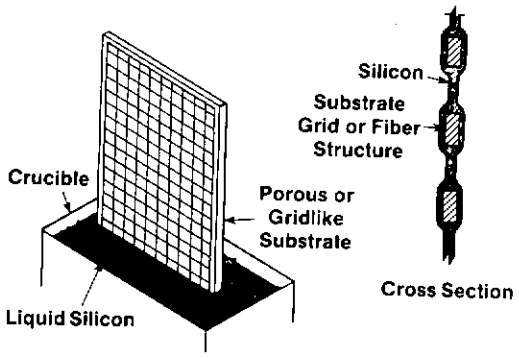

Fig. 25. Schematic of IBM and SERI CCC process/Siemens S-WEB process.

Liquid silicon does not perfectly wet solid silicon, and the nonzero contact angle θ is approximately 11°. The meniscus height h in this case is

$$h = a(1 - \sin\theta)^{1/2}. \quad (15)$$

Thus, the M_2 meniscus height is about 6–7 mm. A general implication of the high M_2 meniscus is a greater tolerance of mechanical and thermal perturbations, since no melt shaper is close to the solid/liquid interface.

One of the techniques, WEB (fig. 23), still has stringent thermal control requirements. This is because propagation of the bounding dendrites into precisely supercooled melt regions at the sheet edges must occur simultaneously with normal freezing of the sheet or web between the dendrites. Growing of wide webs is difficult because of the intricacies associated with propagating a wide button and subsequent widely spaced coplanar dendrites from the initial seed dendrite. In addition, the technique is quite sensitive to thermal stresses which can easily disrupt the growth

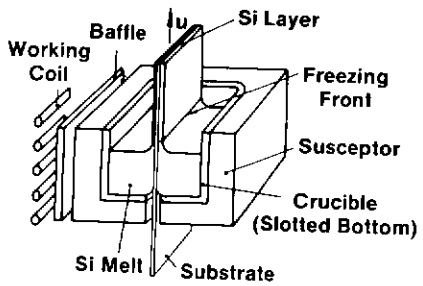

Fig. 26. Schematic of LEP RAD process.

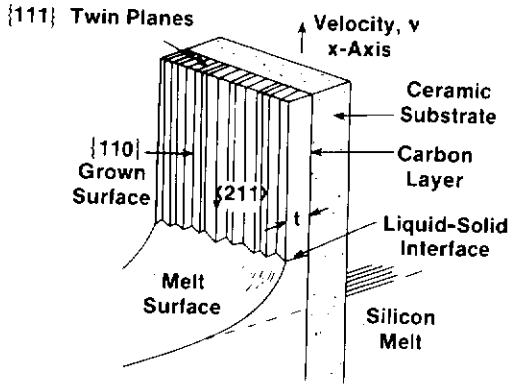

Fig. 27. Schematic of Honeywell SOC process.

mechanism. WEB ribbons are nearly equal to Czochralski-grown ingots in solar cell performance. In addition to the twin plane boundaries, the webs contain dislocations. Figure 28 is an X-ray topograph of typical dislocation structures in WEB. This material has the best crystallographic perfection of all the widely developed sheet techniques.

By utilizing foreign filaments in place of Si dendrites, ESP achieves easier thermal control (± 5–10°C) and wider ribbons than WEB. The simplicity of the ESP hot-zone can be seen in fig. 29. The crystal structure is not as good as that of WEB, but is large-grained and achieves solar cell efficiencies 90% as high as those from Czochralski ingots. A variety of filament materials can be used, including graphite yarn, SiC fibers, mullite, and quartz fibers. The filaments are introduced into the melt through holes in the quartz crucible bottom. With holes of diameter ϕ, the liquid is stable against leaking for a crucible melt height up to h, where

$$h = 67.4/\phi - 5.82. \quad (16)$$

Both h and ϕ are in mm. Growth can be nucleated either from a seed crystal or from a plate such as graphite. Figure 30 shows an ESP sheet grown from a (110)-surface, $[\bar{1}\bar{1}2]$-axis seed using graphite filaments.

The other processes in the M_2 group (RAD, SOC, CCC, and S-WEB) solidify silicon on a large area substrate passing through the liquid. Thermal and mechanical control are very easy, but the substrate nucleates many grains and results in a small-grained, relatively low-efficiency solar cell. An interesting point about these techniques is that the substrate can physically transport the liquid when it moves at high speeds. In this mode, the solid/liquid interface is not at the tip of the meniscus, but is remotely located from the melt in the crucible. Ribbon pulling speeds can thus be very high. This effect has been particularly utilized for the CCC and S-WEB mesh-like substrates, where liquid films are trapped like soap films between the grids of the mesh. A dendritic growth structure is prevalent in this mode.

All of the high-meniscus methods can tolerate growth from impure silicon, but WEB has restrictions in this area because impurity levels sufficient to cause breakdown of the stable solid/liquid interface will disrupt the twin plane mechanism of

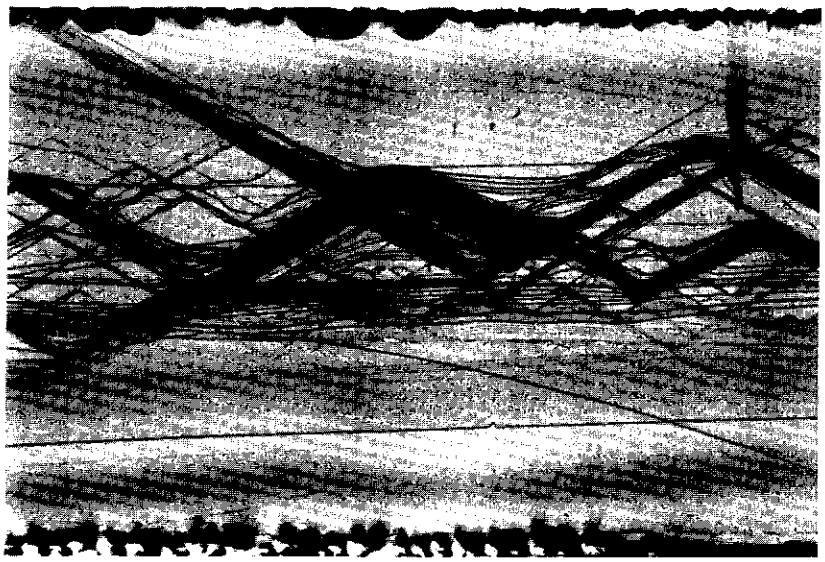

Fig. 28. X-ray topograph of a dendritic web sheet.

growth. Sheets have been grown directly from metallurgical-grade silicon using ESP even in the presence of constitutional supercooling. Figure 31 shows the onset of a constitutional-supercooling-induced surface morphology on an ESP sheet.

In tables 8 and 9, some of the characteristics and factors affecting the stability and purity of the high meniscus growth methods are listed.

Figures 32 to 35 show the sheet processes where an extended, large-area M_3 meniscus is employed: horizontal ribbon growth (HRG), low angle silicon sheet (LASS), interface-controlled crystallization (ICC), roller quenching (RQ), and spinning. These techniques achieve a very fast growth rate through (a) use of a solid/liquid interface area that is greater than Wt, the cross-sectional area of the ribbon, and (b) efficient extraction of the latent heat of fusion. Since the heat of fusion is liberated over an area larger than Wt, the amount to be dissipated per unit area is less than for the

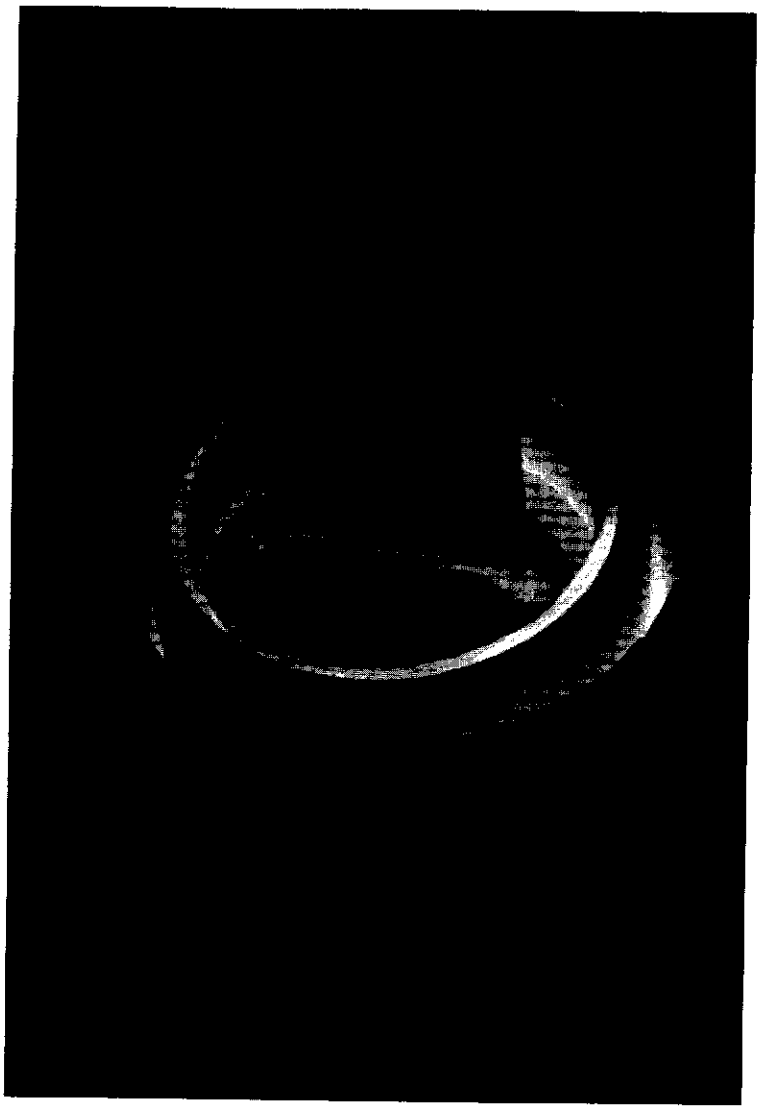

Fig. 29. Growth of a 40 mm wide ESP ribbon.

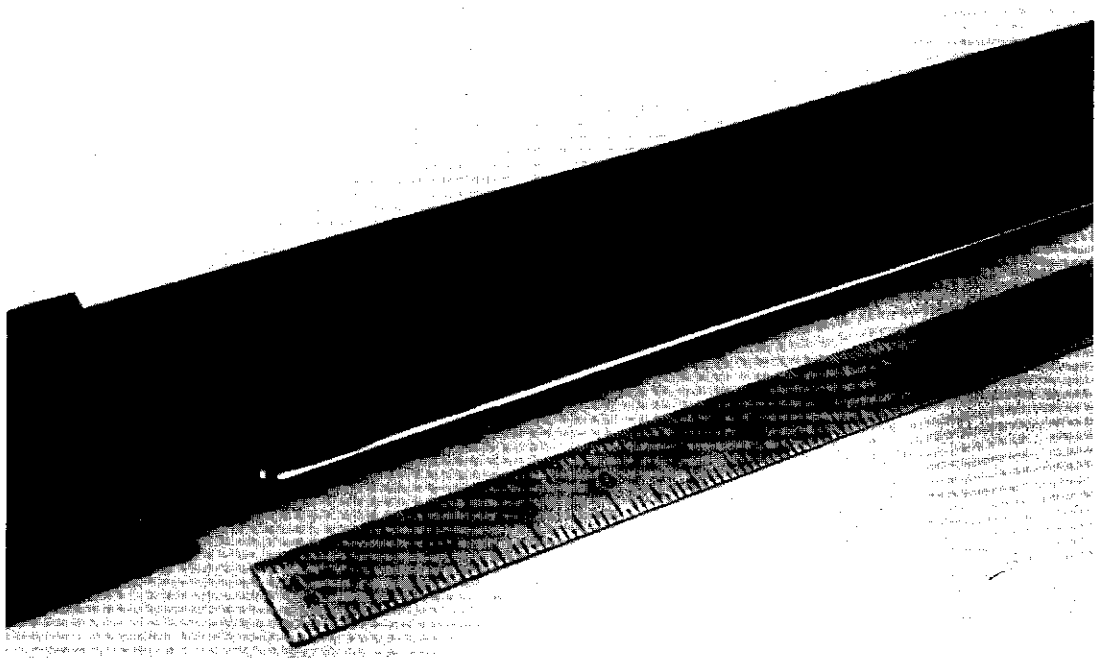

Fig. 30. Silicon sheet grown by edge supported pulling (ESP).

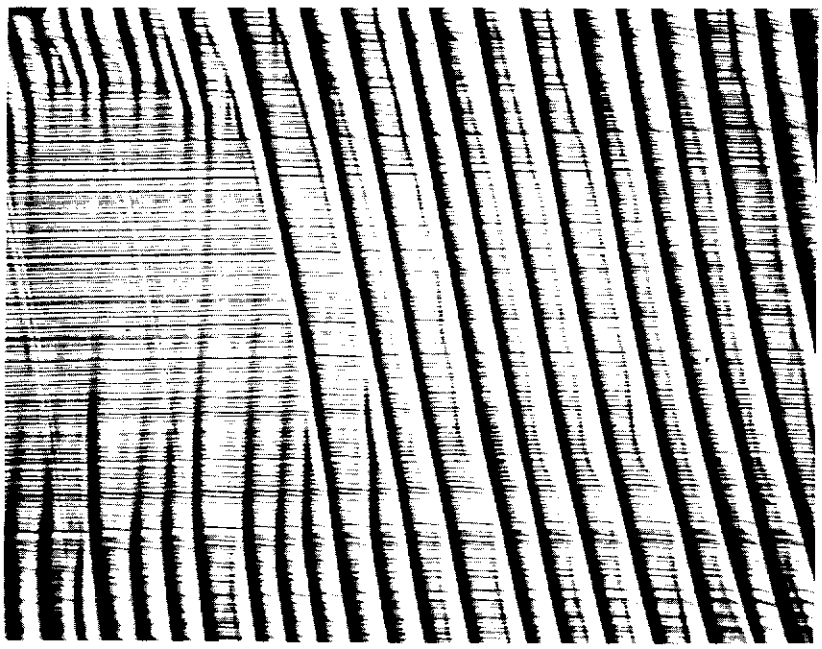

Fig. 31. ESP surface morphology due to constitutional supercooling (35×).

Table 8
Some characteristics of high-meniscus sheet growth methods.

	WEB	ESP	CCC/S-WEB	RAD	SOC
Growth rate (mm/min)	10–70	10–90	40–2000	60–120	40–300
Maximum width (mm)	60	100	40	50	100
Minimum thickness (microns)	80	80	100	50	100
Maximum length (cm)	1100	25	6	3000	100
Crystal structure	single (twins)	large grain	small grain	medium grain	medium grain
Solar cell efficiency (%)	13–16	10–14	4–8	7–13	7–11
Technology/skill	high	low	low	low	low

Table 9
Factors affecting stability and purity of high-meniscus methods.

	WEB	ESP	CCC/S-WEB	RAD	SOC
Meniscus height (mm)	~7	~7	~7	~7	~6
Thermal control (°C)	± few tenths	± 5	± 10	± 1	–
Surface morphology	very smooth	smooth, bowing	undulating	flat (~ 2 μm)	flat, fine grained
Impurity sources	hot zone parts	filaments	grid	carbon ribbon	mullite, carbon
Impurity segregation	$k_0 < k_e < 1$	$k_0 < k_e < 1$	–	$k_e \sim 1$ or less	$k_e \sim 1$ or less
Use of impure silicon	with restrictions	yes	yes	yes	yes
Areas of concern	width, stresses	bowing, stresses	crystal structure	crystal structure	crystal structure

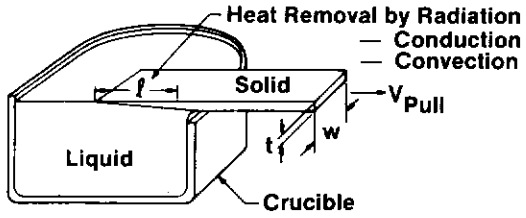

Fig. 32. Schematic of the JSC HRG and EMC LASS techniques.

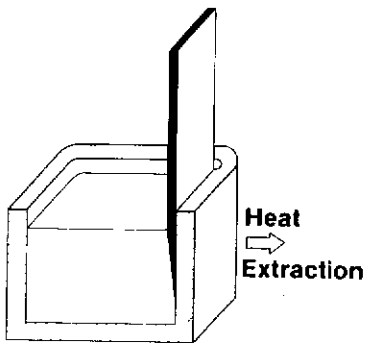

Fig. 33. Schematic of the Heliotronic ICC method.

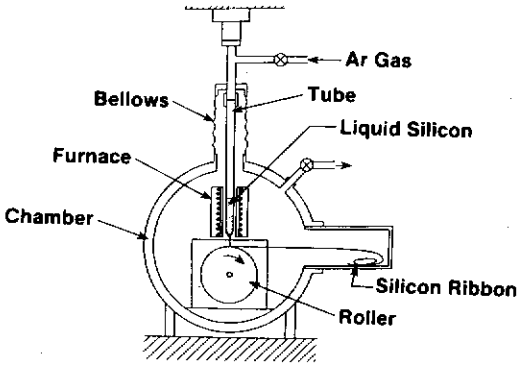

Fig. 34. Schematic of the Tohoku RQ method.

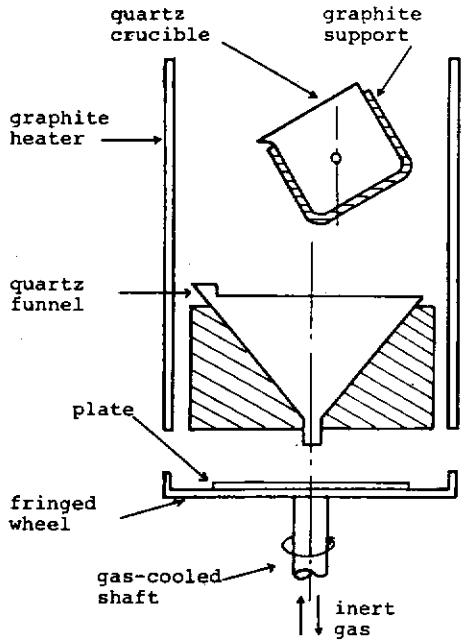

Fig. 35. Schematic of the Hoxan spinning method.

case of M_1 or M_2 menisci. Also, because the ribbon is wedge-shaped at the growth front, the heat-loss surface from which the latent heat is to be removed is very close and nearly parallel to the surface where heat is generated. The separation distance is less than or equal to t. Both of these factors contribute to efficient heat removal and high growth rates.

HRG has been applied to silicon using convective cooling and active thermal control and also in the LASS version where passive thermal modifiers are employed. ICC is a vertical version of the M_3 meniscus. One shaped and cooled wall of the crucible serves as the heat removal means, in conjunction with a thin liquid slag layer that separates the ribbon surface from the crucible wall. The "meniscus" in this case is the liquid silicon in the crucible. The ICC process is currently being extended to an inverted mode, much like roller quenching, but with an intermediary slag layer. Roller quenching is conducted by dispersing a stream of liquid silicon downward onto the cylindrical surface of a rapidly rotating, large-diameter, water-cooled metal wheel. Thus, in this case, the M_3 meniscus is inverted. The liquid is above the solidifying wedge of silicon and heat is removed from the lower surface of the wedge which contacts the water-cooled metal wheel. This nearly instant heat dissipation accounts for the extraordinary growth rates achieved. Spinning is a similar quenching method, but it is a batch sheet casting process that uses the flat horizontal surface of a rotating disc.

Tables 10 and 11 list some of the characteristics and factors that affect the stability and purity of the extended-meniscus growth methods.

In addition to meniscus geometry, the degree of shaper/melt interaction is a major factor in determining the PV performance of silicon sheets, since it can influence both grain size and purity levels. Figure 36 groups the various growth methods by both meniscus geometry and shaper/melt interaction. The three groups from left to

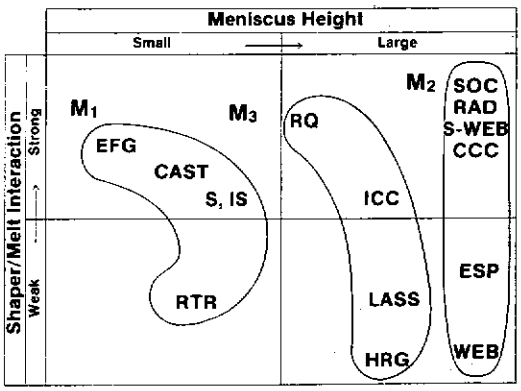

Fig. 36. Placement of growth methods by meniscus height and shaper/melt interaction.

Table 10
Some characteristics of extended-meniscus sheet growth methods.

	HRG	LASS	ICC	Spinning	RQ
Growth rate (mm/min)	100–900	90–700	120	6×10^3	2×10^6
Maximum width (mm)	50	150	50	100	50
Minimum thickness (μm)	200	300	400	300	20
Maximum length (cm)	>200	900	80	10	–
Crystal structure	single and dendritic	dendritic	twins and mm G.S.	mm grains	10–30 μm columnar
Solar cell efficiency (%)	9–10, AM1, No AR	9–11, AM1, AR Coat	–	6–10, AM1, AR coat	5, AM1, CVD-epi
Technology/skill	–	–	–	–	–

Table 11
Factors affecting stability and purity of extended-meniscus methods.

	HRG	LASS	ICC	Spinning	RQ
Meniscus height	–	–	–	< 0.5 mm	–
Thermal control	–	–	–	easy	–
Surface morphology	irregular dendritic	irregular dendritic	–	irregular	–
Impurity sources	crucible, graphite	crucible, graphite	slag, crucible	plate	air, roller
Impurity segregation	–	–	–	no	no
Use of impure silicon	–	–	–	–	–
Areas of concern	crystal structure	crystal structure	crystal structure	crystal structure	crystal structure

right are associated with the M_1, M_3, and M_2 type of meniscus. Within each group, the degree of shaper/melt interaction increases from bottom to top. Generally speaking, crystal properties are better with low shaper/melt interaction and control is easier with a high meniscus. An extended meniscus appears to be necessary for fast growth.

4.3. Crystal growth rates

In the preceding sections, we have described typical ingot and sheet growth characteristics as well as ingot sawing parameters. To compare the surface area generation rates or throughput of ingot growth and sawing with ribbon growth, we now examine mathematical models for both processes.

When a silicon sheet is grown, surface area is generated at the rate

$$R_s = vW, \tag{17}$$

where v is the linear pulling speed and W is the sheet width. For ingots, the rate of surface area generation R_i is made up of two parts. During growth, potential surface area (*if* the ingot was wafered) is generated at a rate

$$R_g = AN_w v, \tag{18}$$

where A is the cross-sectional area of the ingot (πr^2 for a round ingot), N_w is the number of wafers that *could* be cut per unit length, and v is the ingot pulling speed. Once the ingot is grown, it must be wafered. If a saw blade can cut A_b area per unit time and there are N_b blades in the saw, then the saw can produce R_w surface area per unit time from the ingots:

$$R_w = A_b N_b. \tag{19}$$

The combined rate of surface area generation from ingot technology is

$$R_i = 1/(1/R_g + 1/R_w) \quad (20)$$

$$= AA_bN_bN_wv/(AN_wv + A_bN_b). \quad (21)$$

The maximum growth rate expected for silicon ingot technologies $v_i(\max)$ occurs when the temperature gradient in the melt at the solid/liquid interface approaches zero and to first order is given by

$$v_i(\max) = (1/L\varrho_m)(\sigma\varepsilon K_m T_m^5/r)^{1/2}, \quad (22)$$

where L is latent heat of fusion (12.1 kcal/mol.), ϱ_m is density at the melting temperature (2.29 g/cm^3), σ is the Stefan–Boltzmann constant (5.67×10^{-8} J/K^4 m^2 s), ε is the emissivity (0.46), K_m is the thermal conductivity at the melting temperature (0.287 W/cm K), T_m is the melting temperature (1685 K), and r is the ingot radius. A similar expression gives the maximum growth rate $v_s(\max)$ for sheet growth methods that have a solid/liquid interface area Wt, where W is the sheet width and t is the thickness:

$$v_s(\max) = \frac{1}{L\varrho_m}\left(\frac{\sigma\varepsilon(W+t)K_mT_m^5}{Wt}\right)^{1/2}. \quad (23)$$

Achieved growth rates are about 0.3 times the theoretical maximum values, because of the difficulty of realizing growth from isothermal melts in cold environments. In this sense, $v_i(\max)$ and $v_s(\max)$ represent upper limits not likely to be reached or exceeded. The derivation of eq. (23) assumes that (a) heat loss from the crystal is only by radiation to a cold environment; (b) the solid liquid interface is planar; (c) the thermal conductivity of the crystal varies inversely with temperature; and (d) the surface emissivity ε of the crystal is temperature-independent. A one-dimensional linear heat flow approach is used.

Heat from the solidification front is dissipated by conduction along the ribbon and radiation from the ribbon surface. Heat conduction along the ribbon is given by

$$Q = AK\frac{dT}{dx} = WtK\frac{dT}{dx}, \quad (24)$$

where A is the ribbon cross-sectional area, K is the thermal conductivity of the ribbon, x is the distance along the ribbon from the solid/liquid interface, and T is the crystal temperature.

Heat loss from an element dS of the ribbon surface dx long via radiation to a cold environment is

$$dQ = \sigma\varepsilon T^4 dS = 2(W+t)\sigma\varepsilon T^4 dx. \quad (25)$$

For many materials of interest, particularly semiconductors such as silicon, the solid conductivity K can be approximately expressed as $K = K_mT_m/T$ [assumption (c) above]. Making this substitution in eq. (24) and combining eqs. (24) and (25), we get the differential equation

$$\frac{d}{dx}\left(T^{-1}\frac{dT}{dx}\right) = \frac{2(W+t)\sigma\varepsilon T^4}{WtK_mT_m}. \quad (26)$$

The solution of eq. (26) for boundary conditions

$$T = 0, \frac{dT}{dx} = 0 \text{ at } x = \infty$$

and

$$T = T_m \text{ at } x = 0$$

is

$$T = \left[2\left(\frac{(W+t)\sigma\varepsilon}{WtK_mT_m}\right)^{1/2}x + T_m^{-2}\right]^{-1/2}. \quad (27)$$

The derivative of eq. (26) evaluated at $x = 0$ is

$$\left(\frac{dT}{dx}\right)_{x=0} = \left(\frac{dT}{dx}\right)_m = -\left(\frac{\sigma\varepsilon(W+t)T_m^5}{WtK_m}\right)^{1/2}. \quad (28)$$

The maximum growth rate or pulling speed $v_s(\max)$ occurs when the temperature gradient in the melt at the interface approaches zero and is given by

$$v_s(\max) = \frac{-K_m}{L\varrho_m}\left(\frac{dT}{dx}\right)_m, \quad (29)$$

where $(dT/dx)_m$ is the temperature gradient in the crystal at the solid/liquid interface. Combining eqs. (28) and (29) results in the maximum growth rate under the stated assumptions [i.e., eq. (23)]. Figure 37 is a graphical representation of eqs. (22) and (23). If the ratio W/t is large, the maximum

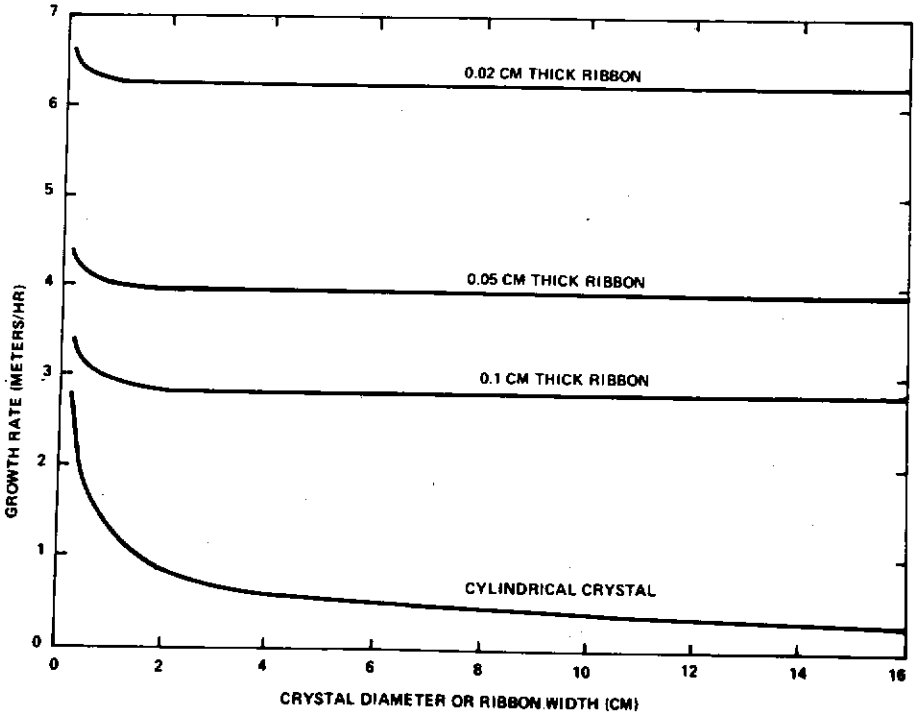

Fig. 37. Maximum growth rate as a function of ribbon width or crystal diameter for silicon.

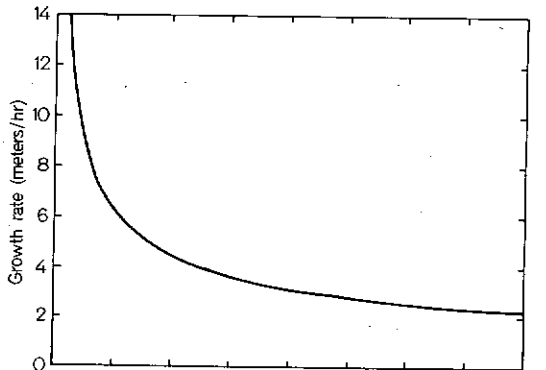

Fig. 38. Maximum growth rate versus thickness for silicon sheets with an M_1 or M_2 meniscus (non-dendritic growth).

sheet growth rate is independent of W and depends only on t, as shown in fig. 38.

Using eqs. (17) and (21) with geometry-dependent upper growth-rate limits from eqs. (22) and (23), we can now compare the surface area generation rates for ingot growth with sawing (R_i) and sheet growth (R_s), as in fig. 39. The curved lines in the figure are for ingot growth with ID sawing (one and 10 saws per ingot) and MBS sawing using blade packs that contain 100, 500, and 1000 blades (N_b). For ID sawing, A_b was assigned the value 0.15 m^2/h, with N_w = 2000/m. For MBS sawing, A_b = 0.007 m^2/h/blade and N_w = 2500/m were used. The straight lines represent 200 μm thick ribbon growth. The rates for a single ribbon and up to five multiple ribbons with an M_1 or M_2 meniscus are displayed. From fig. 38, it is evident that this type of ribbon is unlikely to ever be grown faster than 10 m/h (16 cm/min) in a non-dendritic mode at useful thicknesses (> 100 μm). Faster growth has been demonstrated for the M_3 meniscus, and the lines shown for HRG and RQ growth in fig. 39 represent achieved values.

It is evident that wafering is the rate-limiting step in ingot technology. It is not clear that either ingots or sheets have a distinct edge in achieving highest throughput rates of good quality solar cell material. Ingot technology is burdened with sawing costs and material waste–factors that do not enter into the comparison shown in fig. 39.

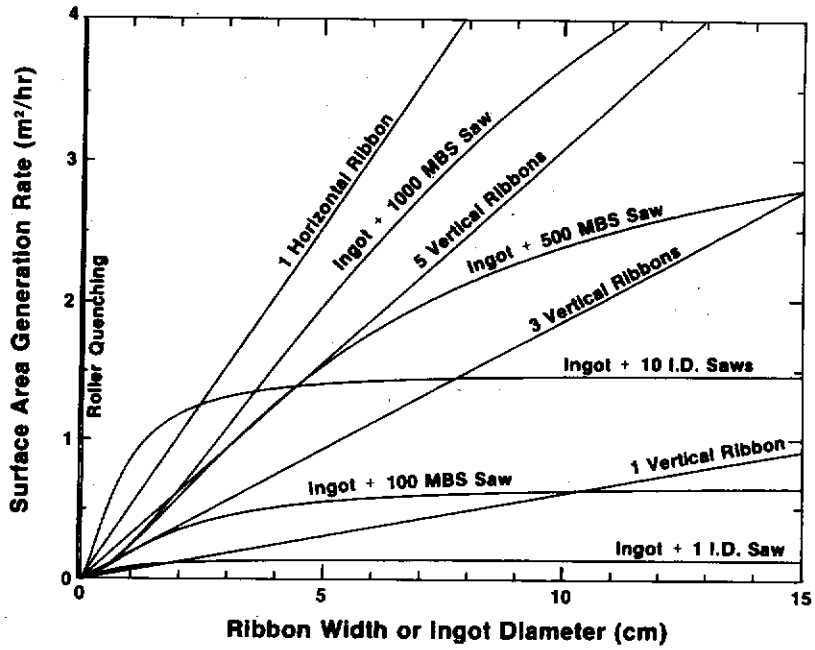

Fig. 39. Surface area generation rates as a function of width for various sheet and ingot/wafering technologies.

5. Future trends

In ingot technology, the wafering step represents a serious obstacle to achieving high throughputs. Some progress has been made recently in MBS sawing, but only on a small scale. Future work should address the attainment of smoothly functioning, rugged, durable, large blade packs.

An advantage of one of the ingot approaches, casting, is that solidification need not be the rate-limiting factor for R_g; i.e., solidification can occur with a low capital equipment cost, independent of melting and pouring. Thus, very high throughputs could be achieved in a mode of operation more like a metallurgical foundry than a crystal growth lab. However, some indications are that high efficiencies are necessary for large-scale PV deployment. In that case, the crystal structure of Bridgman and cast silicon may not be adequate. The FZ growth method, which can achieve high-lifetime, low-resistivity crystals, may then be of more importance. 19% AMI silicon cells have already been made, and material and device fabrication improvements should make efficiencies greater than 20% possible in the near future.

No ideal sheet growth method, encompassing crystal perfection, flat smooth surfaces, high purity, easy control, and high throughput, seems to have been attained yet, although all of these characteristics have been achieved singularly. Some methods (e.g., ESP) have made encouraging progress in a compromise approach to achieving these attributes. Future directions here will be aimed at combining good sheet crystal quality with high throughput. Thermally induced stress is one problem common to all M_1 and M_2 techniques. Its role in the M_3 extended-meniscus methods is at present unclear. The fast growth methods appear to be limited in crystal structure quality. Roller quenching and melt spinning tend to result in small columnar grains. Horizontal and ICC growth have a tendency to propagate unwanted dendrites; this is a problem even in fast modes of the CCC/S-WEB technique. Dendrite structures, once formed at the growth front (as shown in fig. 40), can propagate very rapidly in a linear direction within the (111) twinning plane

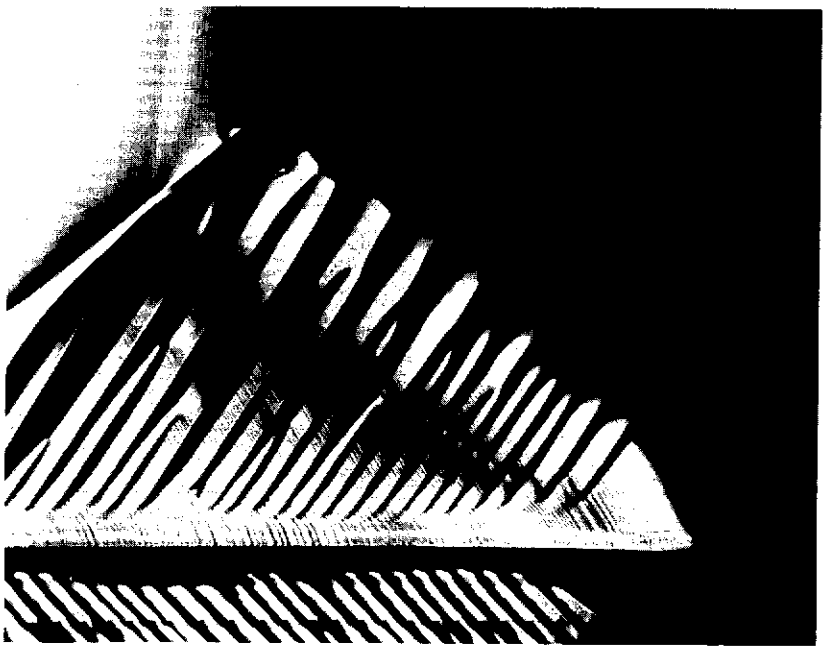

Fig. 40. Photomicrograph showing an early stage of dendritic growth breaking 1.9 mm ahead of a non-dendritic advancing horizontal sheet edge.

while growing quite slowly in perpendicular directions. Dendrite growth rates in supercooled silicon melts have measured as large as 2.5 m/min in the fast direction and a factor of 25 slower in perpendicular directions. It is not known whether fast, controlled sheet growth can be maintained without a dendritic growth mechanism.

It is encouraging that so many different approaches to growing silicon crystals for photovoltaics are progressing so rapidly, and that it appears to be possible to attain both high-efficiency devices using sophisticated growth methods and lower efficiency devices using simple growth methods with silicon.

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