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Galvanic Corrosion of Stacked Metal Gate Electrodes During Cleaning in HF Solutions

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Introduction

According to the ITRS Roadmap [1], new dielectric and metal gate materials will be required for high performance and low stand-by power applications at the 45 nm technology node and beyond. Currently, many candidate materials are under investigation. Based on the state-of-the-art [2,3,4], some of the most likely candidates to be used as metal gate electrodes include TiN, TaN, Mo and Ru. To address the workfunction tuning issue in this future generation of transistors, a possible approach is to use a metal layer on the high-k dielectric to control the workfunction and a conductor material on top to make the gate electrical contact (fig. 1). As a result, it creates a risk of galvanic enhanced corrosion at the gate electrode level during wet cleaning. We have studied galvanic coupling between the dissimilar materials of the gate electrode (TiN, Mo, Ru, PolySilicon). The study focuses on diluted HF mixtures, which in general show overall better compatibility with metal gates than strong oxidizing chemistries. Diluted HF based mixtures are used for residual high-k removal and post-etch residues removal [5]. In addition, it is also used for removal of oxide hardmask after etching of the metal gate stack.

As a model system, Ru, Mo or TiN are selected as first metal in the stack (workfunction metal) and silicon based materials as second material on top (conductor). Hence, it basically creates a PolySi/Metal contact. Depending upon the integration scheme, different anode/cathode ratios can be present (fig. 1). In the classical integration scheme the post etch residues and the hardmask are removed after etching of the full gate stack (fig. 1a). Since the hardmask is often silicon oxide-based, this approach will result in an attack of the isolation oxide by diluted HF solutions. An alternative approach involves a two steps etching that stops first on the workfunction metal layer (fig. 1b). The hardmask removal is done and then the metal layer is etched. This complex approach has the advantage to decrease the recess of the field oxide which is especially important for future 3D finFET transistors structures where box oxide recess should be minimized.

Experimental details

Blanket layers of the metal gate materials under investigation were deposited on 100 nm thermal SiO_2 grown on 200mm Si wafers. Then 80 nm films of Ru, 50 nm of Mo, 70 nm of TiN and 100 nm of PolySi were deposited on the oxide by physical vapor deposition (PVD) for Ru, Mo and TiN and chemical vapor deposition (CVD) for PolySi. The doped PolySi received a Boron dose of 1E15 atoms/cm^2 at 15KeV followed by a RTP anneal.

For electrochemical measurements, wafer pieces were mounted in a custom-build Teflon body liquid cell with a Viton O-ring to fit pieces. The exposed area is 0.28 cm^2. The metal gate material under investigation is connected to the working electrode of a Potentiostat/Galvanostat (IM6 from Zahner). Open-circuit potentials were recorded from the time of immersion of the sample into the electrolyte. Potentiodynamic polarization curves were measured at a scan rate of 1mV.s^{-1} from the open circuit potential to anodic or cathodic directions after a steady-state open-circuit potential was

reached. The reference electrode is a plastic body gel filled electrode resistant to dilute HF (Sensorex). In this work, all the potentials are referred to this reference electrode. Galvanic current were measured with the Potentiostat/Galvanostat in Zero-Resistance Ammeter (ZRA) configuration. For galvanic current measurements, the anode and the cathode are placed face to face separated by a distance of 2 mm filled by the electrolyte. The solutions were prepared with ultra pure water and 49% HF electronic grade. The samples were used as deposited and a new sample was used for each experiment. All the experiments were done in a cleanroom environment class 1000. The cleaning solution was deoxygenated or oxygen saturated by 1h30min of N_2 or O_2 bubbling.

In addition, 170 nm wide meander lines consisting of undoped or doped PolySi deposited on TiN or Mo on top of HfO_2 were prepared. The PolySi/metal stack was fully etched until the HfO_2 or partially etched until the metal layer before exposure to HF solutions. The patterned structures were cleaned in a 200 mm single wafer cleaning tool with different diluted HF solutions and the corrosion after the different treatments was evaluated using Scanning Electron Microscope inspection (Nova200 Nano SEM).

Results

The extend of galvanic corrosion between dissimilar materials will depend upon different factors, such as the electrochemical properties of the materials that can act as an anode or cathode, the respective anode/cathode area ratio and finally the electrolyte properties of the cleaning solutions.

Various Gate stacks - A large potential difference exists between the various materials in dilute HF (fig. 2). This will be the driving force for the galvanic corrosion phenomena increasing the corrosion kinetic of the less noble material and decreasing the corrosion of the more noble material. PolySi has the more negative corrosion potential. It will therefore suffer from increased corrosion upon coupling to TiN, Mo or Ru. It can be observed that for an identical cathode/anode area ratio we can expect a larger galvanic attack for PolySi/Ru contact than PolySi/Mo and PolySi/TiN contacts.

In figure 3, the galvanic current measured for PolySi/PolySi is at the level of the detection limit of the tool. For PolySi/TiN, the galvanic current is below 1E-5 A/cm^2. This corresponds to an estimated PolySi etch rate below 0.2 nm/min and it is not a significant increase compared to the intrinsic etch rate of the B doped PolySi in HF of 0.11 nm/min. Consequently, the galvanic enhanced corrosion is negligible for 1:1 area ratio. But for PolySi/Ru with 1:1 area ratio, the galvanic coupling increases the PolySi corrosion to 1.75 nm/min, which is 16 times faster than without Ru coupling. Thus for conventional planar CMOS, with area ratio from 1:1 down to 7:1 depending upon the metal gate and PolySi layers thicknesses, the galvanic corrosion will be an issue only for highly noble materials like Ru coupled with highly active ones like PolySi.

Anode/Cathode area ratio - However for future 3D transistors, alternative integration schemes are being introduced to reduce the loss of the field oxide by keeping the metal gate on the wafer surface during the removal of the oxide hardmask (fig. 1b). As a consequence, the relative area of exposed metal and polySi leads to unfavorable anode/cathode ratio. It follows that the galvanic current increases significantly and cannot be neglected anymore even for a PolySi/TiN couple as shown in figure 4. By increasing the TiN surface area by a factor of one hundred compared to the PolySi surface, the galvanic current increases by more than one order of magnitude.

Dissolved oxygen and electrolyte flow – In figure 4, it is also shown that the galvanic current increases with the oxygen concentration dissolved in the electrolyte. Furthermore the current increases with the cathode rotation speed as shown in table I. These results indicate that oxygen reduction takes place on the cathode surface in HF aerated solution. The dissolved oxygen transport mechanism towards the cathode limits the overall corrosion rate. Consequently a continuous liquid flow increases the galvanic current because it can promote the oxygen supply to the cathode surface. We can conclude that a quiescent oxygen free HF mixture will lead to less galvanic corrosion than an aerated mixture dispensed with a spray or nozzle as for most single wafer cleaning tools with chemical recirculation loop.

Tests on structures - The galvanic corrosion at the level of the transistor gate stack in HF solutions is illustrated with tests structures (fig. 5, 6 and 7). Some PolySi lines were patterned directly on TiN or Mo layers with an HfO_2 underlayer.

The PolySi/TiN couple is not likely to generate a large galvanic current for a 10:1 area ratio as it can be concluded from figure 2: a galvanic current of 1E-5 A/cm^2 is measured for a 1:1 contact between PolySi and TiN and consequently for a 10:1 anode/cathode ratio corresponding to gate structures shown in figure 1a, the current should be less than 1E-5 A/cm^2. So the enhanced corrosion should be negligible. No corrosion is apparent on the SEM cross section after 10 min in 0.5%HF on a single wafer cleaning tool (fig. 5). But for gates patterned using the second approach, the process flow leads to PolySi lines coupled with a large area of TiN. This results in a dramatic attack of the PolySi gate electrode in 0.5 wt.%HF (fig. 6).

According to the electrochemical results obtained on macroscopic electrodes of blanket materials (fig. 2), a larger corrosion for a PolySi/Mo couple is expected compared to a PolySi/TiN couple. This result is confirmed by figures 6 and 7 showing a larger attack for the Mo contact.

Summary

This work demonstrates that future metal gate electrodes can form a galvanic cell in dilute HF solutions and can result in an increased corrosion of the less noble material. In the worst case, it could lead to fully removal of small gate electrodes during wet processing. Depending on the gate stack and the integration scheme, the galvanic corrosion at the gate could be a major problem. In this case, dissolved oxygen and flow rate of the HF mixture during cleaning offer opportunities to minimize the galvanic corrosion impact.

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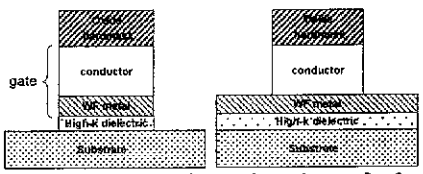

Figure 1: Two possible integration schemes for future generation of transistors a) complete etching of the gate stack prior hardmask removal and b) two steps etching.

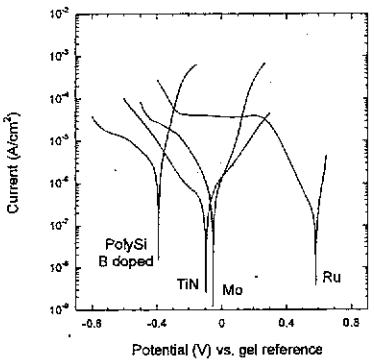

Figure 2: Potentiodynamic polarization curves in 2 wt.% HF aerated in static solution - scan rate 1mV/s.

Table I: Calculated etch-rate from galvanic currents for PolySi with/without Ru coupling in 2 wt.%HF aerated.

	No coupling	Coupling with Ru area ratio1:1		
Ru rotation (rpm)	0	0	200	1000
etchrate (nm/min)	0.11	1.8	11.9	17.1

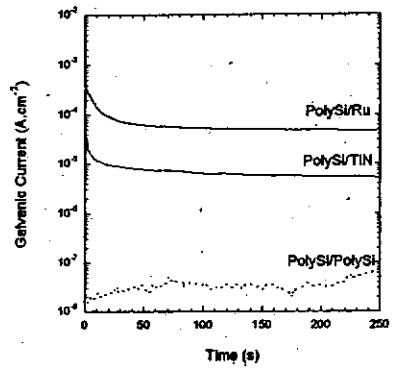

Figure 3: Galvanic current density versus time in 2 wt.% HF aerated and static (anode/cathode ratio 1:1).

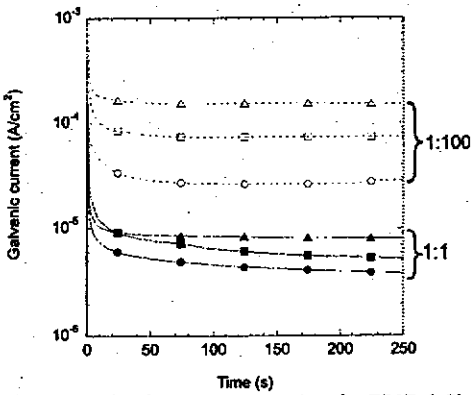

Figure 4: Galvanic current versus time for TiN/PolySi couples in static 2 wt.%HF (Δ) oxygen saturated, (□) aerated or (o) deaerated with anode/cathode ratios 1:1 (solid line) and 1:100 (dash line).

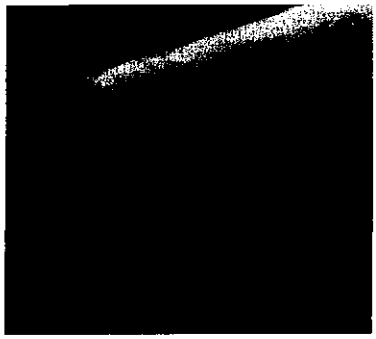

Figure 5: SEM cross section picture of undoped PolySi/TiN gate stack fully etched until the HfO_2 layer after 0.5 wt.% HF during 10 min aerated on a single wafer cleaning tool (case of figure 1a).

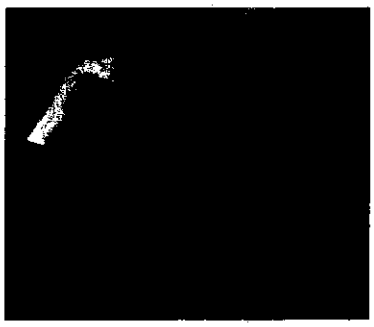

Figure 6: SEM cross section picture of undoped PolySi on TiN/HfO_2 after 0.5 wt.% HF during 10 min aerated on a single wafer cleaning tool (case of figure 1b).

Figure 7: SEM cross section picture of undoped PolySi on Mo/HfO_2 after 0.5% HF during 10 min aerated on a single wafer cleaning tool (case of figure 1b).