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High-Hole-Mobility Silicon Germanium on Insulator Substrates with High Crystalline Quality Obtained by the Germanium Condensation Technique

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Thin SiGe-on-insulator (SGOI) substrates with Ge content varying between 42 and 93% were produced by the Ge condensation technique and full structural characterization was carried out. In a second step, the electrical properties of these substrates were analyzed by the pseudo metal-oxide semiconductor field-effect transistor technique which allowed determination of the carrier low-field mobilities, as well as the density of fixed charges in the buried oxide (BOX) and the density of interface traps at the BOX-SiGe film interface. Optimization of intermediate anneals in argon during the condensation process made the production of high crystalline quality and high-mobility substrates possible (up to 400 $cm^2\ V^{-1}\ s^{-1}$ for a 93% SGOI). Opposite trends were observed for holes and electrons: while the hole mobility increases with increasing Ge content, the electron mobility decreases. In addition, the density of interface traps and also the density of oxide charges were found to increase with increasing Ge content. Possible causes for this increase are discussed.
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While silicon (Si) is being brought to its extreme limit by applying strain (local, global, or process-induced), there is currently extensive interest in high-mobility materials to replace Si for ultimate device scaling. Germanium (Ge) holds two main benefits over Si for metal-oxide semiconductor field-effect transistor (MOSFET) application: it exhibits higher room-temperature bulk carrier mobilities (3900 $cm^2\ V^{-1}\ s^{-1}$ for electrons and 1900 $cm^2\ V^{-1}\ s^{-1}$ for holes as compared to 1400 and 500 $cm^2\ V^{-1}\ s^{-1}$, respectively, for Si) and it has a lower bandgap; therefore, lower supply voltages can be applied. Although the inferior properties of GeO_2 as compared to SiO_2 for gate insulation have obstructed the integration of MOSFETs on Ge, recent expertise acquired on high-κ dielectrics renewed interest in Ge technology.[1,2] p-Channel MOSFETs with performances exceeding the best similar strained Si devices have been demonstrated experimentally.[3,4]

Because there is low availability of Ge on earth, resulting in its high material price, it is most likely that Ge technology will be developed on hybrid substrates where only a thin Ge layer is present on a Si substrate serving as mechanical support. Besides epitaxial Ge layers on Si,[5-7] germanium on insulator (GeOI) substrates not only benefit from the higher transport properties of Ge but offer better electrostatic control for short channel effects and reduced junction capacitances.

Among the many techniques that have been proposed for production of GeOI wafers (layer transfer,[8] wafer bonding and grinding,[9] wafer bonding and etchback,[10] liquid phase epitaxy,[11] fully epitaxial growth using crystalline and lattice matched oxide,[12] etc.), the Ge condensation technique (also referred as thermal mixing) is an interesting approach (wafer scalability, ultrathin GeOI, etc.).[13-15] This method is based on the epitaxial growth of a Si-rich SiGe layer on a silicon-on-insulator (SOI) substrate followed by high-temperature selective oxidation of Si atoms to condense the Ge atoms in a thinner, Ge-rich SiGe layer. The peculiarity of this technique is the concomitance of two phenomena which are, namely, the selective oxidation of Si at the top SiO_2/SiGe interface and the diffusion of Ge through the SiGe and the top Si layer of the SOI. This intermixing prevents Ge from piling-up at the oxidizing top interface and consequently allows Si atoms to always be provided to the oxidation advancing front. In addition, the buried oxide (BOX) and the top thermal oxide act as diffusion barriers for Ge atoms during the whole oxidation process. The lattice constant of a SiGe layer increases with the Ge content. As a first approximation, it increases linearly between the lattice constant of Si to the one of Ge as a function of the Ge content according to Vegard's law.[16] This implies that during the condensation process, a high level of stress is generated in the SiGe layer. This stress can be relaxed by different mechanisms: compliance of the BOX,[17] generation of dislocations,[18,19] or roughening of the SiGe layer.[20] The creation of defects may have an important impact on the final electrical transport properties of the SGOI or GeOI layers.

In this paper we evaluate the structural properties of SiGe layers with Ge atomic fraction varying from 42 to 93% obtained by the Ge condensation technique. As a next step we assess the electrical transport properties of these layers by pseudo-MOSFET measurements. We also demonstrate that the introduction of annealing steps in inert atmosphere (argon) during the condensation process results in an improvement of the crystalline quality and uniformity of the layers, as well as an enhancement of their electrical properties.

Experimental

Ge condensation process.— Sample preparation.— For starting material, 200 mm SOI wafers with a 5×10^{17} atom/cm^3 boron-doped top Si layer of 22 nm and a BOX of 140 nm were used. After a 2% HF clean and a 850°C bake in H_2 at reduced pressure, a 100 nm intrinsic $Si_{0.83}Ge_{0.27}$ layer was deposited using SiH_4 and GeH_4 as gas precursors in an ASM Epsilon 2000 reactor at 600°C. A 7 nm Si cap grown at 650°C was added on top of the stack to avoid Ge oxidation during the early stage of the condensation. The oxidation of the different layers was performed in an ASM vertical furnace with a SiC tube in dry ambient. To minimize the processing time, a three-step oxidation was carried out. A first oxidation at 1150°C allowed increasing the Ge content from 27 to 42%. According to the binary diagram of SiGe alloy,[21] a second oxidation step at 1000°C allowed us to reach a Ge fraction of 75% without melting the layer. Finally, with a last step at 900°C, SiGe-on-insulator (SGOI) substrates with a Ge content of 93% were obtained. In our standard process, hereafter referred to as "no anneal," the dry O_2 oxidizing atmosphere was maintained during the temperature ramping down between oxidation steps, which means that the oxidation

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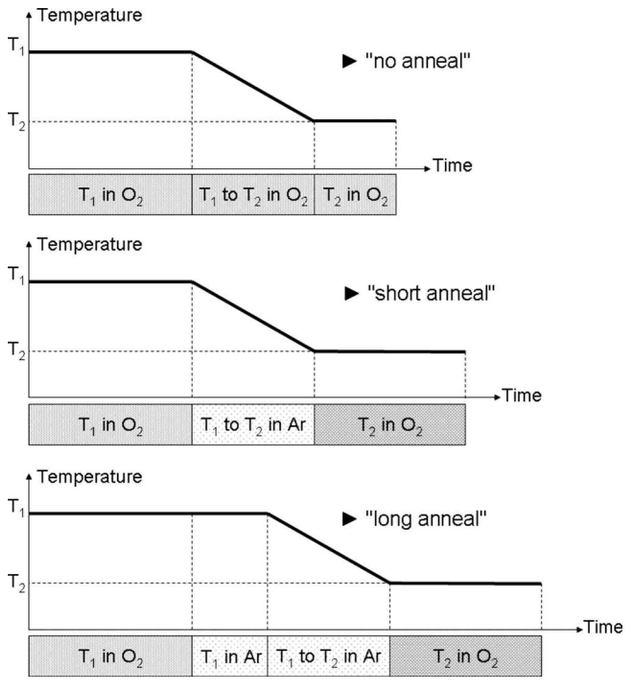

Figure 1. Schematic representation of temperature profile and ambient atmosphere in the furnace for the different types of dry oxidation and Ar anneals.

was continuous through the whole process. SGOI with different Ge contents were obtained by stopping the process during the first, second, or the third oxidation.

In an attempt to improve the crystalline quality and uniformity of the layers, various additional bakes in argon (Ar) atmosphere were implemented between the different oxidation steps. The first type of anneal, hereafter referred to as "short anneal," consisted of replacing the oxidizing atmosphere during the temperature ramp down between two oxidation steps by Ar atmosphere. Because no oxidation occurs during ramp down, the following oxidation step was extended in order to reach the same Ge content as in the standard process. The second type of anneal, hereafter referred to as "long anneal," consisted of a 1 h bake in Ar before ramping down the temperature, followed by another ramp down of temperature in Ar to the next oxidation step. As for the "short anneal" process, because no oxidation occurs during the ramp down, the next oxidation step was extended to reach a similar Ge content as our standard process. A schematic of the different Ar anneal types is given in Fig. 1.

Sample characterization.— The thicknesses of the different layers were determined by cross-sectional scanning electron microscopy (SEM). The crystalline quality was assessed by cross-sectional transmission electron microscopy (TEM). The Ge content in the SiGe layer was measured by Rutherford backscattering spectroscopy (RBS). High-resolution X-ray diffraction (XRD) of the symmetric (004) diffraction peak was used to determine the strain/relaxation and the in-plane lattice constant in the SiGe layers, taking into account the Ge content determined by RBS. XRD was also used to qualitatively assess the crystalline quality of our films. Atomic force microscopy (AFM) was used to measure the surface roughness of the SGOI layers after removal of the top thermal oxide in 2% HF.

Pseudo-MOSFETs measurement.— The pseudo-MOSFET technique is a fast and efficient method to characterize electrical properties of any film on insulator substrate at the wafer scale.[22,23] After oxidation, the thermal oxide was removed in HF and 5×5 mm square islands were patterned in the SiGe layers down to the BOX by dry etching with SF_6 chemistry using a photoresist mask. To

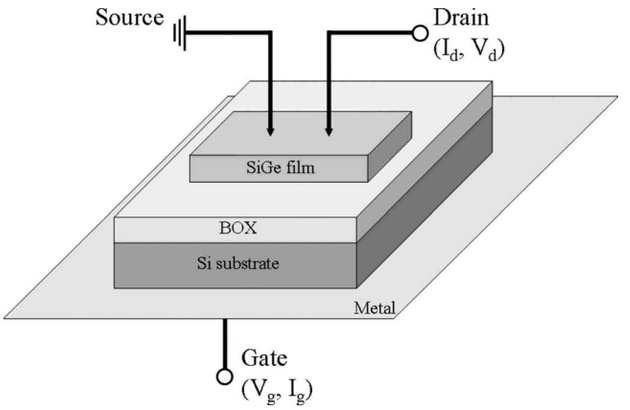

Figure 2. Schematic representation of the pseudo-MOSFET measurement.

form a source and a drain, two pressure adjustable probes were contacted on the SiGe film acting as a transistor body. The Si substrate was used as the gate and the BOX as gate dielectric to activate either a hole ($V_g < 0$ V) or an electron channel ($V_g > 0$ V) at the SiGe/BOX interface (Fig. 2). For each sample, five $I_d(V_g)$ curves were recorded at a low drain bias of 0.2 V using the same probe pressure. The low field mobility was determined using the series resistance independent function Y [see Eq. 1 in which I_d represents the drain current, g_m is the transconductance $(\partial I_d/\partial V_g)$, μ_0 is the mobility, f_g is the geometrical coefficient, C_{ox} is the oxide capacitance, V_d is the drain voltage, V_g is the gate voltage, V_t is the threshold voltage, and V_{FB} is the flatband voltage].[24] In order to ensure reliable measurement, the level of leakage current through the gate oxide was monitored and leaky samples were eliminated from the analysis

$$Y = \frac{I_d}{\sqrt{g_m}} = \sqrt{\mu_0 f_g C_{ox} V_D}(V_g - V_{t/FB}) \quad [1]$$

The oxide charges (Q_{ox}) in the BOX were responsible for V_{FB} shift through Eq. 2 (N_{SiGe} and N_{Si} are the doping level of the SiGe film and the Si substrate, respectively, k is the Boltzmann constant, T is the absolute temperature, and q is the elementary charge).[22] In this later equation, the intrinsic carrier concentration of the SiGe film, $n_{i\ SiGe}$, was calculated using the effective density of states in the conduction band N_c and in the valence band N_v and the bandgap energy E_g that can be found in Ref. 25. Furthermore, the density of interface traps (D_{it}) at the SiGe/BOX interface was calculated from the subthreshold slope (S) through Eq. 3 [22]

$$V_{FB} = \phi_{ms} - \frac{Q_{ox}}{C_{ox}} \quad \text{with } \phi_{ms} = \frac{kT}{q}\ln\left(\frac{N_{SiGe}}{n_{iSiGe}}\frac{n_{iSi}}{N_{Si}}\right) \quad [2]$$

$$I_d = I_0 \exp\left(\frac{V_g}{S}\right) \quad \text{with } S = 2.3\frac{kT}{q}\left(1 + \frac{C_{Si} + qD_{it}}{C_{ox}}\right) \quad [3]$$

Results and Discussion

Structural properties of the SGOI substrates.— Table I gives an overview of the layer properties of some of the SGOI that have been processed for this study. We can observe that while the Ge content in the SGOI increases and the layer thickness decreases, the Ge dose measured by RBS remains constant, confirming that the Ge atoms are not oxidized and effectively trapped between the two oxides during the condensation process. We observed by AFM (Fig. 3) that while the starting SiGe layer is very smooth, a crosshatch pattern appears on the surface of the SGOI as a result of the relaxation of the stress that builds up during the condensation. We also observed that by introducing Ar anneals, the roughness of the SGOI can be

Table I. Properties of SGOI substrates obtained by Ge condensation.

Sample	Oxidation conditions	Ge content (%)	Ge dose (atom/cm^2)	SiGe thickness (nm)	RMS[a] roughness (nm, 10 × 10 μm^2 area)
As grown	—	27	1.54×10^{17}	104	0.40
A	No anneal	42	1.50×10^{17}	63	1.34
B	No anneal	55	1.50×10^{17}	44	2.10
C	No anneal	74	1.49×10^{17}	35	5.70
C′	Short anneal	75	1.49×10^{17}	35	1.22
D′	Long anneal	93	—	29	—

[a] RMS: root–mean–square.

reduced to a reasonable value (Table I). The drastic reduction of surface roughness using Ar anneal for the 75% Ge atomic fraction samples (sample C and C′) is mainly explained by the improvement in film thickness uniformity, as discussed later. However, the reason the roughness of the 75% Ge SGOI obtained with Ar anneal (sample C′) is lower that the one of the 55% Ge SGOI sample (sample B) is unclear at the moment. TEM imaging of the different samples (see Fig. 4) revealed that it is crucial to introduce anneals in Ar during the condensation process in order to produce high crystalline quality and a uniform SGOI layer with high Ge atomic fraction. While TEM characterization provides both layer thickness uniformity and crystalline information only on a short length scale, extended SEM cross sections were used to check layer uniformity through the whole wafer diameter. Finally, crystalline quality over a large length scale was checked by XRD, as shown in Fig. 5. The comparison between

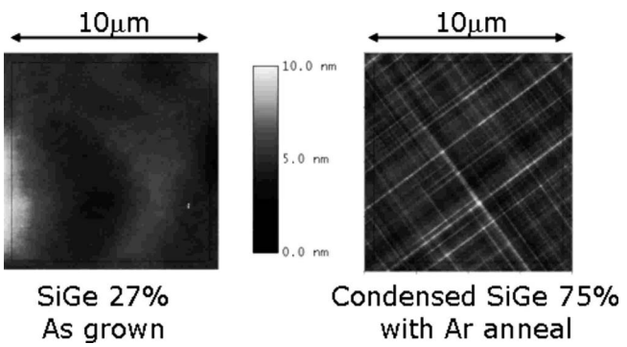

Figure 3. AFM image of SGOI substrates before and after the condensation process, showing the appearance of a crosshatch pattern due to the relaxation of the layer.

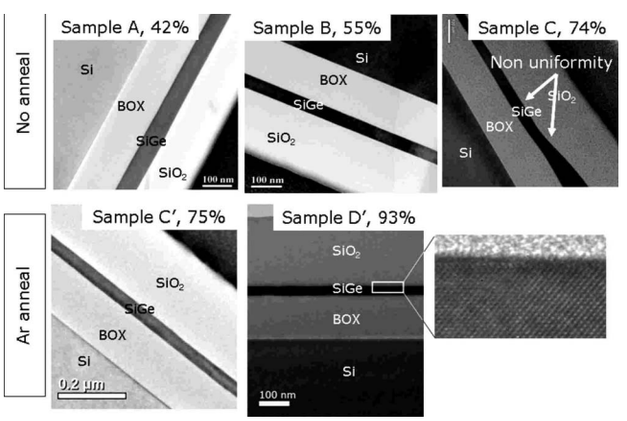

Figure 4. Cross-sectional TEM images of the different SGOIs with increasing Ge content. Comparison of sample C and C′ clearly demonstrate the beneficial effect of the Ar anneal on layer uniformity.

sample C (SGOI with 74% Ge obtained by condensation without anneals in Ar) and sample C′ (SGOI with 75% Ge obtained by condensation with short anneal in Ar) clearly shows that the crystalline quality is improved for the same level of condensation: the intensity of the diffraction peak is increased and the peak becomes more symmetric when Ar anneals are used during the condensation (the peak also shifts to a higher diffraction angle due to a higher degree of relaxation of the layer, as discussed below). The intermediate Ar anneals are beneficial to reduce the threading dislocation density by an annihilation mechanism.[26,27] Another possible effect is the reduction of the piling up of Ge at the oxidizing interface by allowing intermixing in the SiGe layer.[14] The piling up of Ge atoms at the top $SiGe/SiO_2$ interface is more likely to happen for the low-temperature oxidation steps in which the diffusion of Ge is relatively slow as compared to the oxidation. The piling up of Ge atoms at the interface can result in two detrimental effects: local melting of the layer and the participation of Ge atoms in the oxidation process resulting in the formation of a mixed oxide. The formation of a mixed oxide has to be avoided in order not to lose any Ge atoms. We could not measure any Ge in the formed thermal oxide by energy-dispersive X-ray spectroscopy (TEM-EDX), so we think that in the case of sample C, the nonuniformity might be the result of local melting during the oxidation. The in-plane lattice constant of the different SGOI was found to increase during the condensation process. It monotonically varies between the lattice constant of Si

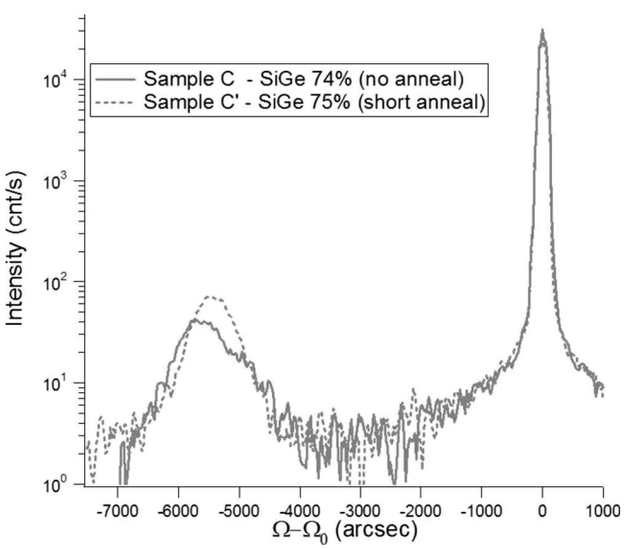

Figure 5. High-resolution XRD symmetrical scan around the (004) diffraction peak showing the improvement of the crystalline quality of the SGOI films with 75% Ge atomic fraction when an Ar anneal is used during the condensation process. (The diffraction peak on the left originates from the SiGe film, whereas the right peak is the diffraction peak from the Si substrate.)

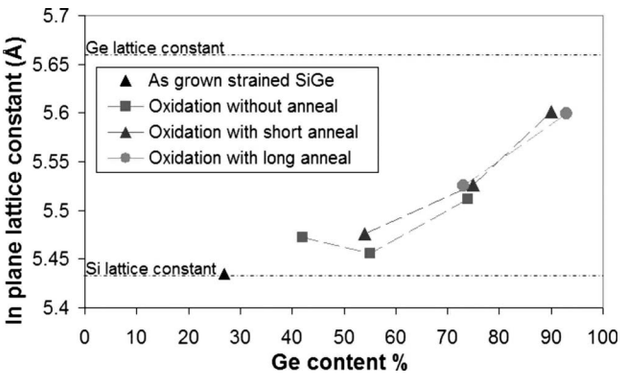

Figure 6. Evolution of the in-plane lattice constant of SGOI substrates as a function of their Ge content and as a function of the type of anneal used in addition to condensation.

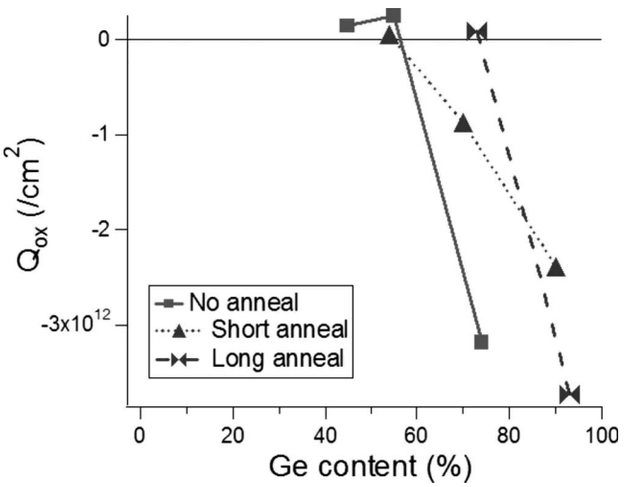

Figure 8. Density of fixed oxide charge (Q_{ox}) in the BOX as a function of the Ge content in the SGOI and as a function of the type of anneal used in addition to the condensation.

and the one of Ge (see Fig. 6), evidencing relaxation of the stress that builds up in the layer during the condensation process. In opposition to this general trend, for the sample obtained by condensation without anneal (square symbols), the in-plane lattice constant of the SGOI with 42% Ge is calculated to be larger than for the SGOI with 55%. This is due to the uncertainty in Ge content determination by RBS (~1%) and to the uncertainty of the Poisson ratio of SiGe films (linear variation assumed). It is worth noting that the SGOI obtained by oxidation with Ar anneals is significantly more relaxed (larger in-plane lattice constant) than without Ar anneals (the relaxation rate increases from 20 to 40% and from 50 to 59% for SGOI with 55% Ge and for SGOI with 75%, respectively). However no difference was observed between the samples that received long or short Ar anneals. Relaxation of the films occurs by the formation of stacking faults, as observed by cross-sectional TEM (not shown here). Extended imaging revealed that the density of such defects remains lower than 10^8/cm^2, even for the samples with high Ge fractions obtained by condensation with Ar anneals.

Electrical properties of the SGOI substrates.— While well-behaved transistor characteristics were observed on SGOI substrates with Ge content up to 55%, we observed degraded subthreshold slopes for higher Ge concentration samples, revealing that the density of interface traps at the BOX/SiGe interface increases during the condensation process (Fig. 7). The SiGe films were found to be fully depleted, as evidenced by the absence of a "leakage" current between V_{FB} and V_t. The flatband and threshold voltages were found to shift to positive gate voltages with increasing Ge content, which made the activation of an electron channel impossible for Ge contents above 70%. The density of oxide charges in the BOX was extracted from the flatband shift V_{FB} (Fig. 8). We can observe that the density of charges in the BOX is increasing drastically for SGOI for Ge atomic fractions above 70%. The reason for the creation of charges in the BOX is unclear for the moment. We can speculate that for such a long high-temperature treatment, Ge and dopants (in our case boron) might diffuse into the BOX and be the source of those charges. However, we could not detect by TEM-EDX nor by RBS any traces of Ge in the BOX within the detection limit of 1%. Boron is known to be easily integrated in a growing oxide but also to diffuse in SiO_2 oxide, resulting in positive flatband voltage shift for p-channel MOSFETs.[28] Another possible reason for the degradation of the BOX with increasing Ge content can be some process-induced damage during the condensation. We show that during the condensation stress is created in the SiGe layer (due to the increase in Ge fraction) and that only part of this strain is relaxed. Obviously, the strained SiGe layer is inducing a large amount of stress to the underlying BOX and structural defects can be created in the SiO_2 matrix. If we now compare the samples with and without Ar anneal, we see that the positive flatband voltage shift is less pronounced in the case of condensation with Ar anneal. This trend can be explained by the fact that during the Ar anneal, we are also curing the defects that were created in the BOX. It is of technological significance to understand the reason for the creation of those charges in the BOX and to try to avoid them. The SGOI and GeOI layers are relatively thin, and even if the devices are built on the surface, electrostatic coupling between the devices and the charges might impact their characteristics.

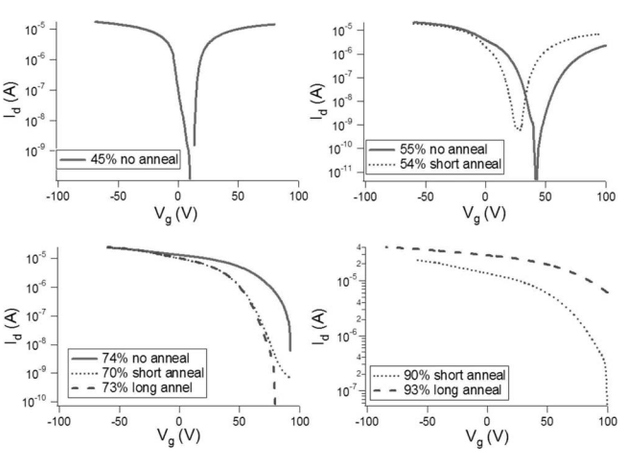

Figure 7. $I_d(V_g)$ characteristics of SGOI substrates measured by the pseudo-MOSFET technique. For the different Ge contents, comparison is made between the different types of Ar anneal.

In Fig. 9 we can observe that with optimized long anneals in Ar, the hole mobility is found to increase with increasing Ge content, whereas the electron mobility drastically decreased for Ge content higher than 50%, as was already observed in Ref. 29. For the sample obtained by condensation without anneal, as can be expected from the increase of Ge fraction, the hole mobility is increasing (Ge has higher hole mobility than Si). However, for the SGOI sample with 75%, the hole mobility drops. This might be explained by the thickness nonuniformity and poorer crystalline quality that were discussed in the previous part. While anneals in Ar do not significantly improve the hole mobility of SGOI for Ge contents up to 54%, we found that short anneals are needed to produce high-hole-mobility SGOI substrates with Ge content of 75% but are not enough to

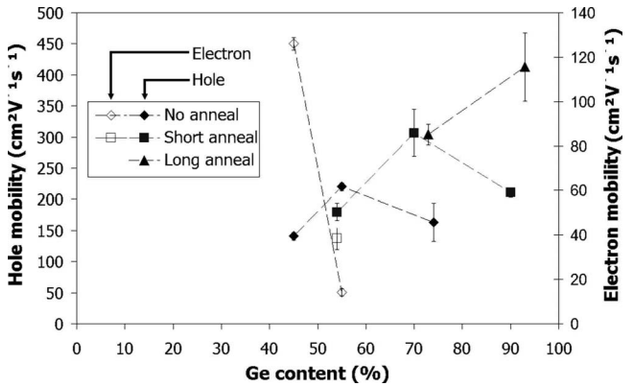

Figure 9. Hole and electron low field mobility of SGOI substrates as a function of the Ge content and as a function of the type of anneal used in addition to the condensation.

produce high-hole-mobility SGOI substrates with 90% Ge atomic fraction. The low hole mobility observed for SGOI with Ge content of 90% obtained by condensation with short anneal should be again related to the thickness nonuniformity and poorer crystalline quality that were observed on such layers. Finally, long anneals are required to produce high-mobility SGOI substrates with Ge content of more than 90%. Therefore we observe a good correlation between the electrical transport properties of the films and their structural characteristics presented in the previous part: an improvement of the uniformity and crystalline quality of the films results in an increase in hole mobility. A high hole mobility of about 400 $cm^2\ V^{-1}\ s^{-1}$ was measured on a 27 nm SGOI with 93% Ge. This represents a factor of 3 improvement over state-of-the-art SOI wafers with a similar thickness[30] and a factor of 2 improvement over strained SOI substrate.[29]

The density of interface traps (D_{it}) at the BOX/SiGe interface is observed to increase with increasing Ge content in the SGOI (Fig. 10). This increase can be due to an increase of dangling bonds at the SiGe/BOX interface or in the structural transition layer. As pointed out earlier, boron can diffuse in oxide and can cause the creation of dangling bonds that are efficient charge traps.[31] Process-induced damage due to the stress imposed by the strained SiGe film can also explain the formation of these interface traps. It is important to notice that the extracted values for the D_{it} are overestimated by the

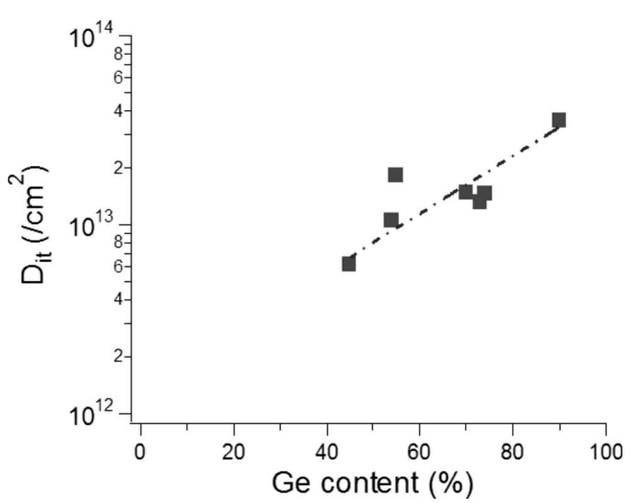

Figure 10. Density of interface trap D_{it} extracted for the different SGOI substrates from the subthreshold slope in weak inversion.

method used here. Pseudo-MOSFET was originally developed to characterize thick films on insulators in which the free surface is far from the channel. When the SiGe film thickness is reduced, the coupling between the free surface which is covered by a native oxide containing a high density of dangling bonds and the channel becomes more and more pronounced. As a result, the extracted parameters for the pseudo-MOSFET are affected: a higher D_{it} and lower mobilities are extracted for thin films as compared to thick films.[30,32] Because the 93% Ge film was the thinnest, we may therefore assume that its mobility, although excellent, was underestimated whereas its D_{it} was overestimated. In any case, postannealing steps in H_2 or forming gas are highly recommended in order to passivate the traps that are generated in the BOX.

Conclusions

The Ge condensation technique was used to produce SGOI substrates with Ge contents ranging from 42 to 93%. A study of the structural properties of the SiGe films revealed that the introduction of intermediate annealing steps in Ar during the condensation process is crucial in order to get high quality and uniform SGOI. The pseudo-MOSFET technique was used to extract the electron and hole mobility at the BOX/SiGe interface and electrical properties of the different SGOI substrates. The electron mobility of the SGOI layers was found to dramatically decrease for Ge contents above 50%, while the hole mobility was found to increase with increasing Ge content. Excellent hole mobility of approximately 400 $cm^2\ V^{-1}\ s^{-1}$ was measured on SGOI with high Ge concentration, even though the properties of the BOX (fixed charge, interface traps) were observed to degrade with increasing Ge content. It is therefore important to optimize the quality of the interface in order to avoid jeopardizing, via interface coupling, the electrical performance of devices processed on the top surface of such SGOI substrates.

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