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Vertically-Aligned of Sub-Millimeter Ultralong Si Nanowire Arrays and Its Reduced Phonon Thermal Conductivity

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Well-aligned of single crystalline silicon nanowires (SiNWs) arrays are synthesized using Ag-assisted electroless etching processes. By examining a wide range of reaction periods from 1 min up to 12 h, our experimental results show that the lengths of fabricated SiNWs do not maintain the linear relationship with the reaction period but feature three evident transitions instead. We find that the diffusion of HF through Ag dendrites is the rate-limiting step for maintaining the galvanic reaction of etching processes. To overcome these limitations, we report a simple and controllable route employing $HNO_3/AgNO_3/HF$ electrolyte solutions, which enables SiNW lengths ranging from several nanometers up to a few hundred micrometers to become linearly dependent on the reaction time. Transmission electron microscopy studies reveal that the SiNWs fabricated by this approach are single crystalline along [100] in axial direction with relatively rough surfaces. In addition, we further measure the thermal conductivities of SiNW arrays with various lengths at 300 K. The resulting value of thermal conductivity in SiNW arrays is only 44% in comparison with bulk Si (100) substrates; that is attributed to the effects of decreased area of phonon transport, as well as increased phonon scattering.
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One dimensional silicon nanostructures have attracted remarkable attentions due to their unique electronic,[1] photonic[2] and thermal properties.[3–5] Silicon nanowires (SiNWs), in particular, have become the promising architecture in the miniaturization of silicon-based devices, enabling many potential applications, such as field-effect transistors (FET),[6,7] solar cells[8] and biological detection.[9] Recently, the thermoelectricity of a single SiNW has been extensively studied, showing its greatly reduced thermal conductivity but rarely unaffected Seebeck coefficient and electric conductivity in comparison to bulk silicon; these features make SiNWs a promising high-performance thermoelectric material.[10,11]

The most crucial step that must be addressed in practical applications based on SiNWs is the control over their dimensions and doping level for the formation. These issues remain particularly challenging for constructing the complex SiNW-based devices[12] or integration of multifunctional elements,[13] and one promising solution is the controlled synthesis of ultra-long SiNWs with uniform structures and properties, as reported by Park et al.[14] So far, great efforts have been made to fabricate the ultra-long SiNWs, including vapor-liquid-solid (VLS) growth[14] and thermal evaporation.[15,16] These aforementioned approaches, however, involve serve vacuum condition, high process temperatures and preparation of catalytic materials, making the entire process expensive, complex and incapable of fabricating a large area of well-aligned SiNW arrays.

Among the various fabrication methods available, the utilization of metal-assisted electroless etching[17–21] seems to be a prevailing one. This process involves a rather simple and inexpensive procedure where silicon wafers are immersed into $AgNO_3/HF$ electrolyte solutions at near room temperature. Nevertheless, we find that it demonstrates less controllability of SiNWs length over an hour process. The underlying mechanism is systematically investigated, and a new electroless etching method has demonstrated in the present work, showing the controlled fabrication of SiNW arrays with the desired lengths ranging from several nanometers up to a few hundred micrometers. In addition, the thermal conductivities of fabricated SiNW arrays on Si substrates with various SiNW lengths are measured using a standard transient plane source (TPS) technique. The intrinsic thermal conductivity of SiNW arrays is further identified based on effective thermal resistance model.

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Experimental

Procedures of fabricating SiNW arrays.—The fabrication of SiNW arrays were performed by dipping the single crystal silicon wafers, B-doped Si (100) substrates (1–10 Ω cm), into electrolyte solutions with various durations at 50 C. $AgNO_3/HF$ and HNO_3. $AgNO_3/HF$ electrolyte solutions with concentrations of 0.03/3.7 and 0.05/0.03/3.7 M, respectively, were adopted. After the etching processes, all of the samples were dipped into concentrated HNO_3 (65%) to remove the Ag dendrites that covered the SiNW surfaces.

Measurements of SiNW lengths and diameters.—To examine the relationship between the SiNW lengths and reaction time, we measured the lengths of SiNWs via scanning electron microscope (SEM) (JSM 6390) observation from the flat side of Si substrate. The other side of substrate was adhered to the commercial transparent tape (3M, USA) prior to SiNW fabrication, such that the etching processes can be entirely prohibited in the latter case, as shown in Fig. 1a. In addition, the heights of as-prepared SiNW arrays (left-hand side) and un-etched positions of Si substrates (right-hand side, covered with tape before etching processes) are similar, as evidenced in Fig. 1b. It manifests that the sum of SiNW lengths and the thickness of beneath Si substrates remains the same with respect to the original Si substrates used in fabricating nanowires.

To estimate the diameters of as-prepared SiNWs, SiNWs were carefully scratched from the substrates and dispersed them in ethanol under an ultrasonic bath for 10 min. Several dips of SiNWs suspensions were then placed on a clean holder and we measured the diameters of SiNWs from side view via SEM observations with numbers of over 200 counts. In addition, a transmission electron microscope (TEM) (JEOL 2010) was used to characterize the microstructures of SiNWs.

Thermal conductivity measurements of SiNW arrays.—The transient plane source (TPS, Hard Disk 2500) technique[22,23] was used for measuring the thermal conductivities of as-prepared SiNW arrays. The TPS method utilizes a thin disk-shaped metal strip with a radius of 6.403 mm (S/N 5501) simultaneously as a temperature sensor and heat source, which is sandwiched between two slabs of SiNW samples and clamped together carefully to ensure their rational contact. By supplying a constant current to the metal strip, the subsequent voltage variation over a certain time period (~1 s) from the onset of the heating current is recorded, enabling precise evaluation of the thermal transport properties between the sensor and the test specimen. A series of measurements on eight different samples with fixed dimensions (5×5 cm^2 in area and 520 μm in overall thickness) were performed at 300 K.

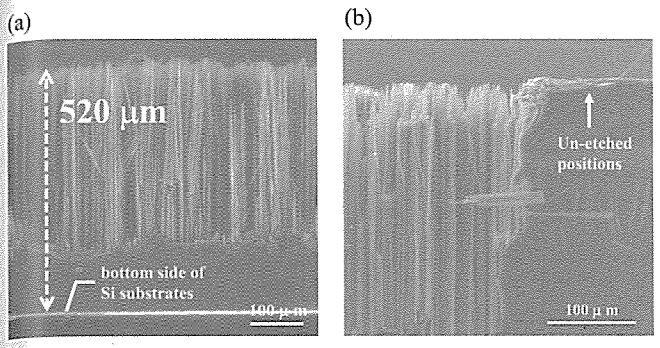

Figure 1. (Color online) Cross-sectional view of SiNW arrays prepared by adhering commercial transparent tape on the (a) bottom and (b) right-hand side of the Si substrates prior to performing the etching processes.

Results and Discussion

Kinetics of SiNW synthesis via Ag-assisted electroless etching process.—The lengths of the Si nanowires have been shown to depend linearly on the etching time in previous research.[19,20] To clarify this relationship, the results of SiNW fabrication via a conventional $AgNO_3$/HF system under wide range of reaction periods ranging from 1 min to 12 h are shown in Fig. 2a. Interestingly, the lengths of as-prepared SiNWs do not always increase linearly with reaction time. Instead, the increase in length can be divided into three regions. In Region I, the lengths of SiNW arrays exhibit a linear dependence on the reaction time, which is in accordance with previous studies.[19,20] In this region, SiNW lengths increase at a constant reaction rate of 0.8 μm/min and can be well-controlled by tuning the etching time. On the other hand, the reaction rate of SiNW formation starts to slow down in Region II as the reaction is sustained for 1.2 h. As shown in Fig. 2a, the average formation rate of SiNWs decreases to 0.6 μm/min after 3 h, and further reduces to 0.4 μm/min after 8 h. Finally, the lengths of the SiNWs become nearly constant regardless of the reaction time from 10 h (Region III) onwards.

To elucidate the underlying mechanism of SiNW formation, the procedures of the three regions are illustrated in Fig. 2b, and the corresponding galvanic reaction is described as follows[17–21]

$$4Ag^+ + Si + 6F^- \rightarrow 4Ag + SiF_6^{2-} \quad [1]$$

The entire reaction starts from the reduction of Ag ions (Ag^+) to the large quantities of Ag nanoparticles covering the Si surface, as illustrated in Fig. 2b. Simultaneously, these Ag ions oxidize the underlying Si atoms at the Ag^+/Si interface; the oxidized Si atoms are dissolved to SiF_6^{2-} by HF enchants. The succeeding dissolution of silicon via a galvanic reaction is promoted by the new generated Ag particles, which nucleate onto the initial Ag seeds and spontaneously form the dendrite structures. The prolonging pores preferentially sink onto the Si substrate along the ⟨100⟩ direction, finally leading to well-aligned nanowires. These processes enable the SiNW lengths to increase linearly with reaction time, which corresponds to Region I. Meanwhile, it should be noticed that the Ag deposits grow with reaction time as well, and form the branched dendrite structures that closely cover the Si surfaces. Moreover, these Ag dendrites begin to impede the diffusion of HF electrolyte reactants to reach the Ag^+/Si interface at the bottom of pores, leading to the slower dissolution rate of Si (Region II). Finally, the galvanic reaction is nearly stopped because the remaining Si substrates are isolated by the abundant number of Ag dendrites (Region III). Accordingly, the overall processes can be broken down into contributions from three steps: (1) oxidation of silicon at Ag seed/Si interface, (2) diffusion of HF across Ag dendrites; and (3) dissolution of silicon oxide by HF. Summarizing our experimental findings as presented in Figs. 2a and 2b, the most critical process that impedes the formation of SiNWs is identified to be step (2). This step dominantly limits the reaction rate of etching Si substrates.

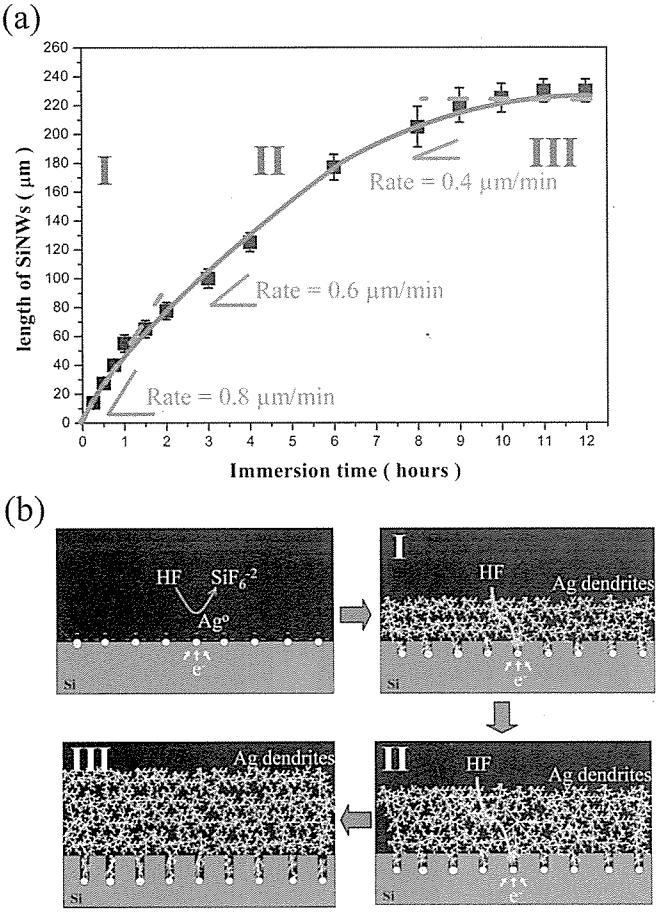

Figure 2. (Color online) (a) Plot of immersion time versus the lengths of SiNW via the $AgNO_3$/HF etching method with three divided regions. The average formation rates of SiNW arrays are 0.8, 0.6, and 0.4 μm/min under 1, 3 and 8 h fabrication, respectively. (b) Schematic illustrations of SiNW array formation on Si substrates.

Controlled fabrication of sub-millimeter long SiNW arrays.—In accordance with the results discussed in the previous section, the difficulty of reliably controlling the lengths of SiNWs via conventional etching manner, particularly in Region III of SiNW formation, is manifested. Furthermore, the lengths of the SiNW arrays are always less than 250 μm in length; this is disadvantageous to the utilization of the current etching method for various SiNW-based devices.[12,13] To overcome these limitations, extremely low concentration of HNO_3 (0.05 M) were added to the $AgNO_3$/HF electrolyte solutions in order to steadily dissolving the formed Ag deposits during the etching processes. Thus, the galvanic reaction in Si can be sustained under prolonging processes, and maintain an invariable formation rate of SiNWs. Notice that excess concentrations of HNO_3 (larger than 0. 5 M) in the HF electrolytes lead to the isotropic etching in Si and leave no aligned SiNWs behind. In contrast, the lengths of fabricated SiNWs remain a nonlinear time dependence by using insufficient HNO_3 in etching processes (see supplemental data)[24]. Herein, the concentration of HNO_3 is unambiguously critical to maintaining SiNWs with long and uniform lengths.

Figure 3a demonstrates the relationship between the reaction time and the lengths of SiNWs fabricated using the HNO_3/$AgNO_3$/HF approach. Clearly, the SiNW lengths increase almost linearly with reaction times ranging from 1 min to 11 h, suggesting that no significant influences from the Ag dendrites are involved in SiNW formation. The reaction rate is maintained at 0.7 μm/min throughout the durations of etching. As illustrated in Fig. 3b, the HF etchants are capable of reaching the Ag^+/Si interface at the bottom of the pores to dissolve the formed silicon oxide by diffusing across the Ag

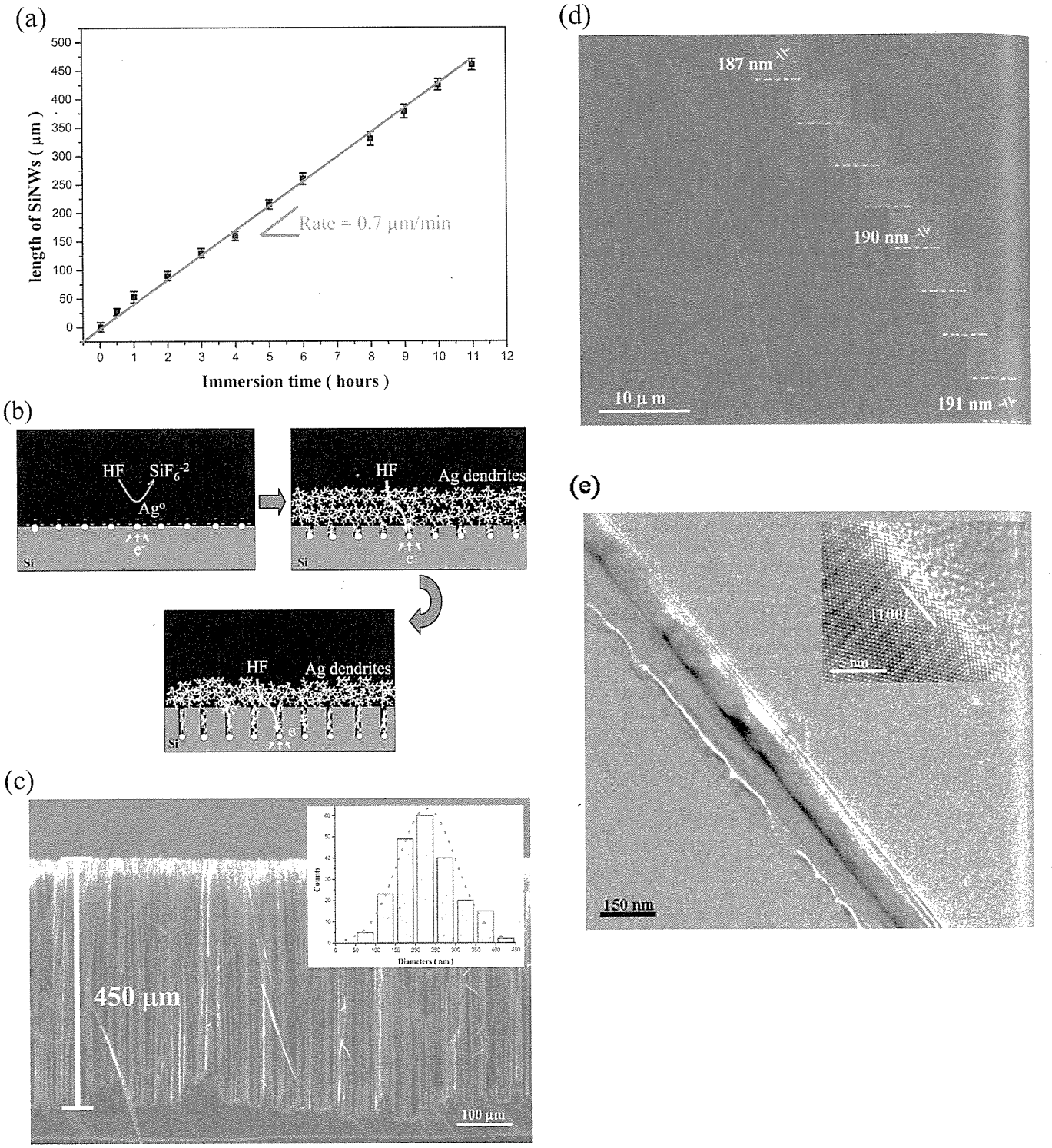

Figure 3. (Color online) (a) Plot of immersion time versus the lengths of SiNW via the $HNO_3/AgNO_3/HF$ etching method. The average formation rate of SiNW arrays is maintained at 0.7 μm/min. (b) Schematic illustrations of SiNW array formation on Si substrates. (c) Cross-sectional view of 450 μm-long SiNW arrays. The inset shows the distribution of SiNW diameters and the average diameter is 203 nm. (d) A series of SEM images of a single SiNW fabricated under 12 h fabrication processes. The diameters of several segments in a SiNW are also marked. (e) TEM image of the as-prepared SiNW. The rough surfaces of fabricated SiNW are clearly visible. Inset is the corresponding HRTEM image, showing that the SiNW is single-crystalline with [100] axial direction.

dendrites. Thus, the overall galvanic reaction proceeds continuously, leaving the prolonging SiNW arrays behind. Furthermore, the $HNO_3/AgNO_3/HF$ method allows the fabrication of ultra-long SiNW arrays, the lengths of which are solely restricted by the thickness of the Si wafer used. As evidenced in Fig. 3c, the lengths of SiNWs can be extended to 450 μm after 11 h reaction; under longer reaction time, however, the etching pores penetrate throughout the Si substrate, resulting in the dispersed SiNWs in the solution completely.

In addition, the diameter distributions of these ultra-long SiNWs were estimated by counting over 200 SiNWs via SEM investigations, as shown in the inset of Fig. 3c. It is found that the SiNW diameters are distributed in the range of 95–402 nm following the

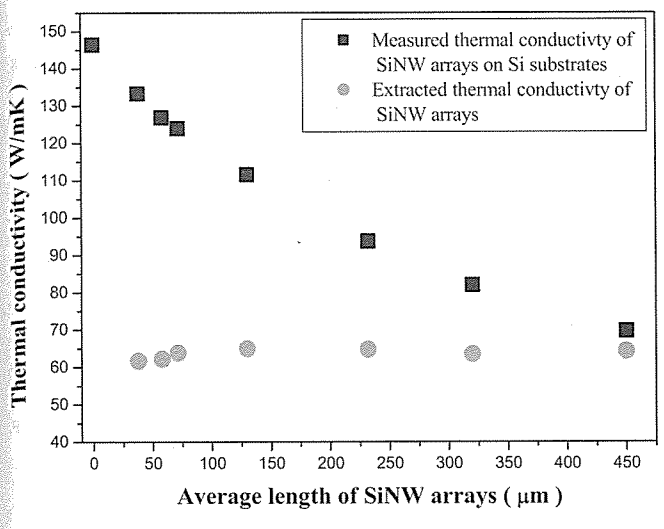

Figure 4. (Color online) The measured thermal conductivity of SiNW arrays on Si substrate (black squares) and the extracted thermal conductivity of bare SiNW arrays (red circles) with respect to the average length of SiNW arrays, respectively.

normal Gaussian distribution; the average value of SiNW diameters is 203 nm. Figure 3d shows a series of SEM images of a single SiNW fabricated under 12 h. Noticeably, the SiNW diameter is quite uniform as evidenced by measurements of the diameters of several segments in a single SiNW (insets of Fig. 3d). Finally, a representative TEM image of as-synthesized SiNWs is shown in Fig. 3e, revealing that the SiNW is straight with a uniform diameter along its long axial direction. In addition, the sidewalls of as-prepared SiNW are considerably rough and the mean roughness is typically in the range of 1–10 nm, similarly to the characteristics of SiNWs fabricated by the conventional $AgNO_3$/HF method.[10] High-resolution TEM image further reveals that the as-prepared SiNW is single-crystalline with [100] axial direction, consistent with the orientation of used Si substrates.

Reduced thermal conductivity of rough SiNW arrays.—By using $HNO_3/AgNO_3$/HF method as discussed in the previous section, the lengths of SiNW arrays can be well controlled to a range of several nanometers up to a few hundred micrometers with essentially fixed diameters. This enables us to identify the intrinsic thermal properties of SiNW structures. Here, we demonstrate the thermal conductivities of SiNW array/bulk Si (100) composites with different lengths of SiNW arrays on Si substrates, as shown by the black squares of Fig. 4, including 38, 58, 72, 130, 232, 385, and 450 μm-long SiNWs. A bare Si (100) substrate is used as a control. The overall thickness, i.e., the sum of SiNW lengths and remaining bulk Si substrates, of eight different samples is always constant (thickness = 520 μm). First, in Fig. 4, the eight sets of measured results show that the overall thermal conductivities ($K_{overall}$) of SiNW/bulk Si (100) composites are inversely dependent on the length of SiNW structures. In addition, the thermal conductivity of bulk Si (100) substrate ($K_{bulk\ Si\ (100)}$) is 146.5 W/mK when the average length of the SiNW arrays is zero (Fig. 4). Specifically, the value of $K_{overall}$ is 69.7 W/mK when the average length of SiNWs is 450 μm, suggesting that the SiNW structures possesses a reduced value of effective thermal conductivity in comparison to bulk Si (100) substrates.

Next, to estimate the thermal conductivity of intrinsic SiNW arrays, a simple theoretical study is carried out using an effective thermal resistance model. As the two thermal resistances representing each contact layer of the SiNW arrays and bulk Si (100) substrates are in series, the overall thermal resistance of SiNW arrays/bulk Si(100) composites, R_o, is given by

$$R_0 = R_1 + R_2 \quad [2]$$

where R_1 and R_2 are the thermal resistances of the SiNW arrays and bulk Si (100) substrates, respectively. Subsequently, the thermal conductivity of a multi-layered structure can be further expressed as following equation

$$\frac{1}{K_{overall}}\frac{T_{overall}}{A} = \frac{1}{K_{SiNW\,arrays}}\frac{T_{SiNW\,arrays}}{A} + \frac{1}{K_{bilk\,Si\,(100)}}\frac{T_{bilk\,Si\,(100)}}{A} \quad [3]$$

where $T_{overall}$, $T_{SiNW\,arrays}$ and $T_{bulk\,Si\,(100)}$ represent the overall thickness of a sample, length of SiNW arrays and the thickness of residual Si (100) substrate, respectively. In addition, A is the cross-sectional area of heat transport (equal to the cross-sectional area of thermal sensor used), and the thermal conductivity of the overall composites, SiNW arrays and bulk Si(100) substrates are defined as $K_{overall}$, $K_{SiNW\,arrays}$ and $K_{bulk\,Si\,(100)}$, respectively. Accordingly, the estimated $K_{SiNW\,arrays}$ is approximately 64.5 W/mK, which is approximately 44% of $K_{bilk\,Si\,(100)}$. This K remained relatively unchanged for the range of SiNW array lengths studied, as denoted by the red circles in Fig. 4.

A possible reason for the reduced value observed may be stem from the reduction of total volume of silicon in the SiNW arrays, when considering the SiNWs as composites of silicon structures with air. Thus, we can present its K value as

$$K_{Si/air\,composites} = K_{bulk\,Si\,(100)} \times v \quad [4]$$

where v represents the volume fraction of SiNWs in Si/air composite structures and is approximately 70%. The calculated $K_{Si/air\,composites}$ from Eq. 4 is 102.6 W/mK, and this value is approximately 1.6 times larger than the extracted value ($K_{SiNW\,arrays}$ = 64.5 W/mK) from our measured results. In fact, the interface and boundary scattering of phonons are introduced in the nanostructured Si, resulting in a significant reduction of phonon thermal conductivity.[3–5,25,26] Furthermore, the fabricated SiNWs via electroless etching process intrinsically present rough sidewalls, as evidenced in Fig. 3e, which impede the transport of phonons by incorporating secondary scattering phases,[4,10] thus further decreasing their K value. In short, the contribution of reduced area in phonon transport as well as increased phonon scattering lead to the K value in the presented SiNW arrays only 44% of the bulk Si (100) substrate value.

Conclusions

The time dependence of SiNW lengths via an Ag-assisted electroless etching method was investigated over a wide range of reaction periods from 1 min up to 12 h. First, using $AgNO_3$/HF as etching agents, the lengths of fabricated SiNWs do not maintain the linear relationship with the reaction period. Instead, three evident transitions are observed; these result from the retardant diffusion of HF across Ag dendrites. Next, these limitations are overcome by means of employing $HNO_3/AgNO_3$/HF electrolyte solutions, which guarantee the linear dependence of SiNW lengths on the reaction time, promising the controllability of SiNW lengths. Finally, the thermal conductivities of SiNW arrays on Si substrates with various SiNW lengths are measured at 300 K. Applying an effective thermal resistance model, the thermal conductivities of SiNW arrays are estimated, showing only 44% of the bulk Si (100) substrate value. This is due to the effects of reduced area of phonon transport, as well as increased interface scattering. These SiNW arrays with controllable lengths ranging from nanometers to submillimeters may pave ways for applications in thermoelectric devices, electro-mechanical systems, and biological detection.

Acknowledgments

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