ELSEVIER

Microelectronic Engineering 41/42 (1998) 551–554

MICROELECTRONIC ENGINEERING

Fabrication of Si nano-wires using anisotropic dry and wet etching

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A new process for the fabrication of silicon wires on SOI material using anisotropic dry and wet etching is proposed. Arrays of silicon pads joined by narrow Si wires have been successfully fabricated. The structures are uniform and precisely controlled, thus demonstrating the reliability of the process and its suitability for nano-device applications.

1. INTRODUCTION

Over the last few years the fabrication of Si nano-structures has received considerable attention in the field of semiconductor technology. The miniaturization of electronic components is very attractive not only as a way for increasing device packing density and reducing power consumption, but also as a means for the implementation of new concepts in electronics. There is, however, a large gap between the present stage of demonstration of Si nano-devices and their production in ULSI circuits using reliable fabrication processes. More experimental studies are needed, taking into account important issues such as process feasibility and reproducibility and structure uniformity. An attractive new development is the process for fabricating ultra-narrow Si wires on Silicon on Insulator (SOI) material proposed by Hashiguchi and Mimura [1], and recently developed by Hiramoto et al. [2]. This process, based on two anisotropic wet etching steps and selective oxidation of silicon (Fig. 1a), offers several benefits: it is not dependent on lithographic resolution, it does not require precise control of the etching time and it leads to uniform Si wires whose dimensions are determined by the Si overlayer thickness of the SOI material. The Si wires so fabricated are parallel to the <110> direction and have a triangular cross-section formed by the (001) surface plane and two {111} planes which intersect at the top of the Si-overlayer. Using this process, quantum wire MOSFETs have been successfully fabricated and Coulomb blockade oscillations have been observed at room temperature [3,4].

Here, we present an alternative process for Si nano-wire fabrication which retains the above benefits and uses techniques compatible with CMOS technology (Fig. 1b). Orthogonal triangle shaped Si wires bounded by the (111) and (110) Si planes are obtained by the use of anisotropic dry etching in combination with crystallographic anisotropic wet etching of silicon.

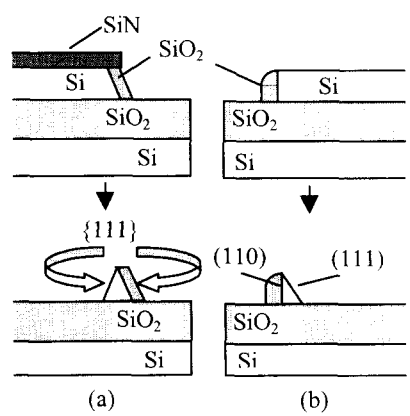


Figure 1. Schematic of the fabrication processes of triangular Si wires proposed by Hashiguchi and Mimura (a) and in the present work (b).

PII: S0167-9317(98)00129-4

2. EXPERIMENTAL

The starting material was a (100)-oriented SIMOX wafer with silicon overlayer and buried oxide thicknesses of 220 nm and 400 nm, respectively. Photoresist was first applied on the wafer and a [110]-oriented line pattern was exposed and developed. The silicon overlayer pattern was then etched using reactive ion etching (RIE) with a mixture of SF_6 and CHF_3 at room temperature, resulting in the formation of Si lines with [110]-oriented vertical sidewalls (figure 2a). The etching process was carried out in a NEXTRAL parallel plate plasma reactor with a rf frequency of 13.56 MHz. The water cooled electrode was covered by a graphite sheet. The rf power was 0.5 W/cm^2 and the pressure 10 mTorr. The gas flow was 25:25 sccm SF_6:CHF_3 (50% mixture).

Following resist removal, a 20 nm dry oxide layer was thermally grown (Fig. 2b) and anisotropic dry etching of the oxide was subsequently performed using RIE (Fig. 2c) under the same as above conditions. End-point detection technique was employed to avoid overetching. The etch process removes the SiO_2 layer from the flat areas while leaving oxide only on the sides of the Si lines. Such a process is currently used in the semiconductor industry for making oxide spacers at the sidewalls of polysilicon gates (LDD devices [5]).

Anisotropic wet etching of the Si lines is finally performed in Ethylenediamine-Pyrocatechol-Water solution, resulting in the formation of very narrow Si wires with an orthogonal-triangle cross-section (Fig. 2d). The composition of EPW was 200 ml E : 30g P : 27 ml W and the bath temperature was held at 40°C [6,7]. Prior to immersion into EPW solution the native oxide which forms on the Si surface was etched in 2% HF for a few seconds and the samples were rinsed in DI water.

Other structures consisting of Si pads joined by Si wires were also fabricated. To obtain such structures, the wafer was resist coated a second time after the oxidation step (Fig. 2b) and a [110]-oriented line/space pattern normal to the [110] direction of the Si lines was exposed and developed. The second RIE step and the wet etching in EPW were then carried out as described above.

The samples were examined by SEM in cross-section and plane view.

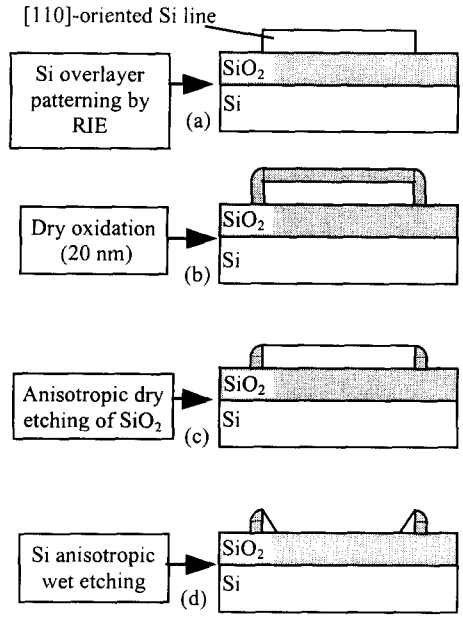


Figure 2. Schematic of the fabrication steps of orthogonal triangle shaped Si wires proposed here.

3. RESULTS AND DISCUSSION

Above all, it should be mentioned that the success of the process proposed here, in terms of uniformity and reproducibility of the Si wires, depends mainly on the following two parameters: First, the anisotropy of the dry etching steps and second, the etch control of the SiO_2 layer during the second RIE step. The RIE operating conditions previously described have been studied in detail by Gogolides et al. [8] and allow the fabrication of highly anisotropic vertical Si lines with low surface roughness. With respect to the etching of the SiO_2 layer, precise end-point detection is an absolute necessity since overetching will affect the size and so the reproducibility of the Si wires. Fig. 3 is a SEM micrograph of a Si line just before the anisotropic wet etching step, corresponding to Fig. 2c. The brightness of the Si line sidewalls is due to the remaining oxide after the second RIE step.

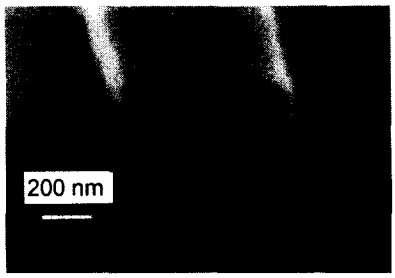


Figure 3. SEM photomicrograph of a Si line prior to anisotropic wet etching.

Thanks to the low etch rate of SiO_2 (~ 10 nm/h) in EPW solution and the high selectivity between the etching rates of the (100) and (111) Si planes, well-controlled Si wires can be easily obtained. Si wires joined to a Si pad are shown in Fig. 4.

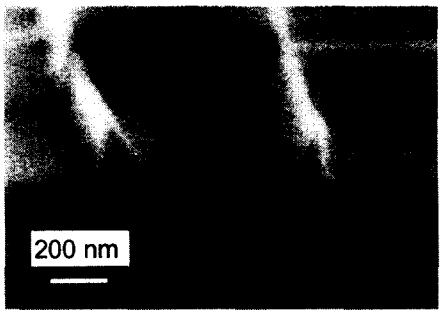


Figure 4. SEM photomicrograph showing a Si pad and two orthogonal triangle Si wires fabricated using the process outlined in Fig. 2.

The structures obtained were uniform over the surface of all the samples as shown in Figure 5.

Using a pattern of 0.3 μm wide lines, Si wires with a 15 nm separation from each other were fabricated (Fig. 6). It should be noted that the geometry of the wet etched regions between two Si pads is similar to that of trenches anisotropically etched in silicon of (100) orientation. The four {111}-oriented sidewalls of the structures are clearly visible in Fig. 6b.

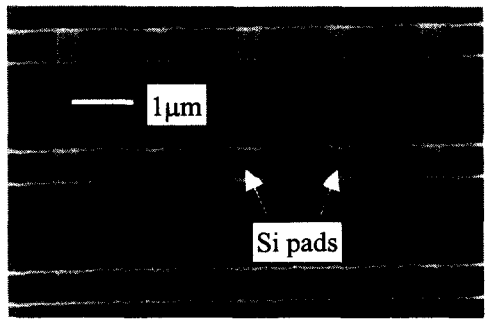
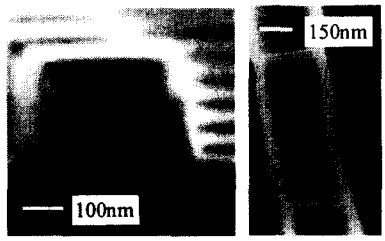


Figure 5. SEM photomicrograph of Si pad arrays where the pads are joined by two Si wires



(a) (b)

Figure 6. Cross-sectional (a) and top view (b) SEM photomicrographs of Si pads and Si wires fabricated in a 0.3 μm wide line

4. CONCLUSION

A new process for the fabrication of Si wires by the use of anisotropic dry and wet etching is proposed. A series of silicon pads joined by narrow Si wires have been successfully obtained using the process described here. The uniformity and reproducible fabrication of these basic device structures demonstrates the reliability of the process and its suitability for nano-device applications. Quantum wire MOSFETs are currently being fabricated utilizing the above described structures.

ACKNOWLEDGEMENTS

The authors are grateful to C. Vieu (L2M/CNRS) for his contribution in SEM analysis.

This work was partially supported by EU through the ESPRIT project FASEM.

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