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CMOS Imaging Devices for New Markets of Vision Systems

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SUMMARY This paper reviews and discusses devices, circuits, and signal processing techniques for CMOS imaging SoC's based on column-parallel processing architecture. The pinned photodiode technology improves the noise characteristics at the device level to be comparable to CCD image sensors and as a result, low-noise design in CMOS image sensors has been shifted to the reduction of noise at the circuit level. Techniques for reducing the circuit noise are discussed. The performance of the imaging SoC's greatly depends on that of the analog-to-digital converter (ADC) used at the column. Three possible architectures of the column-parallel ADC are reviewed and their advantage and disadvantage are discussed. Finally, a few applications of the device and circuit techniques and the column-parallel processing architecture are described.

key words: *CMOS image sensor, pinned photodiode, noise reduction, on-chip image processing, A/D conversion*

1. Introduction

For a long time, charge-coupled devices (CCD's) have been the dominant technology for image sensors because no other technology could serve better performance than the CCD's. However, the development of pinned photo diode technology in CMOS image sensors dramatically improves the image quality and in the past ten years, the interest in CMOS image sensors has increased in all kinds of electronic cameras. CMOS image sensors offer significant advantages over CCD's such as the integration of on-chip signal processing circuitry, low power consumption and special functions and performances like reading region of interest, high-speed readout, digital outputs and range finding. Recent CMOS image sensors have advantage in lower noise performance over the CCD's, especially at high frame rate. Column parallel low-noise readout circuits and analog-to-digital converters contribute the improvement of the noise performance at high frame rates. The performance improvement of the CMOS image sensor as an imaging device accelerates evolving imaging systems to be an imaging system-on-a-chip (SoC).

There are numerous possible architectures on the imaging SoC's. The CMOS technology allows us to integrate a digital processing unit in even each pixel for an ultimate parallel image processing [1]. However, the imaging SoC's with pixel-parallel processing architecture will take a long time to be a dominant technology in applications with sufficient market volume. Column-parallel processing architecture is a reasonable choice for exploiting the features of parallel processing while maintaining the image quality.

This paper reviews devices, circuits and signal processing techniques for the imaging SoC based on column-parallel processing architecture, and discusses a possibility of the near future developments of highly-integrated imaging SoC's with column-parallel processing architectures which may create new markets of vision systems.

2. Imaging SoC Architecture

Figure 1 shows an imaging SoC architecture based on column-parallel mixed analog/digital signal processing. It entirely works as a SIMD (Single Instruction Multiple Datastream) type of parallel processing architecture. The analog frontend (AF) plays a very important role for noise reduction of pixel amplifier noise which is described in the next section. A column-parallel analog-to-digital converter (ADC) array often dominates the readout speed and image quality. Three possible architectures of the column-parallel ADC are discussed in Sect. 4. The design of digital image processing

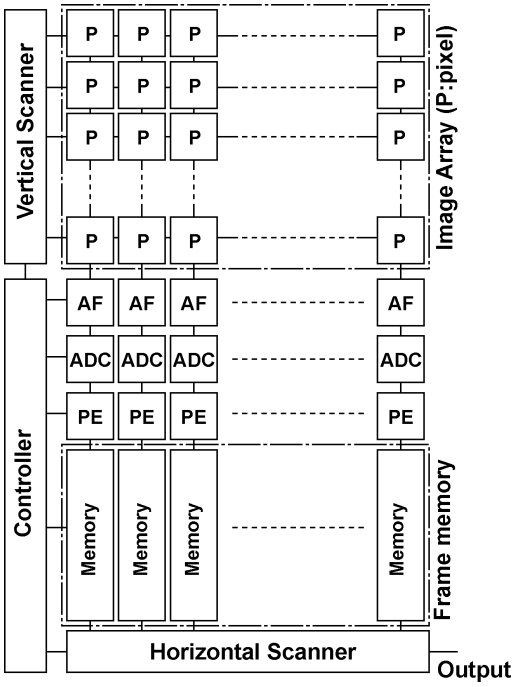

Fig. 1 Imaging SoC architecture with mixed-signal processing (AF: analog frontend, ADC: analog-to-digital converter, PE: processing element).

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element (PE) and memory architecture depends on the application. Though the integration of frame memory is not always necessary, it provides often a great advantage as described in Sect. 5. Using a mixed DRAM/imager technology with sub-100 nm scale, the silicon area of the frame memory will not be of concerns in the near future.

3. High-Sensitivity and Low-Noise Imaging

3.1 Pixel Device Technology

CMOS image sensors have recently attracted much attention in the field of low light level imaging. An active pixel device employing a pinned photodiode and in-pixel charge transfer as shown in Fig. 2 reduces the major noise sources in CMOS image sensors [2], [3]. The pinned photo diode which is originated in the interline transfer type CCD image sensors reduces the dark current noise to be comparable to CCD image sensors [4]. Perfect charge transfer from the photodiode to a floating diffusion and noise canceling so-called correlated double sampling (CDS) at the column readout circuits suppress the reset noise or kTC noise both at the photodiode and floating diffusion. Furthermore, the separation between the photodiode and floating diffusion with the transfer gate leads to a high conversion gain due to the small capacitance of floating diffusion. A problem of the pixel pitch which arises from the use of 4 transistors in each pixel has been overcome by a transistor-sharing technique, where transistors for resetting and amplifying are shared by two or four pixels and the resulting equivalent number of transistors in each pixel is 1.5, 1.75 or 2.5 depending on the type of sharing [5]–[7]. Figure 3 shows an example of CMOS sensor pixel circuits shared in 4 pixels. A CMOS image sensor using the transistor sharing technique reaches the pixel pitch of 1.4 μm [8].

The pinned photodiode technology reduces the noise at the device level to be comparable to CCD image sensors. However, in order to realise a very low-noise image sensor, readout noises due to pixel amplifiers, column readout circuits and output amplifiers must also be reduced. Techniques for low-noise readout architectures for CIS's are discussed in the next section.

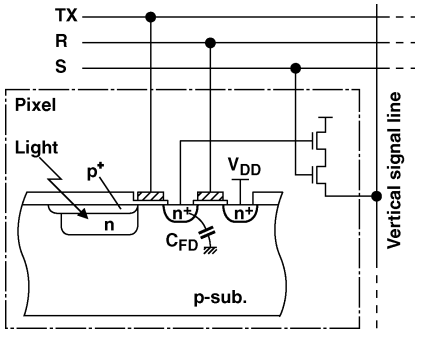


Fig. 2 Pixel structure with pinned photodiode.

3.2 Low-Noise Signal Readout Circuits

In a simple CMOS image sensor architecture, pixel outputs are once read out to column-parallel noise cancellers and then horizontally scanned to the final output. Figure 4 shows a typical column readout circuit used for this type of architecture. The timing diagram is also shown. The reset level and signal level of the pixel output through a pixel source follower are sampled at capacitors C_R and C_S by ϕ_R and ϕ_S, respectively.

By taking the difference between the two sampled levels after horizontal scanning, the reset and fixed pattern noises are cancelled out. At the final stage a wideband buffer amplifier is used. The input referred noise $\overline{V_{n,in}^2}$ of this type of readout circuits is expressed as

$$\overline{V_{n,in}^2} = \overline{V_{n,NC}^2} + \overline{V_{n,OB}^2} \tag{1}$$

where $\overline{V_{n,NC}^2}$ and $\overline{V_{n,OB}^2}$ are mean square noise voltages of the

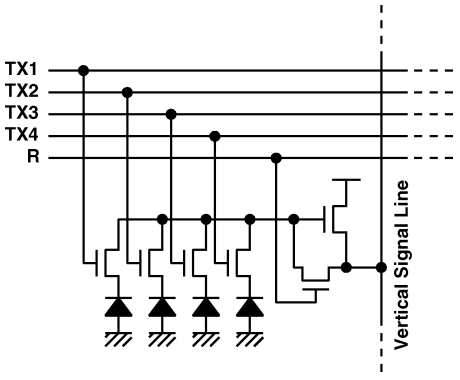
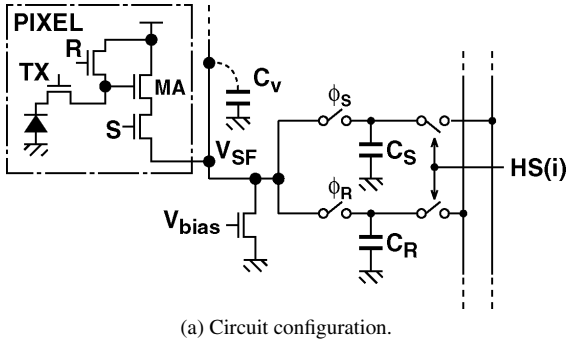
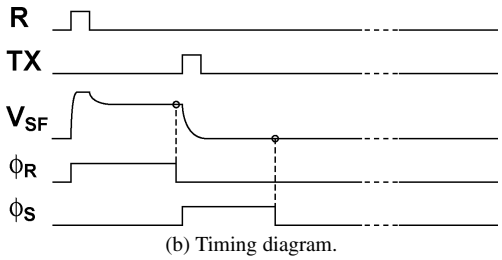


Fig. 3 Pixel circuits sharing transistors in 4 pixels.



(a) Circuit configuration.



(b) Timing diagram.

Fig. 4 Typical noise canceller using two sample-and-hold capacitors.

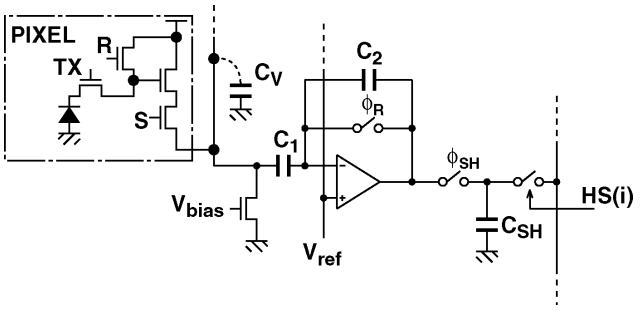


Fig. 5 Amplifying noise canceller.

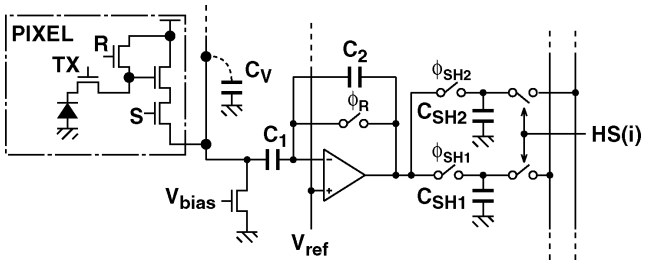


Fig. 6 Double-stage amplifying noise canceller.

column noise canceller including the source follower and output buffer, respectively. Since the noise power is proportional to the bandwidth of the circuits, the random noise level is often dominated by the wideband output buffer amplifier and it may be difficult to design low-noise CMOS image sensors using this type of readout circuits. This problem can be simply overcome by the use of high gain at the column noise canceller.

Figure 5 shows a typical amplifying noise canceller. In the reset sampling phase, a switch controlled by ϕ_R is turned on, and the reset level V_{reset} is sampled at the input capacitor C_1. In the signal sampling phase, the switch controlled by ϕ_R is turned off and the differential charge in C_1 due to the voltage difference of the signal level V_{signal} from V_{reset} at the input is transferred to C_2. The resulting signal at the output of the amplifier is given by

$$v_{out} = \frac{C_1}{C_2}(V_{reset} - V_{signal}) + V_{ref}. \tag{2}$$

This output voltage is sampled at a capacitor C_{SH} when a switch controlled by ϕ_{SH} is turned off. In this noise canceller, the noise-cancelled signal $(V_{reset} - V_{signal})$ is amplified by a gain G_{NC} determined by the capacitance ratio C_1/C_2. The input referred noise of the CMOS image sensor using the amplifying noise canceller is given by

$$\overline{V_{n,in}^2} = \overline{V_{n,NC}^2} + \frac{\overline{V_{n,OB}^2}}{G_{NC}^2} \tag{3}$$

The use of high gain at the column noise canceller directly reduces the noise due to the wideband output buffer amplifier and this simple amplifying is very effective for low-noise CMOS image sensors. The effectiveness of the high-gain column amplifier combined with a pinned photodiode technology is first demonstrated in a low-noise CMOS image sensor with a gain-adaptive column amplifier [9], [10], and soon after this, a very low-noise CMOS image sensor using a column amplifier and a single-slope column A/D converter has been reported [11]. These developments trigger the commercialization of CMOS image sensors with column amplifiers and the column amplifier is becoming an indispensable technology for low-noise CMOS image sensors.

For more efficient noise reduction, a double stage noise canceller shown in Fig. 6 is useful, especially if relatively large gain is used [12].

To understand the effect of the double-stage noise cancelling, knowledge on thermal noise of analog circuits is necessary.

In a simple RC circuit, where the noise is band-limited by the low-pass filtering characteristic of the RC circuit, the mean square noise voltage due to thermal noise is given by

$$\overline{v_n^2} = k_B T R \omega_c \tag{4}$$

where k_B is the Boltzmann constant, T the absolute temperature and ω_c the angular cutoff frequency of the RC circuit. Since $\omega_c = 1/RC$, Eq. (4) becomes a form of well-known kT/C noise.

The input referred thermal noise of the noise canceller of Fig. 4 ($\overline{V_{n,NC}^2}$ of Eq. (1)) if it is referred at the noise canceller input is expressed as

$$\overline{v_{n,NC}^2} \cong 2F_{SF}^2\, \xi_{SF} \frac{k_B T}{g_m} \omega_{c1} \tag{5}$$

where ξ_{SF} is the excess noise factor of the source follower [13], g_m the transconductance of the MOS transistor MA in a pixel, F_{SF} the noise gain factor of the source follower, and ω_{c1} is the cutoff angular frequency of the source follower with the sampling capacitor. A factor of 2 in Eq. (5) is due to noise power doubling effect of CDS operation. Eq. (5) can be understood by an analogy to Eq. (4). The excess noise factor of each transistor is a function of the channel length (L), and it takes approximately 2/3 for $L > 2\,\mu$m, and increases as the channel length decreases. To shrink the pixel size for high resolution, the size of in-pixel transistors must be reduced, causing the large thermal noise. In the source follower with a floating diffusion at the gate input, a noise gain factor F_{SF} due to the positive feedback effect through the gate-to-source capacitance (C_{GS}) of the transistor MA given by

$$F_{SF} = \frac{G_{SF}}{1 - G_{SF}\beta} \tag{6}$$

has to be taken into account, where G_{SF} is a gain of the source follower and β is a feedback factor given by

$$\beta = \frac{C_{GS}}{C_{FD} + C_{GS}} \tag{7}$$

where C_{FD} is floating diffusion capacitance. The cutoff angular frequency ω_{c1} is given by

$$\omega_{c1} \cong \frac{g_{m1}}{F_{SF}} \frac{1}{(C_S + C_V)} \tag{8}$$

if C_R=C_S. Note that the effective transconductance of the input transistor of the source follower is lowered by a factor of $1/F_{SF}$ due to the positive feedback effect. The thermal noise of the noise canceller is finally given by

$$\overline{v_{n,NC}^2} \cong 2F_{SF}\xi_{SF}\frac{k_BT}{C_S + C_V} \tag{9}$$

Eq. (9) is a fundamental formula for calculating the thermal noise of the typical readout circuit of Fig. 4.

The input referred thermal noise of the amplifying noise canceller of Fig. 5 is given by

$$\overline{v_{n,NC}^2} \cong \frac{F_{SF}\xi_{SF}k_BT}{C_V + C_1} + F_{SF}^2\,\xi_{SF}\frac{k_BT}{g_{m1}}\omega_{ca} + \left(\frac{1+G}{G}\right)^2 \xi_a \frac{k_BT}{g_{ma}}\omega_{ca} \tag{10}$$

where ξ_a is an excess noise factor of the operational amplifier, which includes the noise sources of all the internal transistors, g_{ma} the transconductance of the operational amplifier, and ω_{ca} the cutoff angular frequency of the amplifying noise canceller [14]. The cutoff angular frequency is approximately given by

$$\omega_{ca} \cong \frac{g_{ma}}{1+G}\frac{1}{C_{SH}} \tag{11}$$

For $G \gg 1$, the input referred thermal noise is expressed with Eqs. (10) and (11) as

$$\overline{v_{n,NC}^2} \cong \frac{F_{SF}\xi_{SF}k_BT}{C_V + C_1} + \frac{k_BT}{GC_{SH}}\left(F_{SF}^2\,\xi_{SF}\frac{g_{ma}}{g_{m1}} + \xi_a\right) \tag{12}$$

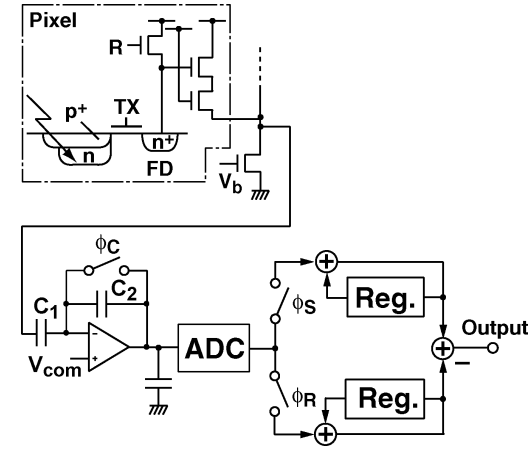
There are three noise components in this amplifying noise canceller. The first and second terms in Eq. (12) are the noises whose source is of the source follower. In the third term in Eq. (12) is due to the operational amplifier's noise. The first term is sampled in the reset level sampling phase at C_1 and is transferred to C_2 in the amplification phase. The second and third terms in Eq. (12) are sampled at the sample-and-hold capacitor, C_{SH} in the amplification phase for signal level sampling.

The first term in Eq. (12) of the single-stage amplifying noise canceller is sampled as a fixed charge, and it is unchanged during the amplification phase. This type of noise component is called "freeze noise." Using two sample-and-hold circuits at the output of the column amplifier, this first term can be cancelled [12]. To do this, the amplified reset level is sampled at one of the sample-and-hold capacitors C_{SH1}, the amplified signal level is sample at C_{SH2} and the difference of the two outputs is taken. This CDS operation in the second stage doubles the uncorrelated noise components. The resulting noise in this double-stage noise canceller is given by

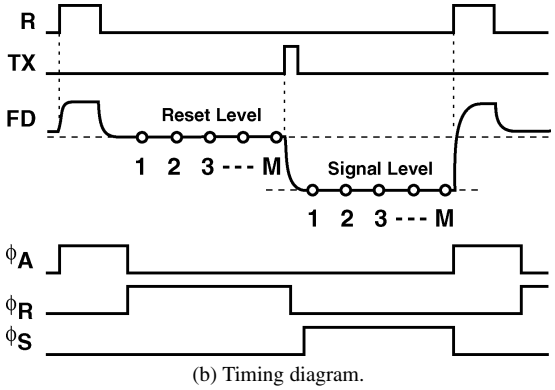
$$\overline{v_{n,NC}^2} \cong 2\frac{k_BT}{GC_{SH}}\left(F_{SF}^2\,\xi_{SF}\frac{g_{ma}}{g_{m1}} + \xi_a\right) \tag{13}$$

for $G \gg 1$. In the noise canceller of Fig. 5, the noise reduction effect by the high gain is limited by the first term in Eq. (12) which is independent of the gain. On the other hand, in the noise canceller of Fig. 6, the noise power is inversely proportional to the gain, and a very-low-noise readout can be expected. The advantage of the double-stage amplifying noise canceller has been experimentally conformed [15]. A low-noise ($3e^-$) CMOS image sensor using the double-stage noise canceller for full HD video cameras has been developed [16].

For further noise reduction, a mixed-signal processing can be used. A simple but effective noise reduction technique is a correlated multiple sampling differential averaging (CMSDA). Figure 7 shows pre-amplified CMSDA circuits. The high-gain switched-capacitor (SC) pre-amplifier is very effective for reducing thermal noise if a freeze noise component is cancelled in the next stage. The pre-amplifier output is sampled and digitized for multiple times using an A/D converter for both the reset and signal levels as shown in the timing diagram of Fig. 7. CDS (correlated double sampling) of the sampled reset and signal levels is carried out in digital domain. The operation of the CMSDA can be described as



(a) Circuit.



(b) Timing diagram.

Fig. 7 Correlated multiple-sampling differential averager with a pre-amplifier.

$$V_{OUT} = \frac{1}{M}\sum_{i=1}^{M}(V_S(i) - V_R(i)) \quad (14)$$

where $V_S(i)$ and $V_R(i)$ are the i-th sample of signal and reset levels of the preamplifier output. Using the CMSDA of M samples, the noise components of Eq. (13) can be reduced by a factor of M. It is very important that the multiple sampling is done for both the reset and signal levels, so that the freeze noise component of the pre-amplifier is cancelled.

Because of the very small-size transistor used in the pixel, noise generated in the transistor, so-called random telegraph signal (RTS) noise is becoming a big problem for low-noise CMOS image sensors. In a recent report, it is shown that the CMSDA is effective not only for reducing the thermal noise but also for reducing RTS noise [17]. A signal processing technique using a histogram of the noise amplitude obtained by the multiple sampling has also been proposed for further reducing RTS noise [17].

4. Column Parallel ADC Architectures

A column-parallel analog-to-digital converter (ADC) is a key element in the imaging SoC's based on column parallel processing architecture. There are three major column-parallel ADC architectures; single-slope integration, successive approximation, and cyclic ADC's.

The single-slope integration type is most widely used for the column parallel ADC, because of its simple circuit configuration and good linearity [18]. It requires one comparator and one counter (or register) in each column. Recently, a CMOS image sensor with high spatial resolution and high frame rate has been developed using a single-slope integration type column parallel ADC with a digital CDS technique as shown in Fig. 8 [19]. A capacitor connected at the pixel output and an auto-zeroing switch for a comparator, an analog CDS is performed for reducing the ADC time for reset level by eliminating the pixel offset. With a ramp signal, the single-slope A/D conversion for reset level is performed first using down-counting mode of the counter. Then signal level is given at the input of the ADC by transferring signal charge to the floating diffusion of the pixel and the single-slope A/D conversion for signal level is performed using up-counting mode of the counter. The difference between up and down counting memorized in the counter corresponds to the digital CDS, and this eliminates effectively the fixed pattern noise caused by the offset of the comparators and clock skew. Using high-speed clock of 297 MHz, 12-bit resolution has been achieved for 2.8 Mpixels at 30 frame/s. It can also be operated at 180 frames/s for 10-bit resolution.

The column-parallel successive approximation (SA) ADC is useful for high-speed CMOS image sensors, since it has higher conversion speed compared to the single-slope integration type [20]. Figure 9 shows a column-parallel SA-ADC with 4b resolution. The reset level of the pixel output is sampled at C_R by the switch ϕ_R and the signal level is sampled at a capacitor array (C/2, C/4, C/8, C/16) for DAC by the switch ϕ_S and connecting the bottom plates of DAC capacitors to ground. Then the DAC capacitors are connected to a reference voltage V_{REF} or remain to be connected to ground, depending on the output of the successive approximation register (SAR). The output of the SAR is renewed by the comparator output such that the DAC output successively approximates the signal input. After repeating several steps, the input of the comparator which is the difference between the sampled reset level and V_X in Fig. 9 is given by

$$V_{COMP} = V_{RESET} - V_{SIGNAL} - V_{REF}\sum_{i=0}^{4} D_i 2^{-i-1} \quad (15)$$

The comparator input approaches to zero at the end of A/D conversion, and the DAC output approximates the noise-cancelled analog input, $V_{RESET} - V_{SIGNAL}$. The digital code stored in the SAR is an A/D conversion result of the corresponding analog input. A 8.3 Mpixel 60 frames/s CMOS image sensor using the column-parallel 10b SA-ADC has been developed [21]. In the SA-ADC, the number of elements is proportional to the bit resolution. Therefore, it is not always suitable for ADC's with high resolution such as 12b or more.

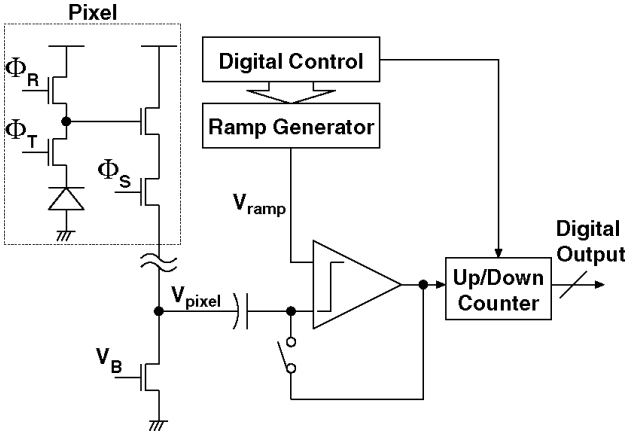


Fig. 8 Single-slope A/D converter with analog and digital double sampling with analog CDS.

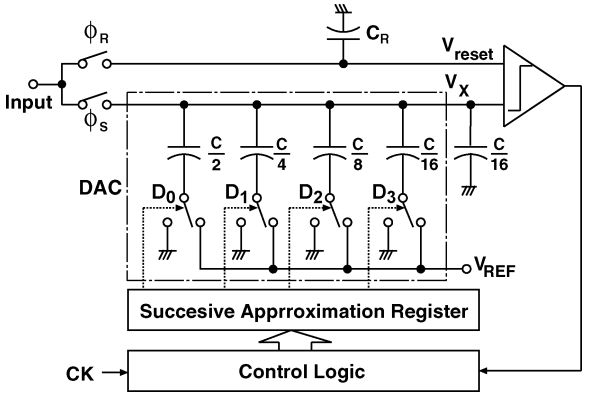


Fig. 9 Successive approximation ADC with a pixel noise canceling function.

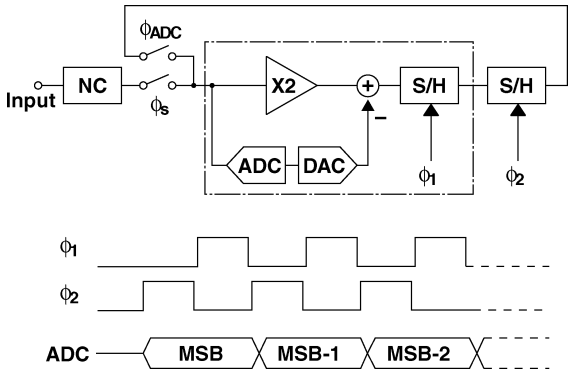


Fig. 10 Cyclic A/D converter to obtain 1.5b every cycle.

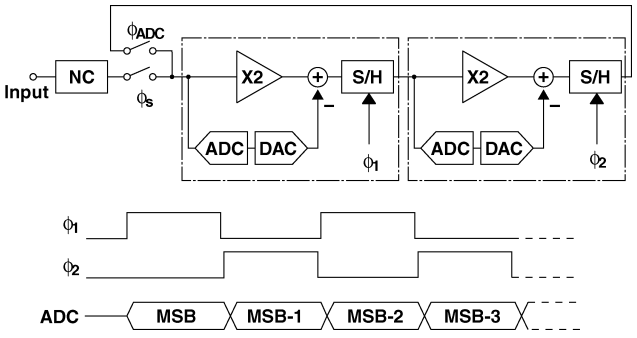


Fig. 11 Cyclic A/D converter to obtain 1.5b every half-cycle.

The cyclic or algorithmic ADC is suitable for high gray-scale resolution and high conversion speed since it requires the number of conversion steps of $N-1$ for an N-bit ADC. There are two types of architectures as shown in Figs. 10 and 11. The pixel output is connected at the input terminal, and the pixel noise is cancelled at NC section. The noise cancelled signal is given to an operation unit of the cyclic ADC by turning a switch controlled by ϕ_s on. The operation unit consists of a low-resolution ADC (sub-ADC) whose digital outputs drive a low-resolution DAC to give a quantized analog estimate of the input. This DAC output is then subtracted from the output of a gain-of-two amplifier to give a residue. The ideal relationship between the input and output is given by

$$X_{i+1} = 2X_i - D_i \tag{16}$$

where $D_i \in \{-1, 0, 1\}$, $(i = 0, 1, \ldots, k-1)$ and it is given by

$$D_i = \begin{cases} 1 & (\text{if } X_{i-1} > 1/4) \\ 0 & (\text{if } -1/4 \le X_{i-1} \le 1/4) \\ -1 & (\text{if } X_{i-1} < -1/4) \end{cases} \tag{17}$$

The digital code after the A/D conversion is of a redundant signed-digit (RSD) representation. The algorithm with the digit set of $\{-1, 0, 1\}$ is also called 1.5b per step algorithm.

An important property of the 1.5b/step algorithm is that the comparator offset up to $\pm 1/4$ of the full scale of the ADC can be corrected in digital domain. This property greatly relaxes the comparator precision and this leads to great reduction of power dissipation of comparators. In Fig. 6, the output of the operation unit is connected a sample-and-hold (S/H) stage and then the S/H output is fed back to the input by turning a switch controlled by ϕ_{ADC} on. This cyclic ADC obtains 1.5b resolution every cycle. In Fig. 7, two operation units are cascaded and the second stage output is fed back to the input. In this case, 1.5 bit resolution can be obtained every half cycle.

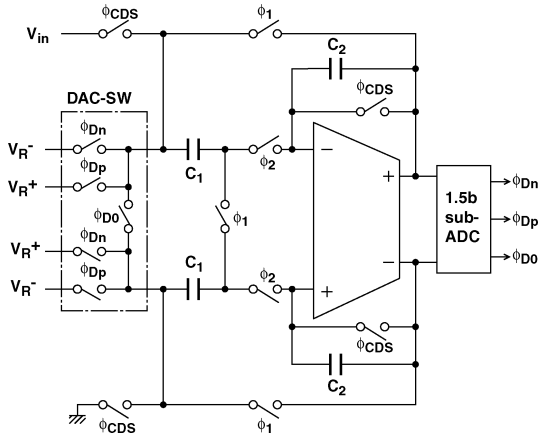


Fig. 12 Cyclic A/D converter with noise canceling function.

Since straightforward configurations of cyclic ADC's imagined by the block diagrams of Figs. 10 and 11 have relatively complicated circuits, simplification of circuit topology is necessary if it is integrated as a column-parallel ADC array of fine-pitch CMOS image sensors [22]. A simplified circuit topology shown in Fig. 12, which is equivalent to Fig. 10, has been proposed [23], [24]. It consists of one operational amplifier, two comparators, 4 capacitors, and transistor switches. A full 12-bit resolution has been achieved in the implementation of a 640×480-pixel wide dynamic range CMOS image sensor which integrates total of 640 cyclic ADC's and operates at the equivalent frame rate of 180 frames/s [25]. A high-speed version of the cyclic ADC, which is equivalent to Fig. 11 is used for a 512×512-pixel 3500 frames/s CMOS image sensor [26].

Table 1 shows a summary of the three types of column-parallel A/D converters. The single-slope integration and successive approximation types have simple circuit configuration, and it can be used for CMOS image sensors with fine pixel pitch of less than $3\,\mu$m [19]. If high gray-scale resolution of more than 12 bits is required, the single-slope integration and successive approximation types have difficulties on the speed and circuit complexity, respectively. The cyclic ADC type can achieve the resolution of 14 bits or more if a digital error correction technique for capacitor mismatches is used, and sufficiently-large capacitors are used for achieving the required SNR. Though the pixel pitch of $10\,\mu$m has been achieved with $0.25\,\mu$m technology, the technology scaling and ADC sharing technique will reduce the pixel pitch to less than $4\,\mu$m.

Table 1 Speed and complexity of three types of column parallel A/D Converters (N: bit resolution).

	# of Conversion Steps	Complexity
Single-Slope Integration	2^N	Simple
		Independent of N
Successive Approximation	N+1	Relatively Simple for N up to 10.
		2^N
Cyclic (1.5b)	N-1	Relatively Complex
		Independent of N

5. Applications

5.1 Wide Dynamic Range Imaging

Cameras for automobile, scientific and industrial applications often require very wide linear dynamic (DR) range with consistently high SNR in whole illumination range. CMOS image sensors are expected to be used for such applications. Numerous methods to expand the DR of CMOS image sensors have been reported [27]. Since most of applications require low-noise and high-sensitivity characteristics in imaging of dark region as well as the DR expansion to bright region, the availability of a low-noise high-sensitivity pixel device with pinned photo-diode structure is particularly important. However, DR expansion methods such as a wide DR pixel with logarithmic response do not allow us to use the pinned photodiode structure.

Recently, a wide dynamic range CMOS image sensor using the pinned photodiode technology has been reported [28], [29]. Figure 13 shows the pixel circuit of the wide dynamic range image sensor.

The pixel has an additional transistor whose gate is controlled by T2 and a capacitor C_S for integrating overflow charge from the photodiode if very bright light is given at the photodiode. During charge accumulation in the photodiode the transistor controlled by T2 is turned on, so that the overflow charge is stored in C_S. The ratio of C_S plus the floating diffusion capacitance C_{FD} to C_{FD} is chosen to be 16. Using this technique, the dynamic range of 100 dB has been achieved. The importance of this method lies in the good linearity of signal accumulation in whole range which relaxes the problem of motion artifact.

A traditional method to expand the dynamic range of image sensors is the synthesis of two or more different exposure time signals. This group of methods generally allows us to use the pinned photodiode technology. A dual sampling using the difference of the signal readout timing [30] is a simple but effective method for DR expansion and a pinned-photodiode CMOS image sensor employing the dual sampling technique for DR expansion has been developed [6]. The dual sampling, however, may not be sufficient to represent the areas of the scene that are too dark to be captured by the short exposure time signals and too bright to be captured by the long exposure time signals. This problem is overcome by using multiple sampling or multiple exposure time signals. A wide dynamic range CMOS image sensor using a multiple sampling technique and in-pixel analog-to-digital conversion (ADC) has been developed and the digital dynamic range of 16b (65536:1) or 96 dB has been achieved [31]. This technology with the in-pixel ADC requires 6 transistors in each pixel.

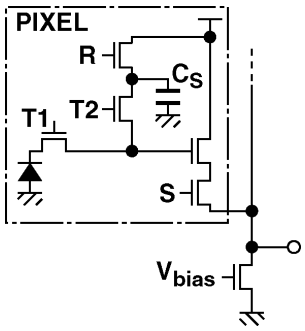


Fig. 13 Wide dynamic range pixel with a lateral overflow integration capacitor.

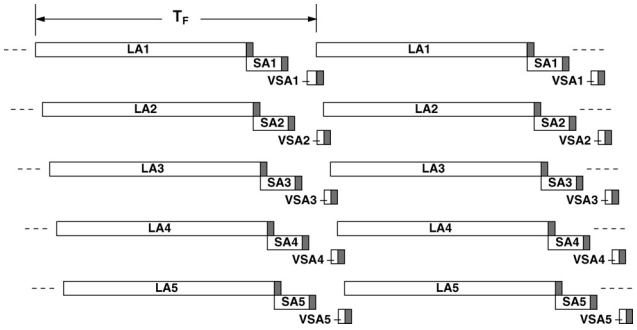


Fig. 14 Accumulation and readout timing of the BROME.

Another method using multiple exposure time signals for wide DR is to use the burst readout of multiple exposure time signals (BROME) in one frame. Figure 14 shows the signal accumulation and readout timing of the BROME method. It is assumed that the sensor has 5 vertical pixels. A long and two short accumulation-time signals are read out in a frame period. The long, short, and very short accumulation periods are denoted by LA, SA, VSA, respectively. Using the time slots for reading the LA signal, the SA signals are accumulated. The VSA signals are accumulated using the time slots for reading the SA signal. The shaded areas show the reading periods. A wide DR 640×480-pixel CMOS image sensor based on the BROME has been developed [23]. Figure 15 shows the chip photograph. In this chip, four different exposure time signals can be read in one

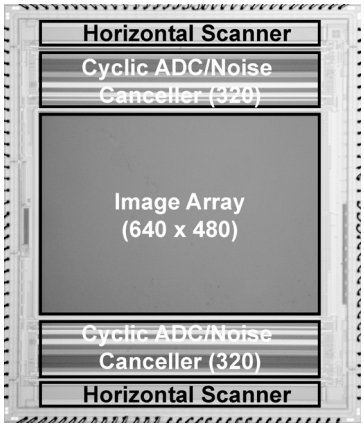


Fig. 15 Wide dynamic range CMOS image sensor.

(a) (b)

Fig. 16 Comparison of images taken by conversional image sensor (a) and wide dynamic range image sensor (b).

frame, and the DR of 120 dB has been achieved. Figure 16 shows a sample image taken by the wide DR image sensor together with an image taken by a conventional CCD camera for comparison. Both the dark inside and bright outside of a tunnel can be clearly captured using the wide DR sensor. Using a technique for reading extremely short exposure time signals which is shorter than one horizontal readout period, the DR is expanded to 153 dB [25].

A key device for reading four different exposure time signals in one frame period with sufficient image quality is a new type of column parallel cyclic ADC with 12b resolution shown in Fig. 12. The compact configuration and high speed allow us integrating the ADC array at the column of the 1/2 inch VGA-size CMOS image sensor with an equivalent readout rate of 180 frames/s and reading four exposure time signals at 30 frames/s.

The read four different exposure time signals are synthesized at an external system and the synthesized image data can be treated as very wide linear digital data. This property is particularly important if the wide dynamic range image is used for image recognitions in real world applications such as automobile, biometrics, and security systems.

Though the wide DR image sensor shown in Fig. 15 integrates register arrays only at the top and bottom of the image array, it is advantageous if the synthesis of wide linear DR image using on-chip frame memory based on the architecture shown in Fig. 1. Reading of high-frequency data from an IC chip leads to the increase of the power dissipation, noise interaction and system cost.

The column-parallel processing using on-chip frame memory leads to the increase of readout speed of image data from the image array to a memory, and greatly relaxes the output data rate from the sensor chip.

5.2 High-Speed Imaging

A High-speed camera is a useful tool for the observation of high-speed phenomena, analysis of high-speed machinery, machine vision, broadcasting, sports, and so on. Recent advances in CMOS image sensor technology provide great impact on high-speed imaging devices. The fastest CMOS image sensor can capture high-speed video sequence of 1024×1024 pixels at 5400 frames/s. The fastest image sensor employs parallel analog outputs and as a result, the camera head becomes large and heavy.

On-sensor analog-to-digital conversion techniques in high-speed CMOS image sensors make the camera head compact, which is an important feature of the high-speed cameras in most of applications. Digital 512×512-pixel CMOS image sensors operating at 5000 frames/s with 10b column-parallel successive approximation ADC and 3,500 frames/s with 12b column-parallel cyclic ADC have been reported [26], [32]. A global electronic shuttering function is indispensable for high-speed image sensors. A highly-sensitive low-noise global shutter pixel using an in-pixel charge amplifier is developed [26].

In digital high-speed image sensors, however, the required wide bandwidth of the digital output causes large power consumption, and the I/O bottleneck limits the achievable frame rate, especially if high resolution is required. On-sensor image compression can be a solution to the problem of the I/O bottleneck.

As an approach to digital high-speed image sensors with compressed data outputs, a prototype CMOS image sensor with on-chip parallel image compression circuits is developed. Figure 17 shows the chip photograph. The chip implemented with $0.25\,\mu$m CMOS technology integrates 256×256-pixel image array, a 256-channel cyclic A/D converter array, input/output buffer memories using 3 transistor DRAM cells, and a 16-channel image compression processing element (ICPE) array. An image compression algorithm suitable for compact design of the ICPE based on 4×4-point 2-dimensional discrete cosine transform, a zigzag scanning using 4blocks, and 1-dimensional Huffman coding is developed. In this prototype chip, high-speed image capturing and compressed data transfer at 3,000 frames/s at the compression ratio of 4.5 and the clock frequency of 16.8 MHz have been demonstrated [33]. The merit of the on-sensor compression can be exploited in high-resolution (Mega pixels) high-speed image sensors. For instance, a 1024×0124-pixel 5,000 frames/s digital image sensor can be realized with a clock frequency of 120 MHz. Though small amount of output buffer memory is integrated in Fig. 17, the integration of a frame buffer memory will enhance the compression ratio and the resulting output data rate.

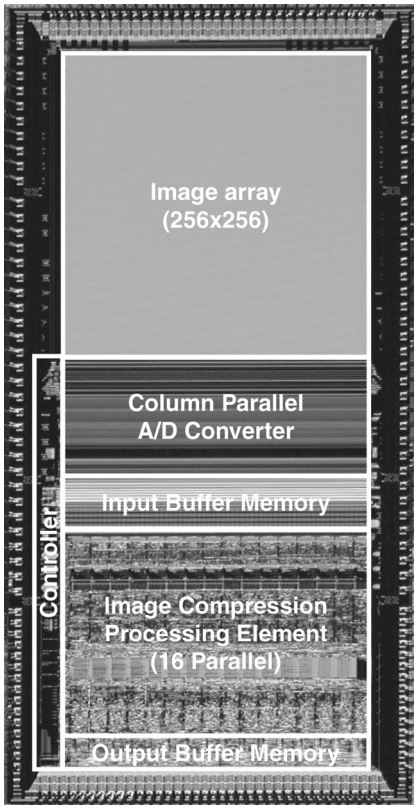


Fig. 17 High-speed CMOS image sensor chip with on-chip parallel image compression circuits.

5.3 Range Imaging or 3-D Imaging

Range image sensors are useful in a variety of applications such as automobile, medicine, robot vision systems, security systems, and so on. Range finding methods for 3-D measurements include the stereo-matching, light-section and time-of-flight (TOF) methods. The TOF method does not require any mechanical parts and is able to capture the 3-D image at video rate. Recently a number of TOF range image sensors have been reported. The reported TOF sensors include CCD-based [34], CCD-CMOS hybrid [35], and CMOS implementations [36]. All these methods are based on basic principle of charge modulation caused by the TOF. Figure 18 shows the cross-sectional view of a CMOS TOF range image sensor. The charge transfer to the right and left side of charge storages, FD1 and FD2 are controlled by high-speed pulses applied to transfer gates TX1 and TX2. The ratio of charges transferred to the right and left depends on the phase of the pulsed light, and hence the charge ratio gives information of the time of flight of light. A CMOS TOF range image sensor with the pixel structure of Fig. 18 and the spatial resolution of 360×240 pixels has been implemented. The TOF range image sensor has a structure of reducing the influence of background light using a pulsed light of very short duty cycles [36]. The range L is measured by the delay of light pulse T_d in each pixel, and it is

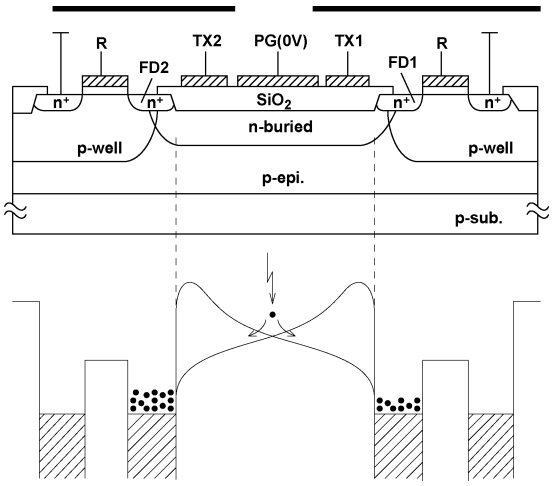


Fig. 18 Pixel structure of time-of-flight range image sensor.

given by

$$L = \frac{c}{2}T_d = \frac{c}{2}T_0\frac{N_2}{N_1 + N_2} \tag{18}$$

where T_o is the light pulse width and N_1 and N_2 are the number of electrons stored in FD1 and FD2, respectively. The range resolution at the worst case where $N_1 = N_2$ is given by [37]

$$\sigma_L = \frac{cT_0}{4}\frac{1}{\sqrt{N_1 + N_2}} \tag{19}$$

The range resolution is determined by the light pulse width and the number of total signal electrons. The use of the small light pulse width directly improves the range resolution. In the TOF range image sensor using the pixel structure of Fig. 18, the range resolution of 5 mm is achieved at 30 frames/s and T_0=25 ns. Since the maximum range which is given by $cT_0/2$ is limited by the choice of T_0, the number of electrons should be increased to improve the range resolution while covering wide range. To increase the equivalent number of electrons, a signal integration using frame memory is useful. The averaging with M frames improves the range resolution by a factor of $\sqrt{M}$. To produce a range image with sufficient range resolution at video rate, the architecture shown in Fig. 1 is useful for high-speed signal readout, averaging and range calculation.

6. Conclusions

In this paper, devices, circuits and signal processing techniques for CMOS imaging SoC's based on column-parallel processing architecture are reviewed and discussed. A column-parallel processing architecture is the best solution to the imaging SoC's for enabling both high functionality and image quality. The noise level in image sensing will be reduced by a mixed analog/digital processing to photon counting level in the near future and many of ultra-high-sensitivity cameras will be replaced by the small-size uncooled cameras using the CMOS imaging SoC's. High-resolution high-speed column-parallel ADC's are enabling

high-speed high-quality imaging, and the digital high-speed CMOS imaging devices will provide a great impact on a variety of fields such as scientific cameras, automobiles, broadcasting, industrial cameras, and consumer products. Imaging SoC's with a column-parallel mixed signal processing system and an on-chip frame memory will be a key technology to create new markets of vision systems.

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